

ZSSC3281

Advanced Dual Channel ARM based Resistive Sensor Signal Conditioner IC

The ZSSC3281 is a dual path sensor signal conditioning IC (SSC) for highly accurate amplification, digitization, and sensor-specific correction of sensor signals. The ZSSC3281 is suitable for bridge and half-bridge sensors, as well as external voltage-source element and single-element sensors (for example, Pt100 and external temperature sensor diodes) powered by an on-chip current source. Digital compensation of the sensor offset, sensitivity, temperature drift, and non-linearity is accomplished via a 32-bit ARM M3 based math core running a correction algorithm with calibration coefficients stored in a non-volatile, reprogrammable memory. The programmable, integrated sensor front-end allows optimally applying various sensors for a broad range of applications.

The ZSSC3281 provides measurement value readouts and programming capabilities via an I2C, SPI, or one-wire interface (OWI). Absolute and ratiometric voltage, current-loop, or interrupt outputs are supported by the ZSSC3281.

Applications

- Calibrated, continuously operating sensors with digital interface and/or analog output: (absolute or ratiometric) voltage or current loop output
- Enables smart, digital sensors for energy-efficient solutions
- (Dual/Diff.) pressure, flow and level sensing
- Industrial applications; for example, process/factory automation
- Consumer / white goods, for example, HVAC, weight scales
- Medical applications, for example, blood pressure, continuous smart health monitors

Features

- Digital communication and calibration interfaces:
 - SPI up to 10MHz
 - I2C (Standard, Fast, Fast+) and I3C SDR
 - One-wire-interface (OWI), up to 100kBit/s
- Accommodates nearly all resistive bridge sensor types (signal spans from 1mV/V up to 500mV/V)
- Supports different sensor element configurations:
 - Resistive bridge or half-bridge
 - Resistive divider string
 - Voltage source
- On-chip temperature sensor
- External temperature sensing supported, for example, sensor-bridge as temperature detector, external diode, etc.
- Programmable 16-bit digital-to-analog-converter and output (supporting “True-0Volt”-output):
 - (0V to 1V) or (0V to 5V) absolute voltage output
 - V_{DD}-ratiometric voltage output
 - 4mA to 20mA current-loop output supported
 - 0V to 10V absolute-voltage output supported
- Wide operational temperature and supply range
- On-chip voltage regulators for sensor supply, and IC operation
- Support for extra regulation by external transistor, for example, JFET (especially for industrial supply voltages >5.5VDC)
- Programmable sensor-signal-conditioning math core
- Reprogrammable, nonvolatile memory (NVM)
- On-chip diagnostics:
 - Sensor connection
 - AFE self-test
 - Memory integrity

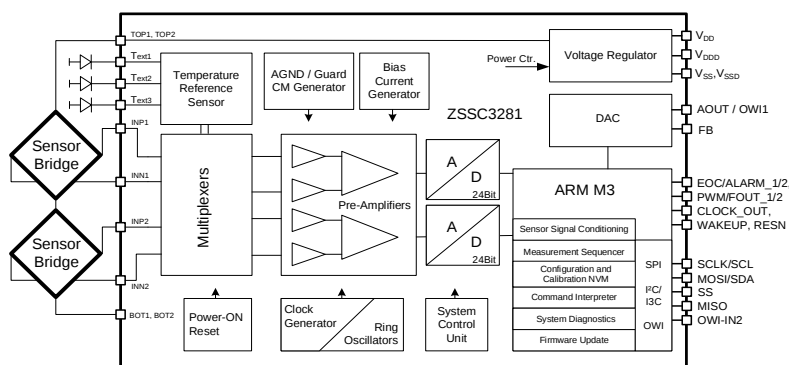


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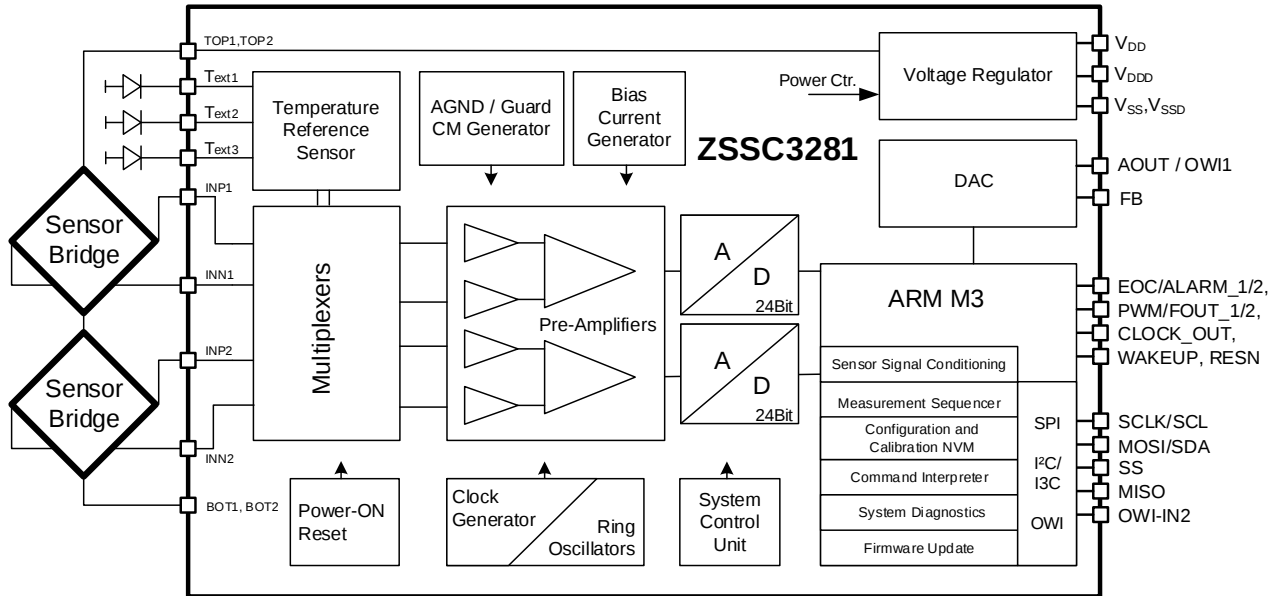
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1. Overview

1.1 Block Diagram



1.2 Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Carrier Type	Temperature
ZSSC3281BC1B	DICE on 304μm wafer no inking		Wafer Box	-40 to 85°C
ZSSC3281BC2B	DICE on 725μm wafer no inking		Wafer Box	-40 to 85°C
ZSSC3281BC5B	DICE on 304μm wafer with inking		Wafer Box	-40 to 85°C
ZSSC3281BC6B	DICE on 725μm wafer with inking		Wafer Box	-40 to 85°C
ZSSC3281BC3R	5 × 5 mm ² 40-QFN	MSL1	13 inch Reel	-40 to 85°C
ZSSC3281BI1B	DICE on 304μm wafer no inking		Wafer Box	-40 to 125°C
ZSSC3281BI2B	DICE on 725μm wafer no inking		Wafer Box	-40 to 125°C
ZSSC3281BI5B	DICE on 304μm wafer with inking		Wafer Box	-40 to 125°C
ZSSC3281BI6B	DICE on 725μm wafer with inking		Wafer Box	-40 to 125°C
ZSSC3281BI3R	5 × 5 mm ² 40-QFN	MSL1	13 inch Reel	-40 to 125°C
ZSSC3281KIT	Modular ZSSC3281 SSC Evaluation Kit including three interconnecting boards, five ZSSC3281 VFPQFN samples, and cable. Software is available for download on www.renesas.com/ZSSC3281 .			

1.3 Pin Configuration

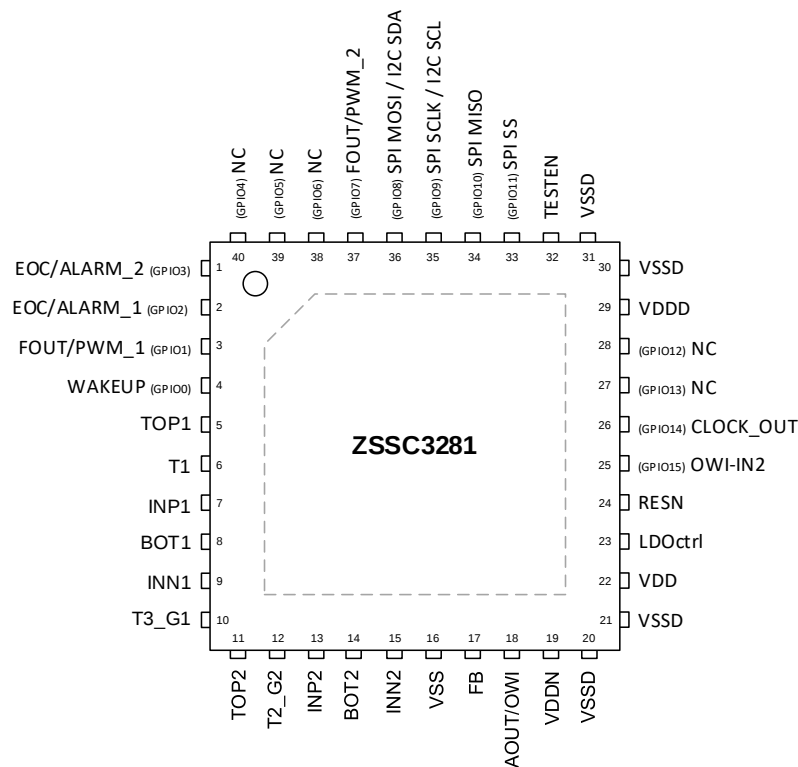


Figure 2. Pin Layout QFN40

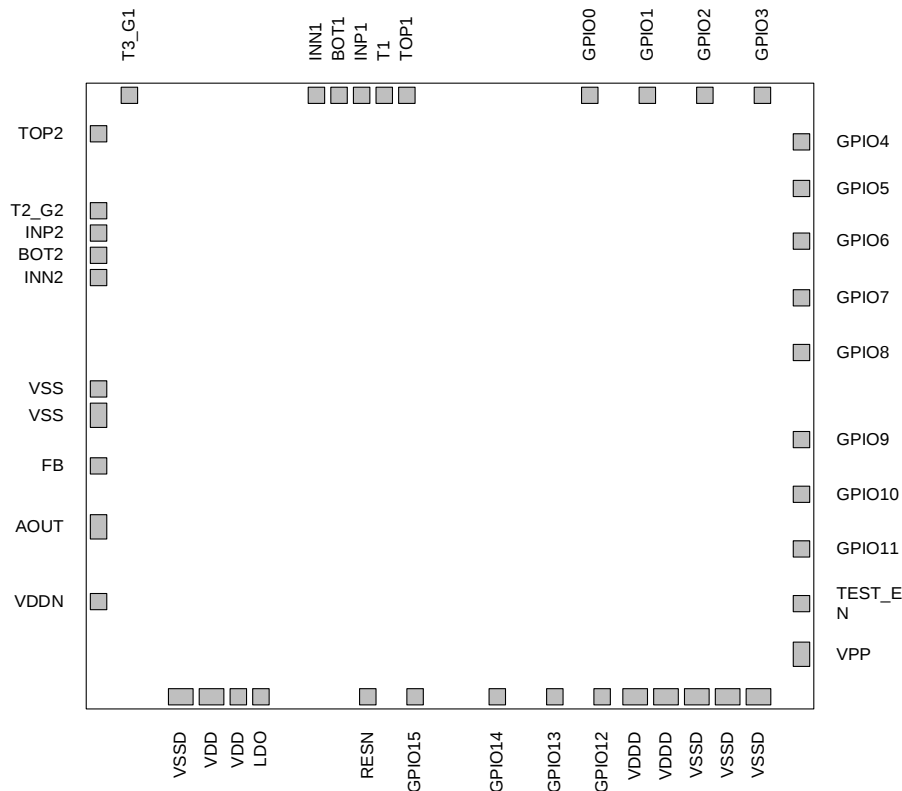


Figure 3. Pad Layout on Die

1.4 Pin Descriptions

QFN40 Pin Number	Name	Type	Description
1	EOC/ALARM_2	Digital Input/Output	GPIO3: mapped to EOC2 function
2	EOC/ALARM_1	Digital Input/Output	GPIO2: mapped to EOC1 function
3	PWM/FOUT_1	Digital Input/Output	GPIO1: mapped to TIMER2 function
4	WAKEUP	Digital Input/Output	GPIO0: mapped to WAKEUP function
5	TOP1	Analog Input/Output	Positive sensor (bridge 1) supply or sensor-signal input
6	T1	Analog Input/Output	External temperature sensor
7	INP1	Analog Input/Output	Positive sensor (bridge 1) signal
8	BOT1	Analog Input/Output	Sensor (bridge 1) ground or sensor-signal input
9	INN1	Analog Input/Output	Negative sensor (bridge 1) signal
10	T3_G1	Analog Input/Output	External temperature sensor 3
11	TOP2	Analog Input/Output	Positive sensor (bridge 2) supply or sensor-signal input
12	T2_G1	Analog Input/Output	External temperature sensor 2
13	INP2	Analog Input/Output	Positive sensor (bridge 2) signal
14	BOT2	Analog Input/Output	Sensor (bridge 2) ground or sensor-signal input
15	INN2	Analog Input/Output	Negative sensor (bridge 2) signal
16	VSS	Ground	Power supply ground
17	FB	Analog Output	Current-loop application feedback output (level below VSS). No connection if not used.
18	AOUT/OWI	Analog Output; Digital Input/Output	Analog smart-sensor output signal and/or OWI interface input/output line.
19	VDDN	Analog Output	Negative voltage output, charge pump buffer cap
20	VSSD	Ground	Digital power supply ground
21	VSSD	Ground	Digital power supply ground
22	VDD	Supply	Power supply
23	LDOctrl	Analog Output	Control output (reference signal) for (optional) external regulator / supply control loop
24	RESN	Digital Input	Digital IC reset (low active); internal pull-up
25	OWI-IN2	Digital Input/Output	GPIO15: mapped to OWI-IN2 function
26	CLOCK_OUT	Digital Input/Output	GPIO14: mapped to CLOCK_OUT function
27	N.C.	Digital Input/Output	GPIO13: not mapped
28	N.C.	Digital Input/Output	GPIO12: not mapped
29	VDDD	analog I/O	Buffer cap connection for internal VDDD
30	VSSD	Ground	Digital power supply ground
31	VSSD	Ground	Digital power supply ground
32	TESTEN	–	Renesas internal use only. Connect to VSSD
33	SPI SS	Digital Input/Output	GPIO11: mapped to SPI SS
34	SPI MISO	Digital Input/Output	GPIO10: mapped to SPI MISO
35	SPI SCLK / I2C SCL	Digital Input/Output	GPIO9: mapped to SPI SCLK / I2C SCL
36	SPI MOSI / I2C SDA	Digital Input/Output	GPIO8: mapped to SPI MOSI / I2C SDA
37	PWM/FOUT_2	Digital Input/Output	GPIO7: mapped to TIMER 1
38	N.C.	Digital Input/Output	GPIO6: not mapped
39	N.C.	Digital Input/Output	GPIO5: not mapped
40	N.C.	Digital Input/Output	GPIO4: not mapped
	Exposed PAD	-	QFN-bottom plate, leave pin floating.

2. Specifications

2.1 Absolute Maximum Ratings

Symbol	Parameter	Conditions	Minimum	Maximum	Units
T_J	Junction temperature			135	°C
T_S	Storage temperature		-45	150	°C
	ESD: Human Body Model Tested per JS-001-2017	Pins: INPx, INN _x , TOP _x , BOT _x , Tx, VDDD		2000	V
		Pins: GPIO _x , VDD, VDDN, VSS, VSSD, LDOctrl, AOUT/OWI, FB, RESN, NC		4000	V
	ESD: Charged Device Model Tested per JS-002-2014	All Pins		750	V
	Latch-up	Tested per JESD78E; Class 2, Level A	-100	+100	mA
V_{DD_max}	Maximum allowed for voltage supply	Referenced to VSS	-0.3	6.5	V
V_{IF_max}	Voltage at digital I/O	Referenced to VSSD	-0.3	5.5	V
V_{FB_max}	Voltage at FB pin	2-wire Current Loop Mode	-2	2	V

1. CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Symbol	Parameter	Conditions	Typical	Units
θ_{JA}	Theta JA	40Ld 5×5 QFN Package, 0 m/s air flow	25.8	°C/W
		40Ld 5×5 QFN Package, 1 m/s air flow	22.4	°C/W
		40Ld 5×5 QFN Package, 2 m/s air flow	20.8	°C/W
θ_{JB}	Theta JB	40Ld 5×5 QFN Package	1.3	°C/W
θ_{JC}	Theta JC	40Ld 5×5 QFN Package	24.4	°C/W

2.3 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{DD}	Power supply voltage	1.8	–	5.5	V
	Flash write/erase	2.7			
	With optional “True-0V” at analog output	2.7			
T_J	Junction temperature (depending on the ordered device, see section 1.2 for details.)	-40	–	125	°C
C_{VDD}	External capacitance between VDD and VSS, without external supply transistor regulation	10 -20%		22 +20%	μF
	External capacitance between VDD and VSS, with (optional) external supply transistor regulation	10 -20%		10 +20%	
C_{V3D}	External capacitance between VDDD and VSS	1 -20%		1 +20%	μF
C_{VDDN}	External capacitance between VDDN and VSS, with optional “True-0V” at analog output	1 -20%		1 +20%	μF
$C_{TOP,EMC}$	Recommended, external capacitance between TOP and VSS for electro-magnetic immunity (EMI)	0	6.8	8	nF
$C_{AOUT,EMC}$	Recommended, external capacitance between AOUT versus VDD and VSS for EMI suppression ¹	0	22	33	nF
I_{Sensor}	Load current through external sensor element ¹	0.005	0.5	2	mA
$V_{DioDrop}$	External temperature diode and RTD input range, drop over external element referenced to T1, T2_G2, T3_G1 pin	0.2	–	1.2	V
V_{Sens_in}	Absolute sensor signal input level, INN, INP pins	0.2	–	1.2	V
$I_{max_AOUT_V}$	Maximum current load at AOUT pin for voltage outputs	0	5	–	mA

Symbol	Parameter	Minimum	Typical	Maximum	Units
SR _{VDD_POR}	Recommended V _{DD} rise slew rate for power-on-reset (POR)	1.5	–	–	V/ms
I _{max_GPIO}	Maximum overall GPIO driver strength			120	mA

- For applications with OWI interface or analog voltage-output.
- With ratiometric sensor supply configuration; for example, a ratiometric bridge or bridge as temperature sensor with internal or external temperature sensitive resistor

2.4 Electrical Specifications

All parameter values are valid only under operating conditions specified in section 2.3. All voltages are referenced to V_{SS}.

Table 1: Electrical Operating Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
IC Supply						
I _{IC}	Current consumption, active mode:	Excluding connected sensor elements (external LDO enabled)				mA
	• low power (current loop)		–	3.3	3.5	
	• high power (depending on settings)		–	8	15	
V _{DD,LDO}	VDD generated with external depletion - NMOS	Programmable in 4 steps:				V
		• 3V	2.85	3	3.15	
		• 4V	3.80	4	4.20	
		• 5V	4.75	5	5.25	
		• 5.25V	5.00	5.25	5.50	
VDDA	Internally generated analog supply		1.6	1.65	1.85	V
Sensor Supply						
TOP	Sensor bias voltage in ratiometric supply mode	Ratiometric sensor voltage supply		VDDA		
I _{bias_TOP}	Sensor bias current used in Source Mode	Programmable in 10 steps: 0μA, 5μA, 10μA, 20μA, 40μA, 80μA, 100μA, 160μA, 200μA, 500μA	0		500	μA
I _{biasN_BOT}	Sensor current used in sink mode	Programmable in 2 steps: 20μA, 100μA	20		100	μA
I _{ERR}	Relative bias current (I _{bias_TOP} and I _{biasN_BOT}) error	Overall	-10		10	%
		Over-temperature	-1		1	%
R _{TH} , R _{TL}	TOP/BOT bias resistor	Programmable in 12 steps: open, 1kΩ, 33kΩ, 2kΩ, 4kΩ, 8kΩ, 10kΩ, 14kΩ, 18kΩ, 20kΩ, 24kΩ, 28kΩ, 40kΩ	1.3		40	kΩ
dR _{TH} , dR _{TL}	TOP/BOT bias resistor process variation		-30		30	%
TK of R _{TH} , R _{TL}	TOP/BOT bias resistor temperature variation	T = -55°C to 125°C			1.3	%

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
Analog-to-Digital Converter (ADC, A2D)						
r _{ADC}	Resolution		10	16	24	Bit
V _{ADCMid} (AGND)	Differential ADC input Common Mode	With internal regulator supplying TOP pin, typical: V _{TOP} /2 = 875mV (=PGA output Common Mode level)	–	0.5	–	V _{TOP}
Δ _{ADC,c}	Differential input offset shift	Sensor signal offset versus maximum sensor signal. Programmable in 8 steps.	0	–	7/8	V _{shift} /V _{fs}
ENOB ¹	Effective number of bits, 3σ _{Noise} based	Gain = 1.32, r _{ADC} = 24-bit, no oversampling	–	17	–	Bit
		Gain = 28, r _{ADC} = 16-bit, no oversampling	–	12	–	Bit
		Gain = 495, r _{ADC} = 24-bit, no oversampling	–	11	–	Bit
Digital-to-Analog Converter (DAC) and Analog Output						
VDD	VDD operating range	AOUT modes using 1V buffer	1.8		5.5	V
		AOUT modes using 5V buffer	2.7		5.5	
t _{AOUTsettle}	Time from digital value applied at DAC and voltage at VOUT	10% to 90% input step: V _{AOUT} at 90% of final value			100	μs
V _{OUT_START}	voltage at AOUT during startup			0		V
V _{AOUT}	Output voltage at pin AOUT	Ratiometric Voltage Mode	0		VDD	V
		1V absolute Voltage Mode	0		1	V
		5V absolute Voltage Mode			5 ²	
		10V absolute Voltage Mode			5 ²	
I _{OUTMAX}	Short current limit at pin AOUT	AOUT modes using 5V Buffer - short to VDD or VSS - programmable in 4 steps	3 8 15 20	5 12 19 25	9 20 23 30	mA mA mA mA
C _{load}	Load capacitance at AOUT	• 2-Wire Current Loop Mode			2	nF
		• all other modes (for example, cap for EMC: 33nF, ECU load: 10nF)			50	
r _{DAC}	Resolution		–	16	–	Bit

¹ ENOB = $\text{LOG}_2(2^{r_{ADC}} / 3\sigma_{Noise})$ with for example, $r_{ADC}[\text{Bit}] = 24$.

² VDD must be $\geq 5.25V$

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
Programmable-Gain Amplifier (PGA)						
G _{amp}	Gain	120 steps	1.32	–	495	V/V
G _{err}	Gain error	Referenced to nominal gain Gain = 1.32...5 Gain = 6...125 Gain = 126...495	-2.5 -5 -10	0	2.5 5 10	%
G _{errTemp}	Gain error over-temperature	Temperature compensated sensors do not require calibration over-temperature.	-0.2		0.2	%
V _{CMin}	Supported input common mode		0.2	0.5	0.7	V _{TOP}
V _{ioffsc}	Differential input offset shift	Programmable in 30 steps Gain1 ≤ 223 Gain1 = 275	-28.1 -22.5	0 0	28.1 22.5	mV
Sensor Signal Conditioning (SSC) Performance						
f _{SSCout}	Output (update) rate	3 measurements: signal+, signal-, diagnosis - r_{ADC} = 16bit - SSC-corrected digital output	–	1.3	–	kHz
		3 measurements: signal+, signal-, diagnosis - r_{ADC} = 14bit - SSC-corrected digital output	–	2.245	–	kHz
		2 measurements: signal+, diagnosis - r_{ADC} = 14bit - SSC-corrected digital output	–	3.36	–	kHz
t _{stepresp}	Step response	3 measurements: signal+, signal-, diagnosis - r_{ADC} = 16bit - SSC-corrected digital output		1.38		ms
		3 measurements: signal+, signal-, diagnosis - r_{ADC} = 14bit - SSC-corrected digital output		0.84		ms
Analog Inputs						
V _{INP1} , V _{INN1} , V _{INP2} , V _{INN2} ,	Absolute sensor input	Voltages at INPx and INNx pin; resulting minimum/maximum differential voltages: -800mV < V _{INDiff} < 800mV	0.2	–	1.2	V
V _{TEXT}	External temperature diode or RTD input range	at T1, T2_G2, T3_G1 pin (see Sensor Supply section of this table and ExtTempBrdglBias for available configuration options)	0.3	–	1.2	V
R _{SENSOR}	External sensor (bridge) resistance	TOP = 1.65V	0.825	–	60	kΩ
		2-wire Current Loop Mode	3.3	–	60	kΩ
V _{DIFFin}	Differential input signal range	Referenced to sensor supply (VDDA _{int})	–	–	800	mV

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
Diagnostics						
R_{open}	Broken sensor: values $>R_{open}$ set a failure flag	• INP1 vs. INN1 • INP2 vs. INN2	100	120	150	k Ω
R_{short}	Shorted sensor: values $<R_{short}$ set a failure flag	• INP1 vs. INN1 • INP2 vs. INN2 • INP1 vs. INP2 • INP2 vs. INN1	120	–	220	Ω
		• open TOP or BOT • short INP or INN to TOP or BOT				
V_{drift}	AFE gain check, run measurement with dedicated gain, compare with stored values	Input value from RDAC is applied	–	–	–	–
V_{RDAC}	RDAC differential output voltage	VDDAx = 1.65V:	–		–	mV
		• S = 00		2		
		• S = 01		10		
		• S = 10		100		
		• S = 11		200		
R_{T_OPEN}	T1, T2_G2, T3_G1 connection check: open	Broken Tx sensor: values $>R_{T_OPEN}$ set a failure flag:	1.6	2	3	M Ω
		• 3 level can be configured • INN is drawn to VSS! --> is not applicable in sensor configuration with one bridge at both frontends!	0.4	0.5	0.6	
			0.07	0.1	0.13	
t_{T_OPEN}	Diagnosis time; depends on C_{IS} and R_{T_OPEN}	Time from diagnose enable to valid output	0.1		10	ms
R_{T_SHORT}	T1, T2_G2, T3_G1 connection check: short to TOP, BOT, INP, INN	Shorted Tx sensor: values $<R_{T_SHORT}$ set a failure flag:				Ω
		• configuration for Pt1000	320	500	650	
VDD	• Programmed (expected) VDD level • VDD drop below the programmed level signalizes a VDD drop	Programmable in 6 steps: 2.2V, 2.7V, 3V, 4V, 5V, 5.25V	2.2		5.25	V
$V_{dropVDD}$	Voltage level, where the VDD drop is detected		70	85	95	%VDD
VDDD _{BOD}	VDDD brown out detection	VDDD < VDDD _{BOD} set a failure flag	67	90	97.5	%VDDD
V_{LOSS}	Power/ground loss with respect to AOUT	• $V_{AOUT} - VDD > V_{LOSS}$ • $V_{AOUT} - VSS < V_{LOSS}$		0.2		V

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
Power-Up						
t _{STA1}	Startup time	V _{DD} ramp up to interface communication	–	–	5	ms
t _{STA2}		V _{DD} ramp up to analog operation; depends on the configuration used	–	–	5	ms
t _{WUP1}	Wake-up time	Sleep to Active State interface communication	–	2	10	μs
Oscillator						
f _{CLK_HF}	Internal HF-oscillator frequency	At T=27°C	15.8	16	16.2	MHz
		Across temperature range	15.4		16.6	
f _{CLK_LF}	Internal LF-oscillator frequency		25	32	41	kHz
Internal Temperature Sensor						
r _{Temp}	Internal temperature sensor resolution	Differential output voltage	–	220	–	μV/K
Digital IO Pins						
V _{IL}	Input low voltage	voltage level where the input is recognized as low level	–		30	%VDD
V _{IH}	Input high voltage	voltage level where the input is recognized as high level	70		–	%VDD
V _{Ihys}	Input hysteresis		10		35	%VDD
V _{OL}	Output low voltage				8	%VDD
V _{OH}	Output high voltage		92			%VDD
I _{OL}	Output drive low current	V _{PAD} = V _{OL}				mA
		VDD = 1.7V	1		2.4	
		VDD = 2.6V	2.7		6.6	
		VDD = 5V	9		20	
I _{OH}	Output drive high current	V _{PAD} = V _{OH}				mA
		VDD = 1.7V	1.2		2.3	
		VDD = 2.6V	3.2		6.4	
		VDD = 5V	10.9		20.2	
I _{pullup}	Weak pull-up current at pin RESN	V _{PAD} = 0V				μA
		VDD = 1.7V	5		13	
		VDD = 2.6V	17		50	
		VDD = 5V	84		250	
I _{pulldown}	Weak pull-down current at pin WAKEUP	V _{PAD} = VDD				μA
		VDD = 1.7V	5		11	
		VDD = 2.6V	17		35	
		VDD = 5V	80		160	
Serial Interfaces						
f _{C,SPI}	SPI clock frequency		–	–	12	MHz
f _{C,I2C}	I2C clock frequency		–	–	1	MHz
f _{C,I3C}	I3C clock frequency		–	–	12.5	MHz
CD _{OWI}	OWI data rate		0.25	–	100	kBit/s
Flash Memory						

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
t_{PROG}	NVM program time	Programming time for complete configuration and calibration page:	—		—	ms
		• $f_{\text{CLK_HF}} = 16\text{MHz}$		360		
		• $f_{\text{CLK_HF}} = 1\text{Mhz}$		740		
n_{NVM}	NVM endurance	Number of reprogramming cycles	20000	—	—	Numeric
$t_{\text{RET,NVM}}$	Data retention		10	—	—	Years

3. Basic System Configuration

3.1 System Modes/System Start

The ZSSC3281 can operate in three different main operating modes:

Cyclic Mode	This is the default mode for continuously operating sensors. In this mode autonomous, cyclically repeated sensor measurements are performed and related digital and/or analog output updates are provided. The cyclic sequences for sensor measurements and system diagnostic measurements are configurable and allow to define the output update rate of the conditioned sensor signals. Cyclic Mode supports only a subset of the defined serial interface commands to guarantee deterministic input-output behavior (especially latencies) and to prevent accidental interruption of the conditioned sensor data stream.
Command Mode	This is the most appropriate mode for evaluation, test, and calibration purposes. In this mode, all supported serial interface commands are available. Command Mode can be used for applications requiring re-occurring digital interaction on functions that are not available in Cyclic Mode or certain system configuration changes.
Sleep Mode	This is the default mode for non-continuously operating sensors. In this mode WAKEUP (GPIO0) pin controls the operation phase and the current consumption of ZSSC3281. Within the active phase of Sleep Mode, a subsets of serial interface commands are supported, new measurement can be started, and results can be gathered. During the power save phase no communication is possible and ZSSC3281 stays in power down phase to allow the lowest possible current consumption.

ZSSC3281 provides a fourth operation mode which is not a user accessible operation mode:

Boot/Diagnosis Mode	Boot Mode: this is immediately active after power-on or reset of ZSSC3281, while the firmware is still in boot-up phase and the Command Interpreter is not functional yet. The serial interfaces are only partly operational in Boot/Diagnosis Mode to allow an external host to read the system status for ZSSC3281. Write access and command execution is not supported. Diagnosis Mode: this indicates the Static Diagnostic Mode (SDM) of the firmware and it is reached if the system self-supervision detects either of the following system faults that could lead to unreliable or unpredictable behavior of the IC: • 2 bit SRAM failures • Internal ARM faults (bus failures, ALU failures, memory or command failures) • CRC failures of CCP page • First time that watchdog triggers In the SDM mode the autonomous, cyclically repeated sensor measurements running in Cyclic Mode are stopped and the analog output is set to LDR, digital outputs (PWM, FOUT, ALARM) are set to high-Z, and CLOCK_OUT remains active. Leaving SDM is possible via watchdog reset or power cycle. Within SDM, the operation mode and the memory error flag inside the status flag is set supporting the detection of Boot or Diagnosis Mode.
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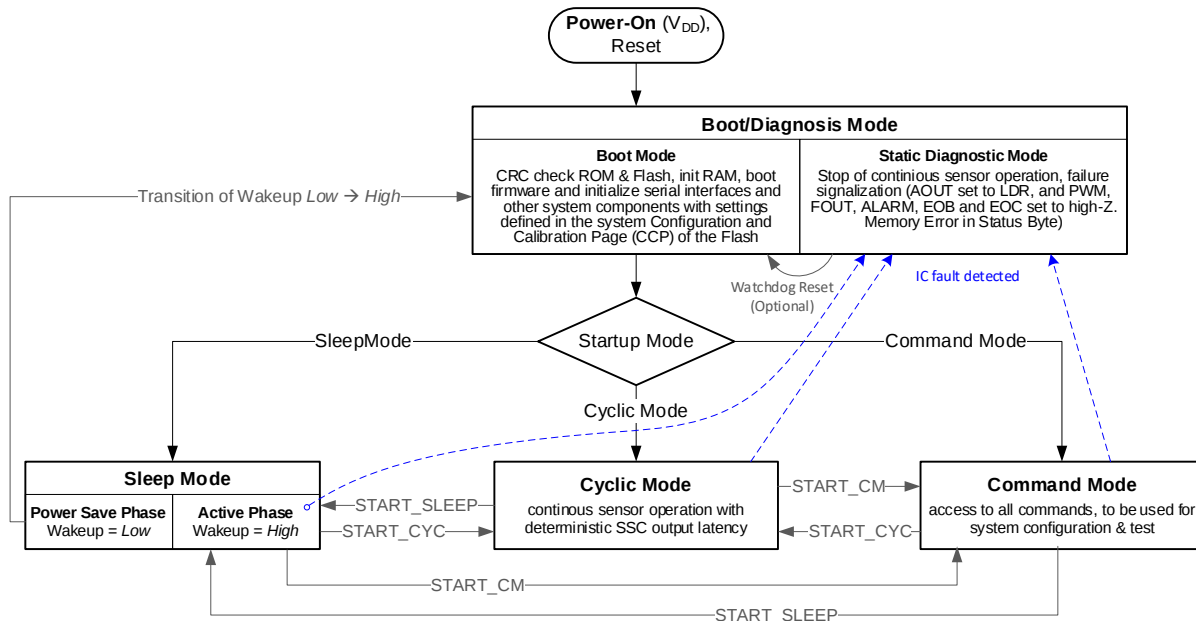


Figure 4:

Main Operating Modes

After power-on (reset) the ZSSC3281 always enters the programmed System Startup Mode (GUI path: *Configure\System Control\System Startup*) as soon as the firmware boot process is finished.

Each of the three operating modes can be set up as the default startup mode. Changing the ZSSC3281 to another operating mode is possible via the mode change and start commands: *START_CM*, *START_CYC* and *START_SLEEP* (see section 10.2.1 for details).

The ZSSC3281 supports three different types of digital interfaces: I2C/I3C, SPI, and OWI. All three interface types are available in the different main operating modes if they were enabled via GUI.

3.2 System Clocks

3.2.1. Internal Oscillators and Specifications

ZSSC3281 is equipped with two internal oscillators:

- Calibrated, first order temperature compensated 16MHz system clock oscillator
- Un-calibrated, first order temperature compensated 32kHz ultra low power oscillator

3.2.2. Main System Clock

The Main System Clock, which drives the ARM MCU, the memories (ROM, Flash, SRAM), and the peripherals is derived from the internal System Clock Oscillator. By default, the oscillator frequency (16MHz) is directly applied across the entire system without further down division. Hardware and software driven clock gating are applied to maintain a low power consumption.

For applications where power consumption of ZSSC3281 is a concern, the Main System Clock can be reduced by choosing a system clock source divider other than the value of div1. The maximum divider factor can be 16 (div16), which sets the Main System Clock to 1MHz.

The system clock divider can be changed via GUI field: *Configure\PowerSupply and Oscillator\System Clock Source Divider*.

If the ZSSC3281 is operated in a 2-Wire Current Loop setup (and respective GUI configurations are made) a reduction of the Main System Clock to 1 MHz is mandatory to meet the maximum system current consumption specification (<4mA) over the entire temperature range. In this case the 'System Clock Source Divider' is not selectable by the user.

3.2.3. Always-On Clock

The 32kHz always-on clock is used by the System Management Unit to control the power-up-sequence of the ZSSC3281 device, as well as by the internal watchdog and the low speed timer.

3.3 System Reset

The ZSSC3281 becomes reset at following scenarios:

Power On Reset Voltage at VDD or VDDD is below limits as specified in section 2.4.

External Reset RESN Pin of ZSSC3281 is set to LOW.

Self-Reset Self supervision via system diagnosis detected a critical system state and sets system in safe reset state.

Table 2: VDDD Power-On-Reset Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V_{riseVDDD}$	reset release voltage	VDDD level where reset is released	1.35		1.8	V
$V_{fallVDDD}$	reset voltage	VDDD level where reset is generated	1.1		1.6	V
$V_{hysVDDD}$	reset hysteresis voltage		50		500	mV

4. Analog Front End (AFE)

4.1 AFE Signal Path

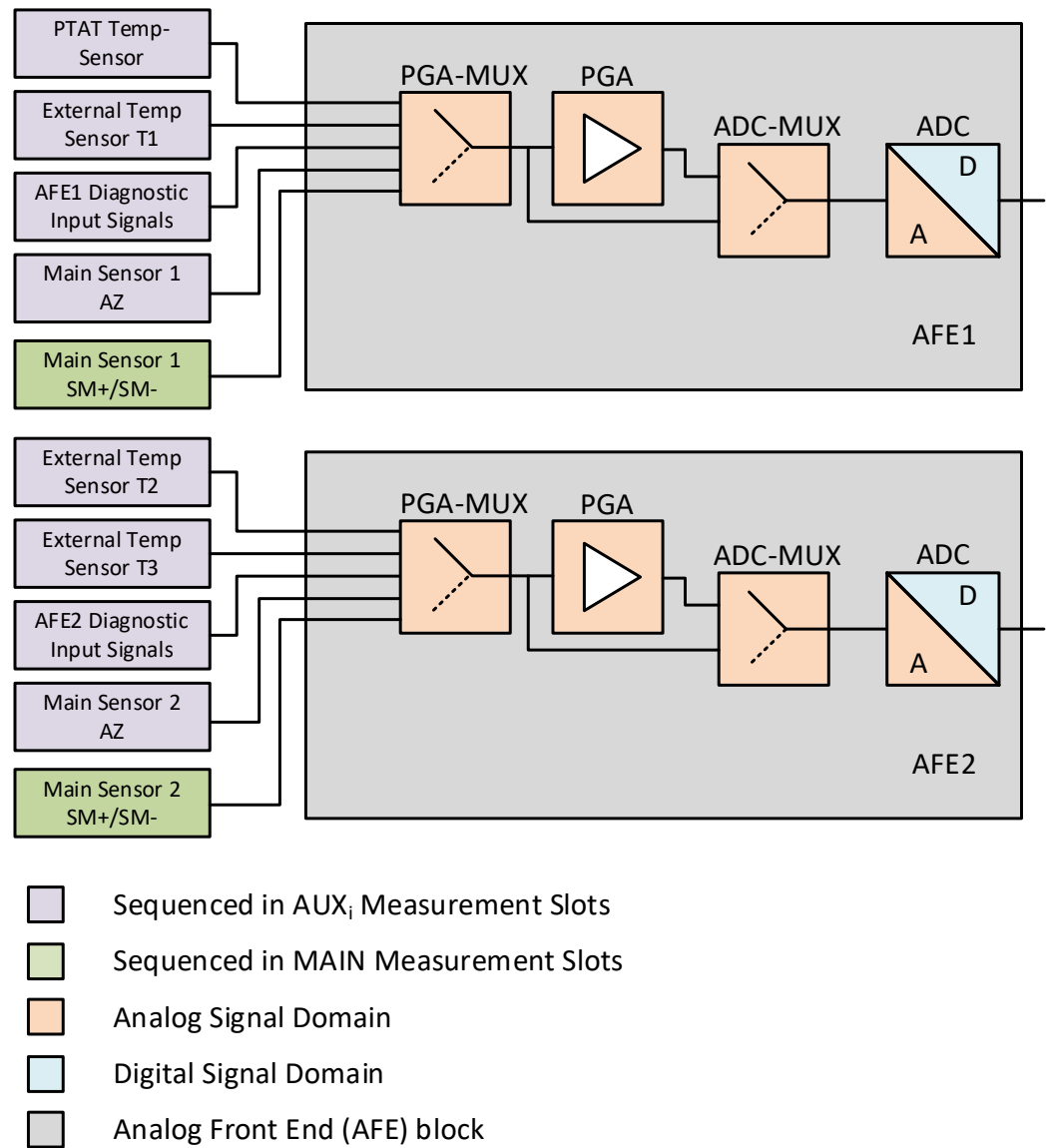


Figure 5: Block diagram Analog Front End

4.2 Bridge Sensor Inputs

4.2.1. Resistive Bridge Sensors

Table 3: Resistive Bridge Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{br}	Bridge resistor	Constant Voltage Mode	0.825		60	k Ω
		Constant Current Mode	0.1			
C_{br}	Bridge capacitance, depends on the required resolution: $\tau = R_{br} \times C_{br}$ defines the settle time.	Filter capacitances C_{br} between INN x /INP x and VSS		1		nF
V_{sig}	Signal span	mV/V is related to the bridge supply			500	mV/V
V_{off}	Signal offset	For example, $V_{sig} = 1\text{mV} \rightarrow V_{off} = 20\text{mV}$			2000 20	% off V_{sig} 1/ V_{sig}

Table 4: Resistive Bridge Application Configurations

Type #	Application Case	AFE1	AFE2	Comment
1	One resistive sensor	Resistive sensor 1	-	
2	Two resistive sensors	Resistive sensor 1	Resistive sensor 2	Not available with 2-wire current loop operation
3	One resistive sensor at both inputs	Resistive sensor 1 (normal speed)	Resistive sensor 1 (low speed)	Not available with 2-wire current loop operation

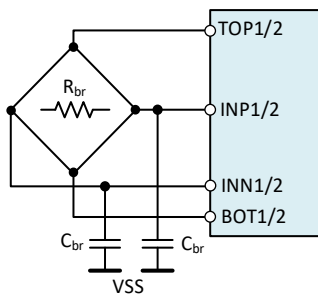


Figure 6: Bridge Sensor Type 1

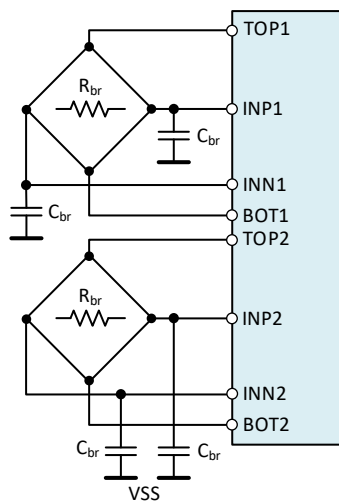


Figure 7: Bridge Sensor Type 2

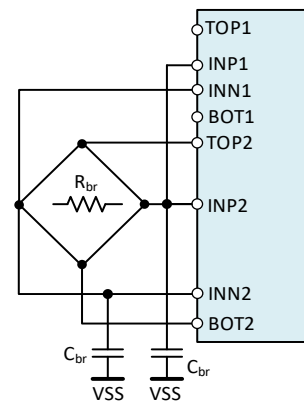
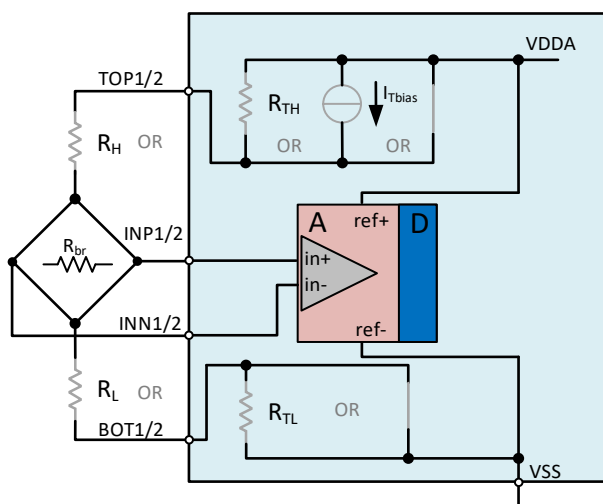


Figure 8: Bridge Sensor Type 3

The resistive bridge can be sourced in either Constant Voltage mode (V-source) or in Constant Current mode (I-source), requires low resistance.



Legend:

Gray components: can be activated “either-or” via the GUI.

Figure 9: Resistive Bridge Bias Configurations

In constant current mode the bridge output must be set into the common input range of the PGA. This can be done with a low side external resistor R_L or with the internal resistor R_{TL} .

In constant Voltage Mode the bridge current can be reduced by inserting the internal high and low side resistors R_{TH} , R_{TL} or by adding external resistors R_H and R_L .

Table 5: Resistive Bridge Supply Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{TOP1/2}$	Output voltage at TOP1/2	Direct voltage output		VDDA		V
C_{TOP_BOT}	Load capacitance				2.2	nF
I_{load}	Load current				2	mA
I_{Tbias}	Current out of TOP1/2		5		500	μA
R_{TH} , R_{TL}	Bias resistor		1.3		40	k Ω

4.3 Auxiliary Temperature Sensor Inputs

4.3.1. Internal PTAT Temperature Sensor

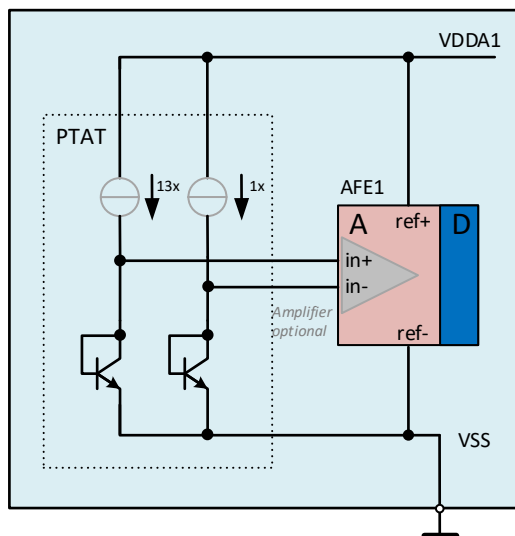


Figure 10: PTAT Sensor Configuration

Table 6: Internal PTAT Parameters

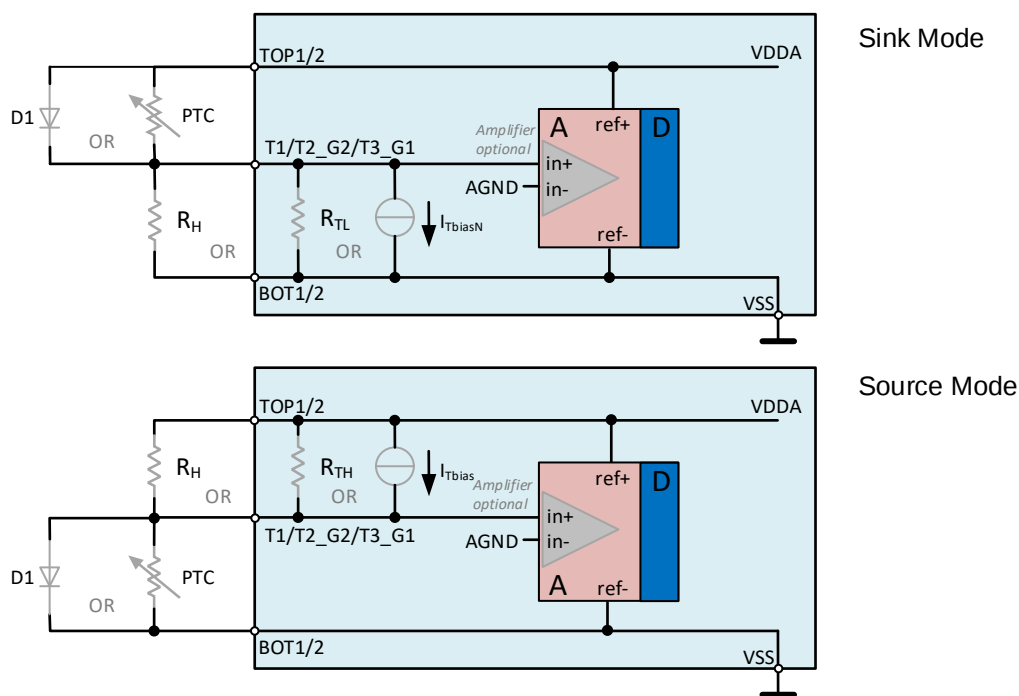
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{meas}	Measurement range		-55		125	°C
E_T	Measurement error	Calibrated	-5		5	K
ADC_{res}	Resolution	Programmable ADC resolution	10		15	bit
T_{res}	Effective resolution	$\pm 1.5\sigma$	2			LSB/°C
S	Sensitivity	Differential output voltage	218		230	$\mu\text{V/K}$

4.3.2. External Temperature Sensors

Three different external sensor types can be used to measure the temperature of the main sensor or a media temperature in the auxiliary signal path of the AFEs:

- PTC
- Diode
- TC Bridge Sensor

The PTC and Diode Sensors can be supplied either in Sink Mode or in Source Mode as shown in Figure 11. The gray marked components can be activated “either-or” via the GUI. The AGND potential is at $VDDA/2$.

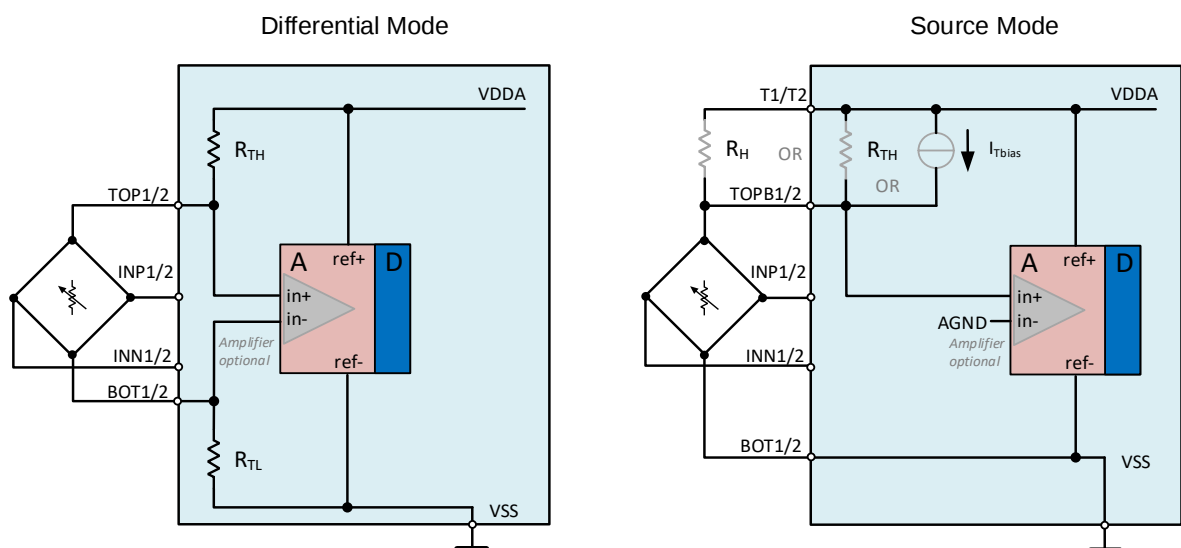


Legend:

Gray components: can be activated "either-or" via the GUI. The AGND potential is at VDDA/2.

Figure 11: PTC, Diode Sensor Bias Configurations

TC Bridge Sensor configurations can be supplied in Differential Mode or Source Mode as shown in Figure 12.



Legend:

Gray components: can be activated "either-or" via the GUI. The AGND potential is at VDDA/2.

Figure 12: TC Bridge Sensor Bias Configurations

Table 7: External Temperature Sensor Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{sensor}	Sensor resistance (PTC/TC Bridge Sensor)		50		1M	Ω
ADC_{res}	ADC resolution	Programmable ADC resolution	10		15	bit
ENOB	Effective resolution	$\pm 1.5\sigma$	14			bit

4.4 Programmable Gain Amplifier (PGA)

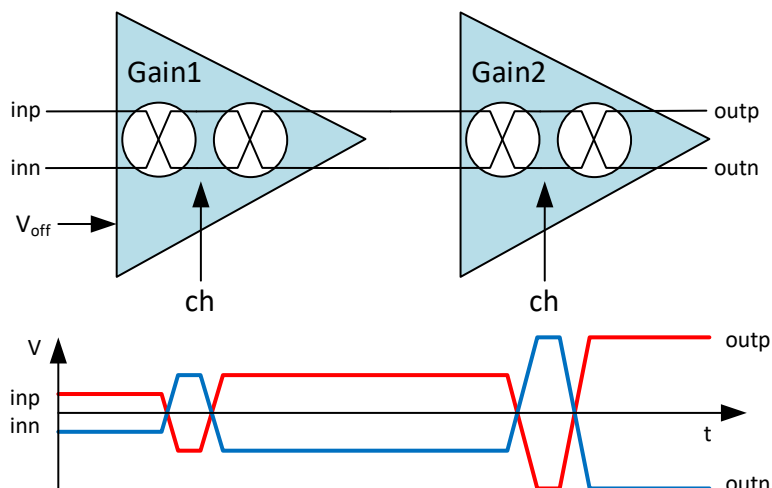


Figure 13: PGA Architecture

The first amplifier (gain1) has a built in PGA offset compensation (auto-zero) that is refreshed at the beginning of every measure cycle. The second stage has no offset compensation. The second stage amplifier offset is present at the PGA output with offset $\times$ gain2. Both PGA amplifier stages have built-in chopper functionality to suppress 1/f noise.

The gain settings that can be selectively programmed for both PGA stages are listed in Table 8.

Table 8: PGA Gain Steps

Gain1	Gain2
1.2	1.1
2	1.2
4	1.3
5.97	1.4
11.9	1.5
19.8	1.6
29.6	1.7
39.2	1.8
58.1	
76.6	
112	
143	
187	
223	
275	

Certain bridge sensors show noticeable DC offsets in their differential output voltage (usable differential voltage range is offset from zero). The sensor DC offset limits the maximum PGA gain, which can be applied without putting the PGA into saturation. To compensate for such sensor offsets, the PGA can be programmed to shift the input signal by a certain offset voltage before it gets gained up. The default shift is 0mV, the offset can be compensated by 15 steps in positive and negative direction as shown in Table 9. The PGA offset shift function is offered only for PGA Gain1 ≥ 11.9 .

Table 9: PGA Input Offset Compensation Steps

$11.9 \leq \text{Gain1} \leq 223$ [mV]	Gain1 = 275 [mV]
0	0
± 1.9	± 1.5
± 3.8	± 3
± 5.6	± 4.5
± 7.5	± 6
± 9.4	± 7.5
± 11.3	± 9
± 13.1	± 10.5
± 15	± 12
± 16.9	± 13.5
± 18.8	± 15
± 20.6	± 16.5
± 22.5	± 18
± 24.4	± 19.5
± 26.3	± 21
± 28.1	± 22.5

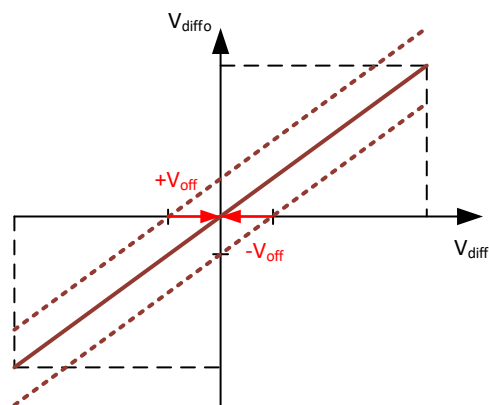


Figure 14: PGA Input Offset Compensation

PGA gain and the Input Offset Compensation value can be programmed separately for the two Main bridge sensors and for the three External auxiliary temperature sensors that can be connected to the ZSSC3281. The PGA Input offset compensation feature is limited to SM+/SM- and SM+ sequencer configurations which are described in section 4.6.

Table 10: PGA Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Gain	Total PGA gain	Programmable in 15/8 steps: - stage1: 15 steps, 1.2 to 275 - stage2: 8 steps, 1.1 to 1.8	1.32		495	V/V
V_{cmi}	Input common mode voltage			$V_{DDA}/2$		V
BW_{PGA}	Bandwidth			5		kHz
t_{az_PGA}	Auto-zero time		10			μs
f_{ch_PGA}	Chopper frequency			100		kHz

4.5 Analog-to-Digital Converter (ADC)

An incremental delta-sigma analog-to-digital converter (ADC) is used to digitize the PGA signal. To allow optimizing the trade-off between conversion time and resolution, the resolution can be programmed from 10-bit to 24-bit. The ADC processes differential input signals around its input common mode level $V_{DDA}/2$. Table 11 lists the ADC resolution, signal ranges, conversion times for a single analog-to-digital conversion, and $V_{DDA} = 1.65V$.

Table 11: ADC Configuration Parameters

ADC Resolution [Bits]	Full Scale Input Voltage V_{fs} [V]	LSB Size V_{LSB} [μV]	Conversion Time, Typical, T_{Conv} [μs]	Conversion Rate, Typical, F_{Conv} [kHz]
10	± 1.418	2768.638	32.54	30.73
11	± 1.425	1391.718	43.75	22.86
12	± 1.431	698.499	59.59	16.78
13	± 1.434	350.189	81.99	12.20
14	± 1.437	175.428	113.68	8.80
15	± 1.439	87.832	158.49	6.31
16	± 1.440	43.958	221.86	4.51
17	± 1.441	21.994	311.48	3.21
18	± 1.442	11.002	438.22	2.28
19	± 1.443	5.503	617.46	1.62
20	± 1.443	2.752	870.94	1.15
21	± 1.443	1.376	1229.41	0.81
22	± 1.443	0.688	1736.38	0.58
23	± 1.443	0.344	2453.33	0.41
24	± 1.444	0.172	3467.25	0.29

The ADC can perform an additional offset shift (independent of the PGA shifting) to adapt input signals with offsets to the ADC input range. Enabling the offset shift causes the ADC to perform an additional amplification of the ADC's input signal by factor $\times 2$. This must be considered for a correct PGA configuration setup.

The ADC offset shift feature is limited to SM+/SM- and SM+ sequencer configurations which are described in section 4.6.

The shift values in Table 12 are related to the input voltages at INP, INN:

- Full scale differential input voltage: $V_{INDiff_fs} = \frac{V_{fs}}{Gain}$
- Differential input shift voltage: V_{INDiff_shift}
- Maximum, minimum differential input voltage: V_{INDiff_max} , V_{INDiff_min}

Table 12: ADC Input Offset Shift Steps

PGA Polarity	ADC Shift Enable	ADC Gain	ADC shift	$V_{INDiff_shift}/V_{INDiff_fs}$	$V_{INDiff_min}/V_{INDiff_fs}$	$V_{INDiff_max}/V_{INDiff_fs}$
Positive	0	$\times 1$	0	no shift	-1	+1
Negative			0	no shift	+1	-1
Positive	1	$\times 2$	1	7/8	-1/16	+15/16
			2	6/8	-2/16	+14/16
			3	5/8	-3/16	+13/16
			4	4/8	-4/16	+12/16
			5	3/8	-5/16	+11/16
			6	2/8	-6/16	+10/16
			7	1/8	-7/16	+9/16
			0	no shift	-1/2	+1/2
Negative			0	no shift	+1/2	-1/2

PGA Polarity	ADC Shift Enable	ADC Gain	ADC shift	$V_{INDIFF_shift} / V_{INDIFF_fs}$	$V_{INDIFF_min} / V_{INDIFF_fs}$	$V_{INDIFF_max} / V_{INDIFF_fs}$
Negative			1	1/8	-9/16	+7/16
			2	2/8	-10/16	+6/16
			3	3/8	-11/16	+5/16
			4	4/8	-12/16	+4/16
			5	5/8	-13/16	+3/16
			6	6/8	-14/16	+2/16
			7	7/8	-15/16	+1/16

4.6 AFE Sequencer

The measurement flow, especially the frequency of Main bridge measurements vs. Auxiliary measurements can be configured by the user. Once started by the ARM MCU, the measurement flow runs autonomously controlled by the AFE. The AFE Sequencer state machine ensures predictable measurement timing in the continuous cyclic operation of ZSSC3281.

The AFE Sequencer carries out AFE measurements based on a measurement slot mechanism. There can be up to eight measurement slots assigned per AFE, which form a single measurement sequence. A measurement sequence can be executed only once (for example, initiated by a dedicated command request) or continuously cycled in Cyclic Mode operation of ZSSC3281.

Each of the measurement slots can be individually configured for the following measurement types:

- Sensor Measurement SM+: bridge inputs INP/INN directly converted (non-inverted)
- Sensor Measurement SM-: bridge inputs INP/INN flipped (inverted)
- Auxiliary Measurement aux_i: cycles through the auxiliary measurement vector

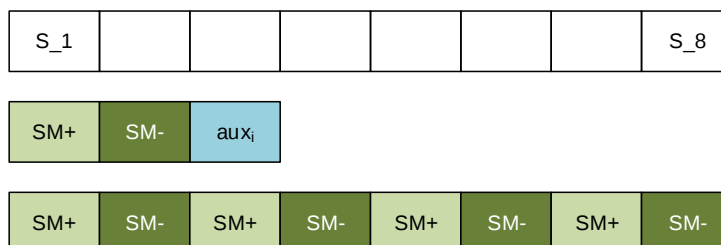


Figure 15: Measurement Slot Configuration with Two Example Configurations

The actual number of measurement slots per measurement sequence can be defined by the user and may vary between 1 and 8. The hardware allows to configure any combination based on the above definitions, but not all combinations lead to reasonable measurement schemes. The GUI supports the user in selecting proper measurement schemes. Figure 15 shows two reasonable example configurations. The measurement schemes are explained in further detail in subsequent chapters 4.6.3 to 4.6.5.

Auxiliary measurements usually have lower response time requirements than measurements on the main sensor bridge. The auxiliary measurements are therefore cycled orthogonal to the main loop of the sequencer. Activated auxiliary measurements become listed in the so called Auxiliary measurement vector. The vector index 'i' gets increased after each executed aux_i slot and starts over after the entire set of active measurements was completed. The configuration options of auxiliary measurements are further detailed in section 4.6.2.

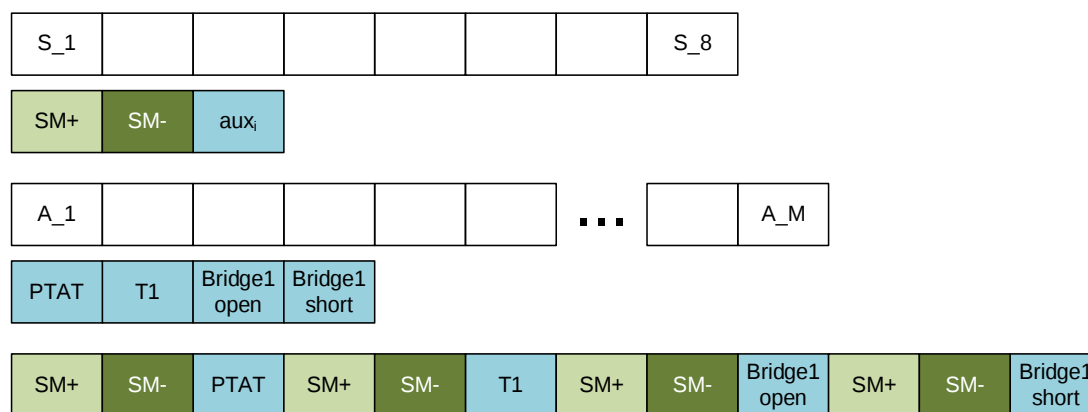


Figure 16: Auxiliary Measurement Configuration, and Corresponding Measurement Flow

Figure 16 illustrates the sequencer operation with an example configuration. During the 3rd measurement slot (configured as aux_i), the first enabled auxiliary measurement is executed ("PTAT", internal temperature sensor). When the measurement sequence (SM+/SM-/aux_i) is executed again in Cyclic Mode, the next enabled auxiliary measurement is executed ("T1", external temperature sensor). Similarly, "Bridge1 open" and "Bridge1 short" diagnostics measurements are carried out in following measurement sequence cycles. During the 5th execution of the measurement sequence, the PTAT auxiliary measurement is carried out again.

4.6.1. Bridge Sensor Measurement Configuration

The main bridge sensor signals can be measured in three ways:

- SM+/SM- (or SM-/SM+) measurement
- SM+/AZ measurement
- SM+ without AUX_AZ measurement



Figure 17: SM+/SM- (or SM-/SM+) Measurement

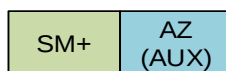


Figure 18: SM+/AZ Measurement

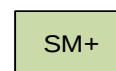


Figure 19: SM+ without AZ Measurement

Configurations in Figure 17 and Figure 18 provide digital offset compensation of the entire signal path in the Analog front end. The configuration in Figure 19 only provides analog offset compensation in the first stage of the PGA. The offsets of the second PGA stage and the ADC offset are not compensated. The performed respective calculations are shown in 1.

In the SM+/SM- configuration, the bridge inputs INP/INN are first converted straight forward in the SM+ measurement slot and second with an internally flipped INP/INN input signal in SM- slot. For the SM+/AZ configuration, the second measurement (AZ) is performed without applied input signal. INP/INN become disconnected from the sensor and internally shorted for AZ measurements.

Since signal integration time the SM+/SM- configuration is twice as long as in the SM+/AZ configuration (same ADC resolution settings assumed), the SM+/SM- configuration achieves approx. 0.5 bit better noise performance than the SM+/AZ configuration. However, the longer input signal integration time of the SM+/SM- configuration leads to an increased measurement latency as described in section 4.6.3 and 4.6.4.

The auto-zero measurement (AZ) belongs to the group of auxiliary measurements and is cycled less often if either of the following options appears:

- further auxiliary measurements are enabled in the auxiliary measurement vector described in section 4.6.2
- accelerated bridge measurements are enabled as described in section 4.6.5.

Since the offset in the internal signal path varies rather slowly, the auto-zero compensation remains very accurate, even for a long auxiliary measurement vector.

Because most sensor applications also require other auxiliary measurements, the assignment of the AZ measurement to the group of auxiliary measurements helps to reduce the worst case measurement latency on the main bridge sensor. This is because the SM- slot as needed in configuration of Figure 17, can be omitted.

The lowest measurement latency is achieved with the “SM+ only” configuration in Figure 19. However, this is only true if no other auxiliary measurements are needed for the desired sensor application.

A further influence on the overall measurement time has the input settling time, which is required depending on the output resistance of the external sensors, respective capacitive loads on the signal lines and the ADC resolution selected by the user. The input settling time is always inserted before an ADC conversion starts and can be configured in the GUI for main bridge measurements via `Configure\AFE\Bridge\SetTime[μs]` and for auxiliary temperature measurements via `Configure\AFE\Temperature\SetTime[μs]`.

Considering achievable measurement latencies and noise performance, configuration in Figure 17 is better when higher ADC resolutions are required or for sensor configurations with fast input settling, while configuration in Figure 18 and Figure 19 are preferable when lower ADC resolutions become selected or for sensor configurations requiring long input settling times (bridge settling time has a considerable impact on the timing budget).

4.6.2. Auxiliary Measurement Configuration

The supported auxiliary measurements are:

- Auto-zero for internal signal path
- Temperature on sensor input T1
- Temperature on sensor input T2
- Temperature on sensor input T3
- Internal PTAT
- AFE diagnostic checks
 - Sensor connection checks for all external sensors (Short to TOPx pin or BOTx pin and Open)
 - Bridge signal range check
 - AFE gain and offset drift supervision via internal reference DAC

They can be activated in the GUI via tabs `Configure\AFE\Sequencer`, `Configure\AFE\Temperature Selection` and `Diagnostic\Sensor\AFE`.

4.6.3. Deterministic Input Step Response with SM+/SM- Configuration

As described in section 4.6.1, sensor configurations with fast input settling or applications requiring higher ADC resolutions are better served with the SM+/SM- scheme for the main bridge measurement. For the following step response consideration, the below application example is used:

- Sensor Measurement (non-inverted)
- Sensor Measurement (inverted)
- Auxiliary Measurement (for example, for sensor temperature)
- Note: SM+ and SM- can be exchanged yielding to the same result

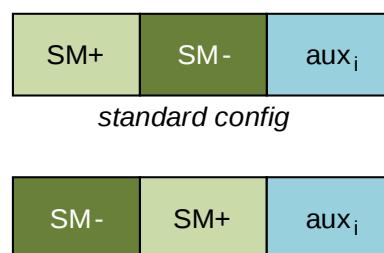


Figure 20: SM+/SM- Configuration

For this use case the worst-case input to output latency consists of:

- 4 sensor A2D-conversion times (duration depending on selected ADC resolution)
- 1 auxiliary conversion time (fixed duration, based on longest auxiliary conversion timing)
- 1 SSC calculation
- 1 settling time at AOUT, if AOUT is enabled

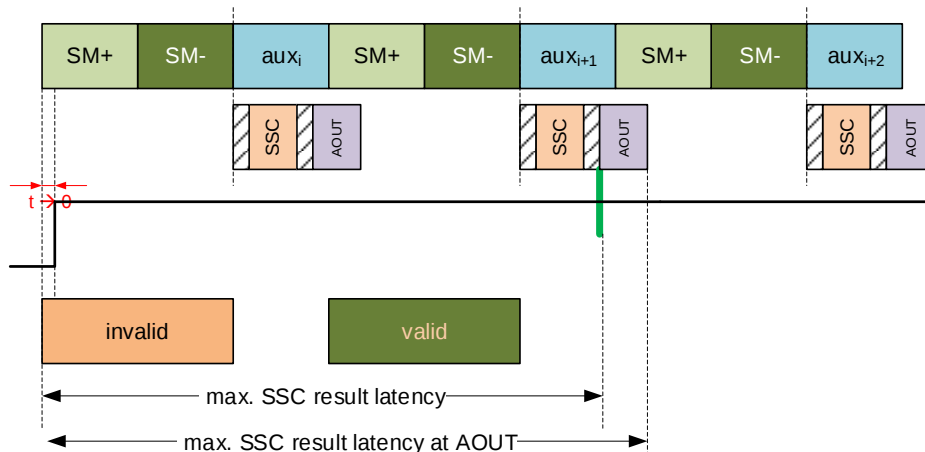


Figure 21: Measurement Flow and Latency for SM+/SM- Configuration

4.6.4. Deterministic Input Step Response with SM+/AZ Configuration

Since the SM+/SM- configuration samples the input signal twice as long as the SM+/AZ configuration and it suffers a noticeable timing overhead for sensor configurations with slow sensor input signal settling, a second SM+/AZ measurement scheme with deterministic step response times is available. For the following step response consideration, the below application example is used:

- Sensor measurement (non-inverted)
- Auxiliary measurement (for example, for sensor path auto-zero and/or sensor temperature) within the auxiliary measurement vector

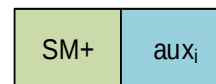


Figure 22: SM+/AZ Configuration

As shown in Figure 23, the worst-case latency consists of:

- 2 sensor AD-conversion times (duration depending on selected ADC resolution)
- 1 auxiliary conversion time (fixed duration, based on longest auxiliary conversion timing)
- 1 SSC calculation
- 1 settling time at AOUT, if AOUT is enabled

Assuming equal ADC resolution settings for the SM+/SM- configuration as described in section 4.6.3 and the SM+/AZ configuration described in this section, the worst case input to output latency is shorter by two sensor AD-conversion times in case of the SM+/AZ setup. The auxiliary measurement duration in the SM+/AZ setup may become slightly longer than for the SM+/SM- configuration, since it is determined by the AZ measurement time if the selected resolution of the main bridge is larger than the resolutions of all other active auxiliary measurements. This is because the resolution of the AZ measurement is set by the resolution of the SM+ measurement and the longest measurement of the auxiliary measurement vector determines the duration of the aux_i slot(s)

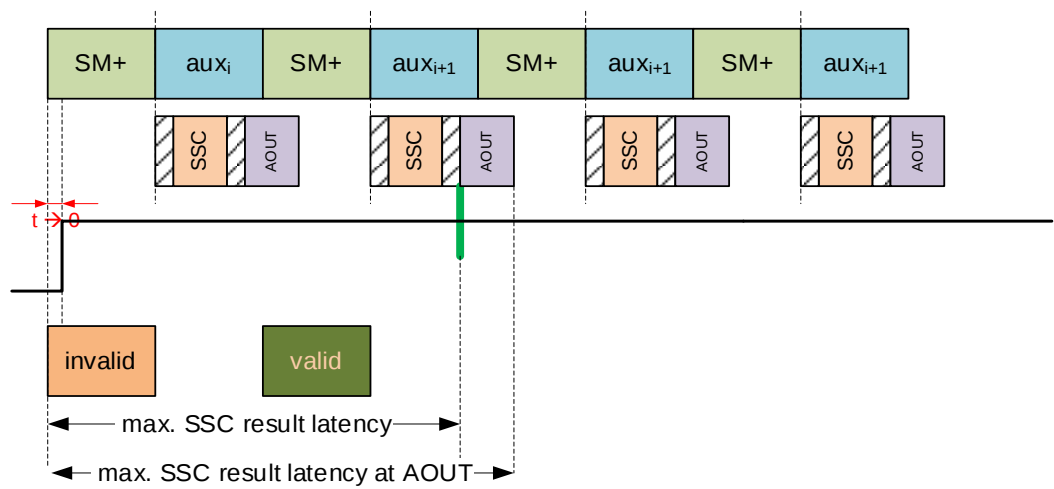


Figure 23: Measurement Flow and Latency for SM+/AZ Configuration

4.6.5. Accelerated Bridge Measurements with Sparsely Inserted Auxiliary Measurements

For applications which focus on highest conversion rates at the bridge sensor input but do not require a deterministic maximum input to output latency of the corrected sensor signal, auxiliary measurements can be sparsely inserted to occur only after a certain number of measurement sequences were executed by the AFE sequencer. This way, auxiliary measurements become executed even more seldom, giving the main sensor bridge measurements priority.

The AFE sequencer can be configured such that an aux_i measurement is only executed (inserted) after every P_x measurement sequence. P can be selected as 2, 4, or 8. Figure 24 shows an example of a measurement flow with P = 2 while Figure 25 uses P = 8 where aux_i measurements are executed after eighth measurement cycle.



Figure 24: Auxiliary Measurement Executed after Every Second Measurement Cycle



Figure 25: Sequencer Setup for Highest Update Rate on Bridge Sensor

4.7 AFE Dual Speed Mode

The AFE Dual Speed Mode operation is intended for single bridge sensor applications that require a fast transient step response combined with a high resolution steady state signal at analog and serial interface outputs. It can be activated in the GUI via Configure\AFE\Sequencer\AFE Selection and Configurability\Dual speed AFE with AOUT.

In AFE Dual Speed Mode the sensor bridge is measured by both frontends (AFE1 and AFE2) in parallel, see Figure 26 for the required schematic. AFE Dual Speed Mode allows the operation of one external temperature sensor (T1) or the internal temperature sensor (PTAT).

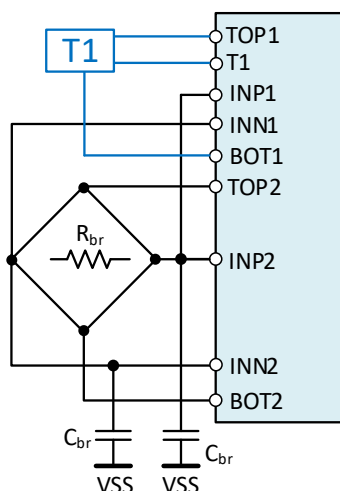


Figure 26: Schematic in AFE Dual Speed Mode

The fast reaction of the bridge sensor input is achieved through AFE1, which runs at low resolution (10 bit) and highest update rate. AFE2 runs on high resolution (SM+/SM- sequencer, 16bit) and a slower update rate according to Table 13. Figure 27 illustrates the sequence of AFE1 and AFE2 measurements.

AFE1

SM+	SM+	SM+	SM+	SM+	SM+	SM+	SM+	SM+	SM+	SM+	SM+	SM+	SM+	SM+	SM+	SM+	SM+	aux _i
-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	------------------

AFE2

SM+	SM-
-----	-----

Note: conversion timing not drawn to exact scale

Figure 27: Sequencer Illustration for AFE1 and AFE2

Table 13: ADC Configuration Parameters for Dual Speed Mode

ADC Resolution [Bits]	Full Scale Input Voltage V_{fs} [V]	LSB Size V_{LSB} [μ V]	Conversion Time, Typical, T_{Conv} [μ s]	Conversion Rate, Typical, F_{Conv} [kHz]
10	± 1.418	2768.638	32.54	30.73
16	± 1.440	43.958	887.44	1.13

A digital algorithm decides whether the SSC conditioned results of AFE1 or AFE2 are forwarded to the outputs. By default, the more precise data of AFE2 is forwarded. As soon as a significant signal step occurs at the bridge sensor inputs, the algorithm switches from the slower AFE2 to the fast AFE1. After the transition to AFE1, the outputs follow the AFE1 results with its speed, accuracy, and noise properties.

AFE1 stays active for at least the duration of approximately two slow AFE2 conversions. If no further significant input signal variation is detected within this time, the algorithm switches back from AFE1 to AFE2. See Figure 28 for a graphical explanation of the algorithm.

An input step is detected if the signal difference between AFE1 and AFE2 crosses Threshold 1 (can be setup via GUI Configure\AFE\Sequencer\Dual Speed AFE with AOUT). Once an input step was detected and outputs were switched to AFE1, a count down timer is started to let AFE1 process a number of approximately 60 samples. The actual sample number is between 57 and 61, depending on the configured AFE2 bridge settling time and is automatically calculated by the GUI. Once the count down timer expired, the outputs are switched back from AFE1 to AFE2 if no further step was detected.

To judge the signal variation after the initial step detection, all new AFE1 measurement results are compared against an AFE1 reference result that was stored at the preceding threshold crossing. A further step is detected when the comparison difference is larger than Threshold 2 (can also be setup via GUI). In this case a new AFE1 reference value is stored and the count down timer is reset which causes another approximately 60 samples from AFE1.

The algorithm detects signal changes which span over multiple AFE1 conversions (see Figure 28), it compares the current measurement result with a reference value from several conversion periods back in time. The user can modify the dynamic behavior of the algorithm by modifying the Threshold 1 and Threshold 2 settings.

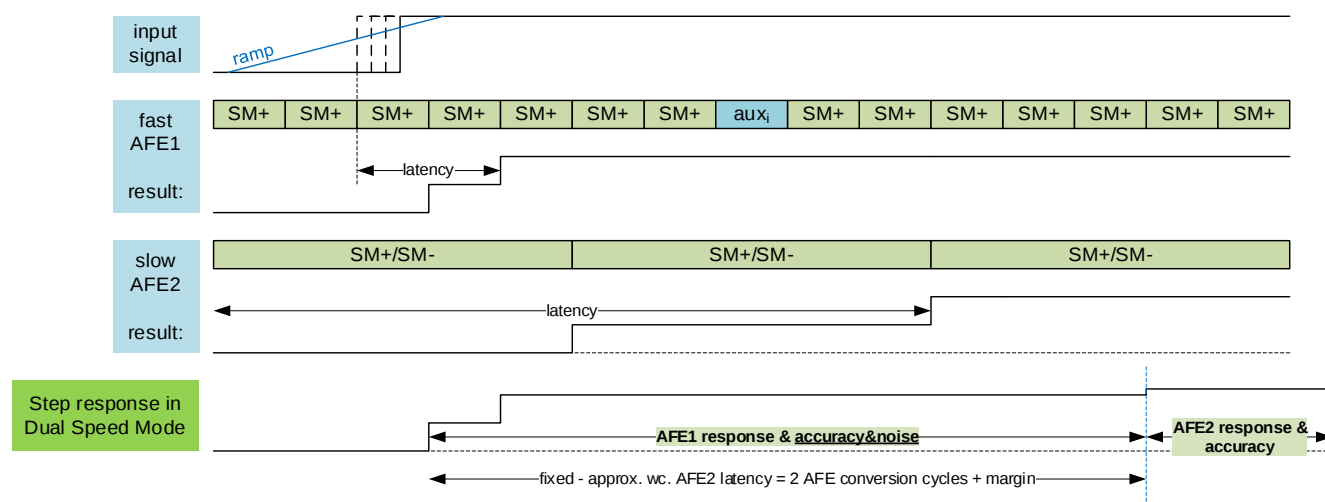


Figure 28: Step Response in Dual Speed Mode for a Significant Single Input Step

The AFE Dual Speed Mode is available for following SSC outputs:

- all Analog Output (AOUT) Modes with exception of 2-wire current loop mode
- all Serial interface outputs

AFE Dual Speed Mode is not available for:

- 2-wire current loop operation
- PWM/FOUT output modes
- Signal Post processing features: EOC, ALARM, Output Filtering.
- AFE diagnosis features

The dynamic Sensor Bridge configuration is fixed to:

- AFE1: 10bit, SM+ only
- AFE2: 16bit, SM+/SM-
- The aux_i cycle in the sequencer becomes automatically activated if T1 or PTAT are selected. If no temperature sensor is selected, the aux_i cycle shown in Figure 27 is removed.

With the dynamic AFE configuration setup a worst case input step latency of 0.35ms is achievable at AOUT. The precise signal settles maximum 5ms after stable input signal.

5. Sensor Signal Conditioning

5.1 Signal Conditioning Data Path

Figure 29 illustrates the sensor signal conditioning flow that is applied for AFE output data to compensate for offset, gain, non-linearity, and temperature effects and to calculate the conditioned data for further output processing. All this basis mathematical subfunctions are described within the sections 5.2 to 5.6.

The signal path from conditioned data to individual output signals is described in section 6.1.

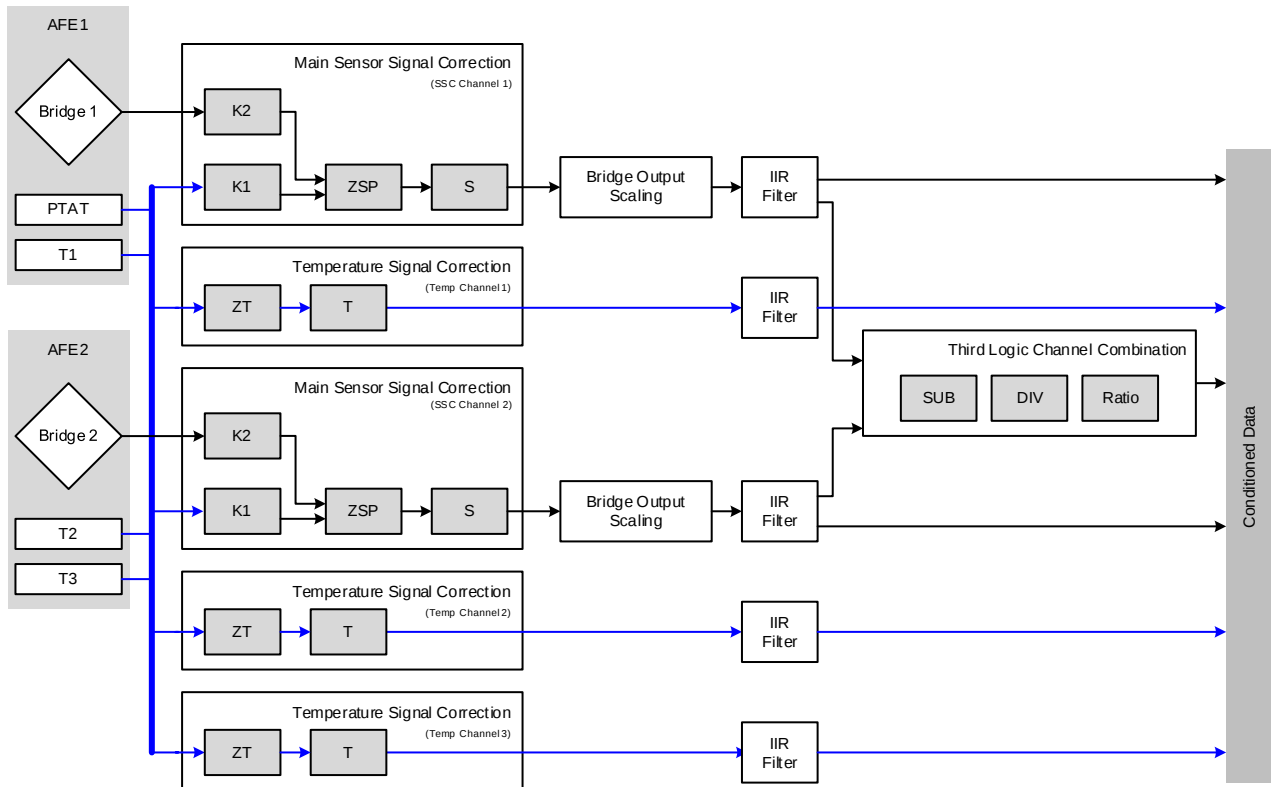


Figure 29: Sensor Signal Flow Chart from Input to Conditioned Data

5.2 Main Sensor Signal Correction

ZSSC3281 supports basic second-order compensation of sensor nonlinearities. The following basic SSC math options are available:

- Sensor signal correction
 - SOT Curve-0: Parabolic compensation curve
 - SOT Curve-1: S-shaped compensation curve
- Temperature signal correction

The parabolic compensation is recommended for most sensor types. The applied SSC math option can be selected in the GUI through the field Calibration\Curve.

The available SSC capabilities for SOT Curve-0 and SOT Curve-1 are described below. The used equation terms are as follows:

		Valid input range
<i>S</i>	Corrected sensor reading output via I2C, OWI, or SPI	0 _{HEX} to FFFFFF _{HEX}
<i>S_Raw</i>	Raw sensor reading from ADC (after AZ correction, depends on Afe1SmConfig)	-7FFFFFF _{HEX} to 7FFFFFF _{HEX}
<i>Gain_S</i>	Sensor gain term	-7FFFFFF _{HEX} to 7FFFFFF _{HEX}
<i>Offset_S</i>	Sensor offset term	-7FFFFFF _{HEX} to 7FFFFFF _{HEX}
<i>Tcg</i>	Temperature coefficient gain term	-7FFFFFF _{HEX} to 7FFFFFF _{HEX}
<i>Tco</i>	Temperature coefficient offset term	-7FFFFFF _{HEX} to 7FFFFFF _{HEX}
<i>T_Raw</i>	Raw temperature reading (after AZ correction)	-7FFFFFF _{HEX} to 7FFFFFF _{HEX}
<i>SOT_tcg</i>	Second-order term for Tcg non-linearity	-7FFFFFF _{HEX} to 7FFFFFF _{HEX}
<i>SOT_tco</i>	Second-order term for Tco non-linearity	-7FFFFFF _{HEX} to 7FFFFFF _{HEX}
<i>SOT_sens</i>	Second-order term for sensor non-linearity	-7FFFFFF _{HEX} to 7FFFFFF _{HEX}
<i>SENS_shift</i>	Post-calibration, post-assembly offset shift	-7FFFFFF _{HEX} to 7FFFFFF _{HEX}
$ \dots $	Absolute value	
$[\dots]_{ll}^{ul}$	Bound/saturation number range from <i>ll</i> to <i>ul</i> , overflow and/or underflow is reported as saturation in the Status Byte	

All raw data and compensation coefficients supplied to the formulas are required in the following 24-bit data format:

Table 14: Data Format of Raw ADC Readings

Bit-Number	23	22	21	20	...	2	1	0
Meaning, Weighting	2^0	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

Table 15: Data Format of 24-bit SSC Coefficients

Bit-Number:	23	22	21	20	...	2	1	0
Meaning, Weighting	0 = positive 1 = negative	2^1	2^0	2^{-1}	...	2^{-19}	2^{-20}	2^{-21}

The compensated result data is supplied in the following 24-bit data format:

Table 16: Data Format of Corrected SSC Results (S and T)

Bit-Number:	23	22	21	20	...	2	1	0
Meaning, Weighting	2^0	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

5.2.1. Pre-calculation

Simplified:

$$K_1 = 2^{23} + \frac{T_Raw}{2^{23}} \times \left(\frac{4 \times SOT_tcg}{2^{23}} \times T_Raw + 4 \times Tcg \right) \quad \text{Equation 1}$$

$$K_2 = 4 \times Offset_S + S_Raw + \frac{T_Raw}{2^{23}} \times \left(\frac{4 \times SOT_tco}{2^{23}} \times T_Raw + 4 \times Tco \right) \quad \text{Equation 2}$$

Complete:

$$K_1 = \left[2^{23} + \left[\frac{T_Raw}{2^{23}} \times \left[\left[\frac{SOT_tco}{2^{21}} \times T_Raw \right]_{-2^{25}}^{2^{25}-1} + 4 \times Tco \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \quad \text{Equation 3}$$

$$K_2 = \left[4 \times \text{Offset_S} + \left[S_Raw + \left[\frac{T_Raw}{2^{23}} \times \left[\left[\frac{SOT_tco}{2^{21}} \times T_Raw \right]_{-2^{25}}^{2^{25}-1} + 4 \times Tco \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \quad \text{Equation 4}$$

5.2.2. SOT Curve-0 (Parabolic Compensation)

Simplified:

$$Z_{SP} = \frac{4 \times \text{Gain_S}}{2^{23}} \times \frac{K_1}{2^{23}} \times K_2 + 2^{23} \quad (\text{delimited to positive number range}) \quad \text{Equation 5}$$

$$S = \frac{Z_{SP}}{2^{23}} \times \left(\frac{4 \times SOT_sens}{2^{23}} \times Z_{SP} + 2^{23} \right) + \text{SENS_shift} \quad (\text{delimited to positive number range}) \quad \text{Equation 6}$$

Complete:

$$Z_{SP} = \left[\left[\frac{\text{Gain_S}}{2^{21}} \times \left[\frac{K_1}{2^{23}} \times K_2 \right]_{-2^{25}}^{2^{25}-1} + 2^{23} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \quad \text{Equation 7}$$

$$S = \left[\left[\frac{Z_{SP}}{2^{23}} \times \left[\left[\frac{SOT_sens}{2^{21}} \times Z_{SP} \right]_{-2^{25}}^{2^{25}-1} + 2^{23} \right]_{-2^{25}}^{2^{25}-1} + \text{SENS_shift} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \quad \text{Equation 8}$$

5.2.3. SOT Curve-1 (S-shaped Compensation)

Simplified:

$$Z_{SS} = \frac{4 \times \text{Gain_S}}{2^{23}} \times \frac{K_1}{2^{23}} \times K_2 \quad (K_1 \text{ and } K_2 \text{ according to Equation 3 and Equation 4}) \quad \text{Equation 9}$$

$$S = \frac{Z_{SS}}{2^{23}} \times \left(\frac{4 \times SOT_sens}{2^{23}} \times |Z_{SS}| + 2^{23} \right) + \text{SENS_shift} \quad (\text{delimited to positive number range}) \quad \text{Equation 10}$$

Complete:

$$Z_{SS} = \left[\frac{\text{Gain_S}}{2^{21}} \times \left[\frac{K_1}{2^{23}} \times K_2 \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \quad \text{Equation 11}$$

$$S = \left[\left[\frac{Z_{SS}}{2^{23}} \times \left[\left[\frac{SOT_sens}{2^{21}} \times |Z_{SS}| \right]_{-2^{25}}^{2^{25}-1} + 2^{23} \right]_{-2^{25}}^{2^{25}-1} + 2^{23} \right]_{-2^{25}}^{2^{25}-1} + \text{SENS_shift} \right]_{-2^{25}}^{2^{25}-1} \quad \text{Equation 12}$$

5.3 Temperature Signal Correction

Temperature is measured either internally by the ZSSC3281, through an additional external element, or by means of a combination of ZSSC3281 internal and external temperature sensing capabilities. Temperature correction contains both linear gain and offset terms as well as a second-order term to correct for any nonlinearities. For temperature, second-order compensation is always parabolic.

The correction equation terms are as follows:

		Valid input range
T	Corrected temperature sensor reading output via digital interface	0_{HEX} to $\text{FFFFFF}_{\text{HEX}}$
Gain_T	Gain coefficient for temperature	$-7\text{FFFFFF}_{\text{HEX}}$ to $7\text{FFFFFF}_{\text{HEX}}$
T_{Raw}	Raw temperature reading after AZ correction	$-7\text{FFFFFF}_{\text{HEX}}$ to $7\text{FFFFFF}_{\text{HEX}}$
Offset_T	Offset coefficient for temperature	$-7\text{FFFFFF}_{\text{HEX}}$ to $7\text{FFFFFF}_{\text{HEX}}$
SOT_T	Second-order term for temperature source nonlinearity	$-7\text{FFFFFF}_{\text{HEX}}$ to $7\text{FFFFFF}_{\text{HEX}}$
T_{Shift}	Shift for post-calibration/post-assembly offset compensation	$-7\text{FFFFFF}_{\text{HEX}}$ to $7\text{FFFFFF}_{\text{HEX}}$

The correction formula is best represented as a two-step process as follows:

Simplified:

$$Z_T = \frac{4 \times \text{Gain_T}}{2^{23}} \times (T_{\text{Raw}} + 4 \times \text{Offset_T}) + 2^{23} \quad (\text{delimited to positive number range}) \quad \text{Equation 13}$$

$$T = \frac{Z_T}{2^{23}} \times \left(\frac{4 \times \text{SOT_T}}{2^{23}} \times Z_T + 2^{23} \right) + T_{\text{shift}} \quad (\text{delimited to positive number range}) \quad \text{Equation 14}$$

Complete:

$$Z_T = \left[\left[\frac{\text{Gain_T}}{2^{21}} \times [T_{\text{Raw}} + 4 \times \text{Offset_T}] \right]_{-2^{25}}^{2^{25}-1} + 2^{23} \right]_{-2^{25}}^{2^{25}-1} \quad \text{Equation 15}$$

$$T = \left[\left[\frac{Z_T}{2^{23}} \times \left[\left[\frac{\text{SOT_T}}{2^{21}} \times Z_T \right]_{-2^{25}}^{2^{25}-1} + 2^{23} \right]_{-2^{25}}^{2^{25}-1} + T_{\text{shift}} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \quad \text{Equation 16}$$

5.4 Bridge Output Scaling

ZSSC3281 offers a linear rescaling function to amplify or compress a partial region of the sensor input range to the desired signal output range. Figure 30 illustrates the rescaling on an example where the 25% to 75% calibrated signal input range is mapped to the output range of 0% to 100%. The feature is intended for customers who need to separate product derivatives after a common sensor calibration step.

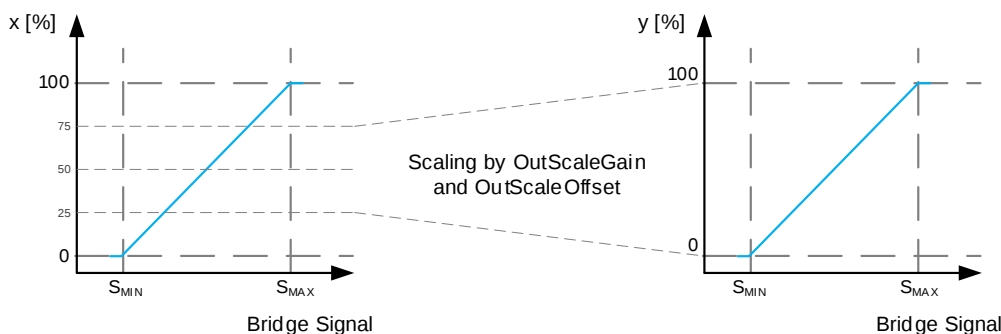


Figure 30: Example: Bridge Output Scaling Function for Scaling 25% - 75%, to final 0% - 100%

The rescaling feature applies the following formula to the SSC conditioned outputs of the main bridge sensor:

$$y = \left[\frac{8 \cdot \text{OutScaleGain}}{2^{23}} \times (x + 8 \times \text{OutScaleOffset}) \right]_0^{2^{24}-1} \quad \text{Equation 17}$$

The Coefficients *OutScaleGain* and *OutScaleOffset* are stored in the CCP (Configuration and Calibration Page) of ZSSC3281 in signed magnitude format. According to Table 17 *OutScaleGain* is limited to a maximum gain of 4 and the *OutScaleOffset* can vary from -1.5 to 0 related to the SSC result number range 0 to ~2.

Table 17: Examples for Bridge Output Scaling

Input Relative – x [%]		OutScaleGain		OutScaleOffset		Output Relative – y [%]	
		real	CCP content (decimal)	real	CCP Content (decimal)		
0	50.0	2.000	2097152	0.0	0	0	100
0	33.3	3.003	3148876	0.0	0	0	100
0	25.0	4.000	4194304	0.0	0	0	100
25	50.0	4.000	4194304	-0.5	-524288	0	100
25	75.0	2.000	2097152	-0.5	-524288	0	100
50	100.0	2.000	2097152	-1.0	-1048576	0	100
75	100.0	4.000	4194304	-1.5	-1572864	0	100

Table 18 lists the mapping of CCP register content to output scaling coefficients.

Table 18: Data Format of Output Scaling Coefficients in CCP

Bit-Number:	23	22	21	20	...	2	1	0
Meaning, Weighting	0 = positive 1 = negative	2^2	2^1	2^0	2^{-1}	...	2^{-19}	2^{-20}

The GUI supports the calculation of *OutScaleGain* and *OutScaleOffset* based on provided relative input and output range specifications (Can be set on the GUI tab Configure\Output Scaling).

5.5 IIR Filter

The conditioned outputs of the two main sensor bridge channels CH1 and CH2 and the conditioned outputs of the temperature channels TCh1 to TCh3 can be low pass filtered for noise reduction. Each channel is equipped with an independent configurable IIR Filter. The mathematical filter description is as follows:

$$y_0 = x_0 \quad \text{Equation 18}$$

$$y_i = y_{i-1} + \frac{(x_i - y_{i-1}) \times \text{Diff}}{\text{Avg}} \quad \text{Equation 19}$$

where:

$$\text{Diff} = \text{FiltDiff} + 1 \quad \text{Equation 20}$$

$$\text{Avg} = 2^{\text{FiltAvg}} \quad \text{Equation 21}$$

FiltDiff and *FiltAvg* represent the filter coefficients which are stored as unsigned 3-bit values per filter channel in *lirFiltCoeffReg* inside the CCP of ZSSC3281. They are determined by the GUI (Configure\Filter) depending on the filter Tau selections made by the user. For a stable system, the $\text{Diff} \leq \text{Avg}$ must be ensured.

The filter Tau can be calculated by:

$$\frac{\text{Diff}}{\text{Avg}} = \alpha \approx \frac{1}{\tau_{dig}} = \frac{\Delta T}{\tau_{(ana)}} \quad \text{Equation 22}$$

$$\tau_{dig} = -\frac{1}{\ln(1-\alpha)} \quad \text{Equation 23}$$

τ_{dig} is given in number of digital samples.

5.6 Third Logic Channel Combination

The potentially pre-scaled and filtered two main sensor bridge channels Ch1 and Ch2 of ZSSC3281 can be mathematically combined to calculate the output of a third logic channel Ch3. Channel Ch3 is only available in the synchronized AFE mode which is enabled via the GUI menu Configure\AFE\Sequencer\AFE Selection and Configurability\selection: "AFE1+AFE2, config equally".

The calculation result on Ch3 is available through serial interface read out only. The digital output format is signed 32-bit (two's complement), see Table 19. Outputting the Ch3 result at AOUT and FOUT/PWM is possible for subtraction and ratio only. Division is readable via digital interfaces only.

The Third Logic Channel (TLC) can be configured via the GUI menu Configure\TLC menu.

Following mathematical operations are available:

- Subtraction: (Ch1 – Ch2) or (Ch2 – Ch1)
- Division: (Ch1 / Ch2) or (Ch2 / Ch1)
- Ratio: If Ch1 == Ch2 then Ch3 = 1
Else if Ch1 < Ch2 then Ch3 = Ch1 / Ch2
Else Ch3 = 2 – (Ch2 / Ch1)

Note: Division calculation can lead to math saturation, which is not suppressed by firmware.

Calibration of the sensor channels Ch1 and Ch2 must still be done independently applying the single channel calibration routines.

Table 19: Data Format of Logic Output Channel Ch3 at Serial Interface

Bit-Number	31	30	...	24	23	22	21	20	...	2	1	0
Meaning, Weighting	-2^8	2^7	...	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

6. Post Processing Options for Conditioned Sensor Signals

6.1 Signal Post Processing Flow Chart

Figure 31 illustrates the signal flow from conditioned data to individual output signals. All basis mathematical subfunctions are described within the sections 6.2 to 6.6.

The signal path from AFE output data to conditioned data is described in section 5.1.

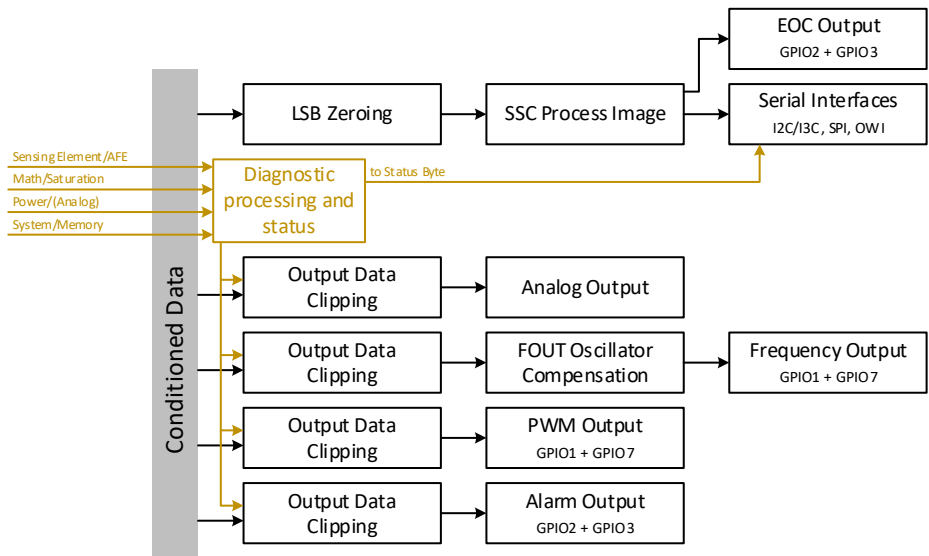


Figure 31: Sensor Signal Flow Chart from Input to Output

6.2 LSB Zeroing

All internal calculations are performed with higher precision than the selected ADC resolution, and the output results on digital interfaces are normalized for all channels except SSC CH3 (Third Logic Channel) before providing on the digital interfaces as defined by:

$$\text{DigitalOutputValue} = \text{Conditioned Data AND } (2^{\text{ADC Resolution}} - 1)$$

Equation 24

6.3 SSC Process Image

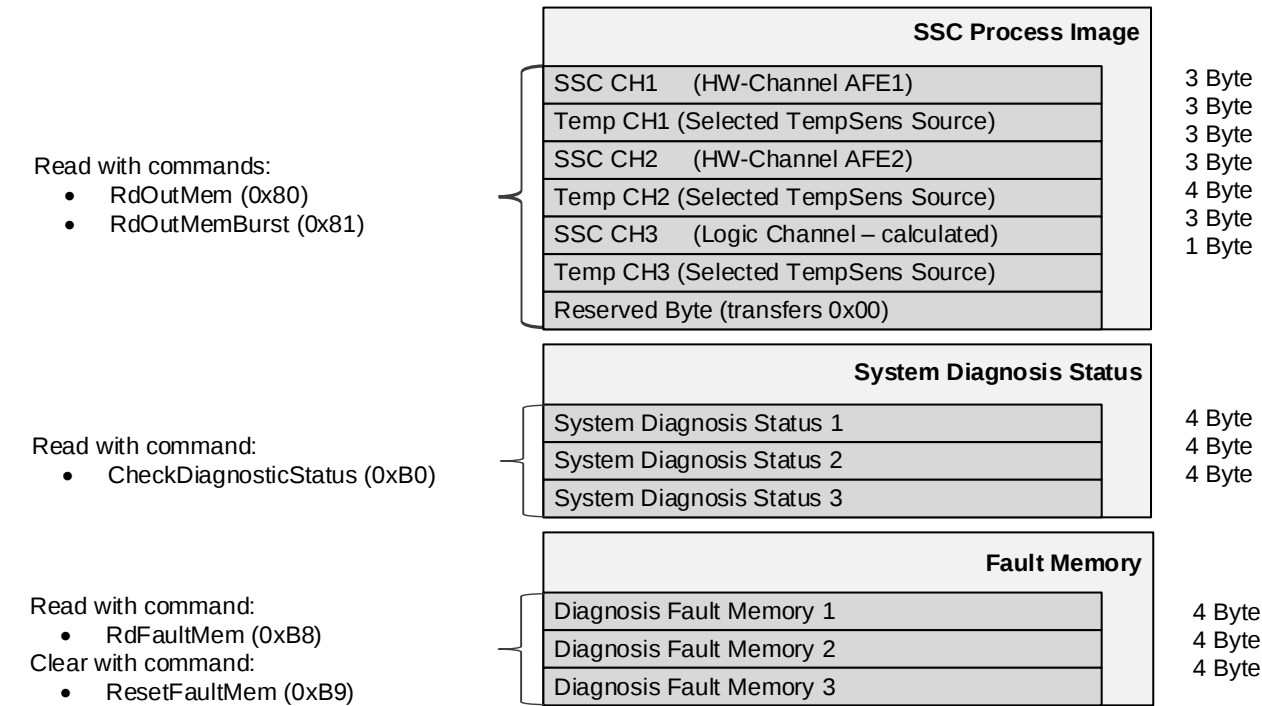


Figure 32: SSC Process Image, System Diagnosis Status and Fault Memory Map

ZSSC3281 handles all continuous process data communication with a host system through memory interfaces called SSC Process Image, System Diagnosis Status, and Fault Memory.

The data in the SSC Process Image is updated as soon as respective AFE measurements are completed, and the related sensor signal conditioning operations are carried out. It always reflects the most up-to-date known status of the connected sensor system. The SSC Process Image holds data of both main sensor, three temperature signals and for the third logic channel.

Status information from all activated system diagnosis checks are contained inside the System Diagnosis Status and the Fault Memory which allows the host system to check for the source of system failure states that were reported in the Status Byte of a previously received command response. The structure of the system diagnosis status words is described in section 7.2.

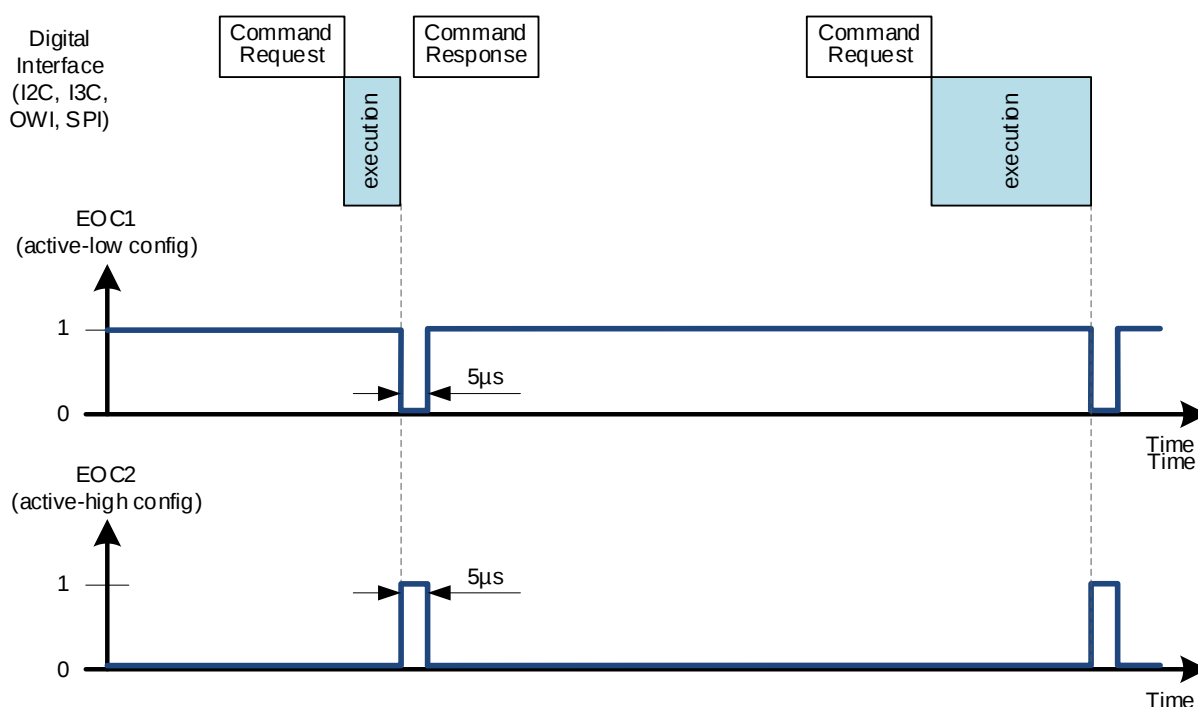
6.4 EOB/EOC/Alarm Functions

The Pins EOC/ALARM 1 (GPIO2) and EOC/ALARM 2 (GPIO3) can be configured to operate either as an end-of-busy (EOB) in Command and Sleep Mode, or end-of-conversion (EOC) transducer or as a configurable switch/alarm transducer for the respective SSC conditioned outputs of the main bridge sensors in Cyclic Mode.

To support different external logic, the global setting for polarity of the EOB/EOC/ALARM outputs can be configured as active high or active low (can be setup via GUI Configure\EOC/ALARM\Output Polarity).

6.4.1. EOB Function

The end-of-busy (EOB) function can be enabled as an additional functionality within Command Mode and Sleep Mode (setup via GUI Configure\System Control) to allow upper MCUs receiving interrupt signals after finishing ZSSC3281's internal command execution. If EOB is enabled, a short signal pulse of approximately 5 μ s wide (see Figure 33) is generated on enabled EOC pins.

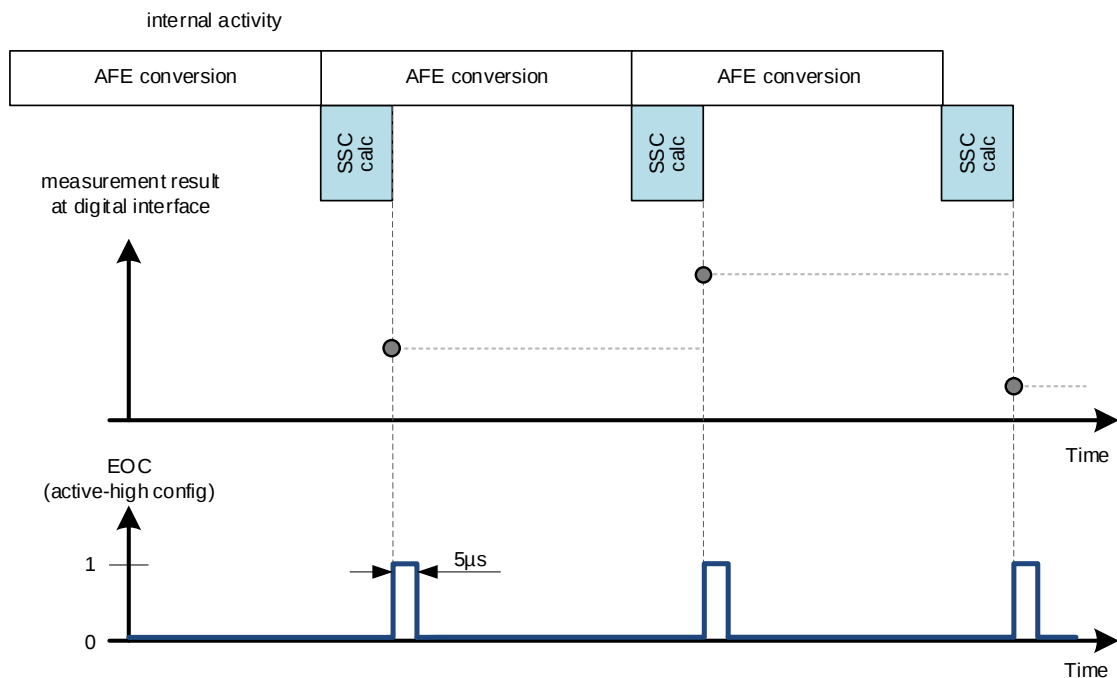


Note: timing relations are not to scale, they are qualitative illustrations only

Figure 33: EOB Behavior - Signalization of End-of-Busy

6.4.2. EOC Function

If the EOC output mode is active (can be setup via GUI Configure\EOC\ALARM\Selected Mode\EOC), an EOC event is signalled at the GPIO pin as soon as a new SSC-corrected measurement result of the bridge sensor is available for read out by the host system. The EOC signal pulse is approximately 5µs wide (see Figure 34).



Note: timing relations are not to scale, they are qualitative illustrations only

Figure 34: EOC Behavior - Signalization of End-of-Conversion

Important Notes:

- The EOC Output Mode is not available in AFE Dual Speed Mode.
- The EOC Output Mode is not available in PWM/FOUT Mode
- The EOC1 Output Mode is not available if the serial OWI interface is activated

6.4.3. ALARM Function

If the ALARM output mode is active (can be setup via GUI Configure\EOC\ALARM\Selected Mode\Alarm) further configuration options exist:

- Single threshold comparison vs. Window comparison
- Range definition for ALARM (above/below vs. inside/outside)
- Hysteresis setting
- Persistence setting

Figure 35 shows the ALARM output signalling in the possible four different modes. The dotted black lines reflect the behavior for zero hysteresis, while the dotted blue lines take a configured threshold hysteresis into account.

The lower charts of Figure 35 feature a special signal transient example. If the measurement result jumps from one sample to another from above the upper to below the lower alarm threshold (or vice versa), the alarm state remains the same since the logic conditions of the Window comparison mode permit this.

The configured hysteresis value (GUI tab Configure\EOC\ALARM\Hysteresis) defines the hysteresis half width or "offset". The total hysteresis width is effectively twice the configured hysteresis value.

The ALARM persistence can be set between 0 and 255. A persistence value >0 requires the signal to remain above or below the threshold for the selected number of consecutive pulses before the ALARM output state is changed. The value of 0 effectively disables the persistence feature and the logic checks for a single occurrence of the threshold condition only.

If AFE1 and AFE2 are running asynchronously, the EOC/ALARM outputs are also evaluated independently after the SSC operation was completed. In case of synchronous setup, the evaluations happen at about the same time but AFE1 is evaluated first.

The alarm thresholds and hysteresis values are stored in the respective CCP registers using the data format as shown in Table 20.

Table 20: Data Format of Alarm Thresholds and Hysteresis

Bit-Number:	23	22	21	20	...	2	1	0
Meaning, Weighting	2^0	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

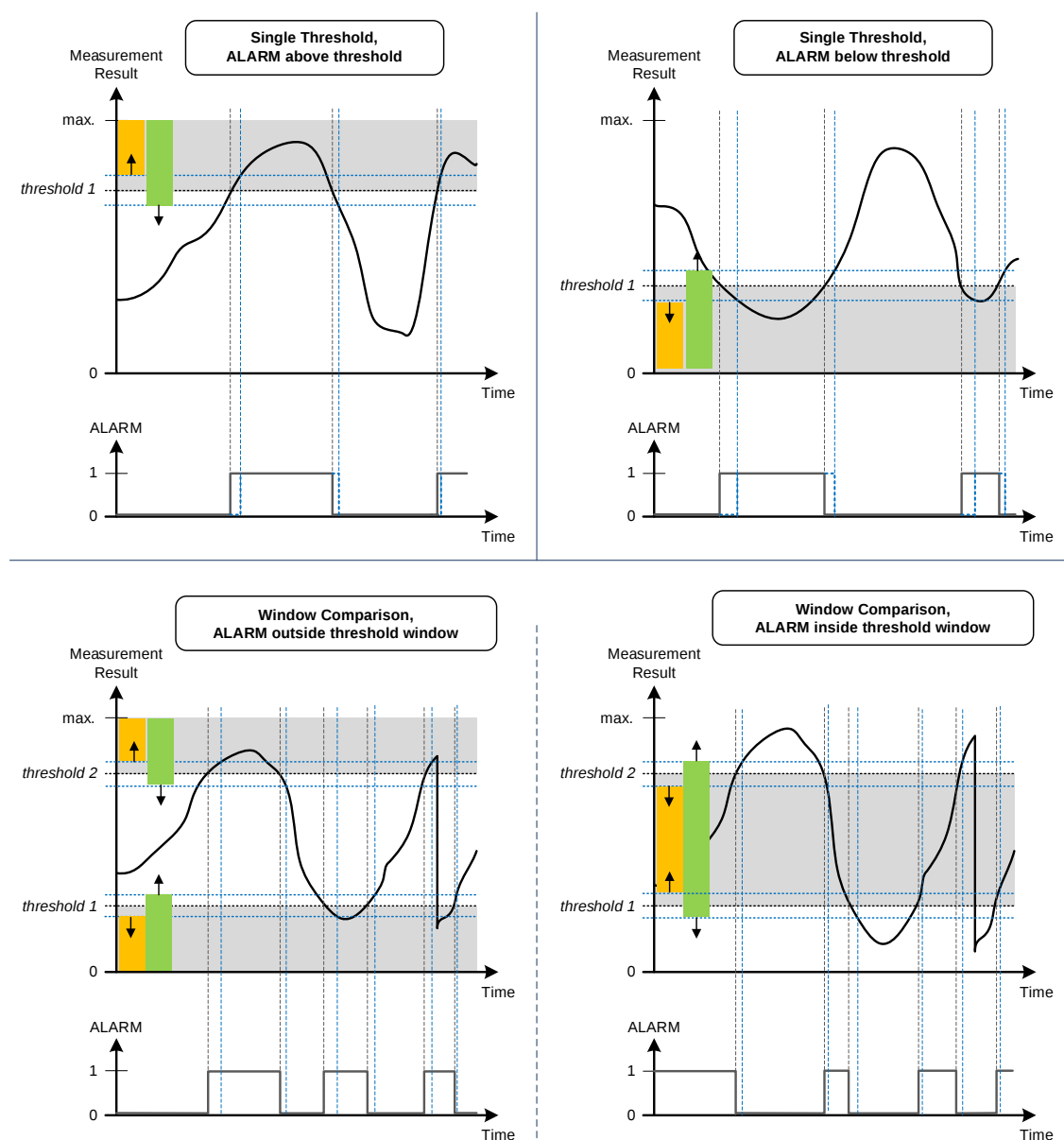


Figure 35: Behaviour of ALARM Feature in Four Different Modes

6.5 Output Data Clipping

The signaling of a diagnosis failure state can also be activated on the analog output AOUT or the digital outputs PWM/FOUT via GUI tab Diagnostic\General. If the signalization of Diagnostic State at AOUT and PWM/FOUT is enabled, discovered diagnostic failure states can be either mapped to the Upper or the Lower Diagnostic Range (UDR and LDR) of the output span (GUI tab Diagnostic\Sensor\AFE).

The boundaries of the upper and lower diagnostic ranges are configurable via the GUI tab Configure\Output Preprocess. They are typically set to 5% and 95% of the full-scale output level but can be modified to the application needs.

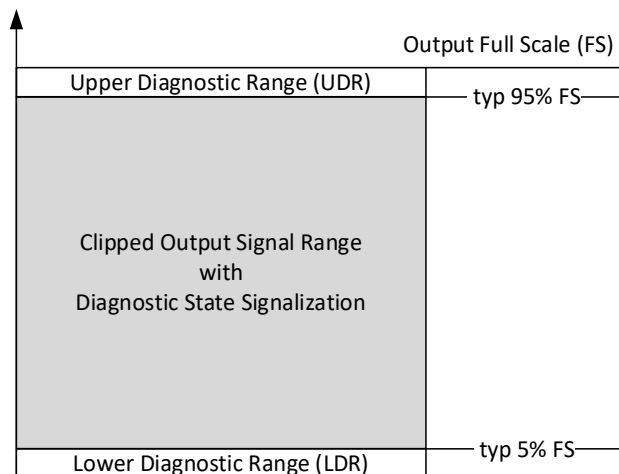


Figure 36: AOUT and PWM/FOUT Output Ranges with Active Diagnostic State Signalization

To prevent false interpretation of very large or very low output signals (UDR and LDR ranges), the conditioned data is clipped to fit into the remaining output range between UDR and LDR before it is forwarded to the AOUT and PWM/FOUT outputs.

Important Notes:

- There is no rescaling of the conditioned data performed at this stage.
If rescaling of the conditioned data to the clipped output signal range is required, use the Bridge Output Scaling feature (see section 5.4.) or use different target values during the SSC calibration process.
- The digital output data which is accessible on the serial interfaces (read from the SSC Process Image) is not clipped since a diagnosis failure condition is signaled there within the Status Byte.

6.6 FOUT Oscillator Compensation

Frequency output requires a stable base frequency. The internal oscillator provides the base frequency for frequency modulation (see section 9.1). To minimize the resulting temperature drift, it can be compensated via internal PTAT temperature sensor by the following compensation mathematics:

x	Corrected sensor signal selected for Frequency Output	Valid input range
y	Temperature compensated output signal for Frequency Output	0_{HEX} to $\text{FFFFFF}_{\text{HEX}}$
T_Raw_{PTAT}	Raw temperature reading of PTAT (after AZ correction)	$-7\text{FFFFFF}_{\text{HEX}}$ to $7\text{FFFFFF}_{\text{HEX}}$
Fm_SOT	Second-order term for frequency modulation	$-7\text{FFFFFF}_{\text{HEX}}$ to $7\text{FFFFFF}_{\text{HEX}}$
Fm_Gain	Gain term for frequency modulation	$-7\text{FFFFFF}_{\text{HEX}}$ to $7\text{FFFFFF}_{\text{HEX}}$
Fm_Offset	Offset term for frequency modulation	$-7\text{FFFFFF}_{\text{HEX}}$ to $7\text{FFFFFF}_{\text{HEX}}$

Note: The compensation mathematics requires enabling the internal PTAT temperature measurement within the AUX measurements.

All raw data and compensation coefficients supplied to the formulas are required in the 24-bit data format described in Table 21, Table 22, Table 23, and Equation 25.

Table 21: Data Format of Raw ADC Readings

Bit-Number	23	22	21	20	...	2	1	0
Meaning, Weighting	-2^0	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

Table 22: Data Format of Corrected SSC Results

Bit-Number	23	22	21	20	...	2	1	0
Meaning, Weighting	2^0	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

Table 23: Data Format of 32-bit SSC Coefficients

Bit-Number:	31	30	29	28	27	...	2	1	0
Meaning, Weighting	2^{-1}	2^0	2^{-1}	2^{-2}	2^{-3}	...	2^{-28}	2^{-29}	2^{-30}

$$y = \left[x \times \left(4 \times Fm_SOT \times T_Raw_{PTAT}^2 + Fm_Gain \times T_Raw_{PTAT} + Fm_Offset \right) \right]_0^{32-1}$$

Equation 25

7. Sensor and System Diagnosis

The ZSSC3281 Sensor and System Diagnosis function can detect several false conditions on externally connected sensors and monitor long term gain and offset drifts of the Analog front end. This makes ZSSC3281 well suited for sensing applications that require increased system reliability as well as for predictive maintenance supervision done by the host system.

7.1 Sensor and AFE Diagnostic Features

The supported Sensor and AFE Diagnostic features are summarized in Table 24.

Table 24: Sensor and AFE Diagnosis Functions

Monitored Input or Component	Failure Category	Failure Condition ¹
Main sensor bridge 1	INP or INN open	INP to INN resistance >125kΩ
	INP or INN shorted	INP to INN resistance <170Ω
Main sensor bridge 2	INP or INN open	INP to INN resistance >125kΩ
	INP or INN shorted	INP to INN resistance <170Ω
Temperature sensor T1	Short to Top (TOP)	T1 to TOP resistance <500Ω
	Short to Bottom (BOT)	T1 to BOT resistance <500Ω
	Open	T1 resistance >2MΩ, 500kΩ, 100kΩ
Temperature sensor T2	Short to Top (TOP)	T2 to TOP resistance <500Ω
	Short to Bottom (BOT)	T2 to BOT resistance <500Ω
	Open	T2 resistance >2MΩ, 500kΩ, 100kΩ
Temperature sensor T3	Short to Top (TOP)	T3 to TOP resistance <500Ω
	Short to Bottom (BOT)	T3 to BOT resistance <500Ω
	Open	T3 resistance >2MΩ, 500kΩ, 100kΩ
AFE1	Gain Drift	Gain check deviates by provided percentage from previously stored reference value
	Offset Drift	Offset check deviates by provided permillage from previously stored reference value
AFE1	Gain Drift	Gain check deviates by provided percentage from previously stored reference value
	Offset Drift	Offset check deviates by provided permillage from previously stored reference value

1. Typical values. Further specifications are provided in section 2.4.

For all active sensor inputs and AFEs, the checks can be enabled selectively on the GUI tab Diagnostic\Sensor AFE.

The AFE gain drift check employs an internally connected resistive DAC to create itself a defined input signal. The internal DAC can generate four different input voltages: 2mV, 10mV, 100mV, 200mV. The GUI proposes the most suitable setting based on other configurations made for the AFE. The selected voltage level is stored in the CCP.

In order to make proper use of the long-term AFE gain and offset drift checks, a device dependent reference value must be acquired and stored during the sensor calibration process. The GUI supports this via the 'Get' button which is located in front of the GainRef and OffsetRef fields.

Command B2_{HEX}, allows the test of all enabled sensor checks.

Table 25: Self Diagnostic Measurement Command

Command Code	Return	Description	Command Mode	Cyclic Mode
B4 _{HEX} followed by 0XYY _{HEX}	2 bytes	Self-Diagnostic Measure for AFE1 & AFE2 0X_{HEX} - AFE1: 00_{HEX} - AFE2: 01_{HEX} - YY_{HEX} – see table below	Yes	No
YY	Measurement		Return	
05 _{HEX}	External temperature sensor, T1, check short to top		0000_0000_0000_000X _{BIN}	
06 _{HEX}	External temperature sensor, T1, check short to bottom		0000_0000_0000_000X _{BIN}	
07 _{HEX}	External temperature sensor, T1, check open		0000_0000_0000_000X _{BIN}	
0A _{HEX}	External temperature sensor, T2, check short to top		0000_0000_0000_000X _{BIN}	
0B _{HEX}	External temperature sensor, T2, check short to bottom		0000_0000_0000_000X _{BIN}	
0C _{HEX}	External temperature sensor, T2, check open		0000_0000_0000_000X _{BIN}	
0F _{HEX}	External temperature sensor, T3 (pin GUARD), check short to top		0000_0000_0000_000X _{BIN}	
10 _{HEX}	External temperature sensor, T3 (pin GUARD), check short to bottom		0000_0000_0000_000X _{BIN}	
11 _{HEX}	External temperature sensor, T3 (pin GUARD), check open		0000_0000_0000_000X _{BIN}	
1B _{HEX}	Main bridge sensor connection check open		0000_0000_0000_000X _{BIN}	
1C _{HEX}	Main bridge sensor connection check short		0000_0000_0000_000X _{BIN}	
27 _{HEX}	Offset drift (calculated diagnosis result)		0000_0000_0000_000X _{BIN}	
28 _{HEX}	Gain drift (calculated diagnosis result)		0000_0000_0000_000X _{BIN}	

7.2 Sensor and System Diagnosis Status

Table 26: System Diagnosis Status Mapping to Status Byte

	Meaning	Class ¹	Representation in Status Byte of Command Response				@AFE1	@AFE2	System Diagnosis Status	
			bit[1]	bit[0]	bit[6]	bit[2]			Word#	Bit#
			Sensor Fault	Saturation ²	Power Supply OK	Memory Error				
	reserved									0
bridge sensor connection check	AFE1 sensor broken connection check → INP1 or INN1 open: $R > R_{open}$	S	X				x			1
	AFE1 sensor shorted connection check → INP1 – INN1 shorted: $R < R_{short}$	S	X				x			2
	AFE1 sensor leakage check: INP1 to VSS	S	X				x			3
	AFE1 sensor leakage check: INN1 to VSS	S	X				x			4
	AFE1 sensor signal range check: INP1	S	X				x			5
	AFE1 sensor signal range check: INN1	S	X				x			6
	AFE2 sensor broken connection check → INP2 or INN2 open: $R > R_{broken}$	S	X					x		7
	AFE2 sensor shorted connection check → INP2 – INN2 shorted: $R < R_{short}$	S	X					x		8
	AFE2 sensor leakage check: INP2 to VSS	S	X					x		9
	AFE2 sensor leakage check: INN2 to VSS	S	X					x		10
	AFE2 sensor signal range check: INP2	S	X					x		11
	AFE2 sensor signal range check: INN2	S	X					x		12
	Reserved									13
	Reserved									14
	Reserved									15
(external) temperature sensor connection check	AFE1 temperature sensor broken connection check → T1 open: $R > R_{T_OPEN}$	S	X				x			16
	AFE1 temperature sensor shorted connection check → T1 – TOP shorted: $R < R_{T_SHORT}$	S	X				x			17
	AFE1 temperature sensor shorted connection check → T1 – BOT shorted: $R < R_{T_SHORT}$	S	X				x			18
	AFE2 temperature sensor broken connection check → T2 open: $R > R_{T_OPEN}$	S	X					x		19
	AFE2 temperature sensor shorted connection check → T2 – TOP shorted: $R < R_{T_SHORT}$	S	X					x		20
	AFE2 temperature sensor shorted connection check → T2 – BOT shorted: $R < R_{T_SHORT}$	S	X					x		21
	AFE2 temperature sensor broken connection check → T3 open: $R > R_{T_OPEN}$	S	X					x		22
	AFE2 temperature sensor shorted connection check → T3 – TOP shorted: $R < R_{T_SHORT}$	S	X					x		23
	AFE2 temperature sensor shorted connection check → T3 – BOT shorted: $R < R_{T_SHORT}$	S	X					x		24
	Reserved									25...31

	Meaning	Class ¹	Representation in Status Byte of command response				@AFE1	@AFE2	System Diagnosis Status	
			bit[1]	bit[0]	bit[6]	bit[2]			Word#	Bit#
			Sensor Fault	Saturation ²	Power Supply <u>OK</u>	Memory Error				
parametric checks in analog sensor path	AFE1 Gain Drift	S	X				x		1	0
	AFE1 Offset Drift	S	X				x			1
	AFE2 Gain Drift	S	X					x		2
	AFE2 Offset Drift	S	X					x		3
	Reserved									4 to 31
parametric checks in digital data path	SSC calculation unit OR raw output data saturation channel 1, bridge sensor data	S		X					2	0
	SSC calculation unit OR raw output data saturation channel 1, temperature sensor data	S		X						1
	SSC calculation unit OR raw output data saturation channel 2, bridge sensor data	S		X						2
	SSC calculation unit OR raw output data saturation channel 2, temperature sensor data	S		X						3
	SSC calculation unit: channel 3, bridge sensor data	S		X						4
	SSC calculation unit OR raw output data saturation channel 3, temperature sensor data	S		X						5
	Reserved									6 to 31

1. Failure classification S: Safe Failure, system response via digital interfaces still reliable.
2. Saturation is cleared in system diagnosis status memory before each command execution except 0x80 and 0x8 Read Output Memory Commands, and 0xA8 Start Sleep Mode command and 0xA9 Start Command Mode.

Since the SSC Process Image data is continuously updated as soon as new measurement data becomes available, it may happen that Diagnosis Faults disappear before the host has read them via the CheckDiagnosticStatus command 0xB0.

To allow system failure detection at a later point in time, ZSSC3281 additionally stores all appeared system diagnosis failures in a separate volatile fault memory. The fault memory has the same organization as the system diagnosis status memory and becomes cleared only via ClearFaultMem (0xB9) command or a system reset. The fault memory can be read via RdFaultMem (0xB8) command.

8. Analog Output

The conditioned and post processed output data of one of following channels can be made available as analog output signal at the Analog Output AOUT

- Bridge Sensor Channel 1
- Bridge Sensor Channel 2
- Third Logic Channel
- Temperature Channel 1
- Temperature Channel 2
- Temperature Channel 3

Depending on the configuration of the Analog Output Driver, different output modes, like ratiometric voltage output, absolute voltage output and current mode output are supported.

8.1 Analog Output Driver Modes

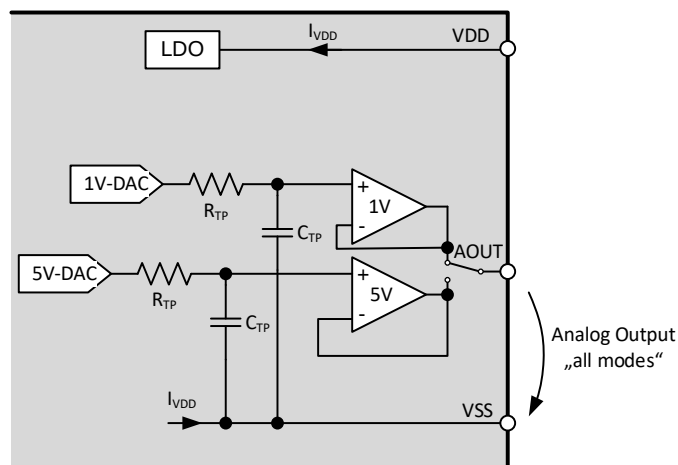


Figure 37: Block Schematic AOUT Driver

The Analog Output Driver contains two separate output buffers, one for a full-scale voltage of 1V and another one for full scale voltages ranging up to VDD. The following functional assignments apply:

- 1V buffer: 1V absolute Voltage Mode
2-wire current loop mode
3-wire current loop mode
- 5V buffer: Ratiometric Voltage Mode
5V absolute Voltage Mode
10V absolute Voltage Mode

The 5V buffer offers a programmable output current limiting function which is not available for the 1V buffer. The 5V buffer requires the VDD to be in the range between 2.7V and 5.5V for proper operation.

8.2 Analog Output Configuration

8.2.1 Negative Voltage Generation for AOUT

To support True-0V signals on the Analog Output (AOUT), ZSSC3281 provides an option to externally supply a negative voltage rail for the AOUT buffer at VDDN. VDDN supply specifications are shown in Table 27. The external circuitry must ensure to not generate a VDDN voltage of less than -0.5V to prevent latchup conditions for the internal circuitry.

The negative VDDN voltage can also be generated by an internal charge pump circuit. The internal charge pump can be activated through GUI field: Configure\AOUT\VDDN Charge Pump. The field Configure\AOUT\VDDN Load allows to set a maximum current that the internal charge pump can supply.

The activation of the internal charge pump at VDDN considerably increases the power consumption of ZSSC3281 and needs to be carefully considered in applications where current consumption of the sensor device (sensor + ZSSC3281) is a critical parameter. The VDDN charge pump can only be used for VDD $\geq$ 2.7V.

If no True-0V signals are required at AOUT, the user must disable the VDDN charge pump in the GUI and directly connect VDDN with VSS on PCB level.

The charge pump function is only available for all AOUT Operation Modes with Voltage Output. The charge pump circuit requires an external buffer capacitor C_{VDDN} and a Schottky Diode to work properly.

Table 27: Parameter Negative Voltage for AOUT

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD _{CP}	VDD operating range of internal charge pump		2.7		5.5	V
VDDN	Negative voltage supply for analog output (AOUT)	Internally generated, requires activation of VDDN charge pump		V _{ExtSchottky}		V
		Externally supplied	0	-0.3V	-0.5V	V
I _{VDDN}	Available charge pump load current	Programmable in 4 steps.			0.5 1 3 5	mA
I _{VDD}	Additional charge pump current consumption at VDD	0.5mA load current	0.5	4.5	5	mA
		• 1.0mA load current	1	9	10	
		• 3.0mA load current	3	15.5	17	
		5.0mA load current	5	25	30	
C _{VDDN}	Buffer capacitance at pin VDDN			1		μF
V _{FW-Schottky}	Forward voltage of external Schottky diode			0.3	0.5	V

8.2.2. Ratiometric Voltage Mode

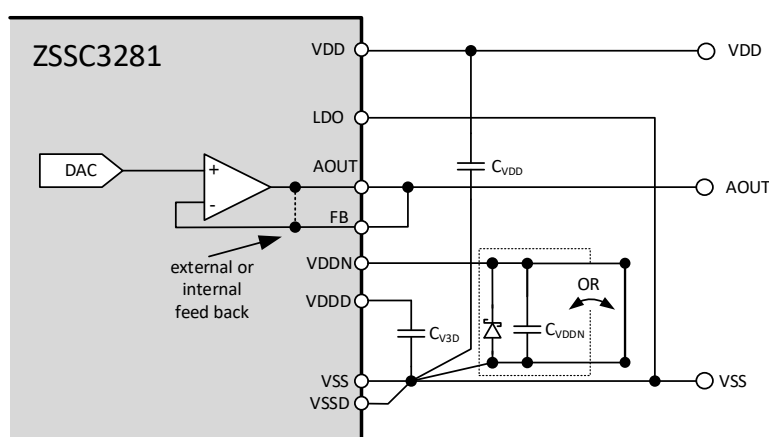


Figure 38: Ratiometric Output Mode Configuration at AOUT

The SSC output can be ratiometric mapped to 0 to VDD range with the application circuit shown in Figure 38 and activation of the Ratiometric Voltage Mode in the GUI via Configure\AOUT\Operation Mode\Ratiometric Voltage.

In Ratiometric Output Mode the reference voltage for the AOUT DAC is identical to the VDD level.

8.2.3. 5V Absolute Voltage Mode

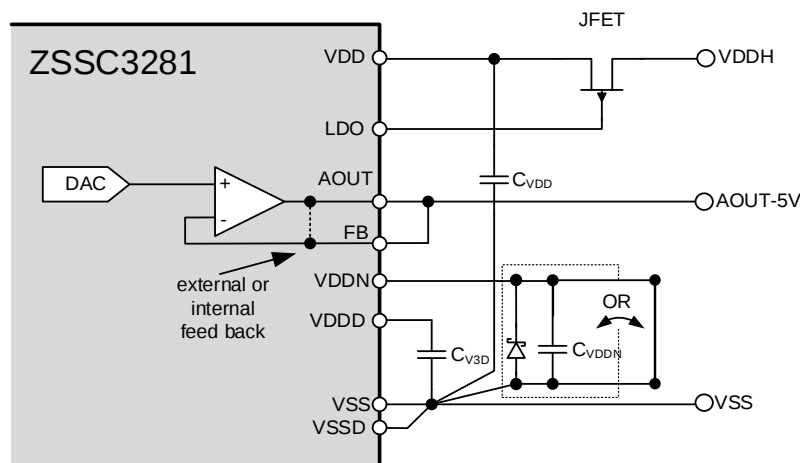


Figure 39: 5V Absolute Output Voltage Configuration at AOUT

The SSC output can be mapped to 0V to 5V voltage range with the application circuit shown in Figure 39 and activation of the 5V Absolute Voltage Mode in the GUI via Configure\AOUT\Operation Mode\Absolute Voltage 0V – 5V. This AOUT mode requires the external regulator supply configuration to be active in the GUI with the regulated VDD set to 5.25V.

The applied reference voltage for the AOUT DAC is directly derived from VDD through a digital factory calibration coefficient.

8.2.4. 10V Absolute Voltage Mode

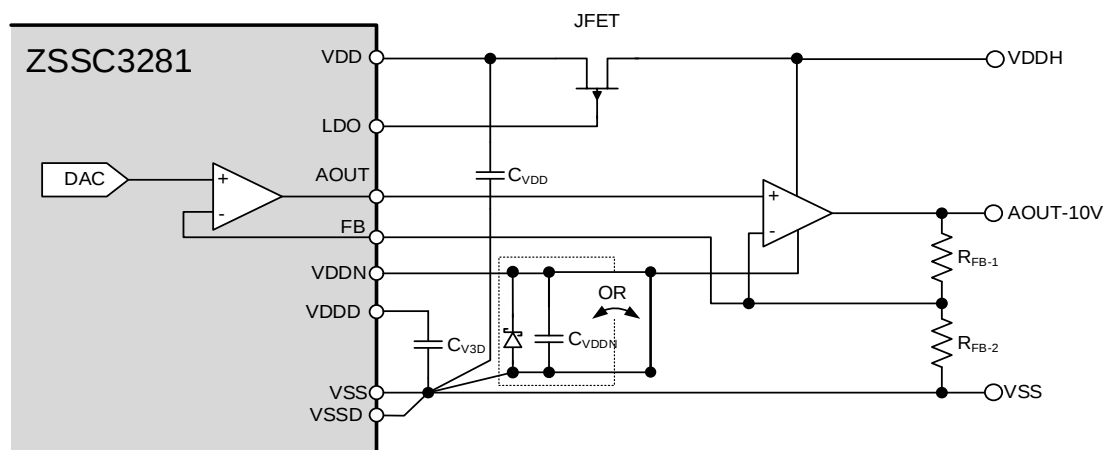


Figure 40: 10V Absolute Output Voltage Configuration at AOUT

The SSC output can be mapped to 0 to 10V voltage range with the application circuit shown in Figure 40 and activation of the 10V Absolute Voltage Mode in the GUI via `Configure\AOUT\Operation Mode\Absolute Voltage 0V – 10V`. This AOUT mode requires the external regulator supply configuration to be active in the GUI with the regulated VDD set to 5.25V.

The applied reference voltage for the AOOUT DAC is directly derived from VDD through a digital factory calibration coefficient. In order to obtain a 0V to 10V output signal at AOOUT-10V the following condition must be met: $R_{FB-1} = R_{FB-2}$. The external Operational Amplifier should be offset compensated.

8.2.5. 1V Absolute Output Voltage Mode

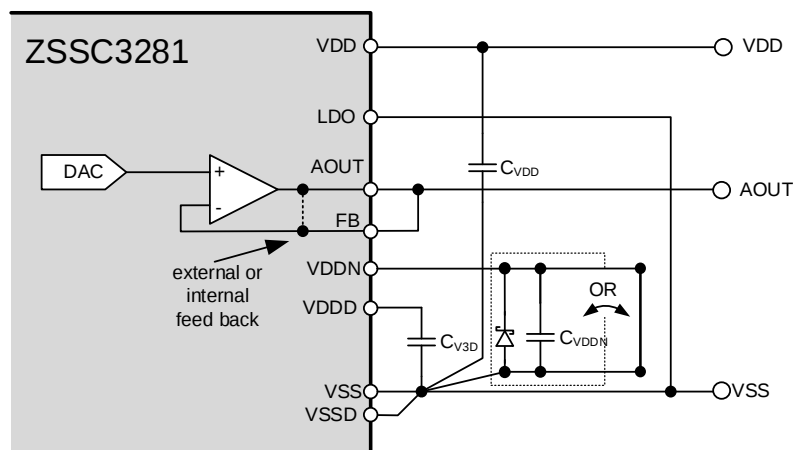


Figure 41: 1V Absolute Output Voltage Configuration at AOUT

The SSC output can be mapped to 0V to 1V voltage range with the application circuit shown in Figure 41 and activation of the 1V Absolute Voltage Mode in the GUI via `Configure\AOUT\Operation Mode\Absolute Voltage 0V – 1V`.

The applied reference voltage for the AOUT DAC is generated from an internal factory calibrated bandgap source.

8.2.6. 2-Wire Current Loop Mode

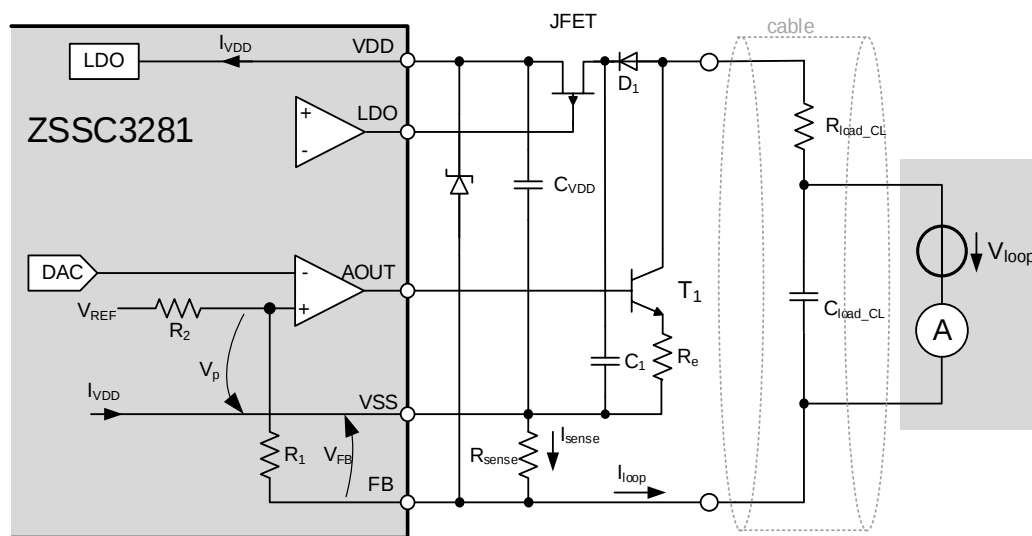


Figure 42: 2-Wire Current Loop Configuration at AOUT

Table 28: External Components in 2-Wire Current Loop Mode

Symbol	Parameter	Min	Typ	Max	Unit
R _{sense}	Feedback resistor		42		Ω
R _e	Emitter resistor		150		Ω
T ₁	Bipolar Transistor	For example, BCX56-16			

The ZSSC3281 can be operated in two wire current loop configuration as shown in Figure 42. It requires the activation of 2-Wire Current Loop Mode in the GUI via Configure\AOUT\Operation Mode\2-Wire Current Loop. Because the signal current is typically expected to range from 4mA to 20mA on the 2-wire cable, the total operating current of the ZSSC3281 IC and the connected resistive bridges must stay below 4.0mA. To achieve this, the clock frequency of ZSSC3281 needs to be reduced to 1MHz, which impacts input to output signal latency and selectable

AFE resolutions. 2-Wire Current Loop Mode also requires the activation of the external JFET pre-regulator. This, as well as the system clock frequency reduction are ensured by the GUI when 2-Wire Current Loop is selected at AOUT tab.

Besides production calibrated parameters of ZSSC3281, the value of the external resistor R_{sense} also determines the available min/max signal current range on the cable. To compensate for tolerances of R_{sense} , the GUI offers a post calibration option to calibrate the current loop current to the required absolute accuracy. The function recalculates the default CCP parameters 'CL2_Offset' and 'CL2_Delta' based on the entered R_{sense} (typical value), required and measured I_{min} and I_{max} values. To activate the optimized values, a Write Memory operation needs to be triggered by the user. 'CL2_Offset' and 'CL2_Delta' determine the swing of the AOUT voltage to cover the 4mA to 20mA current output signal.

The user can select the signal which shall be mapped to the 2-Wire Current Loop output via the drop-down menu Configure\AOUT\AOUT Pin Mapping.

8.2.7. 3- Wire Current Loop Mode

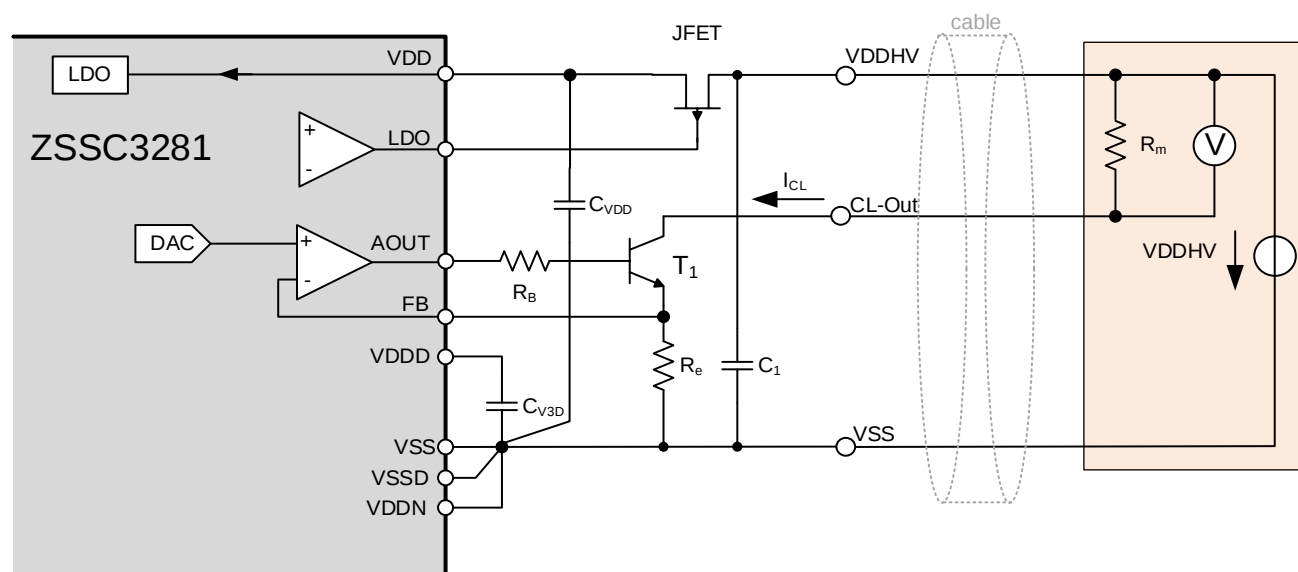


Figure 43: 3-wire NPN Current Loop Configuration at AOUT

Table 29: External Components in 3-Wire Current Loop Mode

Symbol	Parameter	Min	Typ	Max	Unit
R_e	Emitter resistor		43		Ω
R_b	Base resistor		4700		Ω
T_1	Bipolar Transistor	For example, BCX56-16			

The SSC output can be mapped to an input current at CL-Out in the application circuit shown in Figure 43 and by activation of the 3-Wire Current Loop Mode in the GUI via Configure\AOUT\Operation Mode\3-Wire Current Loop.

The signal current at CL-Out is typically required to range from 4 to 20mA. The available min/max signal current range at CL-Out depends on the actual value of the external emitter resistor R_e .

To compensate for tolerances of R_e , the GUI offers a post calibration option to calibrate the current loop current to the required absolute accuracy. The function recalculates the default CCP parameters 'CL3_Offset' and 'CL3_Delta' based on the entered R_e (typical value), required and measured I_{min} and I_{max} values. To activate the optimized values, a Write Memory operation needs to be triggered by the user. 'CL3_Offset' and 'CL3_Delta' determine the swing of the AOUT voltage to cover the 4mA to 20mA current output signal.

The user can select the signal to map to the 3-Wire Current Loop output via the drop-down menu Configure\AOUT\AOUT Pin Mapping.

9. Digital Outputs/Output Modulation

The conditioned and post processed output data of two of the following channels can be made available as modulated digital output signal at the pins FOUT/PWM_1 (GPIO1) and FOUT/PWM_2 (GPIO7)

- Bridge Sensor Channel 1
- Bridge Sensor Channel 2
- Third Logic Channel
- Temperature Channel 1
- Temperature Channel 2
- Temperature Channel 3

The channel assignment to the output pins and the type of output modulation can be selected in the GUI via Configure\DOOUT tab. There will be two types of output modulation supported:

- Frequency Modulation
- Pulse Width Modulation

9.1 Frequency Modulation

The minimum and maximum frequencies of the frequency modulation output can be configured via GUI on the Configure\DOOUT tab.

The frequency accuracy of the Frequency Modulation Output is determined by the frequency accuracy of the internal oscillator. Compensation mathematics for temperature drift of the oscillator is described in section 6.6.

Table 30: FOUT Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FOUT _{MIN}	Minimum output frequency		100		255	Hz
FOUT _{MAX}	Maximum output frequency		1000		10000	Hz
FOUT _{ERR}	Frequency error	FOUT feature operated with non-compensated internal oscillator clock	-5%		5%	

9.2 Pulse Width Modulation

PWM can be enabled and configured via GUI on the Configure\DOOUT tab. PWM base frequency can be adjusted according to Table 31.

Table 31: PWM Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PWM _{BaseFreq}	PWM Base Frequency	Stepsize: 500Hz in range 0.5kHz to 15kHz	0.2	0.5	15	kHz

10. Digital Interfaces

10.1 Serial Interfaces

For sensor data read out, ZSSC3281 supports three digital interface protocols in slave mode operation:

- I2C/I3C
- SPI
- OWI (One-Wire-Interface)

Digital slave interfaces do not initiate data communication with the master system themselves but have to quickly react on arbitrary received read/write requests from the master.

To maintain short response times in continuous Cyclic Mode operation, ZSSC3281 is equipped with a dedicated DMA controller, which can read the content of the SSC Process Image (see section 6.6) without interaction of the ARM MCU.

The DMA controller supports one active digital interface at the time. After reset, the DMA controller activates and locks the serial interface for further communication that first received a valid telegram. A telegram is valid if:

- the address match was pass for I2C/I3C or OWI and the first 8 bit of telegram data were received
- the Slave Select (SS) was activated for SPI and first 8 bit of telegram data were received on MOSI

As soon as one of the three interfaces was locked by DMA controller, potential data streams from the other interfaces are blocked. A different interface can only be selected after reset of ZSSC3281.

10.1.1. Command/Response Format

All three interfaces operate on the same command request and response format. The number of data bytes which need to follow the command byte in the command request or are returned after the Status Byte in command response, assuming the command execution was completed, is specific to the command code.

Table 32: Command Request Format

Command	Command Byte								Data Bytes
	7	6	5	4	3	2	1	0	
Valid Command	8-bit command								[Data Bytes]

Table 33: Command Response Format

Command Response	Status Byte								Data Bytes	
	7	6	5	4	3	2	1	0		
Previously received command in execution, response pending, New command not accepted, retry later	Telegram Error Flag	0	Power Supply OK	Busy Flag	1	SSC Mode 00: Command Mode 01: Cyclic Mode 10: Sleep Mode 11: Boot/Diagnosis Mode	Memory Error	Sensor Connection Fault	Saturation ¹	NONE
Command successfully processed		0			0					[Data Bytes]

1. Cleared before each command execution except for 0x80 and 0x81 Read Output Memory commands, 0xA8 Start Sleep Mode command, and 0xA9 Start Command Mode.

A list of supported command codes, the number of command and response data bytes and the command function description can be found in section 10.2.1.

If a command is still processed by the ZSSC3281 when the response read starts, the BusyFlag of the Status Byte is set and no response data is returned. The response data stream only contains a repeated Status Byte until the transaction is ended. The BusyFlag within the Status Byte changes as soon as the command execution is completed.

10.1.2. Advanced Error Response

Beside the command and response format there is an option for an advanced error response. This option can be enabled in the GUI at the tab Configure\System Control and supports failure detection during communication with ZSSC3281.

If this feature is enabled, it will replace the Status Byte with an Error Response Byte in case that a command error as shown in Table 34 was detected. This Error Response Byte will be repeated continuously as long as the host requests data. By this replacement it can easily be detected if a command error was detected since the MSB of the error response byte is set. MSB is cleared in case of a normal Status Byte.

Table 34: Command Response Format

Command Status	Error Response Byte (MSB always set)	
	Error Code	Interpretation of Error Code
Command unknown in Cyclic Mode	80 _{HEX}	Not Successful
Command CRC Byte aborted/missing (if protocol CRC was enabled)	90 _{HEX}	Incomplete
Command CRC failed (only possible if protocol CRC was enabled)	82 _{HEX}	CRC Error
Expected Data CRC Byte aborted/missing (only possible if protocol CRC was enabled)	90 _{HEX}	Incomplete
Data CRC failed (only possible if protocol CRC was enabled)	82 _{HEX}	CRC Error
Mandatory data aborted	90 _{HEX}	Incomplete
Command not authorized	A0 _{HEX}	Not Authorized
Mandatory data not in range	B0 _{HEX}	Argument Error
Command failed or not known (if in Command)	80 _{HEX}	Not Successful

10.1.3. I2C/I3C

ZSSC3281 supports I2C communication in StandardMode, FastMode, FastMode+, and it supports high speed communication in I3C Single Data Rate (SDR) Mode on I2C SCL and I2C SDA pins. The I2C/I3C interface is listening to receive a telegram after system startup or system reset as long as the SPI Slave Select (pin SPI SS) signal is not active.

I2C/I3C communication mode is selected and locked after I2C/I3C address match was pass and the first 8 bit of telegram data were received.

The interface settings, and a selection whether to use the traditional I2C or the advanced I3C communication mode, can be made in the GUI at the tab Configure\Serial Interfaces in section I2C/I3C.

I3C is an MIPI standard (<https://www.mipi.org/specifications/i3c-sensor-specification>) which is based on the traditional I2C protocol but extends the physical layer and the protocol layer towards higher communication speeds and improved management of the slave communication parameters by the I3C master. It allows In-Band Interrupts through which an I3C slave can signal an interrupt request to the I3C master via the SCL/SDA lines. Inband Interrupts are not supported by ZSSC3281.

Table 35: I2C/I3C Interface Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SlvAddr	I2C slave address Static I3C address	ZSSC3281 delivery default		0x3C		
f _{SCL}	Interface clock	I2C Mode	0.1		1.0	MHz
		I3C Mode	0.1		12.5	MHz
D _{I2C}	Duty cycle		33	–	50	%

Timing and protocol details of the I2C communication in Standard Mode, Fast Mode, and Fast Mode+ are given in I2C-Bus Specification, Rev.6, UM10204. SCL Clock Stretching is not supported by ZSSC3281.

In I2C/I3C Mode, each Command Request follows the structure shown in Figure 44. Only the number of Data Bytes needed by the command must be sent.

Command Request (I2C/I3C Write)

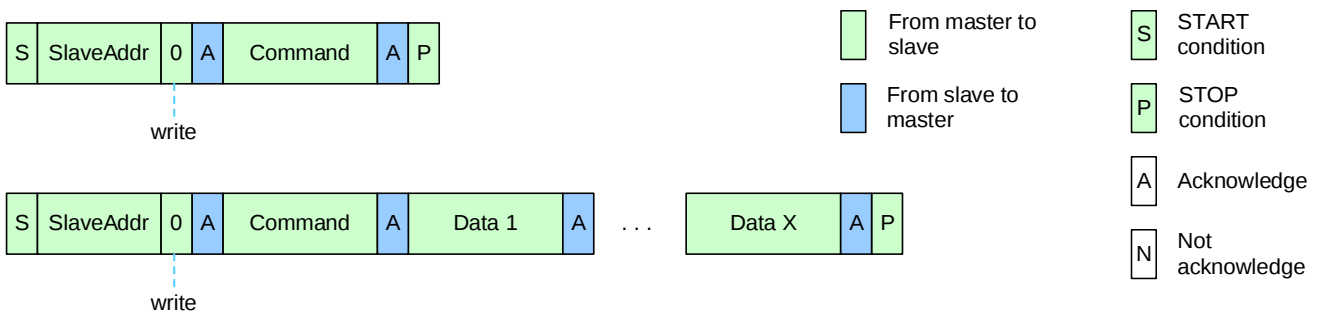


Figure 44: I2C/I3C Command Request

The different options for a response request are shown in Figure 45.

Read Data (I2C/I3C Read)

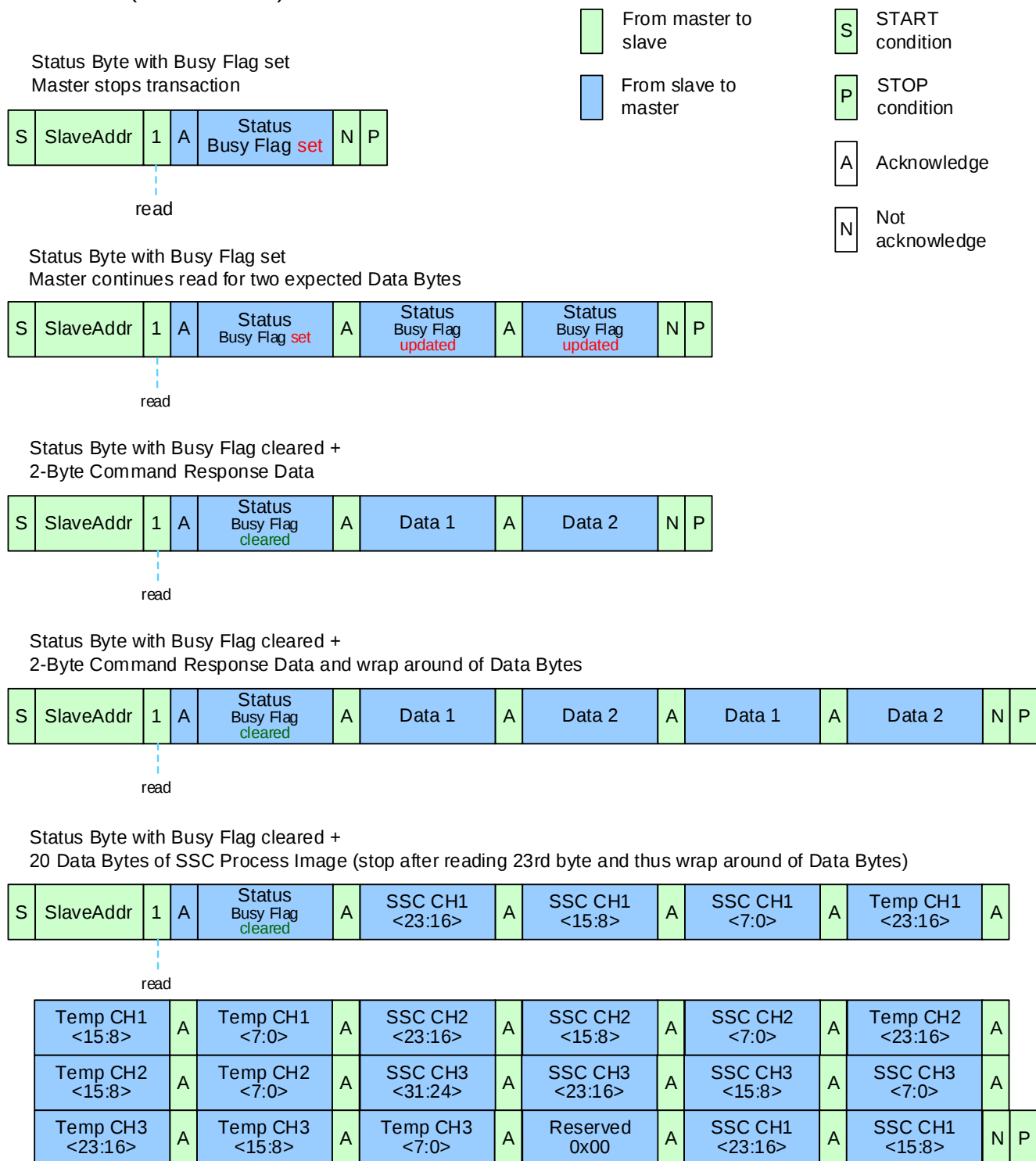


Figure 45: I2C / I3C Response Request

10.1.4. SPI

ZSSC3281 supports SPI communication on the SPI SCLK, SPI MOSI, and SPI MISO pins if the SPI slave select signal is active at the SPI SS pin and no other serial interface was locked yet after reset or power-on.

An active SPI SS signal connects the SPI SCLK and SPI MOSI pins to the SPI slave interface at the DMA controller and disconnects the I2C/I3C slave. As soon as the first 8 bit of data received on MOSI line, the SPI interface is locked as communication interface until the next reset or power-on of the ZSSC3281.

The polarity of the SPI slave select signal is active low by delivery default. It can be changed to active high at the Serial Interfaces tab of the GUI Configure\Serial Interfaces\SPI Slave Select Polarity. The polarity and the phase of the SPI clock can be changed via 'CPHA' and 'CPOL' selection fields at the same GUI tab.

The different combinations of polarity and phase are illustrated in Figure 46 and Figure 47. See Table 36 for the timing parameters.

CPHA=0

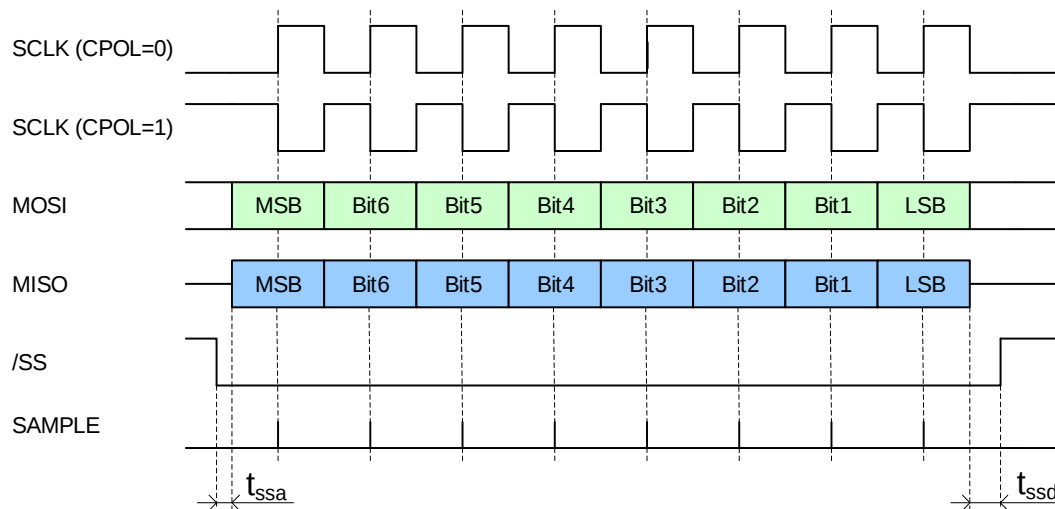


Figure 46: SPI Configuration CPHA=0

CPHA=1

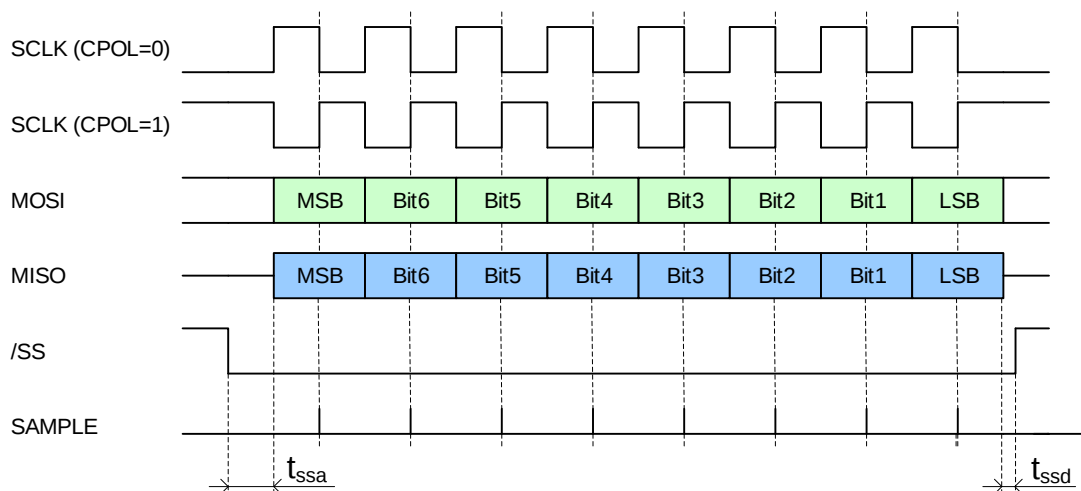


Figure 47: SPI Configuration CPHA=1

Table 36: SPI Interface Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCLK}	Interface clock		0.05	1	12	MHz
D_{SPI}	Duty cycle		40	50	60	%
SR_{SPI}	Input rising and falling edge slew rate		0.26	–	1	V/ns
t_{ssa}	Delay time between SS-activation edge and first edge of SLCK, MOSI or MISO	"Typical" is for $f_{SCLK} \leq 3\text{MHz}$ operation	62.5	–	–	ns
t_{ssd}	Delay time between SS-deactivation edge and last edge of SLCK, MOSI or MISO			50	–	ns
t_{ss}	Delay between SS-deactivation edge of last command and of SS-activation edge for next command		10	–	–	μs

In SPI Mode, each command request follows the structure shown in Figure 48. Only the number of data bytes needed by the command must be sent.

A SPI transaction is started with activation of SPI SS and it is ended with deactivation of SPI SS. A new command request can only be sent at the start of a new transaction, which begins after SPI SS changed from inactive to active state.

Command Request

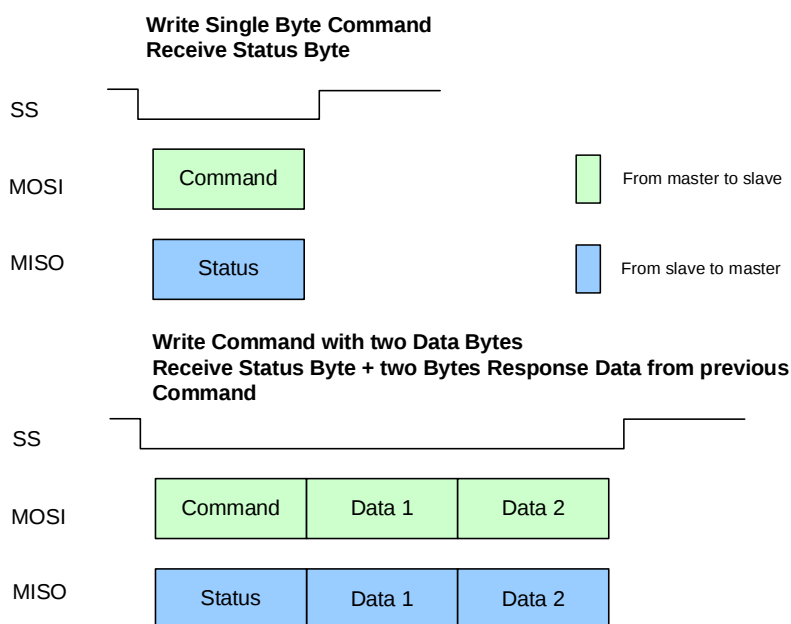


Figure 48: SPI Command Request

In contrast to the I2C/I3C interface the SPI interface supports full duplex communication. Hence, a new command request can already be sent on the MOSI line while response data from the previous command request is returned on the MISO line. According to Figure 48 and Figure 49 ZSSC3181 always responds with Status Byte, even at the very first reading.

If the response data from the previous call is read without triggering a new command request in parallel, the NOP command must be sent on the MOSI line in the first telegram byte of the transaction as shown in Figure 49.

Read Data

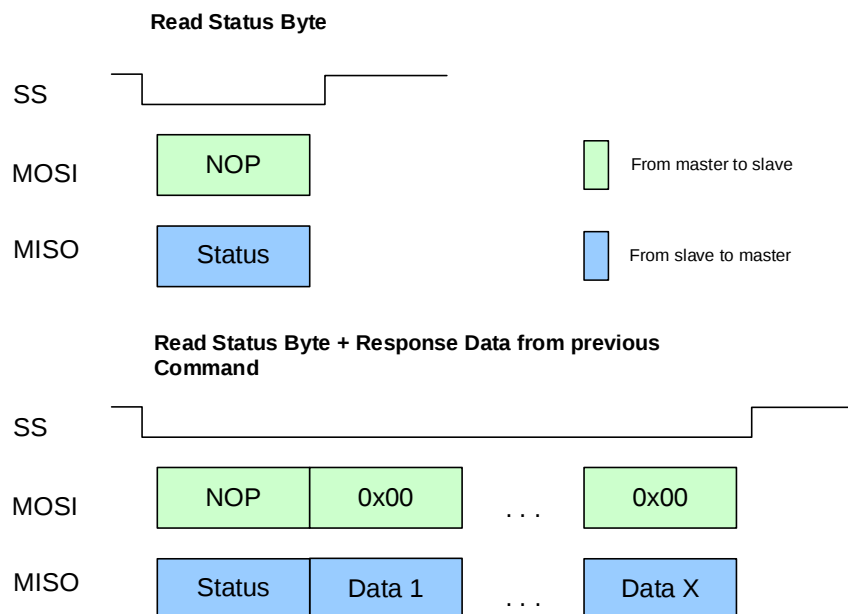


Figure 49: SPI Read Data

10.1.5. One-Wire-Interface

ZSSC3281 employs a one-wire digital interface (OWI) concept. The communication principle of the OWI interface is derived from the I2C protocol.

An advantage of the OWI is that it enables “end of line” calibration, no additional pins are required to digitally calibrate a finished assembly sensor module. Although the OWI is integrated mainly for calibration, it can also be used to read out the calibrated sensor signal continuously or retrieve diagnostic detail information.

The OWI driver and the OWI receiver are usually connected both to the analog output signal pin AOUT. The mode switching at AOUT between Analog Output Mode and OWI Communication Mode is controlled via different selectable OWI operation modes that are described in section 10.1.5.1.

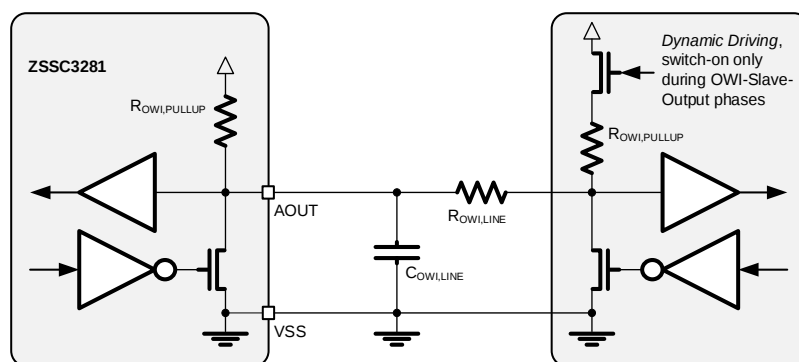


Figure 50: General Block Schematic of the OWI Interface

Some Analog Output configurations, like 2-Wire and 3-Wire Current Loop Mode and the 10V Absolute Voltage Mode require a second OWI input pin (OWI-IN2) because the external AOUT circuitry does not allow to drive a digital signal from an external OWI master into the AOUT pin. A respective application schematic is provided in section 13.3.

The OWI protocol is defined as follows:

- **Idle state**
During inactivity of the bus, the OWI line is pulled up to the supply voltage V_{DD} by an external resistor.
- **Start condition**
When the OWI line is in idle mode, a low pulse with a minimum width of $t_{OWI,START} \geq 10\mu s$ and then a return to high indicates a start condition. Every request must be initiated by a start condition sent by a master. A master can generate a start condition only when the OWI line is in idle mode.
- **Stop condition**
A constant level at the OWI line (no transition from low to high or from high to low) for at least twice the period of the last transmitted valid bit indicates a stop condition. Without considering the last bit-time, a stop condition is generated with a constant level at the OWI line for at least 20ms.

The master finishes a transmission by changing back to the high level (idle mode). Every command must be closed by a stop condition to start the processing of the command. The master must interrupt a sending slave after it has completed a data request by clamping the OWI line to the low level for generating a stop condition.
- **Valid data**
Data is transmitted in bytes (8 bits) starting with the most significant bit (MSB). Transmitted bits are recognized after a start condition at every transition from low to high at the OWI line. The value of the transmitted bit depends on the duty ratio between the high phase and high/low period (bit period, $t_{OWI,BIT}$ in Table 38). A duty ratio greater than $1/8$ and less than $3/8$ is detected as 0; a duty ratio greater than $5/8$ and less than $7/8$ is detected as 1. The bit period of consecutive bits must not increase to more than 1.5 times the previous bit period or decrease to less than half of the previous bit period because a stop condition is detected in this case.
- **Write operation**
During transmission from master to slave (WRITE), the address byte including a set data direction bit (0 for WRITE) is followed by a command byte and, depending on the transmitted command, by an optional number of data bytes. The internal ARM MCU evaluates the received command and processes the requested routine. Figure 51 illustrates the writing of a command with two data bytes and a command without data bytes.

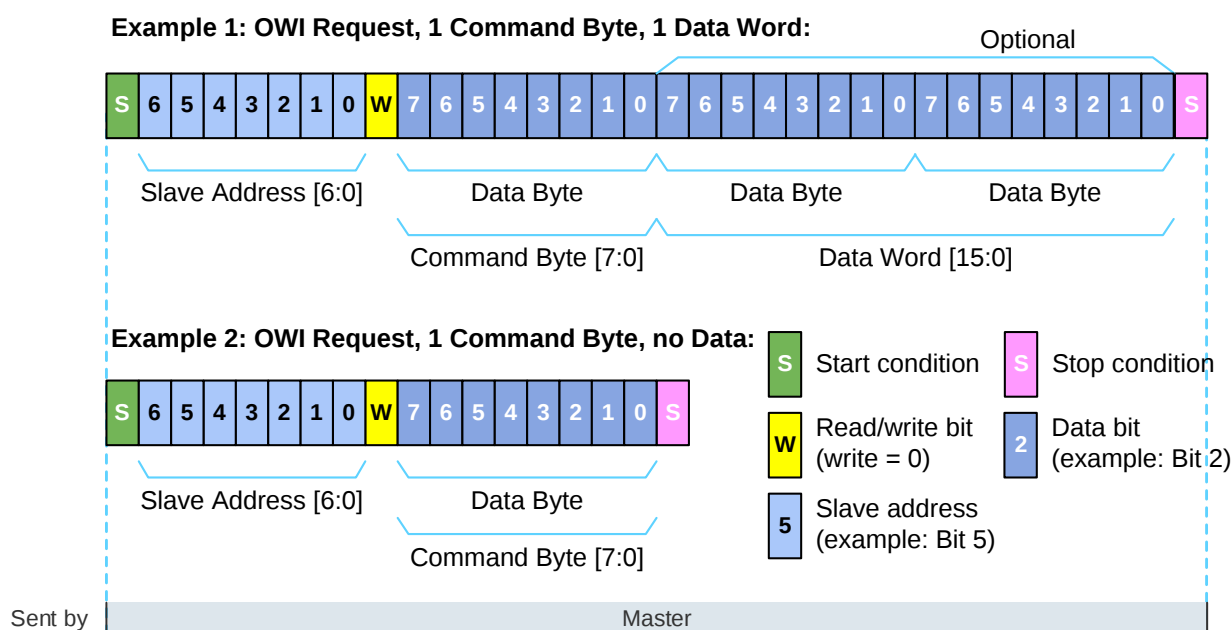


Figure 51: OWI Write Operation/Command Request

- Read operation

After a data read request from the master to the slave (matching address byte and data direction bit = 1 for READ), the slave answers by sending data from the interface output registers. The master must generate a stop condition after receiving the requested data (see Figure 52).

The data in the output registers is sent continuously until a stop condition is detected. After transmitting all available data, the slave starts repeating the data. The data of an ongoing OWI transaction is fixed. It does not get updated with newly available conditioned results. To receive new output data a new OWI read transaction must be started.

Example: OWI Read Operation, Status Byte (+n) Data Bytes*:

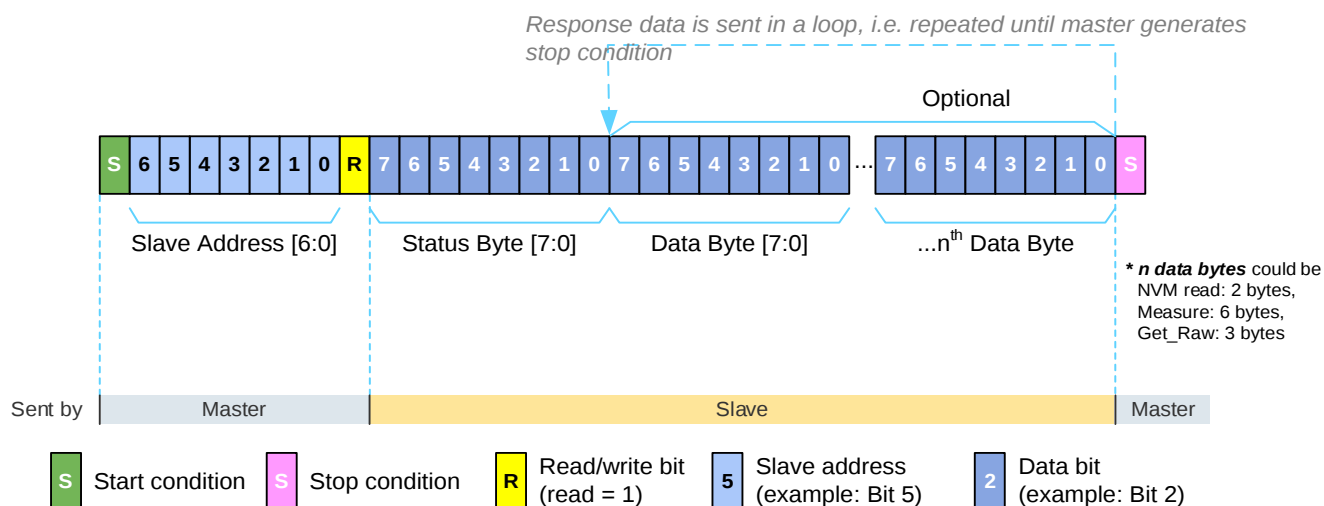


Figure 52: OWI Read Operation

The length of the OWI-line and the size of $R_{OWI,PULL}$ (if it is statically connected to AOUT), and consequently the resistive and capacitive loads, influence the maximum possible interface speed and minimum bit period. Additional capacitance on the OWI1 (AOUT) line can improve RF disturbance robustness und harsh EMC conditions. Table 37 shows practical OWI interface dimensioning examples and the resulting maximum signal frequencies (minimum possible bit periods).

The ZSSC3281's OWI interface properties and timing capabilities are given in Table 38.

Table 37: OWI Dimensioning Examples

$C_{OWI,LOAD}^1$ \ $R_{OWI,PULL}$ (+ $R_{OWI,LOAD}$)	1.8 k Ω	2.5 k Ω	3.3 k Ω	5.5 k Ω	10.0 k Ω
1nF	20 μ s	20 μ s	21 μ s	35 μ s	63 μ s
10nF	113 μ s	157 μ s	207 μ s	345 μ s	628 μ s
22nF	249 μ s	345 μ s	456 μ s	760 μ s	1381 μ s
33nF	373 μ s	518 μ s	684 μ s	1140 μ s	2070 μ s
44nF	497 μ s	691 μ s	912 μ s	1520 μ s	2762 μ s
51nF	576 μ s	801 μ s	1057 μ s	1760 μ s	3205 μ s

1. Examples are shown with statically connected $R_{OWI,PULL}$, and with minimum bit period: $t_{OWI,BIT}$.

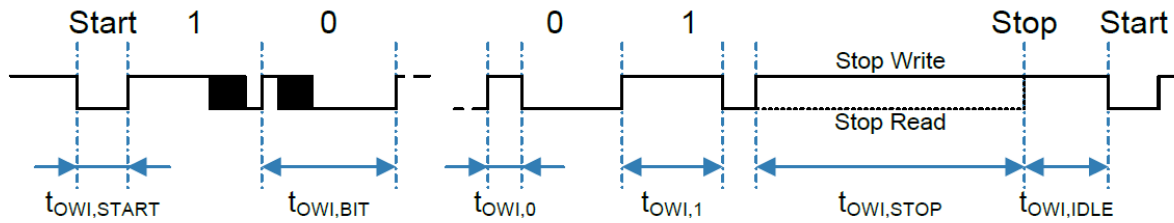


Figure 53: OWI Telegram



Figure 54: Typical OWI Communication on AOUT in Voltage Out Mode

Table 38: OWI Timing Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{OWI,WINDOW}$	OWI-Startup "Listening" Window	Time after power-on in which the OWI can be enabled by a valid OWI-Start-Condition and command				ms
		OWI Window Mode		400		
		OWI Analog Mode		200		
$t_{OWI,IDLE}$	Bus free time between start and stop condition		1		30	μ s
$t_{OWI,START}$	Hold time start condition		10			μ s
$t_{OWI,BIT}$	Bit time		10	40	4000	μ s
$t_{OWI,0}$	Duty ratio bit '0'		0.125	0.25	0.375	$t_{OWI,BIT}$
$t_{OWI,1}$	Duty ratio bit '1'		0.625	0.75	0.875	$t_{OWI,BIT}$
t_{OWI,BIT_DEV}	Bit time deviation	Tolerated variation of Bit time from bit to bit	0.55	1.0	1.45	$t_{OWI,BIT}$
$t_{OWI,STOP}$	Hold time stop condition	t_{OWI,BIT_L} is the bit time of the last valid bit	1.5	2.5		t_{OWI,BIT_L}
$C_{OWI,LOAD}$	Capacitive load at OWI line		—	2.2	50	nF
$R_{OWI,PULL}$	Pull-up resistance – master		0.3	0.47	3.3	k Ω
$R_{OWI,LOAD}$	Resistive OWI line load		20	$0.01 \times R_{OWI,PULL}$	—	Ω

An enabled OWI interface is checked after power-on or reset of ZSSC3281 for incoming telegrams. The OWI interface is locked by DMA controller for further communication if it is the first which received a telegram with a matching slave address and at least 8bit of telegram data. The OWI communication mode can only be left by power-on or reset of the ZSSC3281.

10.1.5.1. OWI operation modes

The ZSSC3281 allows utilization of the OWI interface in different application configurations. The respective configuration settings can be made in the GUI via Configure\Serial Interfaces\OWI Mode.

- OWI Disable/OWI Off

This mode deactivates the OWI interface. For example, this could be applied in cases when an analog-output smart sensor is configured and calibrated using the OWI interface and the OWI is not available for end user access after calibration and final setup/programming.

- OWI Digital (no analog output)

In this mode AOUT does not provide any analog outputs and is only used as OWI pin. There is no startup window limitation for activation of the OWI interface, but if the ZSSC3281 was started in Command Mode or Sleep Mode and no *OWI Startup* (BA_{HEX}) command was received within a window time of 200ms, the system state machine automatically moves to Cyclic Mode.

- OWI Window

The OWI Window Mode is not intended to be used in end applications but useful to run with calibration line due to easier access to OWI communication.

The OWI Window Mode disables the analog output signal driving at AOUT after power-on or reset of ZSSC3281 for a startup window time of $2 \times 200\text{ms}$. During the first 200ms window ZSSC3281 listens on OWI-IN1 (=AOUT) for incoming OWI telegrams. As soon as it receives an OWI Startup (BA_{HEX}) command on OWI-IN1 it locks the AOUT channel for OWI communication. The OWI channel can only be locked if the I2C/I3C and SPI channels remained silent and do not lock the interface first.

If no OWI Startup command was received during the first 200ms startup window, a second 200ms window is started and ZSSC3281 listens on OWI-IN2 for incoming OWI telegrams. If it detects an OWI Startup (BA_{HEX}) command within the second 200ms startup window, it locks the OWI channel to the OWI-IN2 + AOUT communication path.

If no OWI Startup command was received even during the second 200ms startup window, the OWI interface is disabled automatically and the AOUT resumes to its configured analog output function. OWI Window Mode is the factory default OWI mode for AOUT.

- OWI Analog Voltage

The OWI Analog Voltage mode allows to start OWI communication even while the configured voltage output function is already active on AOUT. During a startup window of 200ms after power-on or reset ZSSC3281 listens on OWI-IN1 for incoming OWI telegrams. As soon as it receives an OWI Startup (BA_{HEX}) command on OWI-IN1 it locks the AOUT channel for OWI communication.

The difference to the OWI Window Mode is, that the OWI master has to overdrive the analog output voltage signal at AOUT. To prevent self-locking of the OWI channel without external overdrive from the OWI master (for example, if the conditioned analog output waveform at AOUT matches an OWI telegram by accident), the OWI slave also checks for the occurrence of at least one overdrive drive condition at AOUT (either short to VSS or short to VDD) before it releases a received OWI telegram to the DMA Controller.

If no OWI Startup command was received during the 200ms startup window, the OWI interface is disabled automatically and the AOUT remains in its configured analog output function. OWI activation is not possible until new power-on or reset of ZSSC3281.

10.2 Command Interpreter

10.2.1. Command List

The availability of commands depends on the active main operating mode: Command or Cyclic Mode.

Some commands require an additional argument for successful command execution. If an argument error or missing argument appears, the current command is not executed and a failure is indicated in the extended error response.

Table 39: Command List

Command Code (Byte)	Return	Description	Command Available in		
			Sleep Mode	Command Mode	Cyclic Mode
80 _{HEX}	20-byte SCC data	Read output memory Reads content of output memory which contains following information: • Conditioned Bridge Sensor1 (24 bit) • Conditioned Temperature Channel1 (24 bit) • Conditioned Sensor2 (24 bit) • Conditioned Temperature Channel2 (24 bit) • Logic Bridge Sensor Channel3 (32 bit) • Conditioned Temperature Channel3 (24 bit) • Reserved byte (0x00) (8 bit) Note: If more than 20 data bytes are read by the host, the response data rolls over. In Command Mode or Sleep Mode the last valid output data is provided.	Yes	Yes ³	Yes
81 _{HEX} followed by data XXYY _{HEX}	YY _{HEX} bytes	Read output memory burst Reads content of output memory in burst mode: • XX_{HEX} selects the byte in output memory which is read first • YY_{HEX} defines the number of bytes which is read from output memory Note: If more than YY _{HEX} data bytes are read by the host, the response data rolls over. In Command Mode or Sleep Mode the last valid output data is provided.	Yes	Yes ³	Yes
82 _{HEX} followed by data XXWW _{HEX}	WW _{HEX} × 4 bytes	Read configuration data in burst Reads content of Configuration and Calibration Page (CCP) in burst mode: • XX_{HEX} selects the 32-bit word in CCP which is read first • WW_{HEX} defines the number of words which is read from output memory Note: Maximum supported WW _{HEX} is 0x20	No	Yes ³	No
83 _{HEX} followed by data XXWW _{HEX}	–	(Over-) Write configuration data in burst¹ Writes content of Configuration and Calibration Page (CCP) in burst mode into Shadow RAM: • XX_{HEX} selects the word in CCP which is written first • WW_{HEX} defines the number of words which is written in output memory Note: Maximum supported WW _{HEX} is 0x20	No	Yes ³	No
84 _{HEX} followed by data XXWW _{HEX}	WW _{HEX} × 4 bytes	Read device info data in burst Reads device info data in burst mode • XX_{HEX} selects the word in CCP which is read first • WW_{HEX} defines the number of words which is read from output memory Note: Maximum supported XX _{HEX} is 0x1F Maximum supported WW _{HEX} is 0x20 If XX _{HEX} + WW _{HEX} is > 0x20 the command fails.	No	Yes ³	No

Command Code (Byte)	Return	Description	Command Available in		
			Sleep Mode	Command Mode	Cyclic Mode
88 _{HEX}	–	Copy CCP RAM shadow to flash Programs Configuration and Calibration Page in flash with content from Shadow RAM	No	Yes ³	No
89 _{HEX}	3 bytes CCP Version	Read CCP version	No	Yes ³	No
8A _{HEX}	2 bytes	Read chip hardware version Returns 0x0001	No	Yes ³	No
8B _{HEX}	3 bytes IAP Firmware Version	Read IAP firmware version Returns 0x010000	No	Yes ³	No
8C _{HEX}	No answer is returned (Execution jumps directly to the FW update routines)	Start firmware update Triggers Firmware update procedure.	No	Yes ³	No
8E _{HEX}	8 bytes RCA Firmware Version	Read RCA firmware version Returns 0x01040000D5B7DAC5	No	Yes ³	No
A2 _{HEX}	3 bytes raw data	Raw sensor measurement AFE1 ² Returns unconditioned raw data of Bridge Sensor1	Yes	Yes	No
A3 _{HEX}	3 bytes raw data	Raw sensor measurement AFE2 ² Returns unconditioned raw data of Bridge Sensor2	Yes	Yes	No
A4 _{HEX}	3 bytes raw data	Raw temperature measurement Sensor1 ² Returns unconditioned temperature data for Temperature Channel 1	Yes	Yes	No
A5 _{HEX}	3 bytes raw data	Raw temperature measurement Sensor2 ² Returns unconditioned temperature data for Temperature Channel 2	Yes	Yes	No
A6 _{HEX}	3 bytes raw data	Raw temperature measurement Sensor3 ² Returns unconditioned temperature data for Temperature Channel 3	Yes	Yes	No
A7 _{HEX} followed by data XXYY _{HEX}	20 bytes raw data	Snapshot calibration all sensors ² Returns unconditioned raw sensor and temperature data of all AFE channels that are activated in CCP. - XX_{HEX} minimum average count for AFE1 data - YY_{HEX} minimum average count for AFE2 data XX _{HEX} and YY _{HEX} must be in range 1 to 32 (=20 _{HEX}). The output data format is as follows: - Raw Data Bridge Sensor1 (24 bit) - Raw Data Temperature Channel1 (24 bit) - Raw Data Bridge Sensor2 (24 bit) - Raw Data Temperature Channel2 (24 bit) 0x00000000 (4 bytes 0x0) (32 bit) - Raw Data Temperature Channel3 (24 bit) 0x00 (1 byte 0x0) (8 bit)	Yes	Yes	No
A8 _{HEX}	–	START_SLEEP Exit Command Mode or Cyclic Mode and transition to Sleep Mode	Yes	Yes	Yes
A9 _{HEX}	–	START_CM Exit Sleep Mode or Cyclic Mode and transition to Command Mode	Yes	Yes	Yes

Command Code (Byte)	Return	Description	Command Available in		
			Sleep Mode	Command Mode	Cyclic Mode
AA _{HEX} followed by data XXYY _{HEX}	20 bytes SSC data (Fully corrected sensor measurement data plus corrected temperature data)	Snapshot measurement all sensors ² Returns conditioned sensor and temperature data of all AFE channels that are activated in CCP. - XX_{HEX} minimum average count for AFE1 data - YY_{HEX} minimum average count for AFE2 data XX _{HEX} and YY _{HEX} must be in range 1 to 32 (=20 _{HEX}). The output data format is as follows: - Bridge Sensor1 (24 bit) - Temperature Channel1 (24 bit) - Bridge Sensor2 (24 bit) - Temperature Channel2 (24 bit) - Third Logic Channel Combination (4 bytes 0x0) (32 bit) - Temperature Channel3 (24 bit) - Reserved byte (0x00)	Yes	Yes	No
AB _{HEX}	–	START_CYC Enter the Cyclic Mode based on configuration in Shadow RAM: continuous measurement cycles, SSC corrections, and automatic, continuous digital and/or analog output updates	Yes	Yes	No
B0 _{HEX}	12 bytes diagnostic result data	Read diagnosis status Responds with the detailed diagnosis status (see section 6.6)	Yes	Yes ³	No
B1 _{HEX}	–	Reset diagnosis status Resets the contents of the diagnosis status register to 00 _{HEX}	Yes	Yes ³	No
B2 _{HEX}	–	Update diagnosis status Executes all activated sensor and system diagnosis checks Note: If a measurement cycle is running concurrently, the diagnostic update happens after completion of the measurement cycle and SSC calculations.	Yes	Yes	No
B3 _{HEX} followed by data (0000 _{HEX} to FFFF _{HEX})	–	Direct DAC stimulus Set the DAC output register with the data in the command and enable/output the respective analog signal through AOUT (according to the AOUT_setup) Note: The DAC output can be switched off by the RESN pin, POR, or a change in the main operating mode	No	Yes	No
B4 _{HEX} followed by parameters 0x0X + 0xYY	2 bytes	Self-diagnostic measure for AFE1 and AFE2 - Parameter 0x0X: - AFE1: 00_{HEX} - AFE2: 01_{HEX} - Parameter 0xYY - See description in section 7.1	No	Yes	No
B5 _{HEX} followed by data XXXXXXXX _{HEX}		Direct linear stimulus of output path Stimulates the selected output path, linear relation between input data and pin output. - Parameter 0xXX - Output Selection: 0: reserved 1: AOUT 2: PWM1 or FM1 (GPIO1) 3: PWM2 or FM2 (GPIO7) - Parameter 0xYYYYYY – Output Value 24bit data value for output, unsigned integer (as SSC value format) - assigned output is static (the output can be switched off by the RESN pin, POR, or a change in the main operating mode)	No	Yes	No
B8 _{HEX}	12 bytes diagnostic result data	Read fault memory Responds with the detailed fault-memory status (see section 6.6)	No	Yes ³	No
B9 _{HEX}	–	Reset fault memory Resets the contents of the fault memory to 00 _{HEX}	No	Yes ³	No

Command Code (Byte)	Return	Description	Command Available in		
			Sleep Mode	Command Mode	Cyclic Mode
BA _{HEX}	–	Startup OWI Initialization command to enter OWI interface operation; only valid for OWI (see section 10.1.5.1)	No	Yes	Yes
FF _{HEX}	Status followed by last output buffer data	NOP Output of read results; only valid for SPI	Yes	Yes	Yes

1. The Overwrite CCP data command 83_{HEX} can be used to optimize evaluation and test routine execution time for analog front-end setup or to configure measurement setups without changing the ZSSC3281's Flash content. Without adding command 88_{HEX} the changes made by 83_{HEX} command are lost after reset of ZSSC3281 reset via the RESN pin or Power On Reset
2. These commands can be used to conduct a measurement without SSC conditioning, e.g., during the smart sensor calibration procedure. No digital correction is performed on the measurement result. The setup and configuration for the raw measurement is the content in the shadow registers that can be pre-loaded (automatically loaded during power-on) from the Flash or by means of the Overwrite command 83_{HEX}.
Use Oversample measurements to obtain noise-minimized measurement results in Sleep or Command Mode. With higher oversampling factors, the command execution time increases proportionally.
3. Command is also available after entering Command Mode from Static Diagnostic Mode (SDM).

11. Firmware Update

ZSSC3281 offers a firmware update function via the serial I2C interface for Renesas provided code (RCA code).

Figure 55 shows the high-level firmware flow. Initiating the firmware update is done by a “start firmware update” command in command mode. This command stores a command sequence in a dedicated register and performs a reset of the device. Due to the required command sequence, the device starts to the update procedure during system boot and performs the firmware update.

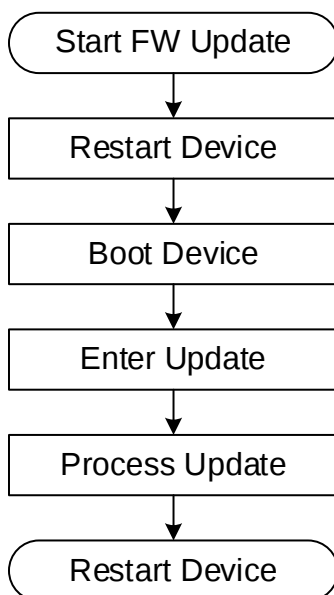


Figure 55 High-level Firmware Update Flow

A firmware update is meant to be executed exclusively via the ZSSC3281 GUI. It can be initiated at the FW Update Tab, where the respective new firmware file can be selected, and the update process can be triggered.

12. Production Configuration

12.1 Configuration and Calibration Page (CCP) Memory Map

12.1.1. Serial Interfaces

Address: 0x00						Register Name: IfbParamCfg																Default: 0x00000000									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default		Description																					
1		EnCrc						0		CRC Checking of Serial Interface Communication 0: Disabled 1: Enabled																					
2		EnErrResp						0		Extended Error Response Mode in Serial Communication 0: Inactive 1: Active																					
4		BypassCmdInterp						0		Bypass of IFB Command Interpreter in Cyclic Mode 0: Inactive 1: Active																					

Address: 0x01						Register Name: I3cslvRegCtrl																Default: 0x000000C0									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default		Description																					
3:0		Instanceld						0		I3C Instance ID 4bit hex value																					
6		Enable						1		I2C/I3C Interface Activation 0: Disabled 1: Enabled																					
7		Model2c						1		Operation Mode of I2C/I3C Interface 0: I3C Mode 1: I2C Mode																					

Address: 0x02						Register Name: I3cslvRegStatAddrCtrl																Default: 0x0000003C									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default		Description																					
6:0		Addr						0x3C		I2C/I3C Static Slave Address 7bit hex value																					

Address: 0x03						Register Name: I3cslvInBandIrqSupport																Default: 0x00000000									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default		Description																					
0		InBandIrq						0x0		I2C/I3C Inband Interrupt Support 0: Disabled 1: Enabled																					

Address: 0x04						Register Name: SpislvParamCfg																Default: 0x00000001															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
Bits		Field Name								Default		Description																									
0		Enable								0x1		SPI Interface Activation 0: Disabled 1: Enabled																									
1		ClockPhase								0x0		SPI Clock Phase 0: CPHA=0 1: CPHA=1																									
2		ClockPolar								0x0		SPI Clock Polarity 0: CPOL =0; Default Low 1: CPOL=1; Default High																									
3		SsPolar								0x0		SPI Slave Select Polarity 0: Active Low 1: Active High																									

Address: 0x05						Register Name: OwislvCtrReg																		Default:			0x00000008						
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Bits		Field Name						Default		Description																							
1		FixedLenEn						0x0		Apply fixed bit length as defined in register OwislvFixedlenReg for transmission instead of the bit length measured for the last received bit. 0: Disabled 1: Enabled																							
2		FamAddrEn						0x0		OWI Family Address Checking 0: Disabled 1: Enabled																							
3		SlvAddrEn						0x1		OWI Slave Address Checking 0: Disabled 1: Enabled																							
5		In1PolarBit						0x0		OWI-IN1 Input Polarity 0: Active Low 1: Active High																							
6		In2PolarBit						0x0		OWI-IN1 Input Polarity 0: Active Low 1: Active High																							
7		OutPolarBit						0x0		OWI-OUT Output Polarity 0: Active Low 1: Active High																							

Address: 0x06						Register Name: OwislvSlvaddrReg																Default: 0x00000028									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default		Description																					
6:0		SlvAddr						0x28		OWI Static Slave Address 7bit hex value																					

Address: 0x07						Register Name: OwislvFixedlenReg																Default: 0x00000140									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default		Description																					
6:0		FixedLen						0x140		Bit length of a single OWI bit in 8MHz clock cycles, relevant only if OwislvCtrReg.FixedLenEn = 1 16bit hex value																					

Address: 0x08						Register Name: OwiModeParam																Default: 0x00000001															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
Bits		Field Name						Default		Description																											
2:0		OwiSlvMode						0x1		OWI Slave Operation Mode 0x0: Off 0x1: Window 0x2: Digital 0x3: Analog5V 0x4: Analog10V 0x5: AnalogCL2 0x6: AnalogCL3 Note: Window as operation mode is not intended to be used in end application.																											

Address: 0x09						Register Name: CntCommParam																Default: 0x0000000A									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default				Description																			
31:0		CntCommParam						0x4				Internal parameter of ZSSC3281 Firmware. Must not be changed.																			

Address: 0x0A						Register Name: CommParamCrc																Default: 0x685AD4EB													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Bits		Field Name						Default				Description																							
31:0		CommParamCrc						0x685AD4EB				Internal parameter of ZSSC3281 Firmware. Must not be changed.																							

12.1.2. Clocks

Address: 0x0B						Register Name: MiscctrlParamCfg.Clkout																Default: 0x00000000													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Bits		Field Name						Default			Description																								
1:0		ClkOutMode						0x0			Clock Output Signal at CLK_OUT Pin (GPIO14) 0x0: Inactive 0x1: Internal High Speed Clock (16MHz) 0x2: Internal Low Speed Clock (32kHz) 0x3: Main System Clock, depends on stetting in Register MiscctrlParamCfg.Divfclk																								

Address: 0x0C						Register Name: MiscctrlParamCfg.Divafeaout																Default: 0x00000008														
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
Bits		Field Name								Default			Description																							
1:0		FreqDivClkAfe								0x0			Clock Divider HighSpeedClock to AFE Clock 0x0: div4 (4MHz AFE clock) 0x1: div8 (2MHz AFE clock) 0x2: div16 (1MHz AFE clock)																							
4:2		FreqDivClkAout								0x2			Clock Divider HighSpeedClock to AOUT Clock 0x0: div1 (16MHz AOUT clock) 0x1: div2 (8MHz AOUT clock) 0x2: div4 (4MHz AOUT clock) 0x3: div8 (2MHz AOUT clock) 0x4: div16 (1MHz AOUT clock)																							
5		Afe2LowSpeedMode								0x0			AFE2 clock speed with respect to AFE1 0: Normal (equal) Speed 1: Quarter Speed																							

Address: 0x0D						Register Name: MiscctrlParamCfg.Divfclk																Default: 0x00000000									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default		Description																					
2:0		Divfclk						0x0		Clock Divider HighSpeedClock to System Clock 0x0: div1 (16MHz System clock) 0x1: div2 (8MHz System clock) 0x2: div4 (4MHz System clock) 0x3: div8 (2MHz System clock) 0x4: div16 (1MHz System clock)																					

Address: 0x0E						Register Name: SmuParamCfg.Anacfg																Default: 0x00000108															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
Bits		Field Name								Default		Description																									
0		ExtldoDisable								0x0		External JFET LDO Activation 0: Enabled 1: Disabled																									
3		PgLossDetect								0x1		Power-Ground Loss Activation 0: Enabled 1: Disabled																									
8:4		ExtldoVolt								0x10		External JFET LDO Voltage if SmuParamCfg.Anacfg.ExtldoDisable set to enabled 0x02: 3.00V 0x04: 4.00V 0x08: 5.00V 0x10: 5.25V																									

Address: 0x0F						Register Name: SmuParamCfg.Extclkcfg																Default: 0x00000000									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name								Default		Description																			
1		EnExtclk								0x0		External Clock Input Activation 0: Disabled																			
2		Type								0x0		External Clock Type 0: Clock																			
23:8		WaitTime								0x0																					

12.1.3. Basic AFE Setup

Address: 0x10						Register Name: AfeBaseCfgParam																Default: 0x00000003															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
Bits		Field Name								Default		Description																									
7:0		AfeActive								0x3		AFE Activation configuration 0x0: None 0x1: AFE1 only 0x2: AFE2 only 0x3: AFE1 and AFE2 0x7: DualSpeed																									
15:8		Afe1SmConfig								0x0		AFE1 Sequencer Configuration 0x0: SM- and SM+ 0x1: SM+ and AUX_AZ 0x2: SM+ only; 0x3: No Main Sensor-Bridge Measurement																									
23:16		Afe2SmConfig								0x0		AFE2 Sequencer Configuration 0x0: SM- and SM+ 0x1: SM+ and AUX_AZ 0x2: SM+ only; 0x3: No Main Sensor-Bridge Measurement																									
31:24		AfeSyncStatus								0x0		AFE1 / AFE2 Synchronization 0x0: Asynchronous measurement 0x1: Synchronized measurement																									

Address: 0x11						Register Name: AfeBaseCfgParam.AfeDsCfg.Reg1																Default: 0x00000000									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default		Description																					
23:0		Thresh1						0x0		Dual Speed Mode Threshold 1																					
31:24		ConvCnt						0x0		Internal Dual Speed Mode parameter – Must not be changed.																					

Address: 0x12						Register Name: AfeBaseCfgParam.AfeDsCfg.Reg2																Default: 0x00000000									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default		Description																					
23:0		Thresh2						0x0		Dual Speed Mode Threshold 2																					

12.1.4. Sensor Bridge

Address: 0x13 0x15						Register Name: Bm1Cfg1 – Sensor Bridge 1 setting Bm2Cfg1 – Sensor Bridge 2 setting																		Default: 0x04000655 0x04000656															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0								
Bits		Field Name										Default		Description																									
3:0		BmPgaGain1										0x5 @ 0x13 0x6 @ 0x14		PGA1 Gain 0x0: 1.20x8: 58.1 0x1: 20x9: 76.6 0x2: 40xA: 112 0x3: 5.970xB: 143 0x4: 11.90xC: 187 0x5: 19.80xD: 223 0x6: 29.60xE: 275 0x7: 39.2																									
6:4		BmPgaGain2										0x5		PGA2 Gain 0x0: 1.10x4: 1.5 0x1: 1.20x5: 1.6 0x2: 1.30x6: 1.7 0x3: 1.40x7: 1.8																									
7		BmPgaPolarity										0x0		PGA Polarity 0: Positive 1: Negative																									
11:8		BmAdcReso										0x6		ADC Resolution 0x0: 10 bit0x8: 18 bit 0x1: 11 bit0x9: 19 bit 0x2: 12 bit0xA: 20 bit 0x3: 13 bit0xB: 21 bit 0x4: 14 bit0xC: 22 bit 0x5: 15 bit0xD: 23 bit 0x6: 16 bit0xE: 24 bit 0x7: 17 bit																									
14:12		BmAdcShift										0x0		ADC Shift $V_{\text{shift}}/V_{\text{fs}}$ 0x0: 00x4: 0.500 0x1: 0.1250x5: 0.625 0x2: 0.2500x6: 0.750 0x3: 0.3750x7: 0.875																									
15		BmBrdgType										0x0		Bridge Supply via TOPx, BOTx 0: Voltage Source 1: Resistor or Current Source																									
17:16		BmSetTime										0x0		Bridge Settling Time before ADC conversion starts 0x0: 20 us 0x1: 40 us 0x2: 60 us 0x3: 80 us																									

Address: 0x13 0x15						Register Name: Bm1Cfg1 – Sensor Bridge 1 setting Bm2Cfg1 – Sensor Bridge 2 setting														Default: 0x04000655 0x04000656											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default		Description																					
21:18		BmBrdgRth						0x0		Rth resistor, applicable if BmBrdgType = 1																					
										0x0: Open										0x6: 14000 ohms											
										0x1: 1333 ohms										0x7: 18000 ohms											
										0x2: 2000 ohms										0x8: 20000 ohms											
										0x3: 4000 ohms										0x9: 24000 ohms											
										0x4: 8000 ohms										0xA: 28000 ohms											
										0x5: 10000 ohms										0xB: 40000 ohms											
25:22		BmBrdgRtl						0x0		Rtl resistor, applicable if BmBrdgType = 1																					
										0x0: Open										0x6: 14000 ohms											
										0x1: 1333 ohms										0x7: 18000 ohms											
										0x2: 2000 ohms										0x8: 20000 ohms											
										0x3: 4000 ohms										0x9: 24000 ohms											
										0x4: 8000 ohms										0xA: 28000 ohms											
										0x5: 10000 ohms										0xB: 40000 ohms											
28:26		BmAdcMux						0x1		ADC Input MUX Setting																					
										0x0: ADC inputs shorted to AGND																					
										0x1: ADC input connected to PGA																					
										0x2: ADC input connected to input (Gain = 1, PGA bypassed)																					
29		BmTest						0x0		Reserved, must remain 0																					
30		BmTestDac						0x0		Reserved, must remain 0																					
31		BmType						0x0		Sensor Type																					
										0x0: Resistive Bridge																					
										0x1: Thermopile / Thermocouple																					

Address: 0x14 0x16						Register Name: Bm1Cfg2 – Sensor Bridge 1 setting Bm2Cfg2 – Sensor Bridge 2 setting																Default: 0x00000210 0x00000210																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0								
Bits		Field Name										Default		Description																									
4:0		BmPgaOffset										0x10		PGA Offset Shift										0x10: 0mV															
														0x1: -1.9 mV										0x11: 1.9 mV															
														0x2: -3.8 mV										0x12: 3.8 mV															
														0x3: -5.6 mV										0x13: 5.6 mV															
														0x4: -7.5 mV										0x14: 7.5 mV															
														0x5: -9.4 mV										0x15: 9.4 mV															
														0x6: -11.3 mV										0x16: 11.3 mV															
														0x7: -13.1 mV										0x17: 13.1 mV															
														0x8: -15.0 mV										0x18: 15.0 mV															
														0x9: -16.9 mV										0x19: 16.9 mV															
														0xA: -18.8 mV										0x1A: 18.8 mV															
														0xB: -20.6 mV										0x1B: 20.6 mV															
														0xC: -22.5 mV										0x1C: 22.5 mV															
														0xD: -24.4 mV										0x1D: 24.4 mV															
														0xE: -26.2 mV										0x1E: 26.2 mV															
0xF: -28.1 mV										0x1F: 28.1 mV																													
8:5		BmBrdglBias										0x0		Sensor Supply Current, applicable if BmBrdgType = 1																									
														0x0: Open/Off;										0x5: 80 uA															
														0x1: 5 uA										0x6: 100 uA															
														0x2: 10 uA										0x7: 160 uA															
														0x3: 20 uA										0x8: 200 uA															
														0x4: 40 uA										0x9: 500 uA															
9		BmAdcEnShift										0x1		ADC Shift & Gain ×2 Enable, activates BmAdcShift setting																									
														0x0: ADC Gain ×1, ADC Shift disabled																									
														0x1: ADC Gain ×2, ADC Shift enabled																									
11:10		BmBias										0x0		AFE Bias Current Setting																									
														0x0: normal operation																									
														0x3: reduced AFE bias current																									

12.1.5. External Temperature Sensor

Address: 0x17 0x19 0x1B					Register Name: ExtTemp1Cfg1 – T1 Sensor setting ExtTemp2Cfg1 – T2 Sensor setting ExtTemp3Cfg1 – T3 Sensor setting																Default: 0x0011C5F1 0x00118502 0x00118502																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
Bits		Field Name									Default			Description																								
3:0		ExtTempPgaGain1									0x1 @ 0x17 0x2 @ 0x19 0x2 @ 0x1B			PGA1 Gain 0x0: 1.2 0x1: 2 0x2: 4 0x3: 5.97 0x4: 11.9 0x5: 19.8 0x6: 29.6 0x7: 39.2															0x8: 58.1 0x9: 76.6 0xA: 112 0xB: 143 0xC: 187 0xD: 223 0xE: 275									
6:4		ExtTempPgaGain2									0x7 @ 0x17 0x0 @ 0x19 0x0 @ 0x1B			PGA2 Gain 0x0: 1.1 0x1: 1.2 0x2: 1.3 0x3: 1.4															0x4: 1.5 0x5: 1.6 0x6: 1.7 0x7: 1.8									
7		ExtTempPgaPolarity									0x1 @ 0x17 0x0 @ 0x19 0x0 @ 0x1B			PGA Polarity 0: Positive 1: Negative																								
11:8		ExtTempAdcReso									0x5 @ 0x17 0x5 @ 0x19 0x5 @ 0x1B			ADC Resolution 0x0: 10 bit 0x1: 11 bit 0x2: 12 bit															0x3: 13 bit 0x4: 14 bit 0x5: 15 bit									
14:12		ExtTempAdcShift									0x4 @ 0x17 0x0 @ 0x19 0x0 @ 0x1B			ADC Shift value V _{shift} / V _{fs} 0x0: 0 0x1: 0.125 0x2: 0.250 0x3: 0.375															0x4: 0.500 0x5: 0.625 0x6: 0.750 0x7: 0.875									
18:15		ExtTempType									0x3			External Temperature Type 0x0: Reserved 0x1: Diode/NTC/PTC sink mode, internal bias 0x2: Diode/NTC/PTC, external bias 0x3: Diode/NTC/PTC source mode, internal bias 0x4: Reserved 0x5: Bridge single ended, internal bias 0x6: Bridge single ended, external bias 0x7: Bridge differential																								
19		ExtTempInput									0x0			External Temperature Sensor Input MUX 0x0: Input connected to PGA 0x1: Input connected to ADC																								

Address: 0x17 0x19 0x1B						Register Name: ExtTemp1Cfg1 – T1 Sensor setting ExtTemp2Cfg1 – T2 Sensor setting ExtTemp3Cfg1 – T3 Sensor setting																Default: 0x0011C5F1 0x00118502 0x00118502																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
Bits		Field Name									Default			Description																								
23:20		ExtTempBrdgRth									0x1			Rth resistor, applicable depending on ExtTempType setting																								
														0x0: Open												0x6: 14000 ohms												
														0x1: 1333 ohms												0x7: 18000 ohms												
														0x2: 2000 ohms												0x8: 20000 ohms												
														0x3: 4000 ohms												0x9: 24000 ohms												
														0x4: 8000 ohms												0xA: 28000 ohms												
														0x5: 10000 ohms												0xB: 40000 ohms												
27:24		ExtTempBrdgRtl									0x0			Rtl resistor, applicable depending on ExtTempType setting																								
														0x0: Open												0x6: 14000 ohms												
														0x1: 1333 ohms												0x7: 18000 ohms												
														0x2: 2000 ohms												0x8: 20000 ohms												
														0x3: 4000 ohms												0x9: 24000 ohms												
														0x4: 8000 ohms												0xA: 28000 ohms												
														0x5: 10000 ohms												0xB: 40000 ohms												

Address: 0x18 0x1A 0x1C						Register Name: ExtTemp1Cfg2 – T1 Sensor setting ExtTemp2Cfg2 – T2 Sensor setting ExtTemp3Cfg2 – T3 Sensor setting																Default: 0x00000210 0x00000010 0x00000010																
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
Bits		Field Name									Default		Description																									
4:0		ExtTempPgaOffset									0x10		PGA Offset Shift 0x1: -1.9 mV 0x2: -3.8 mV 0x3: -5.6 mV 0x4: -7.5 mV 0x5: -9.4 mV 0x6: -11.3 mV 0x7: -13.1 mV 0x8: -15.0 mV 0x9: -16.9 mV 0xA: -18.8 mV 0xB: -20.6 mV 0xC: -22.5 mV 0xD: -24.4 mV 0xE: -26.2 mV 0xF: -28.1 mV										0x10: 0mV 0x11: 1.9 mV 0x12: 3.8 mV 0x13: 5.6 mV 0x14: 7.5 mV 0x15: 9.4 mV 0x16: 11.3 mV 0x17: 13.1 mV 0x18: 15.0 mV 0x19: 16.9 mV 0x1A: 18.8 mV 0x1B: 20.6 mV 0x1C: 22.5 mV 0x1D: 24.4 mV 0x1E: 26.2 mV 0x1F: 28.1 mV															
8:5		ExtTempBrdglBias									0x0		External Temp Sensor Supply Current, applicable depending on ExtTempType setting 0x0: Open/Off; 0x1: 5 uA 0x2: 10 uA 0x3: 20 uA 0x4: 40 uA 0x5: 80 uA										0x6: 100 uA 0x7: 160 uA 0x8: 200 uA 0x9: 500 uA 0xA: -20 uA 0xB: -100 uA															
9		ExtTempAdcEnShift									0x1 @ 0x18 0x0 @ 0x1A 0x0 @ 0x1C		ADC Shift & Gain ×2 Enable, activates ExtTempAdcShift setting 0x0: ADC Gain ×1, ADC Shift disabled 0x1: ADC Gain ×2, ADC Shift enabled																									
11:10		ExtTempBias									0x0		AFE Bias current Setting 0x0: normal operation 0x3: reduced AFE bias current																									
13:12		ExtTempSetTime									0x0		Tx Input Settling Time before ADC conversion starts 0x0: 20 us 0x2: 60 us 0x1: 40 us 0x3: 80 us																									

Address: 0x1D						Register Name: CmConfig[0]																Default: 0x00000000									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default				Description																			
31:0		Reserved						0x0																							

Address: 0x1E						Register Name: CmConfig[1]																Default: 0x00000000									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default				Description																			
31:0		Reserved						0x0																							

Address: 0x1F						Register Name: CmConfig[2]																Default: 0x00000000									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default				Description																			
31:0		Reserved						0x0																							

12.1.6. PTAT Sensor

Address: 0x20					Register Name: PtatCfg1 – PTAT Sensor setting																Default:				0x0000F533													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
Bits		Field Name									Default			Description																								
3:0		PgaGain1									0x3			PGA1 Gain																								
														0x0: 1.2										0x8: 58.1														
														0x1: 2										0x9: 76.6														
														0x2: 4										0xA: 112														
														0x3: 5.67 ³										0xB: 143														
														0x4: 11.9										0xC: 187														
														0x5: 19.8										0xD: 223														
														0x6: 29.6										0xE: 275														
0x7: 39.2																																						
6:4		PgaGain2									0x3			PGA2 Gain																								
														0x0: 1.1										0x4: 1.5														
														0x1: 1.2										0x5: 1.6														
														0x2: 1.3										0x6: 1.7														
														0x3: 1.4 ³										0x7: 1.8														
7		PgaPolarity									0x0			PGA Polarity 0: Positive ³ 1: Negative																								
11:8		AdcReso									0x3			ADC Resolution																								
														0x0: 10 bit										0x3: 13 bit														
														0x1: 11 bit										0x4: 14 bit														
0x2: 12 bit										0x5: 15 bit																												
14:12		AdcShift									0x7			ADC Shift value V _{shift} / V _{fs}																								
														0x0: 0										0x4: 0.500														
														0x1: 0.125										0x5: 0.625														
														0x2: 0.250										0x6: 0.750														
														0x3: 0.375										0x7: 0.875 ³														
17:15		AdcMux									0x1			ADC Input MUX Setting 0x1: ADC input connected to PGA ³																								

³ Renesas recommended

Address: 0x21						Register Name: PtatCfg2 – PTAT Sensor setting																Default:			0x00000010						
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default		Description																					
4:0		PgaOffset						0x0		PGA Offset Shift												0x10: 0mV ⁴									
										0x1: -1.9 mV												0x11: 1.9 mV									
										0x2: -3.8 mV												0x12: 3.8 mV									
										0x3: -5.6 mV												0x13: 5.6 mV									
										0x4: -7.5 mV												0x14: 7.5 mV									
										0x5: -9.4 mV												0x15: 9.4 mV									
										0x6: -11.3 mV												0x16: 11.3 mV									
										0x7: -13.1 mV												0x17: 13.1 mV									
										0x8: -15.0 mV												0x18: 15.0 mV									
										0x9: -16.9 mV												0x19: 16.9 mV									
										0xA: -18.8 mV												0x1A: 18.8 mV									
										0xB: -20.6 mV												0x1B: 20.6 mV									
										0xC: -22.5 mV												0x1C: 22.5 mV									
										0xD: -24.4 mV												0x1D: 24.4 mV									
										0xE: -26.2 mV												0x1E: 26.2 mV									
0xF: -28.1 mV												0x1F: 28.1 mV																			
5		AdcEnShift						0x1		ADC Shift & Gain ×2 Enable, activates AdcShift setting																					
										0x0: ADC Gain ×1, ADC Shift disabled																					
										0x1: ADC Gain ×2, ADC Shift enabled ⁴																					
7:6		Bias						0x0		AFE Bias current Setting																					
										0x0: normal operation ⁴																					
										0x3: reduced AFE bias current																					

⁴ Renesas recommended

12.1.7. AFE Sequencer

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address: 0x22 0x26						Register Name: Afe1MeasCfg1 – AFE1 setting Afe2MeasCfg1 – AFE2 setting																		Default: 0x01020036 0x01020036															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0								
Bits		Field Name								Default		Description																											
1:0		MeasTypeSlot1								0x2		AFE Measurement Type for Slot_x 0x0: None 0x1: SM- 0x2: SM+ 0x3: AUX_i																											
3:2		MeasTypeSlot2								0x1																													
5:4		MeasTypeSlot3								0x3																													
7:6		MeasTypeSlot4								0x0																													
9:8		MeasTypeSlot5								0x0																													
11:10		MeasTypeSlot6								0x0																													
13:12		MeasTypeSlot7								0x0																													
15:14		MeasTypeSlot8								0x0																													
16		EoclrqSlot1								0		End of Conversion Interrupt after Slot_x 0: Disabled 1: Enabled																											
17		EoclrqSlot2								1																													
18		EoclrqSlot3								0																													
19		EoclrqSlot4								0																													
20		EoclrqSlot5								0																													
21		EoclrqSlot6								0																													
22		EoclrqSlot7								0																													
23		EoclrqSlot8								0																													
24		BurstModeSlot1								1		AFE DMA Burst Mode Data Transfer after Slot_x 0: Disabled 1: Enabled																											
25		BurstModeSlot2								0																													
26		BurstModeSlot3								0																													
27		BurstModeSlot4								0																													
28		BurstModeSlot5								0																													
29		BurstModeSlot6								0																													
30		BurstModeSlot7								0																													
31		BurstModeSlot8								0																													

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address: 0x23 0x27						Register Name: Afe1MeasCfg2 – AFE1 setting Afe2MeasCfg2 – AFE2 setting																Default: 0x00000013 0x00000013									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default		Description																					
3:0		NrOfSlots						0x3		Number of active measurement slots 0x0 ... 0x8 selectable																					
5:4		CyclicMode						0x1		Sequencer Run Mode 0x0: Single measurement 0x1: Continuous cyclic measurement 0x2: Discontinuous cyclic measurement, started by trigger																					
7:6		AuxInsertRate						0x0		Insertion Rate of an AUX_i measurement in “Accelerated main measurement” setup 0x0: Disabled 0x1: Every 2 nd 0x2: Every 4 th 0x3: Every 8 th																					
23:8		AuxMaxTime						0x0		Maximum lenght of AUX_i measurement slots within a sequence 0x0000 ... 0xFFFF AFE clock cycles The parameter is calculated based on the relevant timing setups of all active AUX_i measurements to secure all AUX_i measurements have the same duration. This is mainly required for synchronized AFE operation.																					

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address: 0x24 0x28						Register Name: Afe1MeasCfg3 – AFE1 setting Afe2MeasCfg3 – AFE2 setting																		Default: 0x00000018 0x00000300							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name									Default		Description																		
											0x24	0x28																			
31:0		AuxMeasEnable0Aux1									0	0	Activation of Auxiliary measurements																		
		AuxMeasEnable0Aux2									0	0																			Bit 0:
		AuxMeasEnable0Aux3									0	0	Bit 1:		PTAT Sensor S-																
		AuxMeasEnable0Aux4									1	0	Bit 2:		PTAT Sensor S+																
		AuxMeasEnable0Aux5									1	0	Bit 3:		T1 Sensor S-																
		AuxMeasEnable0Aux6									0	0	Bit 4:		T1 Sensor S+																
		AuxMeasEnable0Aux7									0	0	Bit 5:		T1 Sensor, check short to top																
		AuxMeasEnable0Aux8									0	0	Bit 6:		T1 Sensor, check short to bottom																
		AuxMeasEnable0Aux9									0	0	Bit 7:		T1 Sensor, check open																
		AuxMeasEnable0Aux10									0	1	Bit 8:		T2 Sensor S-																
		AuxMeasEnable0Aux11									0	1	Bit 9:		T2 Sensor S+																
		AuxMeasEnable0Aux12									0	0	Bit 10:		T2 Sensor, check short to top																
		AuxMeasEnable0Aux13									0	0	Bit 11:		T2 Sensor, check short to bottom																
		AuxMeasEnable0Aux14									0	0	Bit 12:		T2 Sensor, check open																
		AuxMeasEnable0Aux15									0	0	Bit 13:		T3 Sensor S-																
		AuxMeasEnable0Aux16									0	0	Bit 14:		T3 Sensor S+																
		AuxMeasEnable0Aux17									0	0	Bit 15:		T3 Sensor, check short to top																
		AuxMeasEnable0Aux18									0	0	Bit 16:		T3 Sensor, check short to bottom																
		AuxMeasEnable0Aux19									0	0	Bit 17:		T3 Sensor, check open																
		AuxMeasEnable0Aux20									0	0	Bit 18:		AFE gain diagnosis S+																
		AuxMeasEnable0Aux21									0	0	Bit 19:		AFE gain diagnosis S-																
		AuxMeasEnable0Aux22									0	0	Bit 22:		AFE offset diagnosis																
		AuxMeasEnable0Aux23									0	0	Bit 27:		Bridge Sensor connection check, INP or INN open																
		AuxMeasEnable0Aux24									0	0	Bit 28:		Bridge Sensor connection check, INP and INN shorted																
		AuxMeasEnable0Aux25									0	0	All other bits reserved																		
		AuxMeasEnable0Aux26									0	0																			
		AuxMeasEnable0Aux27									0	0																			
		AuxMeasEnable0Aux28									0	0																			
		AuxMeasEnable0Aux29									0	0																			
		AuxMeasEnable0Aux30									0	0																			
		AuxMeasEnable0Aux31									0	0																			
		AuxMeasEnable0Aux32									0	0																			
														Bit Value Meaning																	
														0: Aux measurement Skipped																	
														1: Aux measurement Executed																	

Address: 0x25 0x29						Register Name: Afe1MeasCfg4 – AFE1 setting Afe2MeasCfg4 – AFE2 setting																Default: 0x00400000 0x00400000									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name								Default		Description																			
										0x25	0x29																				
4:0		AuxMeasEnable0Aux33								0	0	Activation of Auxiliary measurements Reserved																			
		AuxMeasEnable0Aux34								0	0																				
		AuxMeasEnable0Aux35								0	0																				
		AuxMeasEnable0Aux36								0	0																				
		AuxMeasEnable0Aux37								0	0																				
20:5		IdleTime								0x0		In continuous cyclic measurement mode idle times up to 10ms can be asserted between two sequences. IdleTime represents a number of AFE clocks – 4MHz by default																			
21		IrqEnableEoauxins								0		End of Inserted AUX Measurement 0: IRQ disabled 1: IRQ enabled																			
22		IrqEnableEoauxseq								1		End of Aux Sequence 0: IRQ disabled 1: IRQ enabled																			
23		IrqEnableEoauxaz								0		End of AZ Measurement 0: IRQ disabled 1: IRQ enabled																			
24		SensBufDepth								0		Bridge Sensor data buffer depth in SRAM 0: data buffer depth 1 1: data buffer depth 8																			

Address:	0x2A	Register Name:	DiagCfg	Default:	0x00000000
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Address: 0x2B 0x2D						Register Name: DiagSen.Range[0].Inp – AFE1 setting DiagSen.Range[1].Inp – AFE2 setting																Default: 0x00000000 0x00000000									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name								Default		Description																			
15:0		Min								0x0		Reserved																			
31:16		Max								0x0		Reserved																			

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Address: 0x2F 0x30						Register Name: DiagSen.GainChk[0] – AFE1 setting DiagSen.GainChk[1] – AFE2 setting														Default: 0x00000000 0x00000000																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
Bits		Field Name								Default		Description																									
15:0		RefVal								0x0		Gain Reference Value for Gain Drift Diagnosis During sensor calibration an initial AFE Gain Check measurement with a properly defined AFExGainCheckResDacVal setting must be done and the obtained RAW output value shall be stored in this register for later reference.																									
31:16		TolVal								0x0		Gain Tolerance Value for Gain Drift Diagnosis A tolerance value in ADC counts for acceptable gain drift over lifetime shall be stored in this register A gain failure is signaled after the Gain Drift Check if the determined AFE Gain Value is either 																									

Address: 0x31 0x32						Register Name: DiagSen.OfstChk[0] – AFE1 setting DiagSen.OfstChk[1] – AFE2 setting														Default: 0x00000000 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Bits		Field Name								Default		Description																							
15:0		RefVal								0x0		Offset Reference Value for Offset Drift Diagnosis During sensor calibration an initial AFE Offset Check measurement must be done and the obtained RAW output value shall be stored in this register for later reference.																							
31:16		TolVal								0x0		Offset Tolerance Value for Offset Drift Diagnosis A tolerance value in ADC counts for acceptable offset drift over lifetime shall be stored in this register An offset failure is signaled after the Offset Drift Check if the determined AFE Offset Value is either 																							

12.1.9. Temperature Channel Mapping

Address: 0x33						Register Name: TempMapChId																Default: 0x0000001A									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default		Description																					
2:0		Tch1						0x2		Temperature Sensor Source for Temperature Channels 1, 2, 3 0x0: None 0x1: PTAT 0x2: T1 0x3: T2 0x4: T3																					
5:3		Tch2						0x3																							
8:6		Tch3						0x0																							

12.1.10. SSC Algorithm Selection

Address: 0x34						Register Name: MathSbrAlgoSel																Default: 0x00000011									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default		Description																					
3:0		Sensor1						0x1		SSC Algorithm for Bridge Sensors 1 & 2 0x0: None 0x1: SOT Parabolic 0x2: SOT S-Shaped																					
7:4		Sensor2						0x1																							
10:8		TlcOp						0x0		Third Logic Channel Operation 0x0: Subtraction 0x1: Division 0x2: Ratio																					
11		TlcChOrder						0x0		Third Logic Channel Operand Order 0x0: CH1 op CH2 0x1: CH2 op CH1																					

12.1.11. EOC / Alarm

Address: 0x35 0x38						Register Name: EocAlarmPin[0].Reg1 – Pin EOC/ALARM_1 EocAlarmPin[1].Reg1 – Pin EOC/ALARM_2																Default: 0x00000000 0x00000000											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Bits		Field Name						Default		Description																							
23:0		Thresh1						0x0		Alarm Threshold 1 24 bit value, matches SSC output number format																							
24		En						0		EOC / Alarm Activation 0: Disabled 1: Enabled																							
25		Pol						0		Output Polarity 0: Active High 1: Active Low																							
27:26		NrThresh						0x0		Number of Alarm Thresholds 0x0: None (EOC Mode) 1: Single Threshold 2: Window (2 Thresholds)																							
28		Range						0		Alarm Range 0: Above / Outside 1: Below / Inside																							

Address: 0x36 0x39						Register Name: EocAlarmPin[0].Reg2 – Pin EOC/ALARM_1 EocAlarmPin[1].Reg2 – Pin EOC/ALARM_2																		Default: 0x00000000 0x00000000							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name								Default				Description																	
23:0		Thresh2								0x0				Alarm Threshold 2 24 bit value, matches SSC output number format																	

Address: 0x37 0x3A						Register Name: EocAlarmPin[0].Reg3 – Pin EOC/ALARM_1 EocAlarmPin[1].Reg3 – Pin EOC/ALARM_2																Default: 0x00000000 0x00000000									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name								Default				Description																	
23:0		Hyst								0x0				Alarm Hysteresis 24bit value, matches SSC output number format																	
31:24		Persist								0x0				Alarm Condition Persistence before Alarm State is changed 8bit value (0 ... 255)																	

12.1.12. Analog Output (AOUT)

Address: 0x3B						Register Name: AoutSelParam																Default: 0x00000001															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
Bits		Field Name								Default		Description																									
2:0		SelAfeForDac								0x1		Source Signal for Analog Output 0x0: None 0x1: Bridge Sensor Channel 1 0x2: Bridge Sensor Channel 2 0x3: Third Logic Channel 0x4: Temperature Channel 1 0x5: Temperature Channel 2 0x6: Temperature Channel 3																									
5:3		AoutModSel								0x0		Analog Output Driver Mode 0x0: Disabled 0x1: Absolute Voltage Output 0-10V 0x2: Absolute Voltage Output 0-5V 0x3: Absolute V 0-1V 0x4: Ratiometric Voltage Output 0x5: 2-Wire Current Loop 0x6: 3-Wire Current Loop																									

Address: 0x3C						Register Name: AoutRegCtrl																Default: 0x0000001A															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
Bits		Field Name									Default			Description																							
0		AoutEn									0			Analog Output Activation 0: Disabled 1: Enabled																							
2:1		AoutMode									0x1			Analog Output Mode 0x0: Current Loop 5V-RDAC 0x1: VOUT 5V 0x2: VOUT 1V 0x3: Current Loop 1V-RDAC																							
3		AoutHighPowEn									1			AOUT Driver Output Power 0: Low Power 1: High Power																							
4		AoutFeedBackEn									1			AOUT Driver Feedback 0: External 1: Internal																							
6:5		AoutCurrLim									0x0			AOUT Driver Output Current Limitation 0x0: 6 mA 0x1: 12 mA 0x2: 18 mA 0x3: 25 mA																							
7		AoutOffsetCompOff									0			AOUT Driver Offset Compensation 0: Disabled 1: Enabled																							
8		AoutVddnEn									0			VDDN Charge Pump for Negative Supply 0: Disabled 1: Enabled																							
10:9		AoutVddnLoad									0x0			VDDN Charge Pump Load Current 0x0: 0.5 mA 0x1: 1 mA 0x2: 3 mA 0x3: 5 mA																							

Address: 0x3D						Register Name: AoutRegDiag																Default: 0x00000000									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default		Description																					
0		AoutDiagOutEn						0		Diagnosis Level Output at AOUT 0: Normal Operation Mode 1: Diagnosis Output Mode																					
2:1		AoutDiagOutValue						0x0		Analog Output Mode 0x0: V _{AOUT} = VSS 0x2: V _{AOUT} = 96% VDD 0x1: V _{AOUT} = 5% VDD 0x3: V _{AOUT} = VDD																					
3		AoutDiagVddaEn						0		VDDA Diagnosis if VDDA regulator for AOUT is turned on 0: Disabled 1: Enabled																					

Address: 0x3E						Register Name: AoutCl2Coeff																Default: 0x00000000									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default		Description																					
15:0		COffset						0x0000		2-Wire Current Loop Calibration Coefficient CL2_Offset 16 bit Value																					
31:16		CIDelta						0x0000		2-Wire Current Loop Calibration Coefficient CL2_Delta 16 bit Value																					

Address: 0x3F						Register Name: AoutCl3Coeff																Default: 0x00000000									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default		Description																					
15:0		COffset						0x0000		3-Wire Current Loop Calibration Coefficient CL3_Offset 16 bit Value																					
31:16		CIDelta						0x0000		3-Wire Current Loop Calibration Coefficient CL3_Delta 16 bit Value																					

12.1.13. System Startup

Address: 0x40						Register Name: StartupParamCfg																Default: 0x00000001									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default		Description																					
0		StartInCmMode						1		System Startup in Command Mode 0: Disabled 1: Enabled																					
8		EobEn						0		End of Busy Enable 0: Disabled 1: Enabled																					

12.1.14. IIR Filter

Address: 0x41						Register Name: IirFiltCoeffReg																Default: 0x00000000									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default				Description																			
2:0		FiltSbr1Avg						0x0				IIR Avg Value Sensor Bridge 1																			
5:3		FiltSbr1Diff						0x0				IIR Diff Value Sensor Bridge 1																			
8:6		FiltSbr2Avg						0x0				IIR Avg Value Sensor Bridge 2																			
9:11		FiltSbr2Diff						0x0				IIR Diff Value Sensor Bridge 2																			
14:12		FiltTemp1Avg						0x0				IIR Avg Value Temperature Channel 1																			
17:15		FiltTemp1Diff						0x0				IIR Diff Value Temperature Channel 1																			
20:18		FiltTemp2Avg						0x0				IIR Avg Value Temperature Channel 2																			
23:21		FiltTemp2Diff						0x0				IIR Diff Value Temperature Channel 2																			
26:24		FiltTemp3Avg						0x0				IIR Avg Value Temperature Channel 3																			
29:18		FiltTemp3Diff						0x0				IIR Diff Value Temperature Channel 3																			

12.1.15. General AFE Configuration

Address: 0x42						Register Name: AfeConfig																Default: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
Bits		Field Name								Default		Description																									
1:0		BM1ChpMode								0x0		PGA Chopper Mode Bridge Sensor 1 0x0: 100 kHz 0x1: 200 kHz																									
3:2		BM2ChpMode								0x0		PGA Chopper Mode Bridge Sensor 2 0x0: 100 kHz 0x1: 200 kHz																									
5:4		ExtTemp1ChpMode								0x0		PGA Chopper Mode External Temperature Sensor T1 0x0: 100 kHz 0x1: 200 kHz																									
7:6		ExtTemp2ChpMode								0x0		PGA Chopper Mode External Temperature Sensor T2 0x0: 100 kHz 0x1: 200 kHz																									
9:8		ExtTemp3ChpMode								0x0		PGA Chopper Mode External Temperature Sensor T3 0x0: 100 kHz 0x1: 200 kHz																									
11:10		TChpMode								0x0		PGA Chopper Mode PTAT Temperature Sensor 0x0: 100 kHz 0x1: 200 kHz																									
12	BM1NoiseInt1								0		ADC 10μV Noise Reduction 0: Disabled 1: Enabled																										
13	BM2NoiseInt1								0																												
14	ExtTemp1NoiseInt1								0																												
15	ExtTemp2NoiseInt1								0																												
16	ExtTemp3NoiseInt1								0																												
17	TNoiseInt1								0																												
18	CMNoiseInt1								0		Reserved																										
19	CMDitheringEnable								0		Reserved																										
20	Vdda1Brownout								0		AFE1 Vdda Brownout Diagnosis 0: Disabled 1: Enabled																										
21	Vdda2Brownout								0		AFE2 Vdda Brownout Diagnosis 0: Disabled 1: Enabled																										
22	Vdda3Brownout								0		AOUT Vdda Brownout Diagnosis 0: Disabled 1: Enabled																										
23	CM1En								0		Reserved																										
24	CM2En								0		Reserved																										
25	Afe2LowSpeed								0		AFE2 clock speed with respect to AFE1 0: Normal (equal) Speed 1: Quarter Speed																										
20:26		AfeMisc								0x0		Reserved																									
31	CLMode								0		AFE Operation Mode for 2-Wire Current Loop application 0: Disabled 1: Enabled																										

12.1.16. Output Modulation

Address: 0x43						Register Name: OutModConf																Default: 0x27106400															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
Bits		Field Name								Default		Description																									
1:0		Sel								0x0		Output Modulation Type 0x0: No Output Modulation 0x1: Frequency Modulation 0x2: Pulse Width Modulation																									
4:2		ChGpio1								0x0		Source Signal for FOUT/PWM_1 0x0: Not Used 0x1: Bridge Sensor 1 0x2: Bridge Sensor 2 0x3: Third Logic Channel 0x4: Temperature Channel 1 0x5: Temperature Channel 2 0x6: Temperature Channel 3																									
7:5		ChGpio7								0x0		Source Signal for FOUT/PWM_2 0x0: Not Used 0x1: Bridge Sensor 1 0x2: Bridge Sensor 2 0x3: Third Logic Channel 0x4: Temperature Channel 1 0x5: Temperature Channel 2 0x6: Temperature Channel 3																									
15:8		FmMinFreqPwmMap								0x64		Frequency Modulation – Minimum Frequency in Hz 8bit value in range 100 to 255 Pulse Width Modulation – PWM Mapping Selects if the conditioned result is inverted. 0x0: SSC _{Max} = 100% and SSC _{Min} = 0% 0x1: SSC _{Max} = 0% and SSC _{Min} = 100%																									
31:16		FmMaxFreqPwmBaseFreq								0x2710		Frequency Modulation – Maximum Frequency in Hz 16bit value in range 1,000 to 10,000 Pulse Width Modulation – PWM Base Frequency 0x0: 200Hz 0x1: 500Hz 0x2: 500Hz + 1× 500Hz = 1kHz 0x3: 500Hz + 2 × 500Hz = 1kHz 0x4...0x31: 500Hz + ({FmMinFreqPwmMap}-1) × 500Hz 0x32: 500Hz + 31 × 500Hz = 15kHz																									

12.1.17. Output Clipping, Diagnostic Range Assignment and Watchdog

Address: 0x44						Register Name: DiagClipOutCfg.SysDiagCfg														Default:				0x0DA50000																																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																																						
Bits		Field Name								Default		Description																																																									
0		DiagOutEn								0		Output Signalization of Diagnostic State at AOUT and PWM/FOUT 0: Disabled 1: Enabled Notes: - Enabling this feature requires enabling ClipOutEn. - DiagOutEn sets the AOUT and PWM/FOUT to either 0% (LDR) or 100% (UDR) Failure signalization of saturation requires enabling of any additional AFE or sensor diagnosis functions.																																																									
1		ClipOutEn								0		Two-Sided Clipping to Upper and Lower Diagnostic Limit 0: Disabled 1: Enabled Note: Clipping limits are defined in DiagClipOutCfg.ClipOutLvl register.																																																									
23:16		WatchdogDisableKey								0xA5		Watchdog Disable Key 0xA5: Watchdog disabled All other codes enable watchdog																																																									
27:24		WatchdogTimeout								0xD		Watchdog Timeout <table><tr><td>0x0:</td><td>8m</td><td>0x0:</td><td>8m</td></tr><tr><td>0x1:</td><td>10ms</td><td>0x1:</td><td>10ms</td></tr><tr><td>0x2:</td><td>20ms</td><td>0x2:</td><td>20ms</td></tr><tr><td>0x3:</td><td>30ms</td><td>0x3:</td><td>30ms</td></tr><tr><td>0x4:</td><td>40ms</td><td>0x4:</td><td>40ms</td></tr><tr><td>0x5:</td><td>50ms</td><td>0x5:</td><td>50ms</td></tr><tr><td>0x6:</td><td>60ms</td><td>0x6:</td><td>60ms</td></tr><tr><td>0x7:</td><td>80ms</td><td>0x7:</td><td>80ms</td></tr></table>																										0x0:	8m	0x0:	8m	0x1:	10ms	0x1:	10ms	0x2:	20ms	0x2:	20ms	0x3:	30ms	0x3:	30ms	0x4:	40ms	0x4:	40ms	0x5:	50ms	0x5:	50ms	0x6:	60ms	0x6:	60ms	0x7:	80ms	0x7:	80ms
0x0:	8m	0x0:	8m																																																																		
0x1:	10ms	0x1:	10ms																																																																		
0x2:	20ms	0x2:	20ms																																																																		
0x3:	30ms	0x3:	30ms																																																																		
0x4:	40ms	0x4:	40ms																																																																		
0x5:	50ms	0x5:	50ms																																																																		
0x6:	60ms	0x6:	60ms																																																																		
0x7:	80ms	0x7:	80ms																																																																		

Address: 0x45						Register Name: DiagClipOutCfg.DiagOutLvl[0]																Default: 0x00007FFE									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default		Description																					
31:0		DiagOutLvl[0]						0x7FFE		Select register for UDR / LDR assignment of diagnostic checks																					

Address: 0x46						Register Name: DiagClipOutCfg.DiagOutLvl[1]																Default: 0x00000000									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default		Description																					
31:0		DiagOutLvl[1]						0x0		Select register for UDR / LDR assignment of diagnostic checks																					

Address: 0x47						Register Name: DiagClipOutCfg.DiagOutLvl[2]																Default: 0x0000003F									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default		Description																					
31:0		DiagOutLvl[2]						0x0		Reserved																					

Address: 0x48						Register Name: DiagClipOutCfg.ClipOutLvl																Default: 0xF3330CCC									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name						Default		Description																					
15:0		ClipOutLow						0xCCC		Lower Clipping Limit 0xCCC: 5% FS																					
31:16		ClipOutHigh						0xF333		Upper Clipping Limit 0xF333: 95% FS																					

12.1.18. SSC Coefficients

Address:		0x4D 0x57		Register Name:																Bs1Coeff.SOffset – Bridge Sensor 1 Bs2Coeff.Soffset – Bridge Sensor 2																Default:		0x00000000 0x00000000							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0														
Bits		Field Name										Default		Description																															
23:0		SOffset										0x0		Sensor offset term <i>Offset_S</i>																															

Address:		0x4E 0x58		Register Name:																Bs1Coeff.SGain – Bridge Sensor 1 Bs2Coeff.SGain – Bridge Sensor 2																Default:		0x00200000 0x00200000							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0														
Bits		Field Name										Default		Description																															
23:0		SGain										0x200000		Sensor gain term <i>Gain_S</i>																															

Address:		0x4F 0x59		Register Name:																Bs1Coeff.SSot – Bridge Sensor 1 Bs2Coeff.SSot – Bridge Sensor 2																Default:		0x00000000 0x00000000							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0														
Bits		Field Name									Default			Description																															
23:0		SSot									0x0			Second-order term for sensor non-linearity <i>SOT_sens</i>																															

Address:		0x50 0x5A		Register Name:																Bs1Coeff.SShift – Bridge Sensor 1 Bs2Coeff.SShift – Bridge Sensor 2																Default:		0x00000000 0x00000000							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0														
Bits		Field Name									Default			Description																															
23:0		SShift									0x0			Post-calibration term <i>SENS_shift</i>																															

Address:		0x51 0x5B		Register Name:																Bs1Coeff.STco – Bridge Sensor 1 Bs2Coeff.STco – Bridge Sensor 2																Default:		0x00000000 0x00000000							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0														
Bits		Field Name								Default				Description																															
23:0		STco								0x0				Temperature coefficient offset term <i>Tco</i>																															

Address:		0x52 0x5C		Register Name:																Bs1Coeff.SSotTco – Bridge Sensor 1 Bs2Coeff.SSotTco – Bridge Sensor 2																Default:		0x00000000 0x00000000							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0														
Bits		Field Name								Default				Description																															
23:0		SSotTco								0x0				Second-order term for Tco nonlinearity <i>SOT_tco</i>																															

Address:		0x53 0x5D		Register Name:																Bs1Coeff.STcg – Bridge Sensor 1 Bs2Coeff.STcg – Bridge Sensor 2																Default:		0x00000000 0x00000000							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0														
Bits		Field Name									Default			Description																															
23:0		STcg									0x0			Temperature coefficient gain term <i>Tcg</i>																															

Address: 0x54 0x5E						Register Name: Bs1Coeff.SSotTcg – Bridge Sensor 1 Bs2Coeff.SSotTcg – Bridge Sensor 2																Default: 0x00000000 0x00000000											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Bits		Field Name								Default				Description																			
23:0		SSotTcg								0x0				Second-order term for Tcg non-linearity <i>SOT_tcg</i>																			

Address:		0x55 0x5F		Register Name:																Bs1Coeff.OutScaleGain – Bridge Sensor 1 Bs2Coeff.OutScaleGain – Bridge Sensor 2																Default:		0x00100000 0x00100000							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0														
Bits		Field Name								Default				Description																															
23:0		OutScaleGain								0x100000				Post SSC Output Scaling Gain																															

Address:		0x56 0x60		Register Name:																Bs1Coeff.OutScaleOfst – Bridge Sensor 1 Bs2Coeff.OutScaleOfst – Bridge Sensor 2																Default:		0x00000000 0x00000000							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0														
Bits		Field Name								Default		Description																																	
23:0		OutScaleOfst								0x0		Post SSC Output Scaling Offset																																	

Address: 0x61 0x65 0x69						Register Name: Tch1Coeff.TOffset – Temp Channel 1 Tch2Coeff.TOffset – Temp Channel 2 Tch3Coeff.TOffset – Temp Channel 3																Default: 0x00000000 0x00000000 0x00000000									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name								Default				Description																	
23:0		TOffset								0x0				Offset coefficient for temperature <i>Offset_T</i>																	

Address: 0x62 0x66 0x6A						Register Name: Tch1Coeff.TGain – Temp Channel 1 Tch2Coeff.TGain – Temp Channel 2 Tch3Coeff.TGain – Temp Channel 3																Default: 0x00200000 0x00200000 0x00200000									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name								Default		Description																			
23:0		TGain								0x200000		Gain coefficient for temperature <i>Gain_T</i>																			

Address:		0x63		Register Name:																Tch1Coeff.TSot – Temp Channel 1																Default:		0x00000000			
		0x67																																				0x00000000			
		0x6B																																				0x00000000			
																																						0x00000000			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0										
Bits		Field Name								Default				Description																											
23:0		TSot								0x0				Second-order term for temperature source <i>SOT_T</i>																											

Address:		0x64		Register Name:																Tch1Coeff.TShift – Temp Channel 1																Default:		0x00000000	
		0x68																																				0x00000000	
		0x6C																																				0x00000000	
																																						0x00000000	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0								
Bits		Field Name								Default				Description																									
23:0		TShift								0x0				Shift for post-calibration/post-assembly offset compensation T_Shift																									

12.1.19. Customer ID

Address: 0xFD						Register Name: Customer_ID_0																Default: 0x00000000									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name								Default		Description																			
31:0		Customer_ID_0								0x0		Customer free register																			

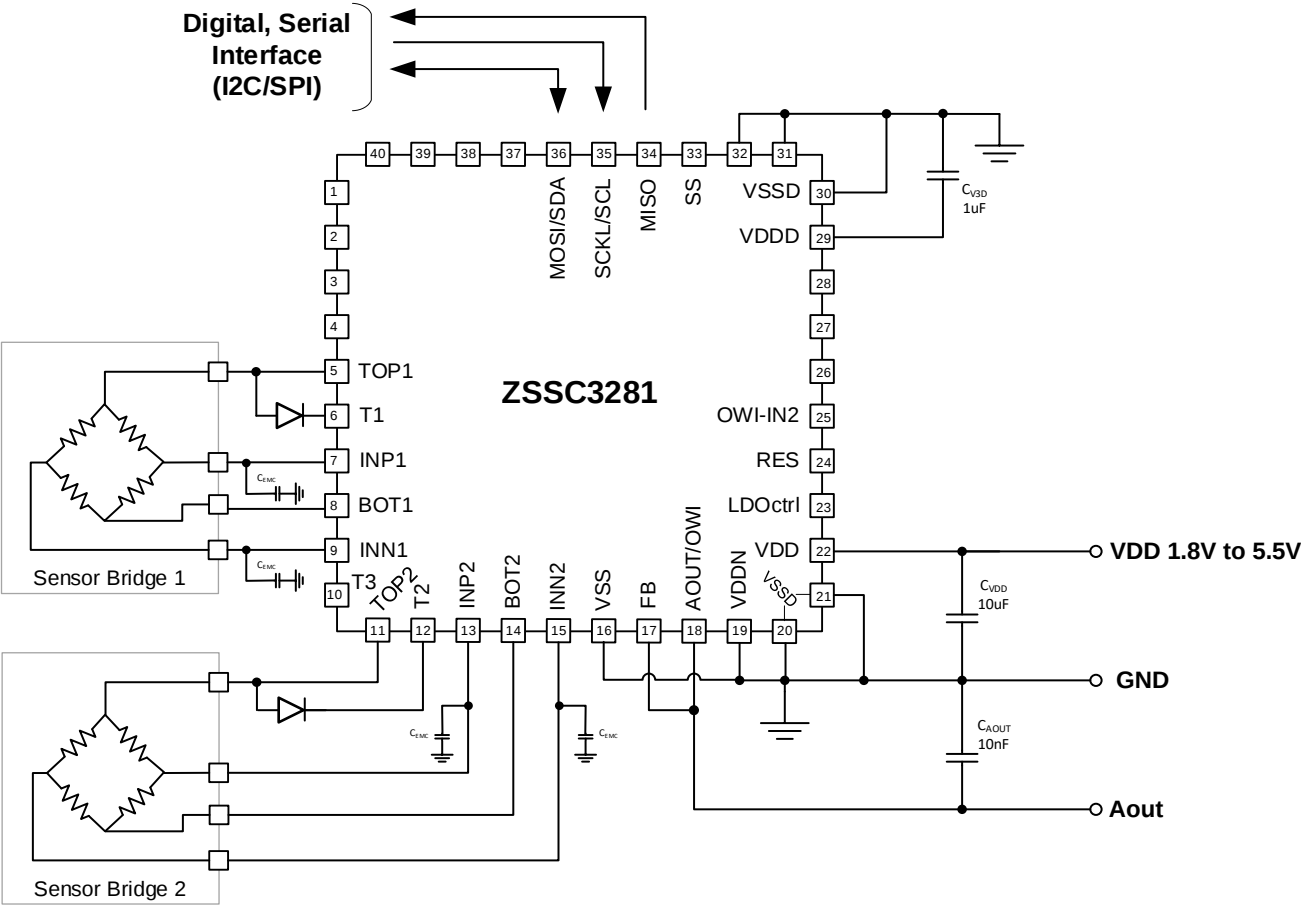
Address: 0xFE						Register Name: Customer_ID_1																Default: 0x00000000															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
Bits		Field Name								Default		Description																									
31:0		Customer_ID_1								0x0		Customer free register																									

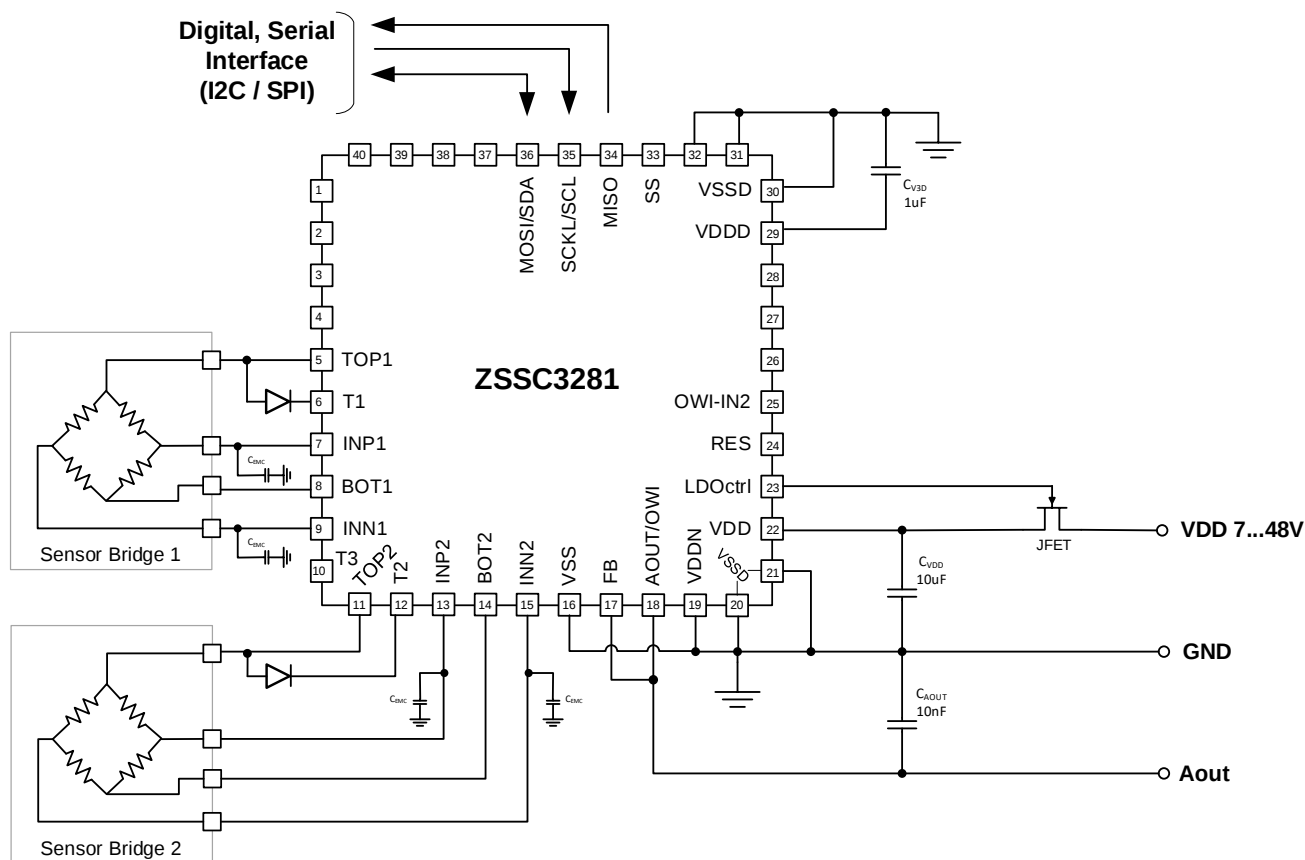
12.1.20. CCP Version

Address: 0xFF						Register Name: CcpVersion																Default: 0x00000401									
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits		Field Name								Default		Description																			
7:0		MajorVer								0x1		CCP Major Version																			
15:8		MinorVer								0x4		CCP Minor Version																			
23:16		PatchVer								0x0		CCP Patch Version																			

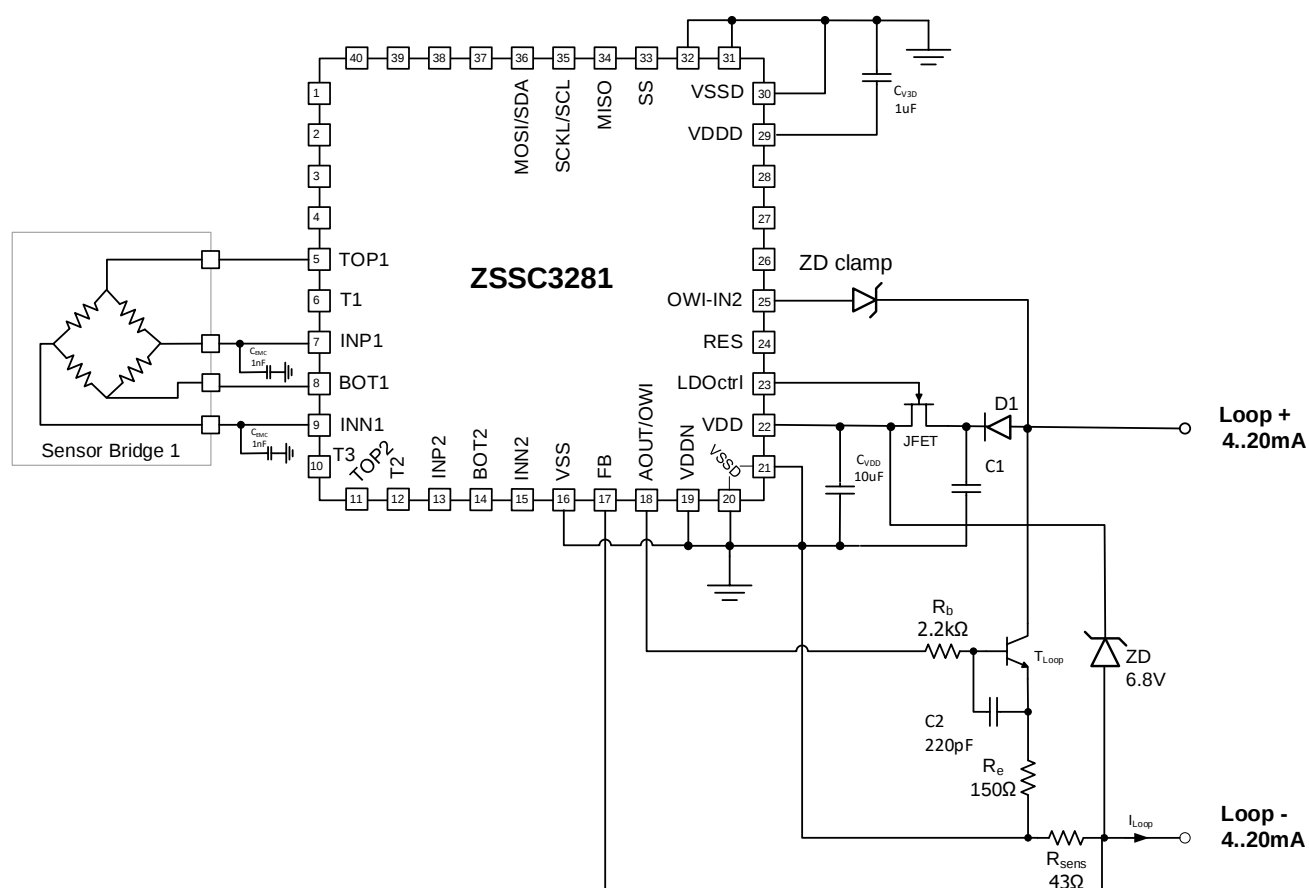
13. Application Information

13.1 2-Bridge Application 1.8V to 5.5V Supply

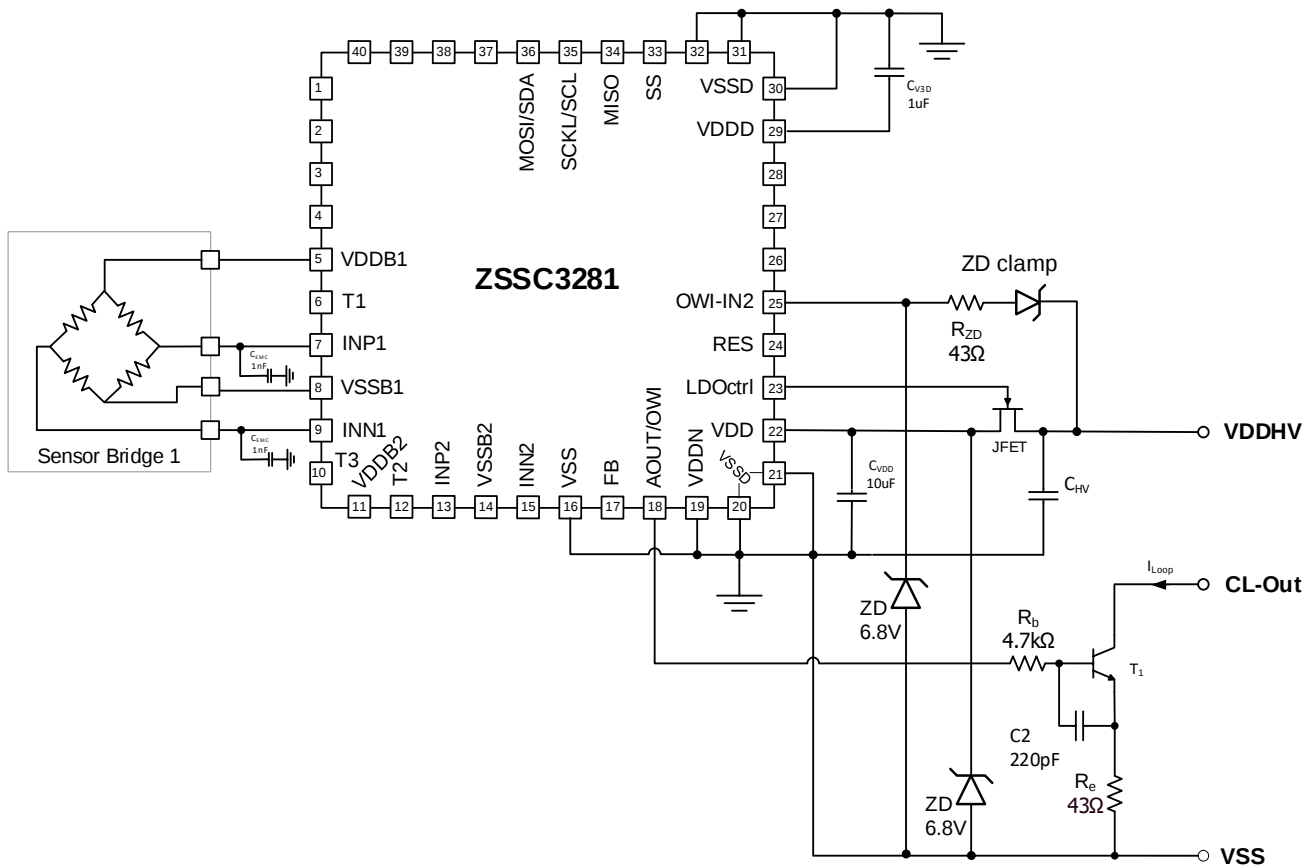




13.3 2-Wire Current Loop Application



13.4 3-Wire Current Loop Application



13.5 Power Supply

13.5.1. Power Supply Modes

ZSSC3281 supports two different main supply modes (Direct VDD Supply and Pre-Regulated High Voltage Supply) and an optional negative voltage supply for the Analog Output Driver. Respective application schematics are shown in sections 13.5.2 and 13.5.3.

Table 40: Power Supply Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VDDHV	High voltage supply	Requires external pre-regulator JFET	VDD+0.5		48	V
VDDN	Negative voltage supply for analog output (AOUT)	Internally generated, requires activation of VDDN Charge Pump		V _{ExtShottky}		V
		Externally supplied	0	-0.3V	-0.5V	V
VSS	Analog ground reference			0		V
VSSD	Digital ground reference			0		V
C _{HV}	External high voltage buffer cap	All applications except 2-wire Current Loop		10		μF

13.5.2. Direct VDD Supply

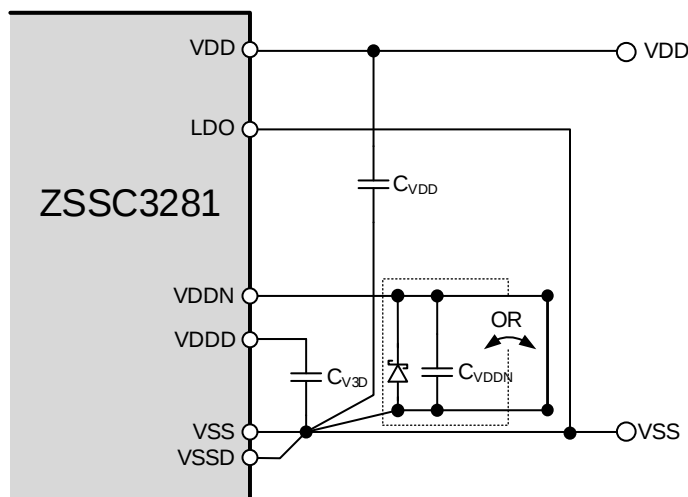


Figure 56: Application with Direct IC Supply

The Direct VDD Supply configuration requires the LDO pin to be connected to VSS on PCB level. To minimize power consumption in all operation modes, the LDO driver circuit is turned off as soon as the user selects 'Direct VDD Supply' mode during device configuration (see GUI Tab: Configure\PowerSupply & Oscillator\Supply Mode).

13.5.3. Pre-Regulated High Voltage Supply

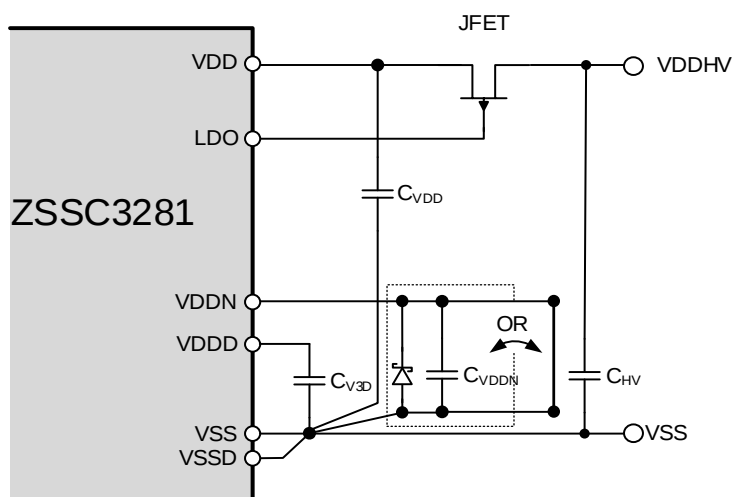


Figure 57: Application with External Regulator

Higher than 5.25V supply voltages require an external JFET as pre-regulation device. The LDO output pin of ZSSC3281 is able to drive the JFET devices listed in Table 41 in a circuit configuration as shown in Figure 57.

Table 41: Supported JFET Devices

Manufacturer	Type	Typical $V_{GS(TH)}$	Typical $I_{D/A}$ at 25°C
Supertex inc.	DN3545	-3.5V to -1.5V	0.2
Infineon	BSP149	-1.8V to -1V	0.66
Infineon	BSS169	-2.9V to -1.8V	0.17

The output voltage of the JFET assisted pre-regulator is configurable as shown in Table 42. In the GUI it can be configured through the field Configure\PowerSupply & Oscillator\Regulated VDD.

Table 42: JFET Assisted VDD Pre-Regulator Parameters

Configurable Pre-Regulator Output Voltage (VDD)	VDDHV Min	VDDHV Max ¹	Unit
3	3.5	48	V
4	4.5	48	V
5	5.5	48	V
5.25	5.75	48	V

1. VDDHV depends on selected external JFET parameters.

Besides the VDD buffer capacitor C_{VDD} another buffer capacitor C_{HV} is recommended on the high voltage supply VDDHV for stability reasons.

13.5.4. Negative Voltage Supply for AOUT

To support True-0V signals on the Analog Output (AOUT), ZSSC3281 provides an option to externally supply a negative voltage rail for the AOUT buffer at VDDN. VDDN supply specifications are shown in Table 40.

The negative VDDN voltage can also be generated by an internal charge pump circuit. The internal charge pump can be activated through GUI field: Configure\AOUT\VDDN Charge Pump.

The charge pump function is only available for all AOUT Operation Modes with Voltage Output. The charge pump circuit requires an external buffer capacitor C_{VDDN} and a Schottky Diode to work properly.

If no True-0V signals are required at AOUT, the user must directly connect VDDN with VSS on PCB level.

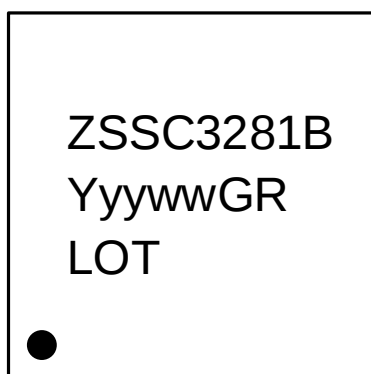
14. Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

[Package Outline Drawing Package Code: NDG40S1 40-VFQFPN 5.0 x 5.0 x 0.9 mm Body, 0.4 mm Pitch \(renesas.com\)](#)

15. Marking Diagram

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.



1. "ZSSC3281B" is the truncated part number.
2. "YyywwGR" where "Y" and "GR" are fixed and "yyww" represents the last digits of the year and week that the part was assembled.
3. "LOT" is the complete lot number of the part.

16. Glossary

Term	Description
A2D	Analog to Digital
ADC	Analog to Digital Converter
AFE	Analog Front End
ARM	Provider of microcontroller core
AUX	Auxiliary measurement, in addition to main sensor bridge measurement
AZ	Auto-zero
BOT	Bottom
CCP	Configuration and Calibration Page
CPU	Central Processing Unit
DAC	Digital to Analog Converter
DMA	Direct Memory Access
EMI	Electromagnetic Interference
EOB	End of Busy
EOC	End of Conversion signal
ESD	Electrostatic Discharge
FB	Feedback input for analog output buffer
FOUT	Frequency Output
HF	High Frequency
IAP	In Application Programming
I2C	Inter Integrated Circuit communication protocol
I3C	High speed communication protocol, extension of I2C standard
IFB	Interface Bridge – DMA Controller for serial interfaces
JFET	Junction Field Effect Transistor
LDR	Lower Diagnostic Range
LSB	Least Significant Bit
M3	Name of used micro controller core, full name is ARM Cortex M3
MCU	Micro Controller Unit
MIPI	Collaborative global organization serving industries that develop mobile and mobile-influenced devices.
MISO	Master-In Slave-Out
MOSI	Master-Out Slave-In
MSB	Most Significant Bit
NMOS	N-channel Metall Oxid Transistor
OWI	One Wire Interface
PGA	Programmable Gain Amplifier
PWM	Pulse Width Modulation
POR	Power On Reset
PTAT	Proportional to absolute temperature current source
RAM	Random Access Memory
RCA	Renesas Code Area
RTD	Temperature dependent resistor
SDR	Single Data Rate
SM-	Main Sensor Measurement, inverted signal polarity
SM+	Main Sensor Measurement, standard (non-inverted) signal polarity

Term	Description
SOT	Second Order Term
SPI	Serial Peripheral Interface
SS	Slave Select
SSC	Sensor Signal Conditioner
TLC	Third Logic Channel
UDR	Upper Diagnostic Range

17. Firmware Revision History

Revision	Date	Description
1.4.0	November 2023	• Enable VDDD brown out detection • Implement FOUT Oscillator Compensation • Implement Static Diagnostic Mode • Implement Watchdog • Implement Sleep Mode • Extend RCA firmware version command • Implement Read CCP Version command (0x89)
1.3.1	March, 2023	• Implement snapshot measurement command (0xAA) • Implement EOB functionality • Implement PWM functionality • Implement TLC mapping to AOUT and FOUT • Implement ratio operation for TLC
1.0.0	May, 2022	Initial release

18. Revision History

Revision	Date	Description
1.3	March 13, 2024	• Fixed default register content for 3C_{HEX} CCP register • Adding details about Advanced Error Response
1.2	December 6, 2023	• Adaptations for Firmware release revision 1.4.0 • Adding examples for SSC Process Image reading via I2C
1.1	April 19, 2023	• Adaptations for Firmware release revision 1.3.1 • Adding Direct linear stimulus of output path command (0xB5) • Adding 3-wire current loop application • Removed command 0x8F (Read Application Firmware) • Adding Package Outline Drawing and Marking Diagram sections
1.0	May, 2022	Initial release

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