RAA215300

High Performance 9-Channel PMIC Supporting DDR Memory, with Built-In Charger and RTC

The RAA215300 is a high-performance, low-cost 9-channel PMIC designed for 32-bit and 64-bit MCU and MPU applications. It supports DDR3, DDR3L, DDR4, and LPDDR4 memory power requirements. The internally compensated regulators, built-in Real-Time Clock (RTC), 32kHz crystal oscillator, and coin cell battery charger provide a highly integrated, small footprint power solution ideal for System-On-Module (SOM) applications. A spread spectrum feature provides an ease-of-use solution for noise-sensitive audio or RF applications.

The RAA215300 has six high-efficiency buck regulators and three LDOs to provide a complete power system. The internal device registers and EEPROM can configure and optimize the RAA215300 for different application requirements, for example, power sequences, output voltages, and switching frequencies. Dynamic Voltage Scaling (DVS) and Sleep modes are supported.

The RAA215300 is available in an 8x8mm, 0.5mm pitch thermally enhanced 56-lead QFN package and is specified for operation across a -40°C to 105°C ambient and -40°C to 125°C junction temperature range.

Features

- Input operating voltage range: 2.7V~5.5V
- 6 synchronous buck regulators (supporting 5A, 3.5A, 2x1.5A, 1A, 0.6A), with settable V_{OUT}
- 3 LDOs (supporting 2x300mA, 50mA), with bypass mode, and settable V_{OUT}
- Dedicated VTTREF for DDR memory
- Auto PFM/PWM, FPWM and ultrasonic modes, with selectable PWM f_{SW}
- Built-in 32kHz crystal oscillator (with bypass), RTC, and coin cell/supercapacitor battery charger
- DVS and sleep modes
- Internally compensated
- Spread spectrum
- I^2C serial interface (up to 1MHz)
- Pb-free (RoHS compliant)

Applications

- MCU/MPU/SoC consumer and industrial power
- FPGA system power
- Building/factory automation system power

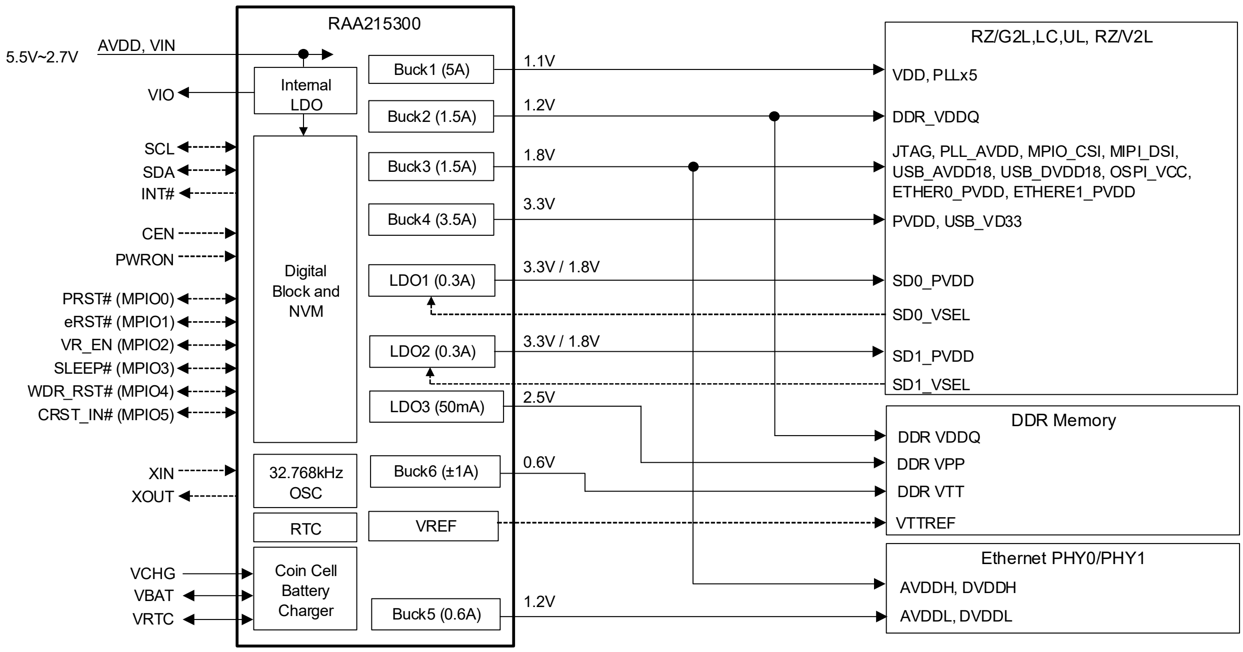


Figure 1. Typical Application Diagram - MPU Power

Contents

1. Overview

1.1 Block Diagram

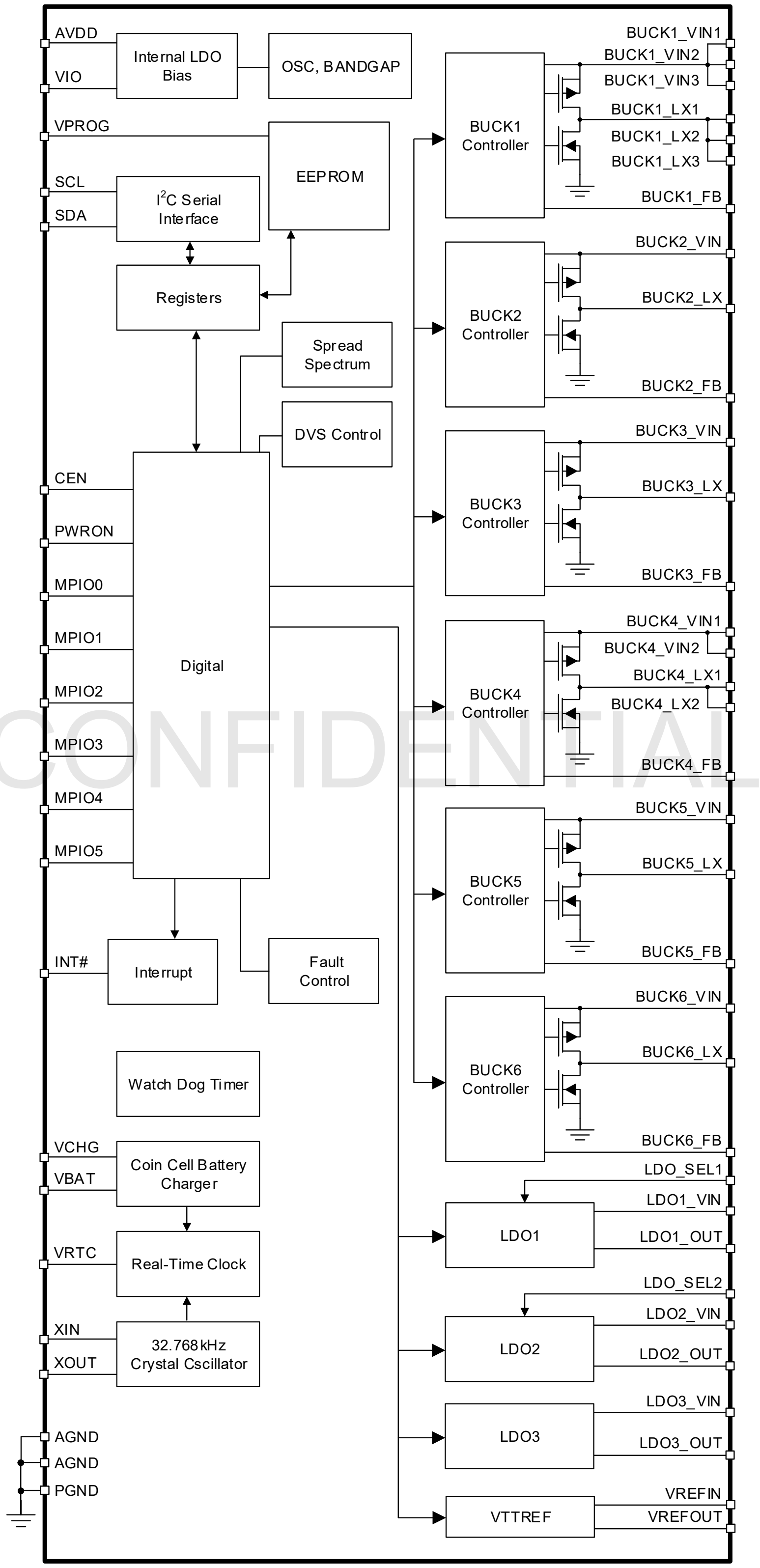
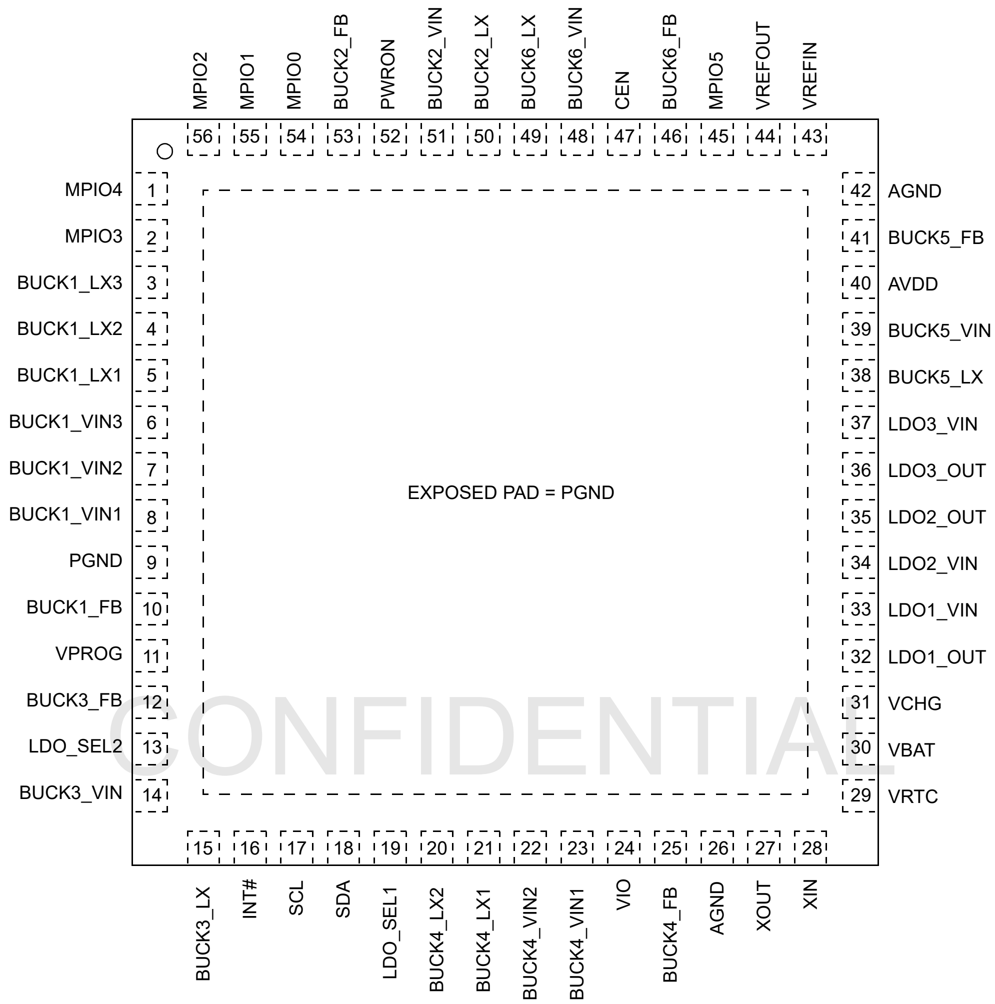


Figure 2. Block Diagram

2. Pin Information

2.1 Pin Assignments



Top View

2.2 Pin Descriptions

Pin Number	Pin Name	Type	Description
1	MPIO4[1]	Input/Output	Multiple general purpose input-output 4
2	MPIO3[1]	Input/Output	Multiple general purpose input-output 3
3	BUCK1_LX3	Output	Buck1 switch node
4	BUCK1_LX2	Output	Buck1 switch node
5	BUCK1_LX1	Output	Buck1 switch node
6	BUCK1_VIN3[2]	Power	Buck1 supply
7	BUCK1_VIN2[2]	Power	Buck1 supply
8	BUCK1_VIN1[2]	Power	Buck1 supply
9	PGND	Ground	Power ground

Pin Number	Pin Name	Type	Description
10	BUCK1_FB	Input	Buck1 feedback
11	VPROG	Power	High voltage supply input for EEPROM programming. Connect to ground in typical application.
12	BUCK3_FB	Input	Buck3 feedback
13	LDO_SEL2	Input	Logic input. Select LDO2 output voltage.
14	BUCK3_VIN[2]	Power	Buck3 supply
15	BUCK3_LX	Output	Buck3 switch node
16	INT#	Output	Interrupt output, open-drain, active low. It can also be configured as clock signal output in Frequency Output (FOUT) mode of the RTC.
17	SCL	Input	I^2C serial clock
18	SDA	Input/Output	Bidirectional I^2C serial data
19	LDO_SEL1	Input	Logic input. Select LDO1 output voltage.
20	BUCK4_LX2	Output	Buck4 switch node
21	BUCK4_LX1	Output	Buck4 switch node
22	BUCK4_VIN2[2]	Power	Buck4 supply
23	BUCK4_VIN1[2]	Power	Buck4 supply
24	VIO	Output	Internal 1.8V LDO output
25	BUCK4_FB	Input	Buck4 feedback
26, 42	AGND	Ground	Analog and digital ground
27	XOUT	Output	Crystal oscillator output. Connect to ground if not used.
28	XIN	Input	Crystal oscillator input. Connect to ground if not used.
29	VRTC	Power	Real-time clock (RTC) power supply. An output that provides power to the RTC and is generated internally from the higher of VBAT and VCHG.
30	VBAT	Power	Charger output to coin cell battery or supercapacitor, or RTC input supply when running from coin cell battery or supercapacitor. If not used, connect to GND.
31	VCHG	Power	Input Supply for VIO LDO, Coin cell battery charger and RTC input power. AVDD, VCHG, and BUCKx_VINx must be the same voltage.
32	LDO1_OUT	Output	LDO1 output
33	LDO1_VIN	Power	LDO1 supply
34	LDO2_VIN	Power	LDO2 supply
35	LDO2_OUT	Output	LDO2 output
36	LDO3_OUT	Output	LDO3 output
37	LDO3_VIN	Power	LDO3 supply
38	BUCK5_LX	Output	Buck5 switch node
39	BUCK5_VIN[2]	Power	Buck5 supply
40	AVDD	Power	Analog and digital supply. AVDD, VCHG, and BUCKx_VINx must be the same voltage.
41	BUCK5_FB	Input	Buck5 feedback
43	VREFIN	Input	Input to VTTREF block. *Note:* Pin has a 1MΩ (typical) internal resistor to GND.

Pin Number	Pin Name	Type	Description
44	VREFOUT	Output	Output from VTTREF block, with value equal to (VREFIN/2). Used as reference for VTT.
45	MPIO5[1]	Input/Output	Configurable multiple purpose input-output 5
46	BUCK6_FB	Input	Buck6 feedback
47	CEN	Input	Chip enable, active high
48	BUCK6_VIN[2]	Power	Buck6 supply
49	BUCK6_LX	Output	Buck6 switch node
50	BUCK2_LX	Output	Buck2 switch node
51	BUCK2_VIN[2]	Power	Buck2 supply
52	PWRON	Input	Regulator output enable
53	BUCK2_FB	Input	Buck2 feedback
54	MPIO0[1]	Input/Output	Configurable multiple purpose input-output 0
55	MPIO1[1]	Input/Output	Configurable multiple purpose input-output 1
56	MPIO2[1]	Input/Output	Configurable multiple purpose input-output 2
-	EPAD	Ground	Exposed thermal pad. Power ground. All regulator PGNDs are internally downbonded to the EPAD.

1. See Multi Purpose I/O for pin function mapping.
2. All buck supplies (BUCKx_VINx) = AVDD = VCHG.

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Voltage (to PGND unless otherwise stated)			
BUCKx_VINx, AVDD, VCHG	-0.3	6	V
VBAT	-0.3	6	V
BUCKx_FB	-0.3	6	V
BUCKx_LXx	-0.3	6	V
BUCKx_LXx[1]		6.7	V
AGND, PGND	-0.3	0.3	V
VPROG	-0.3	24	V
All other pins	-0.3	6	V

1. ≤20ns duration

3.2 ESD Ratings

ESD Model/Test	Rating	Unit
Human Body Model (Tested per JS-001-2017)	±2	kV
Charged Device Model (Tested per JS-002-2018)	±500	V
Latch-Up (Tested per JESD78E; Class 2, Level A)	100	mA

3.3 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W)[2]
56LD, 8x8mm QFN Package	23	0.7

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature (T_J)		+150	°C
Maximum Storage Temperature Range (T_S)	-65	+150	°C
Pb-Free Reflow Profile	see TB493		

3.4 Recommended Operation Conditions

Voltages referred to PGND unless otherwise stated.

Parameter	Minimum	Maximum	Unit
Ambient Operating Temperature Range (T_A)	-40	+105	°C
Operating Junction Temperature (T_J)		+125	°C
BUCKx_VINx, AVDD, VCHG	2.7	5.5	V
VBAT	1.8	5.5	V
MPIOx	-	5	V
CEN, PWRON	-	5	V
VPROG	0	23	V
SCL, SDA	0	3.3	V

3.5 Electrical Specifications

AVDD = VCHG = BUCKx_VINx = 5V, BUCK1_FB = 1.1V, BUCK2_FB = 1.2V, BUCK3_FB = 1.8V, BUCK4_FB = 3.3V, BUCK5_FB = 1.2V, BUCK6_FB = 0.6V, LDOx_VIN = 5V, LDO1_OUT = 3.3V, LDO2_OUT = 3.3V, LDO3_OUT = 2.5V, CEN = HIGH, PWRON = HIGH, AGND = PGND, unless otherwise specified. External components as listed in External Component Selection section (or equivalent), unless otherwise stated. Typical entries apply at +25°C. **Boldface limits apply across the ambient operating temperature range -40°C to +105°C, unless otherwise stated.**

Parameter	Symbol	Test Conditions[1]	Min[2]	Typ	Max[2]	Unit
Input Supply						
AVDD Input Operating Range	$AVDD_{OP}$	AVDD = VCHG = BUCKx_VINx	**2.7**	5	**5.5**	V
BUCK Input Operating Range	$BUCK_{OP}$	BUCKx_VINx	**2.7**	5	**5.5**	V
LDO Input Operating Range	LDO_{OP}	LDOx_VIN	**2.7**	3.3	**5.5**	V
VCHG Input Operating Range	$VCHG_{OP}$	AVDD = VCHG = BUCKx_VINx	**2.7**	5	**5.5**	V
VCHG Falling Slew Rate[3]	$VCHG_{FALL}$	To ensure POR operation of RTC do not exceed the maximum falling slew rate. AVDD = VCHG = BUCKx_VINx			**5**	V/ms
AVDD Undervoltage Lockout Threshold	$AVDD_{UVLO\_R}$	Rising threshold		2.3		V
AVDD Undervoltage Lockout Threshold	$AVDD_{UVLO\_F}$	Falling threshold		2.1		V
AVDD Undervoltage Lockout Threshold	$AVDD_{UVLO\_HYS}$	$AVDD_{UVLO\_HYS} = AVDD_{UVLO\_R} - AVDD_{UVLO\_F}$		200		mV
AVDD Undervoltage Power Down Threshold	$AVDD_{UVPD\_F}$	Falling AVDD, 2.7V setting		2.7		V
		Falling AVDD, 3.0V setting		3.0		
		Falling AVDD, 4.25V setting		4.25		
AVDD Undervoltage Power Down Threshold Accuracy	$AVDD_{UVPD\_ACC}$	Falling AVDD	**-3**		**3**	%
AVDD Undervoltage Power Down Threshold Hysteresis	$AVDD_{UVPD\_HYS}$	$AVDD_{UVPD\_HYS} = AVDD_{UVPD\_R} - AVDD_{UVPD\_F}$		100		mV

AVDD = VCHG = BUCKx_VINx = 5V, BUCK1_FB = 1.1V, BUCK2_FB = 1.2V, BUCK3_FB = 1.8V, BUCK4_FB = 3.3V, BUCK5_FB = 1.2V, BUCK6_FB = 0.6V, LDOx_VIN = 5V, LDO1_OUT = 3.3V, LDO2_OUT = 3.3V, LDO3_OUT = 2.5V, CEN = HIGH, PWRON = HIGH, AGND = PGND, unless otherwise specified. External components as listed in External Component Selection section (or equivalent), unless otherwise stated. Typical entries apply at +25°C. **Boldface limits apply across the ambient operating temperature range -40°C to +105°C, unless otherwise stated. (Cont.)**

Parameter	Symbol	Test Conditions[1]	Min[2]	Typ	Max[2]	Unit
AVDD UVPD Delay	$AVDD_{UVPD\_DLY}$	Falling AVDD		100		µs
Operating Bias Current						
{SHUTDOWN} Supply Current	I_{SHDN_AVDD}	Current into AVDD, CEN = LOW, T_A = 25°C		<1	**7**	µA
{SHUTDOWN} Supply Current	I_{SHDN_VCHG}	Current into VCHG, VBAT < VCHG CEN = LOW, T_A = 25°C		400	**950**	nA
RTC Battery Supply Current	I_{BAT}	VBAT = 3V, AVDD = VCHG = 0V. RTC is enabled in 0x6C[6]. Internal oscillator is enabled in 0x07[6] with external crystal.		400	**950**	nA
		VBAT = 3V, Shipping mode (RTC is disabled in 0x6C[6])		120	**320**	nA
{STANDBY} Supply Current	I_{OP_STANDY}	Total input current. CEN = HIGH, AVDD > UVLO, PWRON = LOW. RTC off.		360	**470**	µA
{ACTIVE} Supply Current	I_{OP_ACTIVE}	Total input current. CEN = HIGH, AVDD > UVLO, PWRON = HIGH All bucks enabled, auto PFM/PWM mode, no load, not switching. All LDOs enabled, no load. RTC on. I^2C on and idle, MPIOx static.		3.2	**4.8**	mA
RTC State Supply Current	I_{OP_RTC}	Total input current, VBAT. VBAT = 3.3V, BUCKx_VINx = AVDD = VCHG = 0V, RTC is enabled and clocking, FOUT is enabled at INT#			**5**	µA
VIO LDO						
VIO LDO Output Voltage	VIO_{OUT}	Not in dropout, no external loading	**1.62**	1.8	**1.96**	V
VIO LDO Current Capability	VIO_{IOUT_RNG}	Additional external loading[4]		20		mA
VIO LDO Current Limit	VIO_{ILIM}	VIO = 90% * VIO_{OUT}	**24**		**41**	mA
VIO Load Transient Response	VIO_{LOAD_TR}	Step: 0 to 20mA in 1µs Step: 20mA to 0 in 1µs	**-3**		**3**	%
VIO LDO Power-Good Rising Threshold	VIO_{PGOOD_Rise}	VIO rising. Percentage of VIO_{OUT}	**-10**	-5	**-2**	%
VIO LDO Power-Good Falling Threshold	VIO_{PGOOD_Fall}	VIO falling. Percentage of VIO_{OUT}	**-15**	-10	**-7**	%
VIO LDO Power-Good Threshold Hysteresis	VIO_{PGOOD_HYS}	$VIO_{PGOOD\_HYS} = VIO_{PGOOD\_Rise} - VIO_{PGOOD\_Fall}$		5		%

AVDD = VCHG = BUCKx_VINx = 5V, BUCK1_FB = 1.1V, BUCK2_FB = 1.2V, BUCK3_FB = 1.8V, BUCK4_FB = 3.3V, BUCK5_FB = 1.2V, BUCK6_FB = 0.6V, LDOx_VIN = 5V, LDO1_OUT = 3.3V, LDO2_OUT = 3.3V, LDO3_OUT = 2.5V, CEN = HIGH, PWRON = HIGH, AGND = PGND, unless otherwise specified. External components as listed in External Component Selection section (or equivalent), unless otherwise stated. Typical entries apply at +25°C. **Boldface limits apply across the ambient operating temperature range -40°C to +105°C, unless otherwise stated. (Cont.)**

Parameter	Symbol	Test Conditions[1]	Min[2]	Typ	Max[2]	Unit
EEPROM						
EEPROM Endurance	EE_{ENDR}	Programming cycles	**1000**			Cycles
Loading EEPROM Data to Registers at Power-On	t_{EE_LOAD}	AVDD valid. CEN = HIGH			**10**	ms
EEPROM Programming Cycle Time	t_{EE_WRITE}	Total time for writing customer banks		216	**238**	ms
BUCK1 (5A) Components as described in Recommended External Components. Additional application details in Buck1.						
Buck1 Output Voltage Target Resolution	$BK1_{RES}$			**4**		bits
Buck1 Output Voltage Range	$BK1_{OUT}$	BUCK1_FB	**0.8**		**1.5**	V
Buck1 Output Voltage Step	$BK1_{STEP}$	BUCK1_FB		50		mV
Buck1 Output Voltage DC Accuracy	$BK1_{ACC}$	BUCK1_FB. PWM operation, I_{OUT} = 5mA, V_{OUT} = 1.1V	**-1**		**1**	%
Buck1 Output Voltage Ripple FPWM	$BK1_{RIP\_FPWM}$	I_{OUT} = 100mA, FPWM mode		10		mVpp
Buck1 Maximum Output Current Capability[5]	$BK1_{IOUT\_MAX}$		**5**			A
Buck1 Output Load Regulation	$BK1_{LOAD\_REG}$	FPWM, VOUT = 1.1V, Over I_{OUT} = 100mA to 5A range		±0.1		%
Buck1 Output Line Regulation	$BK1_{LINE\_REG}$	FPWM, BUCK1_VINx = 4.5V ↔ 5.5V, VOUT = 1.1V, I_{OUT} = $BK1_{IOUT\_MAX}$		±0.1		%
Buck1 Peak Efficiency	$BK1_{EFF}$	Peak efficiency, L = default, $BK1_{FSW}$ set to default[6], maximum V_{OUT}		92	-	%
Buck1 Discharge Resistance	$BK1_{RDCHG}$	BUCK1_FB. Slow setting enabled	35	50	65	Ω
		BUCK1_FB. Medium setting enabled	26	37.5	49	Ω
		BUCK1_FB. Fast setting enabled	17.5	25	32.5	Ω
Buck1 High-Side MOSFET Current Limit	$BK1_{ILIM\_HS}$	PWM operation, sourcing (supplying)	**6.1**	7	**7.7**	A
Buck1 Low-Side MOSFET Current Limit	$BK1_{ILIM\_LS}$	PWM operation, sourcing (supplying)		7.5		A
	$BK1_{ILIMNEG}$	FPWM mode, sinking (receiving)		-0.7		

AVDD = VCHG = BUCKx_VINx = 5V, BUCK1_FB = 1.1V, BUCK2_FB = 1.2V, BUCK3_FB = 1.8V, BUCK4_FB = 3.3V, BUCK5_FB = 1.2V, BUCK6_FB = 0.6V, LDOx_VIN = 5V, LDO1_OUT = 3.3V, LDO2_OUT = 3.3V, LDO3_OUT = 2.5V, CEN = HIGH, PWRON = HIGH, AGND = PGND, unless otherwise specified. External components as listed in External Component Selection section (or equivalent), unless otherwise stated. Typical entries apply at +25°C. **Boldface limits apply across the ambient operating temperature range -40°C to +105°C, unless otherwise stated. (Cont.)**

Parameter	Symbol	Test Conditions[1]	Min[2]	Typ	Max[2]	Unit
Buck1 High-Side Overcurrent Warning Threshold Range	$BK1_{IHC}$	Register settable values [5]	3.6	4.6	5.6	A
			4.4	5.4	6.4	
			4.7	5.7	6.7	
			5.1	6.1	7.1	
Buck1 High-Side Overcurrent Warning Threshold Accuracy	$BK1_{IHC\_ACC}$	default $BK1_{IHC}$ setting	**-1**		**+1**	A
Buck1 PWM Switching Frequency	$BK1_{FSW}$	FPWM mode, 1.11MHz (default) setting		1.11		MHz
Buck1 PWM Switching Frequency Accuracy	$BK1_{FSW\_ACC}$	FPWM mode, I_{OUT} = 0mA, default frequency	**-10**		**+10**	%
Buck1 Soft-Start Slew Rate Range	$BK1_{SS\_SR\_RNG}$	BUCK1_FB	**0.5**	1	**4**	ms
Buck1 Shutdown Slew Rate Range	$BK1_{SHTDN\_SR\_RNG}$	BUCK1_FB	**0.5**	1	**4**	ms
Buck1 DVS Slew Rate Range	$BK1_{DVS\_SR\_RNG}$	BUCK1_FB. Applies to both DVS up and down ramps.	**2**	8	**16**	mV/µs
Buck1 High-Side PMOS On-resistance	$BK1_{RDSON\_HS}$	BUCK1_VINx to BUCK1_LXx, I_{LX} = -150mA		40		mΩ
Buck1 Low-Side NMOS On-Resistance	$BK1_{RDSON\_LS}$	BUCK1_LXx to PGND, I_{LX} = 150mA		28		mΩ
BUCK2 (1.5A) Components as described in Recommended External Components. Additional application details in Buck2.						
Buck2 Output Voltage Target Resolution	$BK2_{RES}$			**4**		bits
Buck2 Output Voltage Range	$BK2_{OUT}$	BUCK2_FB	**1.1**	-	**1.85**	V
Buck2 Output Voltage Step	$BK2_{STEP}$	BUCK2_FB		50		mV
Buck2 Output Voltage DC Accuracy	$BK2_{ACC}$	BUCK2_FB. PWM operation, I_{OUT} = 5mA, V_{OUT} = 1.2V	**-1**	-	**1**	%
Buck2 Output Voltage Ripple FPWM	$BK2_{RIP\_FPWM}$	I_{OUT} = 100mA, FPWM mode		10	**-**	mVpp
Buck2 Maximum Output Current Capability[5]	$BK2_{IOUT\_MAX}$		**1.5**			A
Buck2 Output Load Regulation	$BK2_{LOAD\_REG}$	FPWM, VOUT = 1.2V, Over I_{OUT} = 100mA to 1.5A range		±0.15		%
Buck2 Output Line Regulation	$BK2_{LINE\_REG}$	BUCK2_VINx = 4.5V ↔ 5.5V, VOUT = 1.2V, I_{OUT} = $BK2_{IOUT\_MAX}$		±0.15		%

AVDD = VCHG = BUCKx_VINx = 5V, BUCK1_FB = 1.1V, BUCK2_FB = 1.2V, BUCK3_FB = 1.8V, BUCK4_FB = 3.3V, BUCK5_FB = 1.2V, BUCK6_FB = 0.6V, LDOx_VIN = 5V, LDO1_OUT = 3.3V, LDO2_OUT = 3.3V, LDO3_OUT = 2.5V, CEN = HIGH, PWRON = HIGH, AGND = PGND, unless otherwise specified. External components as listed in External Component Selection section (or equivalent), unless otherwise stated. Typical entries apply at +25°C. **Boldface limits apply across the ambient operating temperature range -40°C to +105°C, unless otherwise stated. (Cont.)**

Parameter	Symbol	Test Conditions[1]	Min[2]	Typ	Max[2]	Unit
Buck2 Peak Efficiency	$BK2_{EFF}$	Peak efficiency, L = default, $BK2_{FSW}$ set to default[6], maximum V_{OUT}		90		%
Buck2 Discharge Resistance	$BK2_{RDCHG}$	BUCK2_FB. Slow setting	35	50	65	Ω
		BUCK2_FB. Medium setting	26	37.5	49	
		BUCK2_FB. Fast setting	17.5	25	32.5	
Buck2 High-Side MOSFET Current Limit	$BK2_{ILIM\_HS}$	PWM operation, sourcing (supplying)	**2.27**	2.5	**2.78**	A
Buck2 Low-Side MOSFET Current Limit	$BK2_{ILIM\_LS}$	PWM operation, sourcing (supplying)		3		A
	$BK2_{ILIMNEG}$	FPWM mode, sinking (receiving)		-0.66		A
Buck2 PWM Switching Frequency	$BK2_{FSW}$	FPWM mode, 0.769MHz (default) setting		0.769		MHz
Buck2 PWM Switching Frequency Accuracy	$BK2_{FSW\_ACC}$	FPWM mode, I_{OUT} = 0mA, default frequency	**-10**		**+10**	%
Buck2 Soft-start Slew Rate Range	$BK2_{SS\_SR\_RNG}$	BUCK2_FB	**0.5**	1	**4**	ms
Buck2 Shutdown Slew Rate Range	$BK2_{SHTDN\_SR\_RNG}$	BUCK2_FB	**0.5**	1	**4**	ms
Buck2 DVS Slew Rate Range	$BK2_{DVS\_SR\_RNG}$	BUCK2_FB. Applies to both DVS up and down ramps.	**2**	8	**16**	mV/µs
Buck2 High-Side PMOS On-Resistance	$BK2_{RDSON\_HS}$	BUCK2_VINx to BUCK2_LXx, I_{LX} = -150mA		120		mΩ
Buck2 Low-Side NMOS On-Resistance	$BK2_{RDSON\_LS}$	BUCK2_LXx to PGND, I_{LX} = 150mA		70		mΩ
BUCK3 (1.5A) Components as described in Recommended External Components. Additional application details in Buck3.						
Buck3 Output Voltage Target Resolution	$BK3_{RES}$			**4**		bits
Buck3 Output Voltage Range	$BK3_{OUT}$	BUCK3_FB	**1.8**		**3.3**	V
Buck3 Output Voltage Step	$BK3_{STEP}$	BUCK3_FB		100		mV
Buck3 Output Voltage DC Accuracy	$BK3_{ACC}$	BUCK3_FB. PWM operation, I_{OUT} = 5mA, V_{OUT} = 1.8V	**-1**		**1**	%
Buck3 Output Voltage Ripple FPWM	$BK3_{RIP\_FPWM}$	I_{OUT} = 100mA, FPWM mode		10		mVpp
Buck3 Maximum Output Current Capability[5]	$BK3_{IOUT\_MAX}$		**1.5**			A

AVDD = VCHG = BUCKx_VINx = 5V, BUCK1_FB = 1.1V, BUCK2_FB = 1.2V, BUCK3_FB = 1.8V, BUCK4_FB = 3.3V, BUCK5_FB = 1.2V, BUCK6_FB = 0.6V, LDOx_VIN = 5V, LDO1_OUT = 3.3V, LDO2_OUT = 3.3V, LDO3_OUT = 2.5V, CEN = HIGH, PWRON = HIGH, AGND = PGND, unless otherwise specified. External components as listed in External Component Selection section (or equivalent), unless otherwise stated. Typical entries apply at +25°C. **Boldface limits apply across the ambient operating temperature range -40°C to +105°C, unless otherwise stated. (Cont.)**

Parameter	Symbol	Test Conditions[1]	Min[2]	Typ	Max[2]	Unit
Buck3 Output Load Regulation	$BK3_{LOAD\_REG}$	FPWM, VOUT = 1.8V, Over I_{OUT} = 100mA to 1.5A range		±0.1		%
Buck3 Output Line Regulation	$BK3_{LINE\_REG}$	BUCK3_VINx = 4.5V ↔ 5.5V, VOUT = 1.8V, I_{OUT} = $BK3_{IOUT\_MAX}$		±0.1		%
Buck3 Peak Efficiency	$BK3_{EFF}$	Peak efficiency, L = default, $BK3_{FSW}$ set to default[6], maximum V_{OUT}		92		%
Buck3 Discharge Resistance	$BK3_{RDCHG}$	BUCK3_FB. Slow setting	35	50	75	Ω
		BUCK3_FB. Medium setting	26	37.5	49	
		BUCK3_FB. Fast setting	17.5	25	32.5	
Buck3 High-Side MOSFET Current Limit	$BK3_{ILIM\_HS}$	PWM mode, sourcing (supplying)	**2.12**	2.5	**3**	A
Buck3 Low-Side MOSFET Current Limit	$BK3_{ILIM\_LS}$	PWM operation, sourcing (supplying)		3		A
	$BK3_{ILIMNEG}$	FPWM mode, sinking (receiving)		-0.55		
Buck3 PWM Switching Frequency	$BK3_{FSW}$	FPWM mode, 1.54MHz (default) setting		1.54		MHz
Buck3 PWM Switching Frequency Accuracy	$BK3_{FSW\_ACC}$	FPWM mode, I_{OUT} = 0mA, default frequency	**-10**		**+10**	%
Buck3 Soft-Start Slew Rate Range	$BK3_{SS\_SR\_RNG}$	BUCK3_FB	**0.5**	1	**4**	ms
Buck3 Shutdown Slew Rate Range	$BK3_{SHTDN\_SR\_RNG}$	BUCK3_FB	**0.5**	1	**4**	ms
Buck3 DVS Slew Rate Range	$BK3_{DVS\_SR\_RNG}$	BUCK3_FB. Applies to both DVS up and down ramps.	**2**	8	**16**	mV/µs
Buck3 High-Side PMOS On-Resistance	$BK3_{RDSON\_HS}$	BUCK3_VINx to BUCK3_LXx, I_{LX} = -150mA		93		mΩ
Buck3 Low-Side NMOS On-Resistance	$BK3_{RDSON\_LS}$	BUCK3_LXx to PGND, I_{LX} = 150mA		57		mΩ
BUCK4 (3.5A) Components as described in Recommended External Components. Additional application details in Buck4.						
Buck4 Output Voltage Target Resolution	$BK4_{RES}$			**4**		bits
Buck4 Output Voltage Range	$BK4_{OUT}$	BUCK4_FB 0.8V, 0.85V, 0.9V, 0.95V, 1V,1.05V, 1.1V, 1.15V, 1.2V, 1.5V, 1.6V 1.8V, 1.85V, 2.2V, 2.5V and 3.3V	**0.8**		**3.3**	V
Buck4 Output Voltage DC Accuracy	$BK4_{ACC}$	BUCK4_FB. PWM operation, I_{OUT} = 5mA, V_{OUT} = 3.3V	**-1**		**1**	%

AVDD = VCHG = BUCKx_VINx = 5V, BUCK1_FB = 1.1V, BUCK2_FB = 1.2V, BUCK3_FB = 1.8V, BUCK4_FB = 3.3V, BUCK5_FB = 1.2V, BUCK6_FB = 0.6V, LDOx_VIN = 5V, LDO1_OUT = 3.3V, LDO2_OUT = 3.3V, LDO3_OUT = 2.5V, CEN = HIGH, PWRON = HIGH, AGND = PGND, unless otherwise specified. External components as listed in External Component Selection section (or equivalent), unless otherwise stated. Typical entries apply at +25°C. **Boldface limits apply across the ambient operating temperature range -40°C to +105°C, unless otherwise stated. (Cont.)**

Parameter	Symbol	Test Conditions[1]	Min[2]	Typ	Max[2]	Unit
Buck4 Output Voltage Ripple FPWM	$BK4_{RIP\_FPWM}$	I_{OUT} = 100mA, FPWM mode		15		mVpp
Buck4 Maximum Output Current Capability[5]	$BK4_{IOUT\_MAX}$		**3.5**			A
Buck4 Output Load Regulation	$BK4_{LOAD\_REG}$	FPWM, VOUT = 3.3V, Over I_{OUT} = 100mA to 3.5A range		±0.1		%
Buck4 Output Line Regulation	$BK4_{LINE\_REG\_3V3}$	BUCK4_VINx = 4.5V ↔ 5.5V, VOUT = 3.3V, I_{OUT} = $BK4_{IOUT\_MAX}$		±0.1		%
Buck4 Peak Efficiency	$BK4_{EFF}$	Peak efficiency, L = default, $BK4_{FSW}$ set to default[6], maximum V_{OUT}		95		%
Buck4 Discharge Resistance	$BK4_{RDCHG}$	BUCK4_FB. Slow setting	35	50	65	Ω
		BUCK4_FB. Medium setting	26	37.5	49	
		BUCK4_FB. Fast setting	17.5	25	32.5	
Buck4 High-Side MOSFET Current Limit	$BK4_{ILIM\_HS}$	PWM operation, sourcing (supplying)	**4**	4.5	**5**	A
Buck4 Low-Side MOSFET Current Limit	$BK4_{ILIM\_LS}$	PWM operation, sourcing (supplying)		5		A
	$BK4_{ILIMNEG}$	FPWM mode, sinking (receiving)		-0.675		
Buck4 PWM Switching Frequency	$BK4_{FSW}$	FPWM mode, 1.54MHz (default) setting		1.54		MHz
Buck4 PWM Switching Frequency Accuracy	$BK4_{FSW\_ACC}$	FPWM mode, I_{OUT} = 0mA, default frequency	**-10**		**+10**	%
Buck4 Soft-Start Slew Rate Range	$BK4_{SS\_SR\_RNG}$	BUCK4_FB	**0.5**	1	**4**	ms
Buck4 Shutdown Slew Rate Range	$BK4_{SHTDN\_SR\_RNG}$	BUCK4_FB	**0.5**	1	**4**	ms
Buck4 DVS Slew Rate Range	$BK4_{DVS\_SR\_RNG}$	BUCK4_FB. Applies to both DVS up and down ramps.	**2**	8	**16**	mV/µs
Buck4 High-Side PMOS On-Resistance	$BK4_{RDSON\_HS}$	BUCK4_VINx to BUCK4_LXx, I_{LX} = -150mA		60		mΩ
Buck4 Low-Side NMOS On-Resistance	$BK4_{RDSON\_LS}$	BUCK4_LXx to PGND, I_{LX} = 150mA		30		mΩ
BUCK5 (0.6A) Components as described in Recommended External Components. Additional application details in Buck5.						
Buck5 Output Voltage Target Resolution	$BK5_{RES}$			**3**		bits
Buck5 Output Voltage Range	$BK5_{OUT}$	BUCK5_FB	**1.2**	-	**3.3**	V

AVDD = VCHG = BUCKx_VINx = 5V, BUCK1_FB = 1.1V, BUCK2_FB = 1.2V, BUCK3_FB = 1.8V, BUCK4_FB = 3.3V, BUCK5_FB = 1.2V, BUCK6_FB = 0.6V, LDOx_VIN = 5V, LDO1_OUT = 3.3V, LDO2_OUT = 3.3V, LDO3_OUT = 2.5V, CEN = HIGH, PWRON = HIGH, AGND = PGND, unless otherwise specified. External components as listed in External Component Selection section (or equivalent), unless otherwise stated. Typical entries apply at +25°C. **Boldface limits apply across the ambient operating temperature range -40°C to +105°C, unless otherwise stated. (Cont.)**

Parameter	Symbol	Test Conditions[1]	Min[2]	Typ	Max[2]	Unit
Buck5 Output Voltage DC Accuracy	$BK5_{ACC}$	BUCK5_FB. PWM operation, I_{OUT} = 5mA, V_{OUT} = 1.8V	**-1**		**1**	%
Buck5 Output Voltage Ripple FPWM	$BK5_{RIP\_FPWM}$	I_{OUT} = 100mA, FPWM mode		15		mVpp
Buck5 Maximum Output Current Capability[5]	$BK5_{IOUT\_MAX}$		**0.6**			A
Buck5 Output Load Regulation	$BK5_{LOAD\_REG}$	FPWM, VOUT = 1.2V, Over I_{OUT} = 100mA to 600mA range		±0.1		%
Buck5 Output Line Regulation	$BK5_{LINE\_REG}$	BUCK5_VINx = 4.5V ↔ 5.5V, VOUT = 1.2V, I_{OUT} = $BK5_{IOUT\_MAX}$		±0.1		%
Buck5 Peak Efficiency	$BK5_{EFF}$	Peak efficiency, L = default, $BK5_{FSW}$ set to default[6], maximum V_{OUT}		94		%
Buck5 Discharge Resistance	$BK5_{RDCHG}$	BUCK5_FB. Slow setting	35	50	65	Ω
		BUCK5_FB. Medium setting	26	37.5	49	
		BUCK5_FB. Fast setting	17.5	25	32.5	
Buck5 High-Side MOSFET Current Limit	$BK5_{ILIM\_HS}$	PWM operation, sourcing (supplying)	**0.9**	1	**1.1**	A
Buck5 Low-Side MOSFET Current Limit	$BK5_{ILIM\_LS}$	PWM operation, sourcing (supplying)		1.4		A
	$BK5_{ILIMNEG}$	FPWM mode, sinking (receiving)		-0.55		
Buck5 PWM Switching Frequency	$BK5_{FSW}$	FPWM mode, 1.54MHz (default) setting		1.54		MHz
Buck5 PWM Switching Frequency Accuracy	$BK5_{FSW\_ACC}$	FPWM mode, I_{OUT} = 0mA, default frequency	**-10**		**+10**	%
Buck5 Soft-start Slew Rate Range	$BK5_{SS\_SR\_RNG}$	BUCK5_FB	**0.5**	1	**4**	ms
Buck5 Shutdown Slew Rate Range	$BK5_{SHTDN\_SR\_RNG}$	BUCK5_FB	**0.5**	1	**4**	ms
Buck5 DVS Slew Rate Range	$BK5_{DVS\_SR\_RNG}$	BUCK5_FB. Applies to both DVS up and down ramps.	**2**	8	**16**	mV/µs
Buck5 High-Side PMOS On-Resistance	$BK5_{RDSON\_HS}$	BUCK5_VINx to BUCK5_LXx, I_{LX} = -150mA		220		mΩ
Buck5 Low-Side NMOS On-Resistance	$BK5_{RDSON\_LS}$	BUCK5_LXx to PGND, I_{LX} = 150mA		105		mΩ
BUCK6 (±1A) VTT Mode. Components as described in Recommended External Components. Additional application details in Buck6.						
Buck6 Output Voltage VTT Mode	$BK6_{OUT\_VTT}$	BUCK6_FB. DDR JEDEC spec. DDR VTT output		VREF OUT		V

AVDD = VCHG = BUCKx_VINx = 5V, BUCK1_FB = 1.1V, BUCK2_FB = 1.2V, BUCK3_FB = 1.8V, BUCK4_FB = 3.3V, BUCK5_FB = 1.2V, BUCK6_FB = 0.6V, LDOx_VIN = 5V, LDO1_OUT = 3.3V, LDO2_OUT = 3.3V, LDO3_OUT = 2.5V, CEN = HIGH, PWRON = HIGH, AGND = PGND, unless otherwise specified. External components as listed in External Component Selection section (or equivalent), unless otherwise stated. Typical entries apply at +25°C. **Boldface limits apply across the ambient operating temperature range -40°C to +105°C, unless otherwise stated. (Cont.)**

Parameter	Symbol	Test Conditions[1]	Min[2]	Typ	Max[2]	Unit
Buck6 Output Voltage DC Accuracy	$BK6_{ACC}$	BUCK6_FB. FPWM mode, I_{OUT} = 5mA, V_{OUT} = 1.8V	**-1**		**1**	%
Buck6 Output Total Accuracy VTT Mode	$BK6_{ACC\_TOT}$	BUCK6_FB. DC + Ripple + Transient. FPWM mode, over line/load/temp. VOUT = 0.6V I_{OUT} -1A → +1A at 2.5A/μs	-30		30	mV
Buck6 Output Voltage Ripple FPWM	$BK6_{RIP\_FPWM}$	I_{OUT} = 100mA, FPWM mode		30		mVpp
Buck6 Maximum Output Current Capability[5]	$BK6_{IOUT\_MAX}$	VTT mode. Source (supply) current for DDR VTT	**1**			A
		VTT mode. Sink (receive) current from DDR VTT	**1**			A
Buck6 Output Load Regulation	$BK6_{LOAD\_REG}$	FPWM, VOUT = 0.6V, Over I_{OUT} = 100mA to 1A range		±0.1		%
Buck6 Output Line Regulation	$BK6_{LINE\_REG}$	BUCK6_VINx = 4.5V ↔ 5.5V, VOUT = 0.6V, I_{OUT} = $BK6_{IOUT\_MAX}$		±0.1		%
Buck6 Peak Efficiency	$BK6_{EFF}$	Peak efficiency, L = default, $BK6_{FSW}$ set to default[6], FPWM mode, VOUT = 0.6V		76		%
Buck6 Discharge Resistance	$BK6_{RDCHG}$	BUCK6_FB. Slow setting	35	50	65	Ω
		BUCK6_FB. Medium setting	26	37.5	49	
		BUCK6_FB. Fast setting	17.5	25	32.5	
Buck6 High-Side MOSFET Current Limit	$BK6_{ILIM\_HS}$	FPWM mode, sourcing (supplying), VTTREF_EN = 1	**2.4**	2.75	**3.2**	A
Buck6 Low-Side MOSFET Current Limit	$BK6_{ILIM\_LS}$	FPWM mode, sourcing (supplying), VTTREF_EN = 1		3.25		A
	$BK6_{ILIMNEG}$	FPWM mode, sinking (receiving), VTTREF_EN = 1		-2.3		
Buck6 PWM Switching Frequency	$BK6_{FSW}$	FPWM mode, 0.667MHz (default) setting		0.667		MHz
Buck6 PWM Switching Frequency Accuracy	$BK6_{FSW\_ACC}$	FPWM mode, I_{OUT} = 0mA, default frequency	**-10**		**+10**	%
Buck6 Soft-start Slew Rate Range	$BK6_{SS\_SR\_RNG}$	BUCK6_FB	**0.5**	1	**4**	ms
Buck6 Shutdown Slew Rate Range	$BK6_{SHTDN\_SR\_RNG}$	BUCK6_FB	**0.5**	1	**4**	ms
Buck6 DVS Slew Rate Range	$BK6_{DVS\_SR\_RNG}$	BUCK6_FB. Applies to both DVS up and down ramps.	**2**	8	**16**	mV/μs
Buck6 High-Side PMOS On-Resistance	$BK6_{RDSON\_HS}$	BUCK6_VINx to BUCK6_LXx, I_{LX} = -150mA		125		mΩ

AVDD = VCHG = BUCKx_VINx = 5V, BUCK1_FB = 1.1V, BUCK2_FB = 1.2V, BUCK3_FB = 1.8V, BUCK4_FB = 3.3V, BUCK5_FB = 1.2V, BUCK6_FB = 0.6V, LDOx_VIN = 5V, LDO1_OUT = 3.3V, LDO2_OUT = 3.3V, LDO3_OUT = 2.5V, CEN = HIGH, PWRON = HIGH, AGND = PGND, unless otherwise specified. External components as listed in External Component Selection section (or equivalent), unless otherwise stated. Typical entries apply at +25°C. **Boldface limits apply across the ambient operating temperature range -40°C to +105°C, unless otherwise stated. (Cont.)**

Parameter	Symbol	Test Conditions[1]	Min[2]	Typ	Max[2]	Unit
Buck6 Low-Side NMOS On-Resistance	$BK6_{RDSON\_LS}$	BUCK6_LXx to PGND, I_{LX} = 150mA		75		mΩ
LDO1 and LDO2 (300mA) Components as described in Recommended External Components. Additional application details in LDO1/2.						
LDO12 Output Voltage Range	$LDO12_{OUT}$	LDO1_OUT, LDO2_OUT 0.8V, 0.9V,1.2V, 1.5V, 1.8V, 2.5V, 3.0V, 3.3V	**0.8**		**3.3**	V
LDO12 Output Voltage DC Accuracy	$LDO12_{ACC\_H}$	I_{OUT} = 1mA and 300mA LDO_{OUT} = 2.5V to 3.3V	**-3**		**3**	%
	$LDO12_{ACC\_M}$	I_{OUT} = 1mA and 300mA LDO_{OUT} = 1.5V to 1.8V	**-4**		**4**	
	$LDO12_{ACC\_L}$	I_{OUT} = 1mA and 300mA LDO_{OUT} = 0.8V to 1.2V	**-5**		**5**	
LDO12 Maximum Output Current Capability	$LDO12_{IOUT}$	LDO1_OUT, LDO2_OUT. External load, sourcing (supplying)	**300**			mA
LDO12 Output Current Limit	$LDO12_{ILIM}$	LDOx_OUT = 10% below regulation target (less positive voltage). LDO1/2 is not expected to operate at this current level continuously.		500		mA
LDO12 Power-Good	$LDO12_{PGOOD}$	Rising threshold is a percentage of the programmed LDO output voltage	**-15**	-10	**-5**	%
		Falling threshold is a percentage of the programmed LDO output voltage	**-21**	-15	**-10**	
		Hysteresis	4	5	6	
LDO12 Load Transient	$LDO12_{LOAD}$	Step: 60mA → 240mA in 1A/µs Step: 240mA → 60mA in 1A/µs	**-3**		**3**	%
LDO12 Load Regulation	$LDO12_{LOAD\_REG}$	VOUT = 2.5V to 3.3V range, I_{OUT} = 1mA to 300mA[5]	**-1**		**1**	%
		VOUT = 1.8V, I_{OUT} = 1mA to 300mA	**-1.25**		**1.25**	
		VOUT = 0.8V, I_{OUT} = 1mA to 300mA[5]	**-2.5**		**2.5**	
LDO12 Line Regulation	$LDO12_{LINE\_REG}$	LDOx_VIN = 2.7V ↔ 5.5V, VOUT = 1.8V, I_{OUT} = 300mA	**-2**		**2**	%
PSRR	$LDO12_{PSRR}$	vs. LDOx_VIN, AVDD. DC to 100kHz, C_{OUT} = default, LDOx_VIN = LDOx_OUT + 0.3V (Not in dropout)			**-40**	dB
		vs. LDOx_VIN, AVDD. 100kHz to 2MHz, C_{OUT} = default, LDOx_VIN = LDOx_VOUT + 0.3V (not in dropout)			**-20**	

AVDD = VCHG = BUCKx_VINx = 5V, BUCK1_FB = 1.1V, BUCK2_FB = 1.2V, BUCK3_FB = 1.8V, BUCK4_FB = 3.3V, BUCK5_FB = 1.2V, BUCK6_FB = 0.6V, LDOx_VIN = 5V, LDO1_OUT = 3.3V, LDO2_OUT = 3.3V, LDO3_OUT = 2.5V, CEN = HIGH, PWRON = HIGH, AGND = PGND, unless otherwise specified. External components as listed in External Component Selection section (or equivalent), unless otherwise stated. Typical entries apply at +25°C. **Boldface limits apply across the ambient operating temperature range -40°C to +105°C, unless otherwise stated. (Cont.)**

Parameter	Symbol	Test Conditions[1]	Min[2]	Typ	Max[2]	Unit
Bypass Mode ON-Resistance	$LDO12_{RDSON}$	I_{OUT} = 100mA		0.33	**0.5**	Ω
LDO12 Dropout Voltage	$LDO12_{DROPOUT}$	I_{OUT} = $LDO12_{IOUT(max)}$			**300**	mV
LDO12 Discharge Resistance	$LDO12_{RDCHG}$	LDOx_OUT. Slow setting	35	50	65	Ω
		LDOx_OUT. Medium setting	26	37.5	49	
		LDOx_OUT. Fast setting	17.5	25	32.5	
LDO3 (50mA) Components as described in Recommended External Components. Additional application details in LDO3.						
LDO3 Output Voltage Range	$LDO3_{OUT}$	LDO3_OUT 0.8V, 0.9V,1.2V, 1.5V, 1.8V, 2.5V, 3.0V, 3.3V	**0.8**		**3.3**	V
LDO3 Output Voltage DC Accuracy	$LDO3_{ACC\_H}$	I_{OUT} = 1mA and 50mA LDO_{OUT} = 2.5V to 3.3V	**-3**		**3**	%
	$LDO3_{ACC\_M}$	I_{OUT} = 1mA and 50mA LDO_{OUT} = 1.5V to 1.8V	**-4**		**4**	
	$LDO3_{ACC\_L}$	I_{OUT} = 1mA and 50mA LDO_{OUT} = 0.8V to 1.2V	**-5**		**5**	
LDO3 Maximum Output Current Capability	$LDO3_{IOUT}$	LDO3_OUT. External load, sourcing (supplying)	**50**			mA
LDO3 Output Current Limit	$LDO3_{ILIM}$	LDO3_OUT = 10% below regulation target (less positive voltage). LDO3 is not expected to operate at this current level continuously.		80		mA
LDO3 Power-Good	$LDO3_{PGOOD}$	Rising threshold is a percentage of the programmed LDO output voltage	**-15**	-10	**-5**	%
		Falling threshold is a percentage of the programmed LDO output voltage	**-21**	-15	**-10**	
		Hysteresis	4	5	6	
LDO3 Load Transient	$LDO3_{LOAD}$	Step: 1mA → 50mA in 1A/µs Step: 50mA → 1mA in 1A/µs	**-3**		**3**	%
LDO3 Load Regulation	$LDO3_{LOAD\_REG}$	V_{OUT} = 2.5V to 3.3V range, I_{OUT} = 1mA to 50mA[5]	**-1**		**1**	%
		V_{OUT} = 1.8V, I_{OUT} = 1mA to 50mA	**-1.5**		**1.5**	
		V_{OUT} = 0.8V, I_{OUT} = 1mA to 50mA[5]	**-3**		**3**	
LDO3 Line Regulation	$LDO3_{LINE\_REG}$	LDO3_VIN = 2.7V ↔ 5.5V, VOUT = 1.8V,I_{OUT} = 50mA		1	**2**	%

AVDD = VCHG = BUCKx_VINx = 5V, BUCK1_FB = 1.1V, BUCK2_FB = 1.2V, BUCK3_FB = 1.8V, BUCK4_FB = 3.3V, BUCK5_FB = 1.2V, BUCK6_FB = 0.6V, LDOx_VIN = 5V, LDO1_OUT = 3.3V, LDO2_OUT = 3.3V, LDO3_OUT = 2.5V, CEN = HIGH, PWRON = HIGH, AGND = PGND, unless otherwise specified. External components as listed in External Component Selection section (or equivalent), unless otherwise stated. Typical entries apply at +25°C. **Boldface limits apply across the ambient operating temperature range -40°C to +105°C, unless otherwise stated. (Cont.)**

Parameter	Symbol	Test Conditions[1]	Min[2]	Typ	Max[2]	Unit
LDO3 PSRR	$LDO3_{PSRR}$	vs. LDO3_VIN, AVDD. DC to 100kHz, C_{OUT} = default, LDOx_IN = LDO3_OUT + 0.3V (not in dropout)			**-40**	dB
		vs. LDO3_VIN, AVDD. 100kHz to 2MHz, C_{OUT} = default, LDOx_IN = LDO3_OUT+ 0.3V (not in dropout)			**-20**	
LDO3 Bypass Mode ON-Resistance	$LDO3_{RDSON}$	I_{OUT} = 10mA		1.3	**1.8**	Ω
LDO3 Dropout Voltage	$LDO3_{DROPOUT}$	I_{OUT} = $LDO3_{IOUT(max)}$			**300**	mV
LDO3 Discharge Resistance	$LDO3_{RDCHG}$	LDO3_OUT. Slow setting	35	50	65	Ω
		LDO3_OUT. Medium setting	26	37.5	49	
		LDO3_OUT. Fast setting	17.5	25	32.5	
VTTREF Components as described in Recommended External Components. Additional application details in VTTREF.						
VREFIN Input Operating Range	$VREFIN_{OP}$		**1.1**		**1.8**	V
VREFIN Undervoltage Lockout Threshold	$VREFIN_{UVLO\_F}$	Falling VREFIN	**0.72**	0.78	**0.84**	V
VREFIN Undervoltage Lockout Hysteresis	$VREFIN_{UVLO\_HYS}$	$VREFIN_{UVLO\_R}$ = $VREFIN_{UVLO\_F}$ + $VREFIN_{UVLO\_HYS}$		20		mV
VREFIN UVLO Falling Delay	$t_{VREFIN\_UVLO\_F\_DLY}$	Falling VREFIN		1		ms
VREFOUT Output Range	$VREFOUT_{RNG}$	VREFOUT = buffered version of VREFIN/2	**0.55**		**0.9**	V
VREFOUT Output Current	$VREFOUT_{IOUT}$	sourcing (supplying)	**10**			mA
		sinking (receiving)	**10**			
VREFOUT Output Current Limit	$VREFOUT_{ILIM}$	sourcing (supplying)	**22**	40	**58**	mA
		sinking (receiving)		40		
VREFOUT Accuracy	$VREFOUT_{ACC\_AC}$	VTTREF_EN = 1 DDR JEDEC spec	**0.49* VREFIN**	0.5* VREFIN	**0.51* VREFIN**	V
	$VREFOUT_{ACC\_DC}$	VTTREF_EN = 1 DDR JEDEC spec	**-0.01* VREFIN**		**0.01* VREFIN**	V
VREFOUT Discharge Resistance	$VREFOUT_{RDCHG}$	VREFOUT. Fast setting		50	65	Ω
		VREFOUT. Medium setting		75	97	
		VREFOUT. Slow setting		100	130	

AVDD = VCHG = BUCKx_VINx = 5V, BUCK1_FB = 1.1V, BUCK2_FB = 1.2V, BUCK3_FB = 1.8V, BUCK4_FB = 3.3V, BUCK5_FB = 1.2V, BUCK6_FB = 0.6V, LDOx_VIN = 5V, LDO1_OUT = 3.3V, LDO2_OUT = 3.3V, LDO3_OUT = 2.5V, CEN = HIGH, PWRON = HIGH, AGND = PGND, unless otherwise specified. External components as listed in External Component Selection section (or equivalent), unless otherwise stated. Typical entries apply at +25°C. **Boldface limits apply across the ambient operating temperature range -40°C to +105°C, unless otherwise stated. (Cont.)**

Parameter	Symbol	Test Conditions[1]	Min[2]	Typ	Max[2]	Unit
Charger Components as described in Recommended External Components. Additional application details in Coin Cell Battery Charger.						
VCHG Operating Voltage Range	$VCHG_{OP}$		**2.7**	5	**5.5**	V
VBAT Charging Voltage Termination Range	$VBAT_{RNG}$	sets VBAT voltage to automatically disable charger operation	**1.8**	3.3	**3.3**	V
VBAT Charging Voltage Termination Step	$VBAT_{STEP}$	VBAT		100		mV
VCHG Headroom	$VCHG_{HD}$	Input voltage headroom. VCHG needs to be above VBAT + $VCHG_{HD}$ to make the charger operate at the programmed charge current	**300**			mV
VRTC Voltage Hysteresis	$VRTC_{HYS}$	Threshold for VRTC supply switching to being derived from VCHG (rather than VBAT), VCHG rising above VBAT + $VBAT_{HYS}$		50		mV
Charge Current Setting Range	$VBAT_{IOUT}$	VBAT. 60µA (default) setting	**20**	60	**60**	µA
Charge Current Accuracy	$VBAT_{IOUT\_ACC}$	VBAT	**-20**		**20**	%
RTC Components as described in Recommended External Components. Additional application details in Real-Time Clock.						
VBAT Operating Voltage Range	$VBAT_{OP}$	Battery backup mode	**1.8**	3.3	**5.5**	V
VRTC Operating Voltage Range	$VRTC_{OP}$	Generated internally from higher of VCHG or VBAT	**1.8**	5	**5.5**	V
Oscillator Frequency	RTC_{FREQ}			32.768		kHz
Oscillator Duty Cycle	RTC_{DUTY}			50		%
I²C						
7-bit Slave Address Range	$I2C_{ADDR\_MAIN}$	Access to non-RTC related registers. 7-bit uniquely programmable in EEPROM	**1**	12	**7F**	Hex
	$I2C_{ADDR\_RTC}$	Access to RTC related registers. 7-bit uniquely programmable in EEPROM	**1**	6F	**7F**	
SCL Clock Frequency	f_{SCL}	Supports standard 100kHz, 400kHz, 1MHz	**-**	-	**1**	MHz

AVDD = VCHG = BUCKx_VINx = 5V, BUCK1_FB = 1.1V, BUCK2_FB = 1.2V, BUCK3_FB = 1.8V, BUCK4_FB = 3.3V, BUCK5_FB = 1.2V, BUCK6_FB = 0.6V, LDOx_VIN = 5V, LDO1_OUT = 3.3V, LDO2_OUT = 3.3V, LDO3_OUT = 2.5V, CEN = HIGH, PWRON = HIGH, AGND = PGND, unless otherwise specified. External components as listed in External Component Selection section (or equivalent), unless otherwise stated. Typical entries apply at +25°C. **Boldface limits apply across the ambient operating temperature range -40°C to +105°C, unless otherwise stated. (Cont.)**

Parameter	Symbol	Test Conditions[1]	Min[2]	Typ	Max[2]	Unit
Logic I/O						
Operating Input Voltage Range	V_{OP_EN}	CEN, PWRON	**0**		**5.5**	V
	V_{OP_MPIO}	MPIOx	**0**		**5.5**	V
	V_{OP_I2C}	SCL, SDA	**0**		**5.5**	V
	V_{OP_LDOSEL}	LDO_SEL1, LDO_SEL2	**0**		**5.5**	V
HIGH 1 Input Voltage Threshold	V_{IH_EN}	CEN, PWRON	**1.2**			V
	V_{IH_MPIO}	MPIOx	**1.2**			V
	V_{IH_I2C}	SCL, SDA	**1.2**			V
	V_{IH_LDOSEL}	LDO_SEL1, LDO_SEL2, in {ACTIVE}	**1.2**			V
LOW 0 Input Voltage Threshold	V_{IL_EN}	CEN, PWRON			**0.4**	V
	V_{IL_MPIO}	MPIOx			**0.4**	V
	V_{IL_I2C}	SCL, SDA			**0.4**	V
	V_{IL_LDOSEL}	LDO_SEL1, LDO_SEL2, in {ACTIVE}			**0.4**	V
Input Hysteresis	V_{EN_HYS}	CEN, PWRON		150		mV
	V_{MPIO_HYS}	MPIOx		150		mV
	V_{I2C_HYS}	SCL, SDA		150		mV
	V_{LDOSEL_HYS}	LDO_SEL1, LDO_SEL2, in {ACTIVE}		150		mV
Input Leakage Current	I_{L_EN}	CEN, PWRON. CEN = 5.5V, PWRON = 5.5V[7]	**-3.5**		**3.5**	µA
	I_{L_MPIO}	MPIOx. MPIOx = 5.5V[7]	**-3.5**		**3.5**	
	I_{L_I2C}	SDA, SCL SDA = SCL = 5.5V	**-1**		**1**	
	I_{L_LDOSEL}	LDO_SELx, LDO_SELx = 5.5V[7]	**-3.5**		**3.5**	
Low Level Output Voltage	V_{OL_MPIO}	MPIOx as output, open-drain. Pull up to 1.8V, sinking 2mA			**0.4**	V
	V_{OL_SDA}	SDA. Pull up to 1.8V, sinking 2mA			**0.4**	
	V_{OL_INT}	INT#. Pull up to 1.8V, sinking 2mA			**0.4**	
High Level Output Voltage	V_{OH_MPIO}	MPIOx as full CMOS output, sourcing 2mA	**1.2**			V

AVDD = VCHG = BUCKx_VINx = 5V, BUCK1_FB = 1.1V, BUCK2_FB = 1.2V, BUCK3_FB = 1.8V, BUCK4_FB = 3.3V, BUCK5_FB = 1.2V, BUCK6_FB = 0.6V, LDOx_VIN = 5V, LDO1_OUT = 3.3V, LDO2_OUT = 3.3V, LDO3_OUT = 2.5V, CEN = HIGH, PWRON = HIGH, AGND = PGND, unless otherwise specified. External components as listed in External Component Selection section (or equivalent), unless otherwise stated. Typical entries apply at +25°C. **Boldface limits apply across the ambient operating temperature range -40°C to +105°C, unless otherwise stated. (Cont.)**

Parameter	Symbol	Test Conditions[1]	Min[2]	Typ	Max[2]	Unit
Protections						
Output Overvoltage Protection Threshold	BK_{OVP_R}	BUCKx_FB rising. Percentage of output voltage target setting (Bucks 1, 2, 3)	**6**	8.5	**11**	%
		BUCKx_FB rising. Percentage of output voltage target setting (Bucks 5 and 6)	**6**	8.5	**12.5**	
	BK_{OVP_F}	BUCKx_FB falling. Percentage of output voltage target setting (Bucks 1, 2, 3)	**4**	6.5	**9**	
		BUCKx_FB falling. Percentage of output voltage target setting (Bucks 5 and 6)	**3**	6.5	**9**	
	BK_{OVP_HYS}	$BK_{OVP\_HYS} = BK_{OVP\_R} - BK_{OVP\_F}$. Percentage of output target setting. (Bucks 1, 2, 3, 5, and 6)		2		
	$BK4_{OVP\_R}$	BUCK4_FB rising. Percentage of output voltage target setting	**5**	10	**15**	
	$BK4_{OVP\_F}$	BUCK4_FB falling below BK_{OVP}. Percentage of output target setting	**4**	8.5	**13**	
	$BK4_{OVP\_HYS}$	$BK4_{OVP\_HYS} = BK4_{OVP\_R} - BK4_{OVP\_F}$. Percentage of output target setting.		1.5		
Output Undervoltage Protection Threshold	BK_{UVP_R}	BUCKx_FB rising. Percentage of output voltage target setting. (Bucks 1, 2, 3, 5, and 6)	**-8**	-5.5	**-2**	%
	BK_{UVP_F}	BUCKx_FB falling. Percentage of output target setting. (Bucks 1, 2, 3)	**-13**	-11	**-8**	
		BUCKx_FB falling. Percentage of output target setting. (Bucks 5 and 6)	**-13**	-11	**-6**	
	BK_{UVP_HYS}	$BK_{UVP\_HYS} = BK_{UVP\_R} - BK_{UVP\_F}$. Percentage of output target setting. (Bucks 1, 2, 3, 5, and 6)		5.5		
	$BK4_{UVP\_R}$	BUCK4_FB rising. Percentage of output voltage target setting.	**-12**	-7	**-2.5**	
	$BK4_{UVP\_F}$	BUCK4_FB falling. Percentage of output target setting.	**-18**	-13	**-8**	
	$BK4_{UVP\_HYS}$	$BK4_{UVP\_HYS} = BK4_{UVP\_R} - BK4_{UVP\_F}$. Percentage of output target setting.		6		

AVDD = VCHG = BUCKx_VINx = 5V, BUCK1_FB = 1.1V, BUCK2_FB = 1.2V, BUCK3_FB = 1.8V, BUCK4_FB = 3.3V, BUCK5_FB = 1.2V, BUCK6_FB = 0.6V, LDOx_VIN = 5V, LDO1_OUT = 3.3V, LDO2_OUT = 3.3V, LDO3_OUT = 2.5V, CEN = HIGH, PWRON = HIGH, AGND = PGND, unless otherwise specified. External components as listed in External Component Selection section (or equivalent), unless otherwise stated. Typical entries apply at +25°C. **Boldface limits apply across the ambient operating temperature range -40°C to +105°C, unless otherwise stated. (Cont.)**

Parameter	Symbol	Test Conditions[1]	Min[2]	Typ	Max[2]	Unit
Output Fault Deglitch Time	$t_{FLT\_DEGLITCH}$	Deglitch time from fault event to INT# assertion for unmasked faults, including: BUCK OV and UV, LDO PGOOD, Thermal Warning and Shutdown.	**0.8**	1	**1.2**	ms
High Current Warning Deglitch Time	$t_{HC\_DEGLITCH}$	Buck1 high current warning		100		µs
Thermal Shutdown Threshold	T_{SHDN}	Junction temperature rising. Thermal shutdown asserted.	**125**	135	**145**	°C
	T_{SHDN_HYS}	Junction temperature falling below T_{SHDN}. Thermal shutdown de-asserted.		30		°C
Thermal Warning Threshold	T_{WARN}	Junction temperature rising. Thermal warning asserted. 120°C setting	**110**	120	**130**	°C
	T_{WARN_HYS}	Junction temperature falling below T_{WARN} Thermal warning de-asserted.		25		°C
Timing						
PWRON Deglitch Time	$t_{PWRON\_DEGLITCH}$			100		µs
MPIOx Deglitch Time	$t_{MPIO\_DEGLITCH}$			1.5		µs

1. All the C_{OUT} listed in Test Condition are nominal values (not derated), unless stated as derated or effective. For details on the recommended components, see External Component Selection.
2. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
3. Follow this supply timing to ensure correct timekeeping of the RTC.
4. When a MPIOx is configured as full CMOS output, the sourcing current comes from VIO.
5. Compliance to datasheet limits is established by one or more methods: production test, characterization, and/or design.
6. At light loads, switching frequency is lower than the setting.
7. There is an internal 2MΩ pull-down resistor at each of the following pins: CEN, PWRON, MPIOx, and LDO_SELx.

4. Typical Performance Graphs

AVDD = VCHG = BUCKx_VINx = 5V, BUCK1_FB = 1.1V, BUCK2_FB = 1.2V, BUCK3_FB = 1.8V, BUCK4_FB = 3.3V, BUCK5_FB = 1.2V, BUCK6_FB = 0.6V, CEN = HIGH, PWRON = HIGH, T_A = +25°C, unless otherwise stated. Refer to the RTKA215300DE0000BU BOM for the components used in the following measurements.

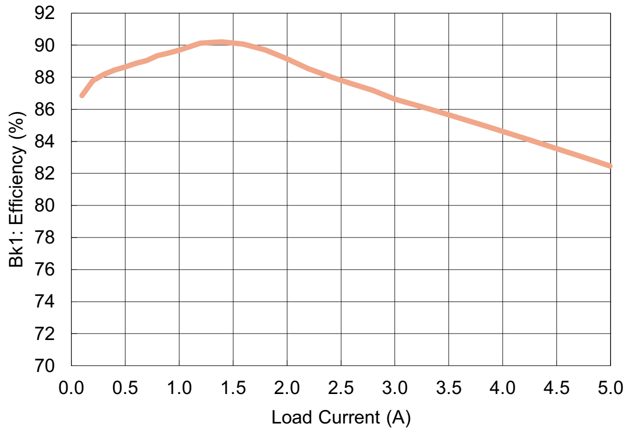


Figure 3. Buck1 Efficiency in Auto PFM/PWM mode

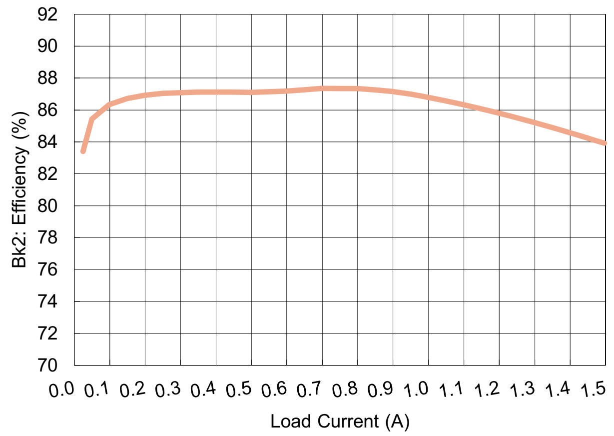


Figure 4. Buck2 Efficiency in Auto PFM/PWM mode

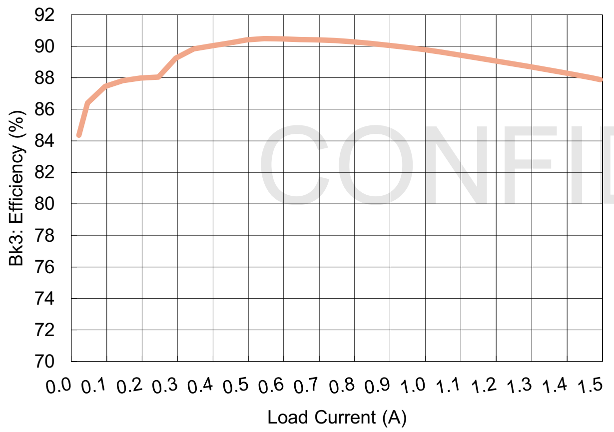


Figure 5. Buck3 Efficiency in Auto PFM/PWM mode

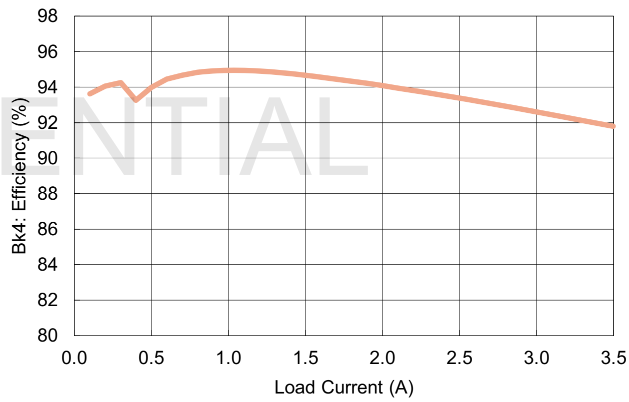


Figure 6. Buck4 Efficiency in Auto PFM/PWM mode

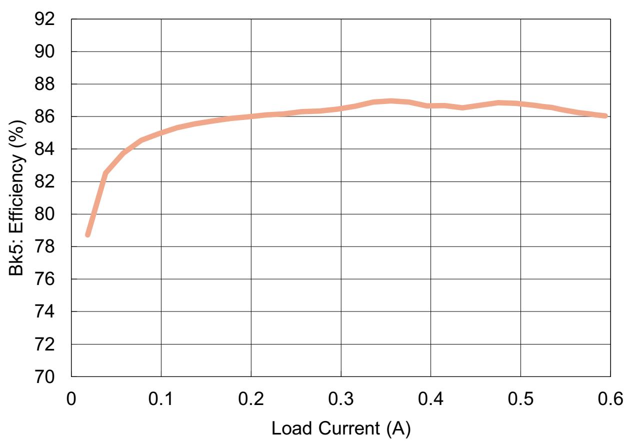


Figure 7. Buck5 Efficiency in Auto PFM/PWM mode

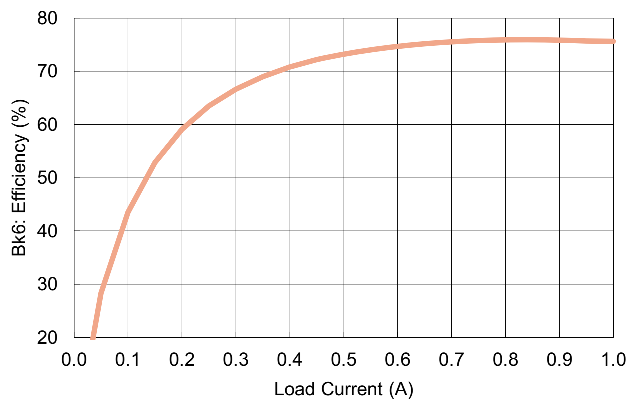


Figure 8. Buck6 Efficiency in VTT configuration (FPWM mode)

5. Serial Interface

The RAA215300 includes a standard I²C serial interface. The 2-wire interface links one or more Masters and uniquely addressable Slave devices. The Master generates clock signals and is responsible for initiating data transfers. The serial clock is on the SCL line and the serial data (bidirectional) is on the SDA line. The RAA215300 supports clock rates up to 1MHz (Fast mode plus) and is downward compatible with standard 100kHz (Standard mode), and 400kHz (Fast mode) clock rates.

The SDA and SCL lines must be HIGH when the bus is free (not in use). An external pull-up resistor (typically 1kΩ to 4.7kΩ depending on clock speed, pull-up voltage, and bus capacitance) or current source is required for SDA and SCL.

The I²C interface is not functional until VIO_PGOOD is high. See VCHG, VBAT, and VRTC for more details.

5.1 I²C General Operation

5.1.1 Data Validity

The data on the SDA line must be stable (clearly defined as HIGH or LOW) during the HIGH period of the clock signal. The state of the SDA line can only change when the SCL line is low (except to create a START or STOP condition). The voltage levels used to indicate a logical 0 (LOW) and logical 1(HIGH) are determined by the V_{IL} and V_{IH} thresholds, respectively, see Electrical Specifications.

5.1.2 START and STOP Condition

All I²C communication begins with a START condition (indicating the beginning of a transaction) and ends with a STOP condition (signaling the end of the transaction).

A START condition is signified by a HIGH-to-LOW transition on the serial data line (SDA) while the serial clock line (SCL) is HIGH. A STOP condition is signified by a LOW-to-HIGH transition on the SDA line while SCL is HIGH. See timing specifications in Electrical Specifications.

The Master always initiates START and STOP conditions. After a START condition, the bus is considered busy. After a STOP condition, the bus is considered free. The device supports repeated STARTs, where the bus remains busy for the continued transaction(s).

5.1.3 Byte Format

Every byte on SDA must be 8 bits in length. After every byte of data sent by the transmitter, there must be an Acknowledge bit (from the receiver) to signify that the previous 8 bits were transferred successfully. Data is always transferred on SDA with the most significant bit (MSB) first. If the data is larger than 8 bits, it can be separated into multiple 8-bit bytes.

5.1.4 Acknowledge (ACK)

Each 8-bit data transfer is followed by an Acknowledge (ACK) bit from the receiver. The ACK bit signifies that the previous 8 bits of data were transferred successfully (master-slave or slave-master).

When the Master sends data to the Slave (for example, during a WRITE transaction), after the 8th bit of a data byte is transmitted, the Master tri-states the SDA line during the 9th clock. The Slave device acknowledges that it received all 8 bits by pulling down the SDA line, generating an ACK bit.

When the Master receives data from the Slave (for example, during a data READ transaction), after the 8th bit is transmitted, the Slave tri-states the SDA line during the 9th clock. The Master acknowledges that it received all 8 bits by pulling down the SDA line, generating an ACK bit.

5.1.5 Not Acknowledge (NACK)

A Not Acknowledge (NACK) bit is generated when the receiver does not pull down the SDA line during the acknowledge clock (that is, the SDA line remains HIGH during the 9th clock), indicating to the Master that it can generate a STOP condition to end the transaction and free the bus.

A NACK bit can be generated for various reasons, for example:

- After an I²C device address is transmitted, there is NO receiver with that address on the bus to respond.
- The receiver is busy performing an internal operation (for example, reset or recall) and cannot respond.
- The Master (acting as a receiver) needs to indicate the end of a transfer with the Slave (acting as a transmitter).

5.1.6 Device Address and $R/\overline{W}$ Bit

After a valid START condition, the first byte sent in a transaction contains the 7-bit Device (Slave) Address plus a direction ($R/\overline{W}$) bit (Device Address Byte). The Device Address identifies which device (of up to 127 addresses on the I²C bus) the Master wishes to communicate with.

After a START condition, the device monitors the first 8 bits received (Device Address byte), and checks for its 7-bit Device Address in the MSBs. If it recognizes the correct Device Address, it ACKs and becomes ready for further communication. If it does not see its Device Address, it sits idle until another START condition is issued on the bus.

Note: The 8th bit (LSB) of the Device Address byte indicates the direction of transfer, READ or WRITE ($R/\overline{W}$). A 0 indicates a WRITE operation - the Master transmits data to the RAA215300 (receiver). A 1 indicates a Read operation - the Master receives data from the RAA215300 (transmitter).

5.2 Device Communication Protocol

5.2.1 7-bit Device Addresses

The RAA215300 employs two 7-bit I²C device/slave addresses. One address accesses settings related to the RTC function (RTC Slave Address) - default address **0x6F** (1101111x). Another address accesses the remainder of the device settings (Main Slave Address) - default address **0x12** (0010010x). The LSB is a direction bit, which can be 0 for a WRITE or 1 for a READ, which is not part of the unique 7-bit I²C device address.

Both addresses are programmable in EEPROM with possible values in the range 0x01~0x7F. The two slave addresses can be the same value for single slave address access to the register space.

5.2.2 Register Size

All the device registers contain 8-bit (byte) data. The data is latched-in after the 8th bit (LSB) is received. If a partial data byte is received, that byte is ignored, but any previously acknowledged bytes are accepted.

5.2.3 I²C Write Operation

A Write operation consists of the master sending a START condition, followed by a valid device address byte (R/W bit set to 0), a Register Address Byte, Data Byte, and a STOP condition. After each byte, the device responds with an ACK. The I²C protocol supports burst writing (automatic incrementing of address pointer). After every successfully transmitted data byte, the device automatically increments the internal register address, so subsequent data bytes are written to sequentially incremental register locations. The master must send a STOP condition after sending at least one full data byte and receiving the associated ACK. If a STOP is issued in the middle of a data byte, the Write for that byte is not performed. The basic write transaction structure is shown in Figure 9.

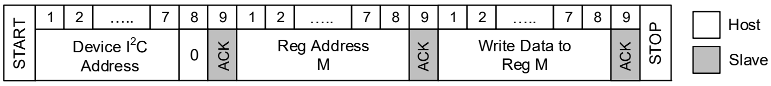


Figure 9. 1-Byte Write to Register M

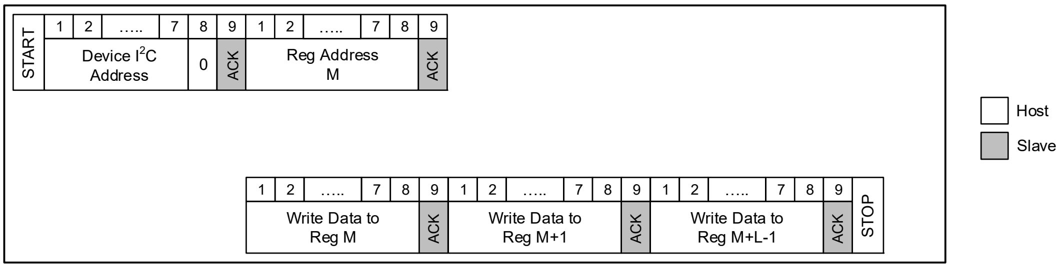


Figure 10. L-Byte Sequential Data Write Starting at Register M

5.2.4 I^{2}C Read Operation

The master sends a START condition, followed by a valid device address byte (R/W bit set to 0), a register address byte, a second (repeated) START, and a valid device address byte (R/W bit set to 1). After each of the three bytes, the device responds with an ACK. The device then transmits data bytes back to the master, and the master ACKs after each byte. The master terminates the Read operation by issuing a NACK and sending a STOP condition.

After every successfully transmitted data byte, the device automatically increments the internal register address, so data bytes are sent out from sequential register locations.

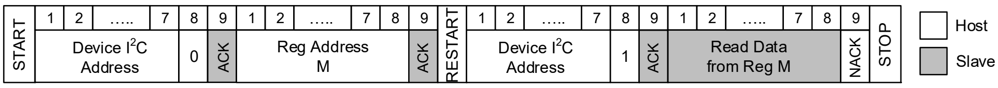


Figure 11. 1-Byte Read to Register M

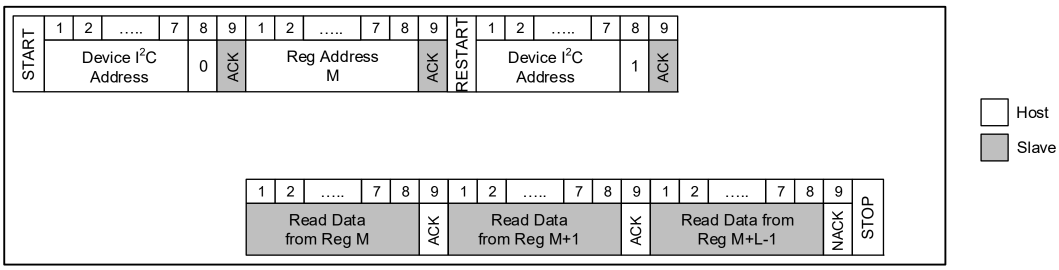


Figure 12. L-Byte Sequential Data Read Starting at Register M

5.2.5 I2C Timing

The timing specifications of the I2C I/O from the I2C specification are shown in Figure 13 and Table 1. The I2C controller provides a slave I2C transceiver capable of interpreting I2C protocol in Standard, Fast, and Fast-mode plus modes.

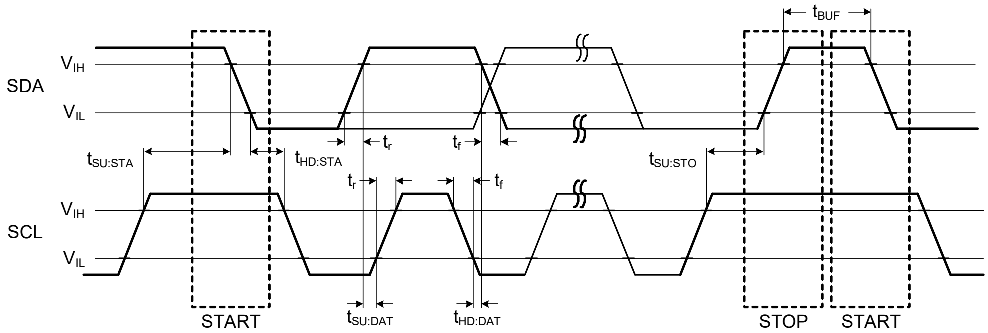


Figure 13. I2C Timing Definitions

Table 1. I2C Timing Characteristics

Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Min	Max	Min	Max	Min	Max	
SCL Clock Frequency	f_{SCL}	0	100	0	400	0	1000	kHz
Hold Time (repeated) START Condition	$t_{HD:STA}$	4.0	-	0.6	-	0.26	-	µs
LOW Period of the SCL Clock	t_{LOW}	4.7	-	1.3	-	0.5	-	µs
HIGH Period of the SCL Clock	t_{HIGH}	4.0	-	0.6	-	0.26	-	µs
Set-Up Time for a Repeated START Condition	$t_{SU:STA}$	4.7	-	0.6	-	0.26	-	µs
Data Hold Time[1]	$t_{HD:DAT}$	0	-	0	-	0	-	µs
Data Set-Up Time	$t_{SU:DAT}$	250	-	100	-	50	-	ns
Rise Time of SDA and SCL	t_r	-	1000	0	300	-	120	ns
Fall Time of SDA and SCL[2][3]	t_f	-	300	20 x (V_{DD}/5.5V)	300	20 x (V_{DD}/5.5V)	120	ns
Set-Up Time for a STOP Condition	$t_{SU:STO}$	4.0	-	0.6	-	0.26	-	µs
Bus Free Time Between a STOP and START Condition	t_{BUF}	4.7	-	1.3	-	0.5	-	µs
Capacitive Load for Each Bus Line	C_b	-	400	-	400	-	550	pF
Pulse Width of Spikes that must be Suppressed by the Input Filter	t_{SP}	-	-	0	50	0	50	ns
Input Capacitance for each SDA and SCL	C_i	-	10	-	10	-	10	pF

1. $t_{HD:DAT}$ is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
2. V_{DD} = External pull-up voltage.
3. In Fast mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

5.3 Unimplemented Registers

All register addresses that are defined in the register map ACK write commands and return data to read commands that address them. Unimplemented registers address ACK write commands but data is ignored, and returns a fixed value of 0x00 to read commands.

6. Registers and EEPROM

The RAA215300 features both volatile (RAM/registers) and non-volatile (EEPROM) memory. The volatile value of each register can be set by writing data to the appropriate register using the selected interface, or it can be recalled and loaded from the integrated EEPROM.

When the device enters into {READ_EE}, digital logic loads the pre-programmed EEPROM data into the volatile register space. When all data is loaded successfully, the device does not reload EEPROM data again unless there has been a power cycle, CEN toggle, or software reset command. See Operating {States} and Transition Conditions.

Volatile register data can be written or read back on the fly, as fast as the I^2C interface can support.

6.1 EEPROM

The RAA215300 integrates high endurance EEPROM to store all IC configurations. The EEPROM is capable of 1000 plus endurance cycles and 10yrs at 85C of data retention.

6.1.1 Writing to the EEPROM

EEPROM programming is initiated through a control byte register. When setting the write bit to 1 in the control byte (0xFF), all the related non-volatile register data are copied to EEPROM on the subsequent I^2C STOP condition. During the EEPROM programming cycle time, the device is internally busy and NACKs to any interface commands, however the buck, LDO outputs, and other IC operations are not halted during the programming time.

When the programming cycle completes, the stored EEPROM data is automatically read back into the register. This provides a way for the host to validate successful programming by reading back the register(s) and comparing it with the value(s) intended to be programmed. If values match, programming was successful. However, if the register data reverts to the previous stored EEPROM value, the EEPROM values were not successfully updated.

6.1.1.1 EEPROM Banks

The RAA215300 EEPROM is partitioned into eight separate banks. All customer banks are (re)programmed each time an EEPROM programming operation commences. For details about each register and bits, see the Register Map.

6.1.1.2 EEPROM Programming Voltage

When programming the EEPROM, the minimum voltage requirement must be met:

- VPROG ≥ 21V

If the condition is not met, the EEPROM programming operations are not successful. If there was insufficient EEPROM programming or reading voltage, the NVM_Error_Latched and EE_Error_Latched bits are set to 1. The fault flags do not affect the power-on sequencer.

6.1.1.3 Step-by-step EEPROM Programming Instructions

1. The device should be in {STANDBY} or onward.
2. Write/set up all the required register values (volatile).
3. Apply sufficient EEPROM programming cycle voltage to VPROG, see EEPROM Programming Voltage.

   Note: This step can occur before Step 2.

4. Set the write bit in the control byte - write register address 0xFF[1] = 1. On the subsequent I²C stop condition, the EEPROM programming cycle commences.
5. The system must wait for the maximum t_{EE_WRITE} time to elapse before attempting further interface activity with RAA215300, or making any changes to the supplies as the device is internally busy with programming operations.

6.1.2 Recalling the EEPROM

There are two ways to load EEPROM data to the device volatile registers:

- **Automatic Recall:** Occurs Operating {States} and Transition Conditions.
- **Manual/Software Recall**: Issue an I²C reset command to the control byte (register 0xFF).

When the EEPROM is being loaded to the registers, the device is internally busy and NACKs to any I²C commands. When all data is loaded successfully, the RAA215300 does not reload the data unless there has been a new power cycle, toggle of CEN, or software recall command.

6.1.2.1 Valid EEPROM Data Check

During the initial automatic recall, the device provides a safety mechanism to effectively stall the power-on process (sequencer) before any blocks become enabled, and output sequencing starts if it is determined that the EEPROM data has not been programmed or checked by the host. This is accomplished by putting the device into {FAULT_OUT}, which allows the system host to first read back by I²C and initially program the EEPROM data loaded to the registers or confirm loaded data are valid for the application. This helps prevent any undesirable application system behavior. The host can verify this event occurred by reading the fault registers and observing if the NVM_Error_Latched fault and Valid_EE_Data latched fault bits are set to 1. This feature is not enabled if registers 0xD9 - 0xDD are all at zero value.

If the register and/or EEPROM data needs to be changed after the host checks any required register data, the host can make the necessary programming changes. When correct register data is set, the host should clear the NVM_Error_Latched fault by writing 1 to it, which clears both NVM_Error_Latched and Valid_EE_Data bits and releases the device to continue the power-on as determined by PWRON and configuration register settings. This gives the host authority to validate the register settings and specifically control when the device is allowed to start the system.

When the required RAA215300 settings are fixed and programmed to EEPROM (that is, the host no longer needs to validate the data at each power-on), programming register EEPROM_ID_1 or EEPROM_ID_2 to any non-zero value in EEPROM authorizes that the EEPROM data is valid. Therefore, the device no longer enters {FAULT_OUT} and awaits host intervention at subsequent power-on events. *Note:* Reprogramming register EEPROM_ID_1 and EEPROM_ID_2 back to 0x00 value causes the device to enter {FAULT_OUT} at future power-on events.

6.2 EEPROM Error Correction

Data stored in EEPROM is protected by error correction codes (ECC), which allows a single bit error in a given memory bank to be corrected. Each EEPROM bank is covered by its own error correction code.

When a bank of EEPROM is programmed, the error correction code for that bank is automatically generated internally and stored in the same bank. When the EEPROM is recalled, the error correction code is checked, and a correctable (single bit) error is automatically corrected.

Should a single bit correction occur, the EE_Bank#_ECC_Corrected status flag and NVM_Error_Latched bit are set. INT# is asserted. The device still transitions states normally to start up. The host can clear the NVM_Error_Latched fault by writing 1 to it, which clears both NVM_Error_Latched and EE_Bank#_ECC_Corrected bits and de-asserts the INT# output. Two-bit errors in any bank are detected and reported as uncorrectable errors by setting the INT# interrupt event, NVM_Error_Latched bit, and EE_Bank#_ECC_Error status flags. The device ignores the other control inputs (such as PWRON) and enters

{FAULT_OUT}. The host should clear the NVM_Error_Latched fault by writing 1 to it, which clears both NVM_Error_Latched and EE_Bank#_ECC_Error bits and releases the device to continue the power-on sequence.

6.2.1 ECC Bank Detail Bits

Each RAA215300 memory bank has dedicated ECC bank detail fault bits to uniquely report if a given bank had either an uncorrected, or corrected ECC error occur. These bits do not affect IC operation, they are simply used to provide additional information in the event of ECC operation.

When an ECC error is uncorrected for a given bank # (that is, EEPROM EE_Read_Error interrupt event occurs), a corresponding detail status bit (EE_Bank#_ECC_Error) is set to 1. The EE_Bank#_ECC_Error status bits can be cleared by writing 1 to the NVM_Error_Latched bit.

When an ECC error is corrected for a given bank #, a corresponding detail status bit (EE_Bank#_ECC_Corrected) is set to 1. The bit(s) can be cleared by the host by writing 1 to the NVM_Error_Latched bit.

7. Power Supplies

The RAA215300 requires one input power supply to power everything. To describe various usage of the power supply, it is helpful to give it various names, but all named parts must be connected together by the PCB. AVDD and VCHG are defined in Pin Descriptions. The input power supply provides power to all voltage regulators, and these connections have various names defined in Pin Descriptions. Connection to the IC is made at many physical locations, identified by name, and each location must have dedicated decoupling capacitance.

7.1 Internal LDO (VIO)

An LDO rejects noise from the VCHG supply and provides a quiet and stable internal supply, VIO, for interface logic.

The LDO is output-compensated and requires a minimum of 1.2µF effective output capacitance, placed close to the VIO pin. See External Component Selection and Device Specific Layout Guidelines.

VIO is enabled as soon as AVDD exceeds its UVLO rising threshold. VIO power-good (VIO_PGOOD) is monitored only after EEPROM is read. The timeout period starts as soon as the FSM enters {WAIT_FOR_VIO}. The timeout period is set by a 2-bit register. See {WAIT_FOR_VIO}.

A register bit is assigned to mask or unmask the VIO_PGOOD signal from INT#. Another register bit shows the status of the VIO power-good fault. When asserted, this fault flag is latched and does not clear automatically. It can only be cleared by writing 1 to the register, hardware reset, or input power cycle.

The VIO LDO is capable of supporting an additional external load of up to 20mA continuously.

7.2 VCHG, VBAT, and VRTC

VRTC is an output that provides power to the RTC. VRTC is generated internally from the higher of VBAT and VCHG. If RTC is used, Renesas recommends placing a capacitor footprint between VRTC and AGND. The capacitor is not populated by default. If RTC is not used, leave VRTC open.

VCHG is the power supply for the coin cell charger and the internal LDO VIO. VCHG must be connected to AVDD, allowing I^2C to be operational when the RTC is in battery mode while AVDD remains above its UVLO falling threshold (for example, AVDD = 2.7V, VBAT = 3V). Given that the input thresholds of the I^2C signals depend on the VIO supply, which is derived from VCHG, the I/Os are effectively disabled when VIO_PGOOD is LOW (invalid). This could occur when CEN is LOW (the main IC is shut down) if AVDD is below its UVLO level, or when the VIO LDO is powering up.

VBAT can be connected to a coin cell battery or a supercapacitor. VBAT is selected to supply VRTC when VCHG falls below the VBAT voltage - entering battery mode operation. When VCHG rises above (VBAT + $VBAT_{HYS}$), the system selects VCHG to supply VRTC.

8. Operating {States} and Transition Conditions

The RAA215300 has a finite-state machine (FSM) to execute transitions between various operational states. The following describes those states and the conditions for transitions.

8.1 {RESET}

If AVDD is below its UVLO falling threshold in any state or CEN = LOW in {STANDBY} or {FAULT_OUT}, the device enters {RESET}. In {RESET}, the digital circuit is held in reset, and if CEN = LOW, the device is powered down. When AVDD is above its UVLO rising threshold and CEN = low, the device is in the SHUTDOWN condition.

8.2 {READ_EE}

When AVDD is above its UVLO rising threshold and CEN = HIGH, EEPROM values are read into the registers. When EEPROM reading/loading is successfully completed, the device sets the NVM_Read_Complete latched flag and then transitions to {WAIT_FOR_VIO}.

Note: There is an error correction system (1-bit error correction and 2-bit error detection) that checks the EEPROM loads correct data. If EE_Bankx_ECC_Error or Valid_EE_Data errors are detected, the state machine sets the NVM_Error_Latched flag bit. If this occurs, the part ignores control inputs (for example, PWRON) and enters {FAULT_OUT}. See Valid EEPROM Data Check and EEPROM Error Correction.

8.3 {WAIT_FOR_VIO}

{WAIT_FOR_VIO} follows successful {READ_EE}. Providing that AVDD is valid and that CEN is high, on entry to {WAIT_FOR_VIO}, a programmable timer (VIO Timeout) starts, and monitoring of VIO_PGOOD begins. If VIO_PGOOD is asserted before the timer expires, the FSM transitions to {STANDBY} before the end of the timeout period. If VIO_PGOOD is not asserted when the timer expires, the FSM transitions to {FAULT_OUT}.

8.4 {STANDBY}

In {STANDBY}, MPIOx (if configured as inputs) and PWRON are responded to. The I^2C interface becomes operational as well. When PWRON is asserted, the FSM enters {STANDBY_EXIT}.

8.4.1 {STANDBY_EXIT}

The FSM stays in this state until a timer expires (typically around 80µs). When the timer expires, the FSM enters {STANDBY_TO_ACTIVE}.

8.4.2 {STANDBY_TO_ACTIVE}

In {STANDBY_TO_ACTIVE}, the output rails are turned on if enabled in the register settings, and MPIOx is asserted if configured as outputs in the register settings. MPIOx can also be configured to inputs that control regulator output power-on timing. See Power-ON for details.

8.4.3 {ACTIVE_TO_STANDBY}

In {ACTIVE}, if PWRON is de-asserted, the FSM transitions to {ACTIVE_TO_STANDBY}. The FSM enters {STANDBY} when the outputs complete the programmed power-off sequence.

8.5 {ACTIVE}

When the output rails and MPIOx complete the programmed power-on sequence, the FSM enters {ACTIVE}.

8.6 {IORESET}

There are three possible causes of the device entering {IORESET}:

- CRST_IN# is asserted when CRST_Fault_EN = LOW
- The watchdog timer expires when WD_PD_EN = LOW
- WD_RST_EN = HIGH; or Warm Reset = HIGH

The MPIOx reset outputs are asserted immediately. See Warm and Cold Reset for details. While in this state, if PWRON is de-asserted, the device transitions to {ACTIVE_TO_STANDBY}.

8.6.1 {IORESET_TO_ACTIVE}

When reset is complete, the reset register bit is cleared automatically and the device enters {IORESET_TO_ACTIVE}. While in {IORESET_TO_ACTIVE}, if PWRON is de-asserted, the FSM enters {ACTIVE_TO_STANDBY}.

8.7 {SLEEP}

{SLEEP} is a mode of operation with selectable alternative power rails settings. Different output voltages may be set, and the buck regulators can each be set to a different operating mode.

While in {ACTIVE}, if SLEEP# is asserted or the SLEEP_State_EN bit is HIGH, the FSM enters {ACTIVE_TO_SLEEP}.

8.7.1 {ACTIVE_TO_SLEEP}

There are two output voltage settings for each rail - one for {ACTIVE} and one for {SLEEP}. When entering {SLEEP}, the voltage transitions to {SLEEP} settings following the power-off sequence. If the voltage settings are different for the two states, the voltages ramp up or ramp down according to the programmed DVS slew rate. When slewing of all output voltages completes, the FSM enters {SLEEP}.

8.7.2 {SLEEP_TO_ACTIVE}

While in {SLEEP}, if SLEEP# is de-asserted or the SLEEP_State_EN bit is LOW, the FSM transitions to {SLEEP_TO_ACTIVE} following the power-on sequence. If the voltage settings are different for the two states, the voltages ramp up or ramp down according to the programmed DVS slew rate. When all output voltage changes complete, the FSM enters {ACTIVE}.

8.8 {FAULT_OUT}

If a fault condition occurs, the FSM enters {FAULT_OUT} after completing the power-off sequence (see Device Monitors, Warnings, and Protections). Depending on the fault type and configured response, the device may turn off all outputs in {FAULT_OUT}. INT# is pulled LOW if not masked from that particular fault. If CEN = LOW, the device enters {RESET}. To exit {FAULT_OUT} and enter {STANDBY}, the fault condition(s) must cease, and all latched fault bits must be cleared by writing 1 to the fault register bit(s).

If the latched fault bit is cleared before all the outputs have finished turning off, the power-up sequence can begin with some outputs already enabled. This behavior can be avoided if necessary by ensuring that there is sufficient delay before clearing the latched fault bit. Alternatively, the cold reset function (Warm and Cold Reset) can be triggered immediately before clearing the latched fault bit to ensure that the power-down sequence completes before powering up again.

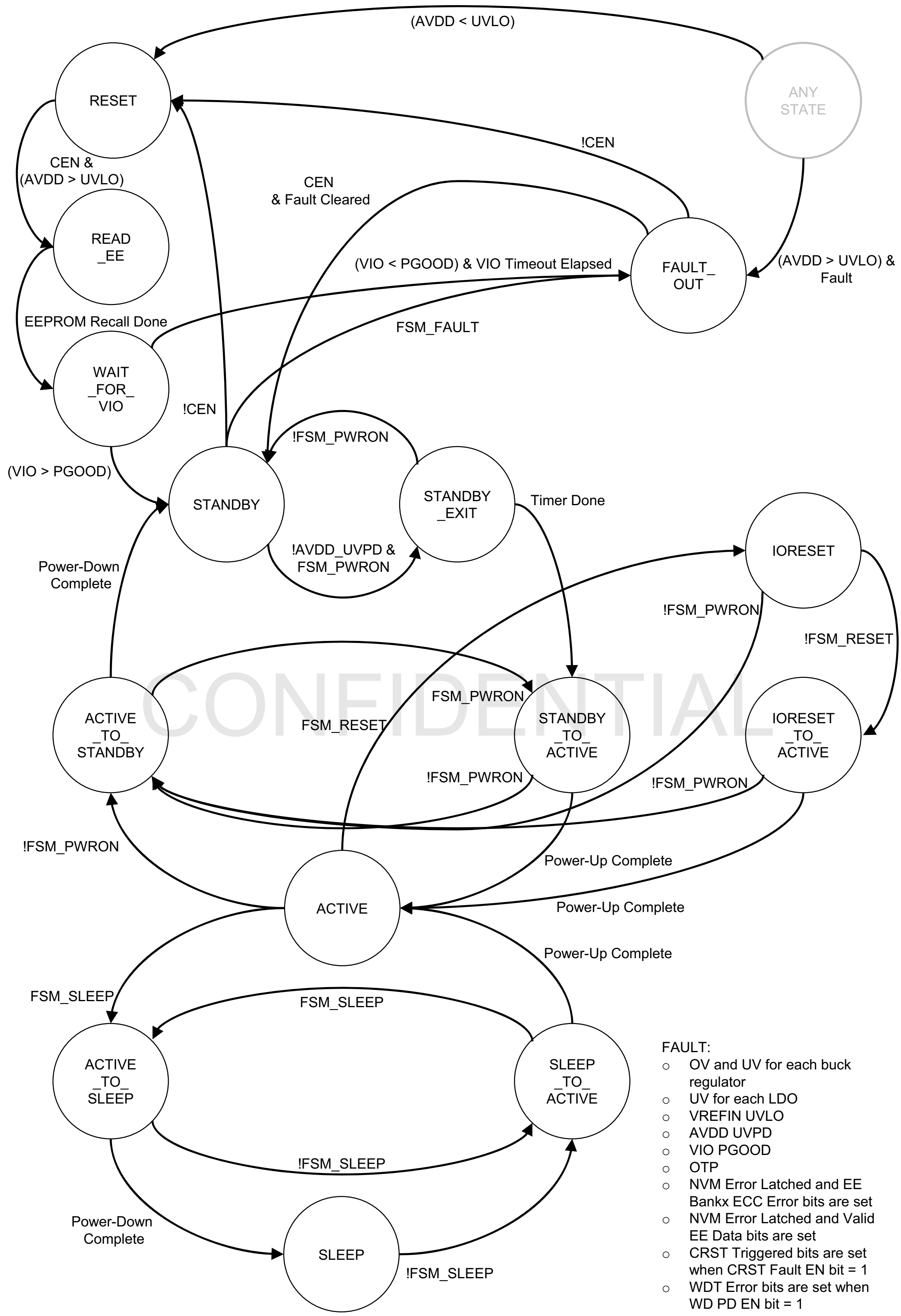


Figure 14. State Diagram

9. Functional Blocks and Application Information

9.1 Chip Enable

The device chip enable (CEN) is an active high, level-sensitive input. When asserted (HIGH), it provides a whole chip enable signal, and when de-asserted (LOW), it disables the device, and all outputs are tri-stated. CEN supports being tied to AVDD. See Electrical Specifications for pin capability.

When asserted, the internal bias circuits power up and check to see if AVDD is above the UVLO threshold. CEN going low in any state where outputs are active causes a sequenced power-down, and a transition to {STANDBY}, then onward to {RESET}.

When the power-off sequence is triggered by CEN going low, a shutdown period starts when the last output is powered off. The shutdown period is set by the maximum Tshutdown setting of the output rails. At the end of the shutdown period, the FSM transitions to {STANDBY} and then {RESET}, which means the on-chip active discharge circuit stops working, and the output capacitors discharge by the external load current.

9.2 PWRON

Power-on (PWRON) is a configurable input offering with an on/off switch or push button support. PWRON polarity is configurable in both on/off switch and push-button mode. When configured as an on/off switch, the input is an active high or low (depending on the polarity setting) level-sensitive input. When configured as a push-button input, the input must be asserted low or high (depending on the polarity setting) for a programmable long duration (in seconds) to internally set the PWRON signal. The supported periods are 1s, 1.5s, 2s, and 3s. A long push button is required for initiating each of the power-on and power-off sequences.

When the internal PWRON signal is asserted, the FSM enters {STANDBY_EXIT}, then onwards to {STANDBY_TO_ACITVE} where it enables the regulators and starts the power-on sequence following the configurations loaded from EEPROM. When the internal signal is de-asserted, all the regulators are powered down, and the MPIOx outputs are asserted following the sequence configured in the register settings.

9.3 Multi Purpose I/O

The RAA215300 includes a set of multiple purpose inputs/outputs (MPIO0~5) with programmable functionalities.

If configured as either a Reset Output, External VR EN Output, or External VR power-good Input, during power-on/off each MPIOx has a power-on/off delay, which is set in MPIOx Power-On and MPIOx Power-Off registers. The power-on and power-off delay can be programmed from 0 to 127ms. The polarity, type, and function of each MPIOx can be configured independently by the MPIOx_Config registers. Each MPIOx can be set to either active low or active high using the register bit MPIOx_Invert. Each MPIOx can be set to general purpose input/output or a specific function. The supported functions for each pin are shown in Table 2. When an MPIOx is set as a general purpose input, its status is read from the MPIO_Input_Status register. When an MPIOx is set as a general purpose output, it can be set to LOW or HIGH using the MPIO_I2C_Output register.

When an MPIOx is set to output, four different types can be selected from register bits MPIOx_Type[1:0]: high impedance, open-drain NMOS output, open-drain PMOS output, or full CMOS output. When set to an open-drain NMOS output, the MPIO needs to be pulled up to an external voltage higher than the VIH threshold through a resistor, but within its allowable operating range. When set to open-drain PMOS output, the MPIO needs to be pulled down to GND through a resistor. When set to full CMOS output, the MPIO does not need an external pull-up voltage as it is pulled up to VIO internally.

It is acceptable to have multiple MPIOx configured with the same function.

The MPIOx configuration registers (0x8A - 0x8F) can be locked by the MPIO Config Lock bit to prevent the user from accidentally changing the MPIOx configurations. When this bit is set to 1, the registers at 0x8A - 0x8F are locked, which means that writing to those registers is ignored. The values in those registers can still be read back. After being set to 1, this bit cannot be set back to 0 until POR.

See the pin mapping shown in Table 2.

Table 2. MPIOx Supported Functions

Function	Type	MPIO0	MPIO1	MPIO2	MPIO3	MPIO4	MPIO5
Unused MPIOx Pin	-	Yes	Yes	Yes	Yes	Yes	Yes
External VR PGOOD Input	Input	Yes	Yes	Yes	Yes	Yes	Yes
Input to I²C Register	Input	Yes	Yes	Yes	Yes	Yes	Yes
PGOOD Output	Output	Yes	Yes	Yes	Yes	Yes	Yes
Reset Output	Output	Yes	Yes	Yes	Yes	Yes	Yes
External VR EN Output	Output	Yes	Yes	Yes	Yes	Yes	Yes
Output to I²C Register	Output	Yes	Yes	Yes	Yes	Yes	Yes
32kHz Clock (32K_CLK)	Output	-	-	Yes	-	-	-
SLEEP#	Input	-	-	-	Yes	-	-
WDT_RST#	Input	-	-	-	-	Yes	-
CRST_IN#	Input	-	-	-	-	-	Yes

9.3.1 Unused MPIOx Pin

If an MPIO is not used, Renesas recommends setting the respective MPIO Type to Disabled (high impedance) and MPIO Function to Disabled in EEPROM. Any MPIO can be disabled. When disabled, it is high-impedance.

If the user does not want to program EEPROM when an MPIO is not used, the MPIO that is configured as an output can be left floating. The MPIO that is configured as an input needs to be connected to a known voltage to ensure it is in the de-assertion state.

9.3.2 External VR PGOOD Input

Any MPIO can be set to perform this function. When asserted, this signal pauses the power-on or power-off sequence timing of the RAA215300, providing a way to sequence the RAA215300 with an external regulator. The expected External VR PGOOD Input delays are set by the applicable MPIO power-on and power-off delays. Only the outputs with delay settings that are larger than the External VR PGOOD Input MPIO delay setting (relative to PWRON) are affected by the assertion or de-assertion of this MPIO input signal.

During power-on, when PWRON is asserted, the External VR PGOOD Input is expected to be asserted by the host within the delay time set in the MPIO Power-On register. If External VR PGOOD Input is not asserted before the MPIO delay expires, the power sequence pauses and waits for the signal to toggle. The delay timers of the outputs start to count when PWRON is asserted and are paused when the External VR PGOOD Input MPIO delay timer expires. When this input is asserted by the host, the power sequence continues. If External VR PGOOD Input is asserted before the MPIO delay expires, the outputs are not paused.

During power-off, when PWRON or CEN is de-asserted, the External VR PGOOD Input is expected to be de-asserted within the delay time set in the MPIO Power-Off register. If External VR PGOOD Input is not de-asserted, the power sequence pauses and waits for the signal to toggle. The delay timers of the outputs start to count when PWRON or CEN is de-asserted and are paused when the External VR PGOOD Input MPIO delay timer expires. When External VR PGOOD Input is de-asserted by the host, the power sequence continues. If External VR PGOOD Input is de-asserted before the MPIO delay expires, the outputs are not paused.

When only one MPIO is set to the External VR PGOOD Input function, the power-on or power-off delay of each output is calculated using Equation 1 where t_x is the delay setting of the output, T is the time when the External VR

PGOOD Input is asserted or de-asserted after PWRON is asserted or de-asserted, and t_{MPIO} is the delay setting of the External VR PGOOD Input.

(EQ. 1) $$t_{delay} = t_x + \max(0, T - t_{MPIO})$$

When multiple MPIOs are set to the External VR PGOOD Input function, the power-on or power-off delay of each output is calculated using Equation 2.

(EQ. 2) $$t_{delay} = t_x + \max(0, T_y - t_{MPIOy}, \ldots, T_N - t_{MPION})$$

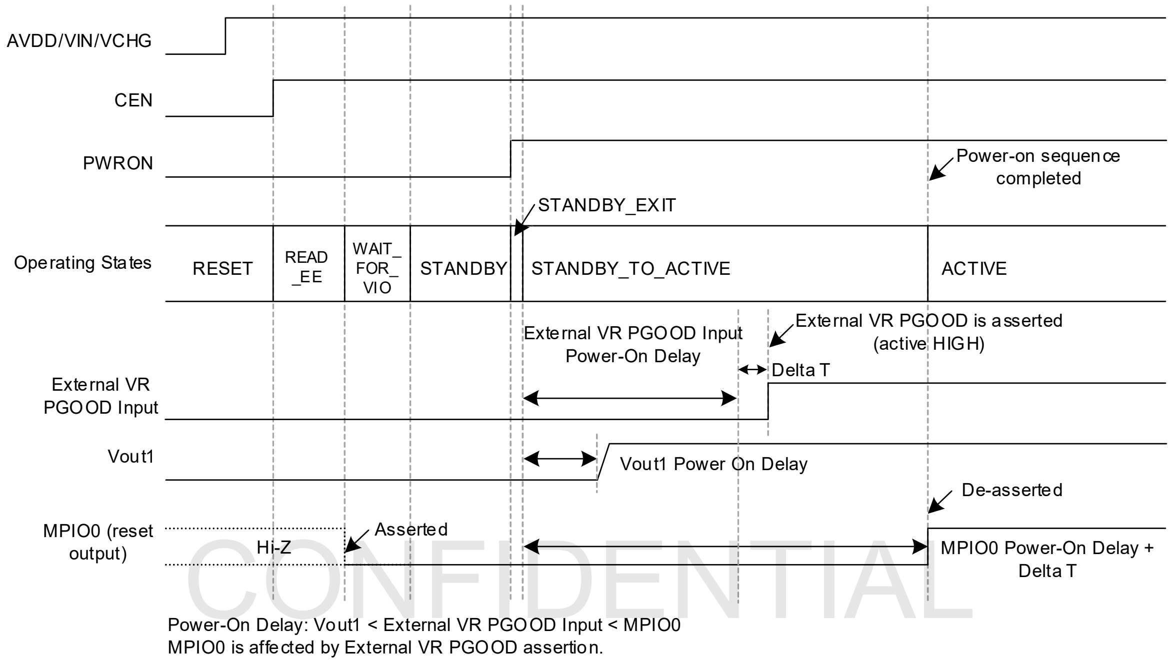


Figure 15. Power-On Example - External VR PGOOD Input

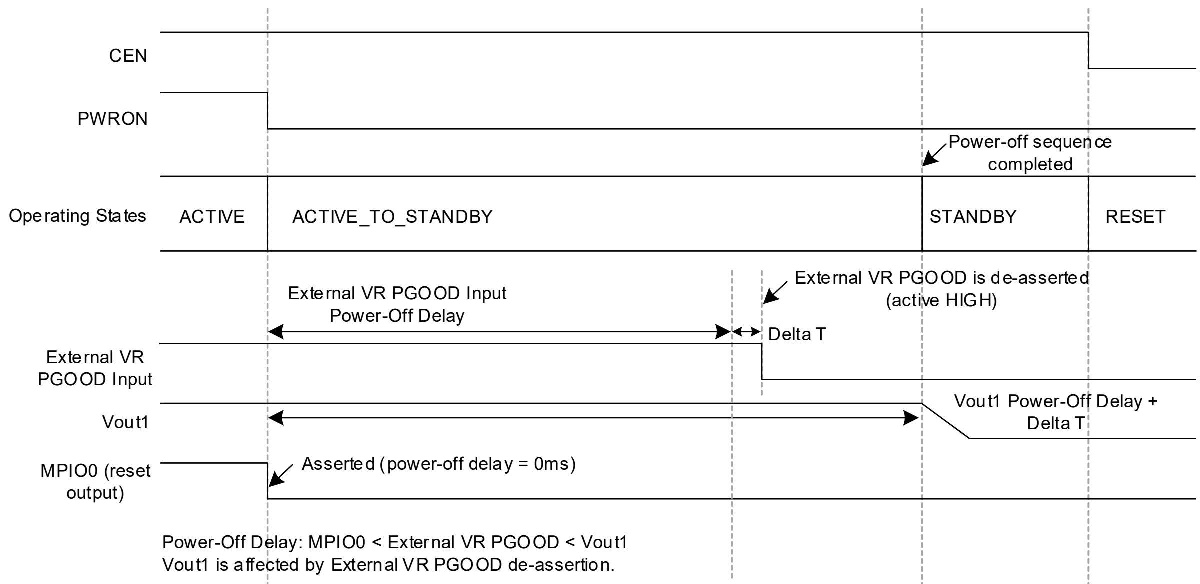


Figure 16. Power-Off Example - External VR PGOOD Input

9.3.3 Input to I2C Register

Any MPIO can be set to support this function. When an MPIO is set to this function, it is a general-purpose input. Its status can be read from the MPIO Input Status register.

9.3.4 PGOOD Output

Any MPIO can be set to support this function. The MPIOx can each be configured to assert PGOOD dependent on the internal power-good signal of a selected rail, or the logical AND of all enabled buck and the power-good signals of the LDO rails. An internal PGOOD signal is asserted when the output voltage is above the PGOOD threshold. PGOOD assertion during power-on signifies the rising threshold has been met, and the soft-start sequence is complete.

When an MPIO is set as a PGOOD output, the MPIO Power-On Delay register bits [3:0] are used to set which regulator output is used for the PGOOD output. In this case, Bits [6:0] in this register are no longer used as a power-on delay.

Note: If any buck or LDO regulator is disabled, and PGOOD output is set to **AND of all regulators PGOOD**, the PGOOD signal is not asserted during power-on. In this case, the PGOOD output needs to be set to another regulator PGOOD.

9.3.5 Reset Output

Any MPIO can be set to support this function. The reset output provides a system reset signal. There can be more than one reset output required in the system, including processor reset (PRST#) and eMMC reset (eRST#). Multiple MPIO can be configured as reset outputs.

The reset output is asserted as soon as the EEPROM recall is completed. During power-on when PWRON is asserted, the reset output is de-asserted after the delay time set in the MPIOx Power-On register. During power-off when CEN or PWRON is de-asserted, the reset output is asserted after the delay time set in the MPIOx Power-Off register.

9.3.6 External VR EN Output

Any MPIO can be set to support this function. This output can be used as an enable signal to control an external regulator power-on/off. It should be configured such that when asserted by RAA215300 the signal enables the external regulator, and when de-asserted it should disable the external regulator.

Any MPIOx with this function is initially de-asserted as soon as the EEPROM recall is completed. During power-on when PWRON is asserted, the VR_EN Output is asserted after the delay time set in the MPIOx Power-On register. During power-off when CEN or PWRON is de-asserted, the VR_EN is de-asserted after the delay time set in the MPIOx Power-Off register.

9.3.7 Output to I2C Register

Any MPIO can be set to support this function. The MPIOx can be asserted HIGH or LOW with software control by setting the related bit in the register.

9.3.8 32kHz Clock (32K_CLK)

Only MPIO2 supports this function. The function provides a driven clock signal output for external devices. The clock frequency is programmable with a maximum setting of 32.768kHz, which is the RTC crystal oscillator frequency. The RTC needs to be enabled by the RTC_EN bit to output this clock signal. If the user does not have an external pull-up voltage, the MPIO2 needs to be configured as a Full CMOS output.

When this function is selected, the MPIO2 Power-Off Delay register Bits [3:0] are used to select the clock frequency. In this case, Bits [6:0] in this register are no longer used as a power-off delay. See the Register Map.

9.3.9 SLEEP#

Only MPIO3 supports this function. This is an edge-triggered, hardware control input to control switching the device between {SLEEP} and {ACTIVE} operating states. The RAA215300 transitions from {ACTIVE} to {SLEEP} (through {ACTIVE_TO_SLEEP}) when SLEEP# is asserted, and transitions from {SLEEP} to {ACTIVE} (through {SLEEP_TO_ACTIVE}) when SLEEP# is de-asserted.

When MPIO3 is set to other functions, the sleep/active state can be controlled by software using the SLEEP_State_EN bit to control {SLEEP} mode entry/exit. When SLEEP State EN bit = 1, the device transitions to {ACTIVE_TO_SLEEP}, and when SLEEP_State_EN bit = 0, the device transitions to {SLEEP_TO_ACTIVE}. The hardware input and software bit control have a logical OR relationship, see Table 3. To maintain hardware control, the bit should be kept at 0, whereas to maintain bit (software) control the hardware input must internally de-assert the signal (0) as determined by the MPIO3_Invert configuration.

Table 3. {SLEEP}<->{ACTIVE} Mode Control

SLEEP# State	SLEEP_State_EN bit setting (0x6C[7])	Selected Operating State
When configured active LOW, MPIO3_Invert = Active low		
LOW (1)	0	{SLEEP}
LOW (1)	1	{SLEEP}
HIGH (0)	0	{ACTIVE}
HIGH (0)	1	{SLEEP}
When configured active HIGH, MPIO3_Invert = Active high		
HIGH (1)	0	{SLEEP}
HIGH (1)	1	{SLEEP}
LOW (0)	0	{ACTIVE}
LOW (0)	1	{SLEEP}

9.3.10 WDT_RST#

Only MPIO4 supports this function. This is a falling edge triggered input signal. When the watchdog timer is enabled, this signal is used to reset it before the timer expires. If the watchdog timer is disabled, this signal is ignored. See Watchdog Timer for the details.

9.3.11 CRST_IN#

Only MPIO5 supports this function. The CRST_IN# input is edge triggered and acts as a hardware reset signal. When the MPIO5_Invert = Active LOW, the signal is asserted on the falling edge of MPIO5. When MPIO5 Invert = Active HIGH, the signal is asserted on the rising edge of MPIO5. The minimum pulse width requirement is 1.5µs (typical) because of internal de-glitching and synchronization to the internal clock. This signal is only valid in {ACTIVE} or {SLEEP}.

When CRST_IN# is asserted:

- If currently in {SLEEP}, the RAA215300 enters {ACTIVE}. The device does not enter {SLEEP} until the reset cycle has been completed or the related latched fault has been cleared.
- The CRST_Triggered_Latched and CRST_Triggered_Live fault bits are set. INT# is pulled LOW if not masked.
- The following occurs if the CRST_Fault_EN bit = Disabled:
  - The RAA215300 enters {IORESET}. Any MPIOx configured as reset outputs are asserted immediately.
  - When CRST_IN# is de-asserted by the host, the reset outputs are de-asserted following the configured power-on sequence. The CRST_Triggered fault bits cannot be cleared until CRST_IN# is de-asserted.
- The following occurs if the CRST_Fault_EN bit = Enabled:

- Any MPIOx configured as reset outputs are asserted and the output rails are shut down following the power-off sequence configured in the register settings. RAA215300 enters {FAULT_OUT}.
- If the latched fault bit is subsequently cleared, the device transitions to {STANDBY}.

Note: Assertion of CRST_IN# is latched until the Sequencer FSM reaches {IORESET}. If CRST_IN# is asserted in {ACTIVE_TO_STANDBY} or {STANDBY_TO_ACTIVE}, the FSM can not reach {IORESET} at that time. The next time the FSM reaches {ACTIVE}, it can act on the latched CRST_IN# assertion, and jumps to {IORESET}.

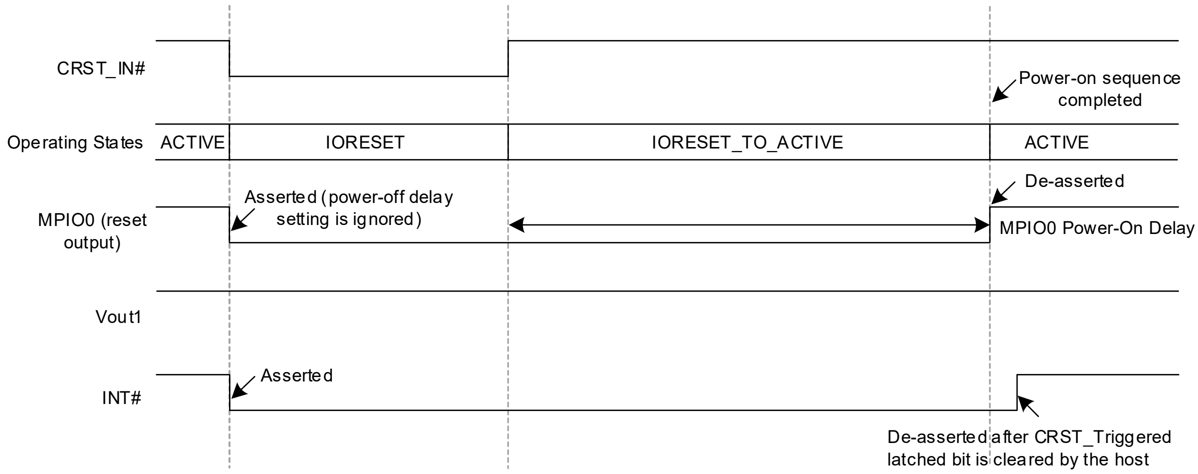


Figure 17. Example of CRST_IN# Operation - CRST_FAULT_EN = Disabled

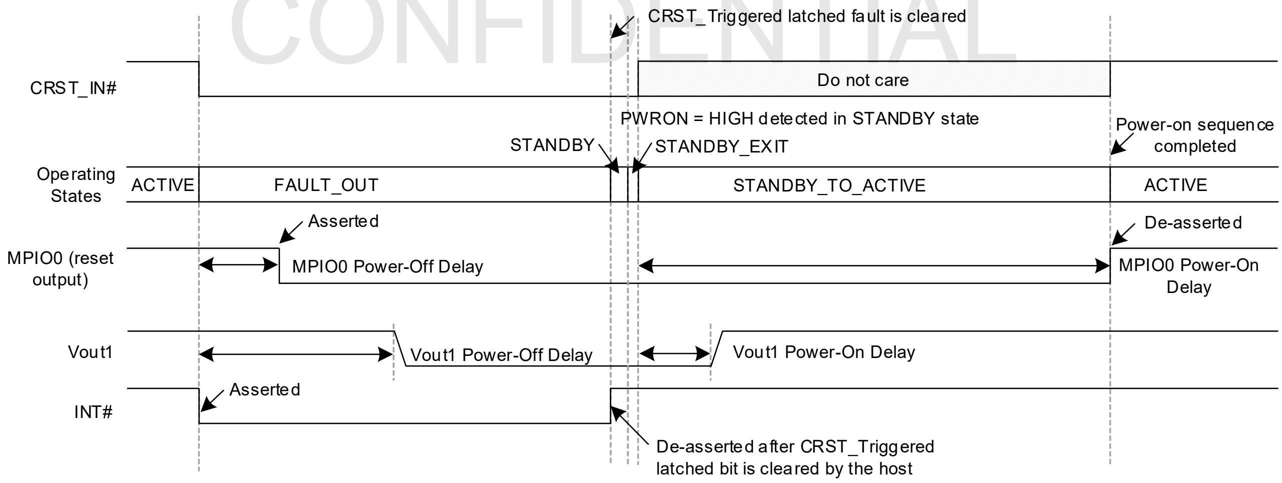


Figure 18. Example of CRST_IN# Operation - CRST_FAULT_EN = Enabled

9.3.12 Alternative Decodes for MPIOx functions

When an MPIO is configured as a PGOOD output, 32K_CLK, or Watchdog Timer Reset (WDT_RST#), the respective MPIOx Power-On Delay or MPIOx Power-Off Delay register bits settings are changed to a different set of decodes which works for this particular function. In this case, Bits [6:0] in this register are no longer used as power-on or power-off delay. See Table 4 for details.

Table 4. Alternative Decodes for MPIOx Functions

MPIOx and Configured Function	Register Bits	Alternative Settings for the Register Bits
MPIO0 configured as PGOOD output	MPIO0 Power-On Delay register Bits [3:0]	Set which regulator is used for PGOOD output at MPIO0
MPIO1 configured as PGOOD output	MPIO1 Power-On Delay register Bits [3:0]	Set which regulator is used for PGOOD output at MPIO1
MPIO2 configured as PGOOD output	MPIO2 Power-On Delay register Bits [3:0]	Set which regulator is used for PGOOD output at MPIO2
MPIO2 configured as 32K_CLK	MPIO2 Power-Off Delay register Bits [2:0]	Set frequency for the 32K_CLK signal
MPIO3 configured as PGOOD output	MPIO3 Power-On Delay register Bits [3:0]	Set which regulator is used for PGOOD output at MPIO3
MPIO4 configured as PGOOD output	MPIO4 Power-On Delay register Bits [3:0]	Set which regulator is used for PGOOD output at MPIO4
MPIO4 configured as Watchdog Timer Reset	MPIO4 Power-Off Delay register Bits [3:0]	Set timeout period for the WDT
MPIO5 configured as PGOOD output	MPIO5 Power-On Delay register Bits [3:0]	Set which regulator is used for PGOOD output at MPIO5

9.4 Watchdog Timer

The WDT starts when the device reaches {STANDBY_TO_ACTIVE}, and is disabled again when the device reaches {STANDBY}. The function can be enabled/disabled in EEPROM.

The WDT feature can be used to detect a system boot-up failure. The function of MPIO4 needs to be set to WDT_RST# and the WD_EN bit needs to be set to 1 to enable this feature. MPIO4 Power-Off register Bits [3:0] are used to set the timeout period when MPIO4 is set to WDT_RST#. Register bits WD_PD_EN and WD_RST_EN are used to set the device behavior when the WDT feature is enabled.

The WDT_RST# input needs to be asserted by the host to reset the timer before it expires. If the watchdog timer expires, the RAA215300 takes the following steps:

1. If currently in {SLEEP}, the RAA215300 enters {ACTIVE} through {SLEEP_TO_ACTIVE}.
2. The WDT_Error_Latched and WDT_Error_Live fault bits are set. INT# is pulled LOW if not masked.
3. The following occurs if the WD_RST_EN bit = Enabled, WD_PD_EN bit = Disabled:
   a. Any MPIOx configured as reset outputs are asserted immediately. The reset outputs are then de-asserted automatically following the power-on sequence.
   b. The WDT stops counting when the WDT_Error fault bits are set. It does not start counting until WDT_RST# is asserted by the host. The WDT_Error fault can only be cleared by writing 1 after WDT_RST# is asserted and before the WDT expires again, or after PWRON is de-asserted.
4. The following occurs if the WD_PD_EN bit = Enabled:
   a. Any MPIOx configured as reset outputs are asserted and the output rails are shut down following the power-off sequence configured in the register settings.
   b. The WDT stops counting when the WDT_Error fault bits are set. It does not start counting until the WDT_Error bit is subsequently cleared by writing 1. The WDT_Error fault cannot be cleared until the

power-off sequence finishes and the device enters {FAULT_OUT}. When the fault is cleared, the WDT starts counting (restarts power-on sequence).

Note: If both WD_PD_EN and WD_RST_EN are set to be enabled, the WD_PD_EN bit has higher priority and WD_RST_EN is ignored.

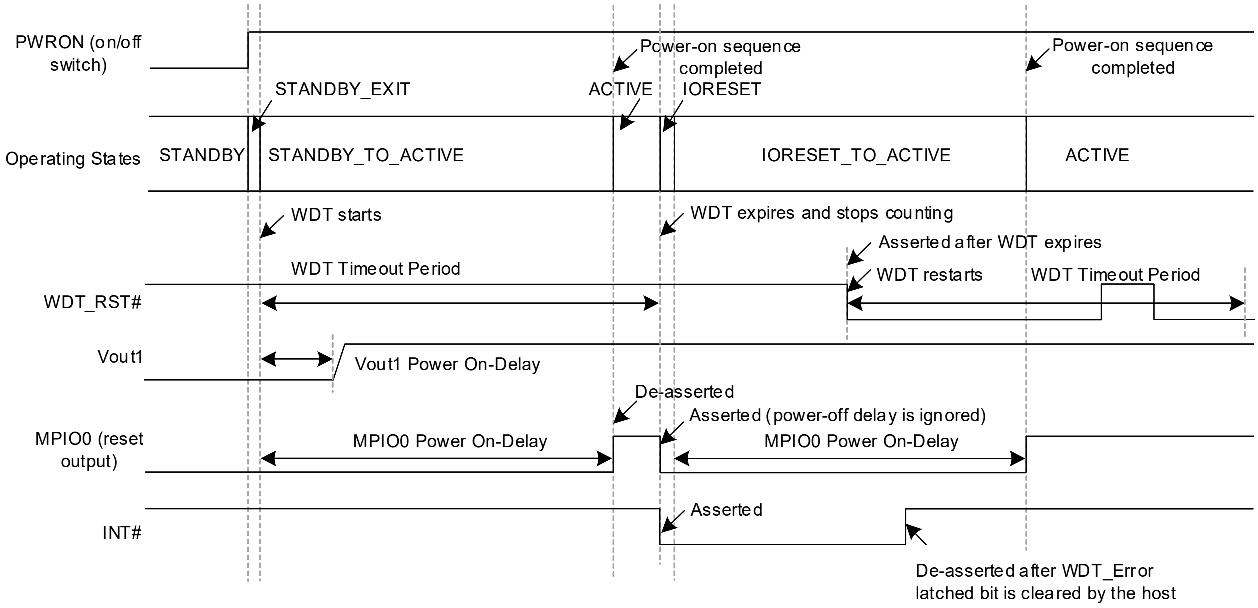


Figure 19. Example of WDT_RST# Operation - WD_RST_EN bit = Enabled, WD_PD_EN bit = Disabled

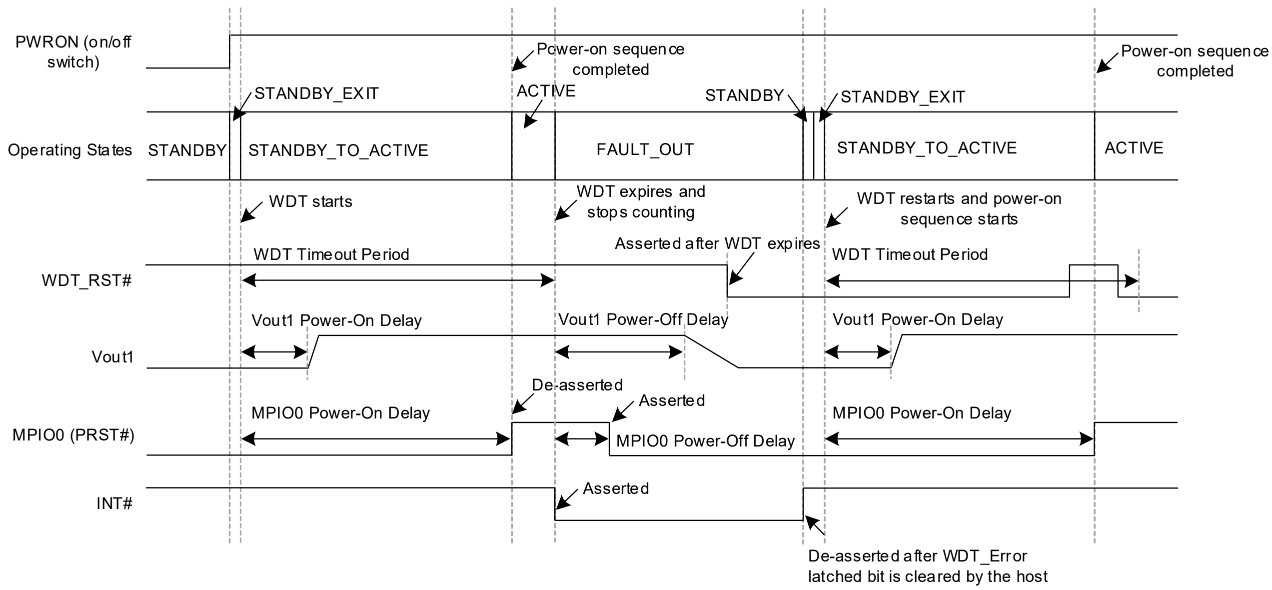


Figure 20. Example of WDT_RST# Operation - WD_PD_EN bit = Enabled

9.5 Power Sequencing

The power sequencing starts when PWRON is asserted in {STANDBY} and the device transitions to {ACTIVE}. The RAA2153000 regulators and MPIOx power-on delays are configured in the EEPROM.

The output voltage of each rail is monitored after it completes soft-start. If there is an undervoltage or overvoltage condition detected, the PGOOD output (if any MPIO is configured to this function) is de-asserted and the device enters {FAULT_OUT} (if these faults are configured to shut down the device).

9.5.1 Power-ON

The power-on delays for all rails are independently programmable from 0~127ms, with a 1ms step. All timing is based on entry to {ACTIVE}.

Each rail has a programmable startup slew rate.

9.5.2 Power-OFF

The power-off delays for all rails are independently programmable from 0~127ms, with a 1ms step. All timing is based on entry to {ACTIVE}.

Each rail has a programmable shutdown slew rate.

9.5.2.1 I²C Trigger Power-Off

The device includes a feature to trigger sequenced power-off operations triggered by an I²C command. Triggering requires sending a specific 8-bit key to the I2C_Trigger_Power_Off_Key bits.

This function is intended for use when the device is configured in long-push button mode, see PWRON.

The following are examples of power-on and power-off sequences in various configurations.

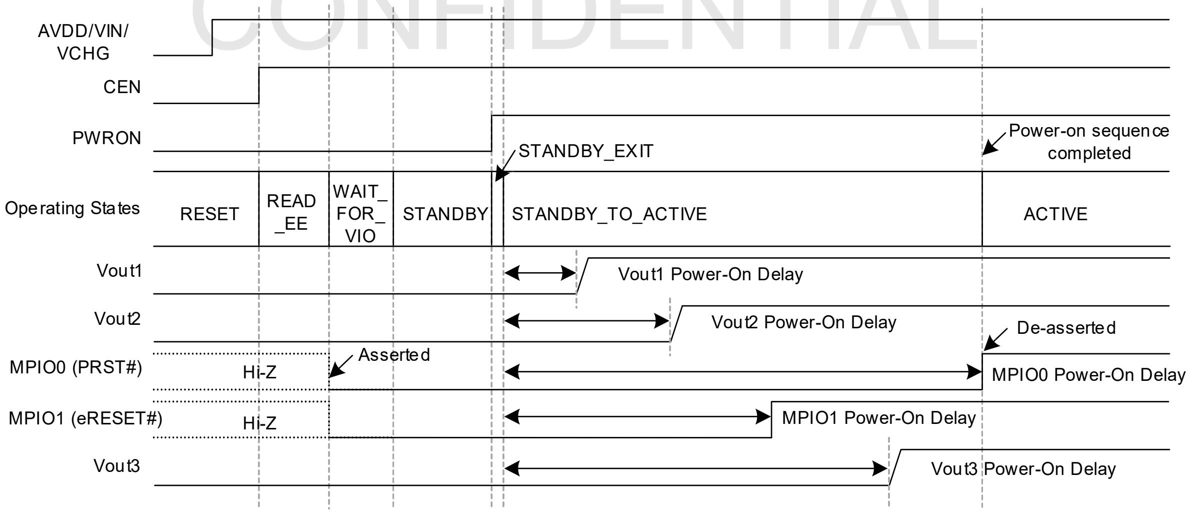


Figure 21. Typical Power-On Example - PWRON as On/Off Switch

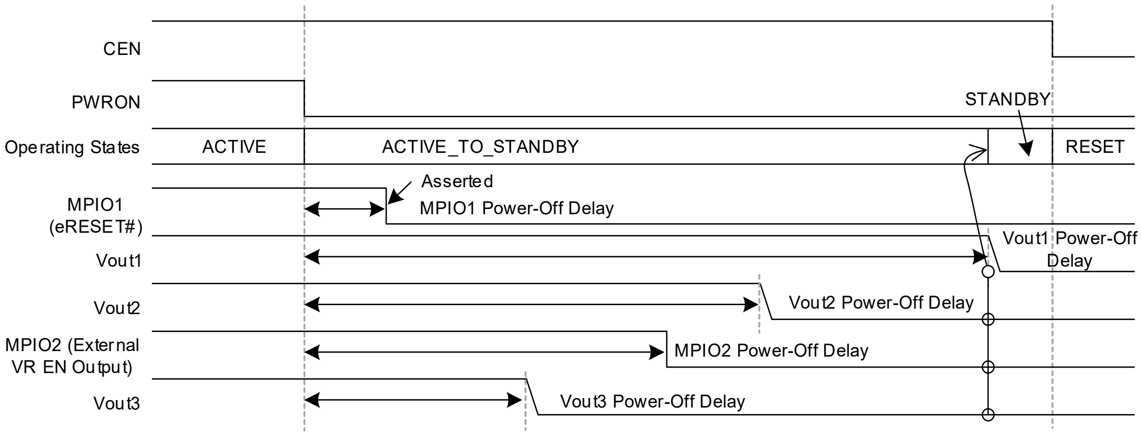


Figure 22. Typical Power-Off Example - PWRON as On/Off Switch

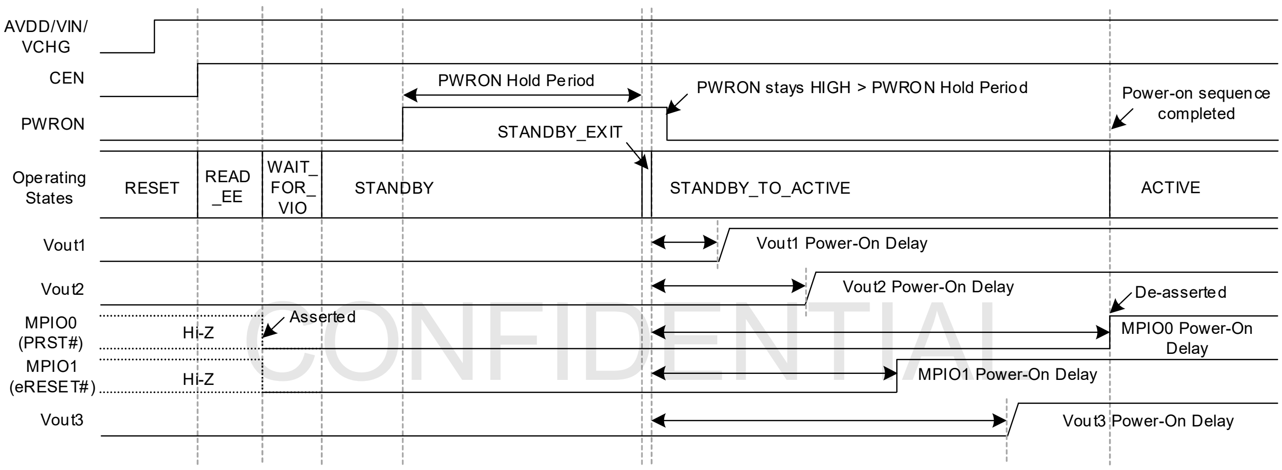


Figure 23. Typical Power-On Example - PWRON as Long Push Button

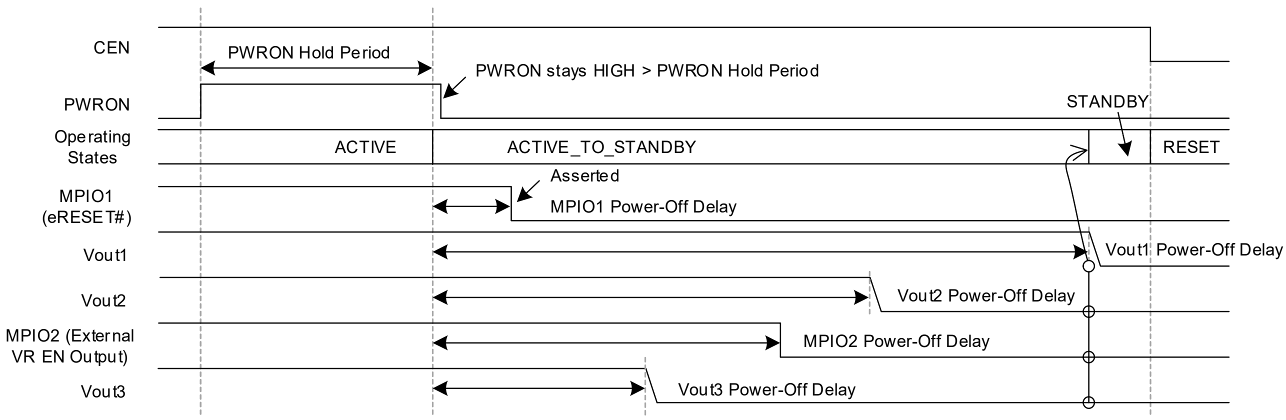


Figure 24. Typical Power-Off Example - PWRON as Long Push Button

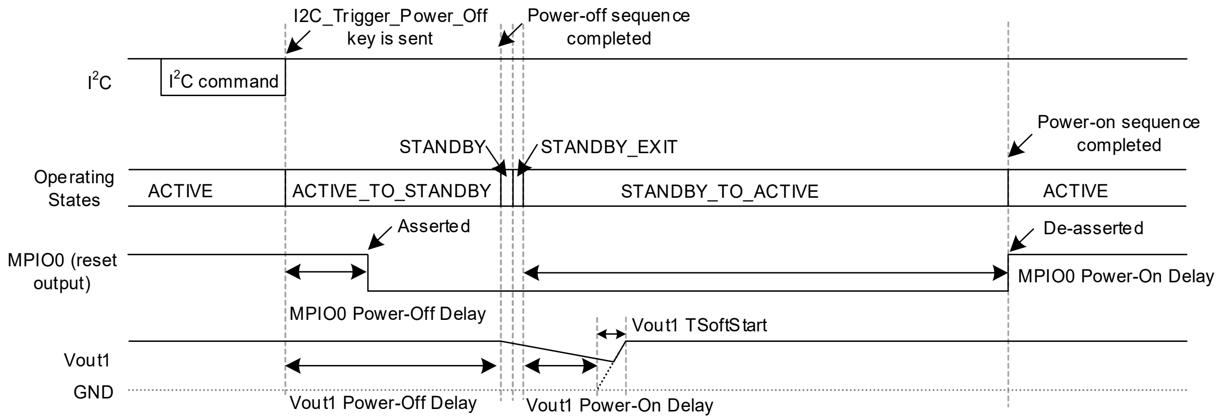


Figure 25. I²C Triggered Power-Off - PWRON = HIGH. PWRON as On/Off Switch, Active HIGH

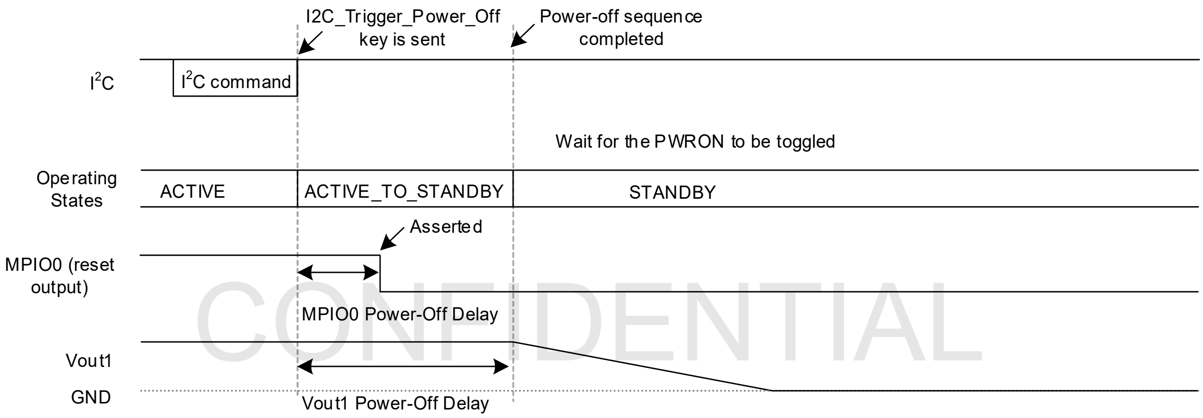


Figure 26. I²C Triggered Power-Off - PWRON = LOW. PWRON as Long Push Button, Active HIGH

9.6 Warm and Cold Reset

The RAA215300 features two types of software-controlled reset functions for controlling the application system (warm reset and cold reset). These resets can be separately triggered by setting the related volatile register bit to 1. Warm and cold reset bits should not be set simultaneously. When the selected reset operation is completed, the bit is automatically cleared to 0 in the volatile register.

The warm reset register bit is used to generate a system reset only. It does not recycle the RAA215300 output power rails. When triggered, the MPIO configured as reset outputs are asserted immediately. The reset signals are then de-asserted following the power-on timing set in their respective MPIOx Power-On Delay register. The LDO_SELx status may be changed because of the processor being reset, and the device responds accordingly.

The cold reset register bit generates a system reset and recycles the output power rails. When triggered, the MPIO configured as reset outputs are asserted following their power-off delay settings, and the output rails power down following their programmed sequence settings. When power-down completes, the FSM enters {STANDBY}. After a programmable delay set by the Cold Reset Delay register bits, the output rails are restarted based on their programmed sequence settings. The reset signals are then de-asserted following the power-on timing set in the respective MPIOx Power-On Delay register.

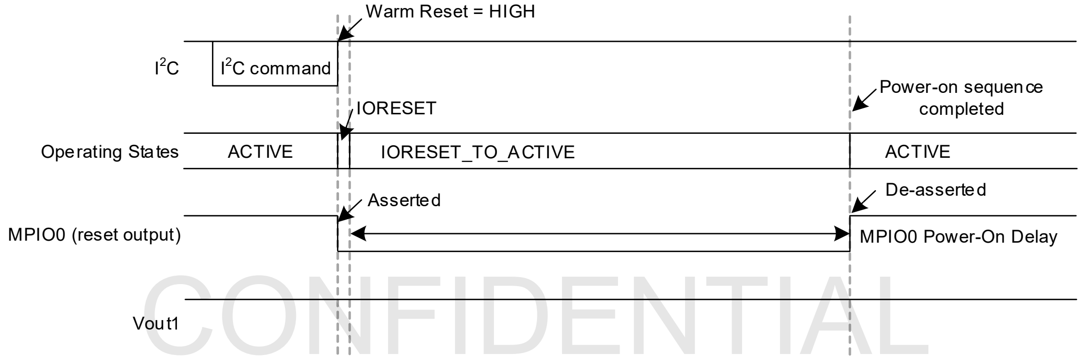


Figure 27. Warm Reset Operation

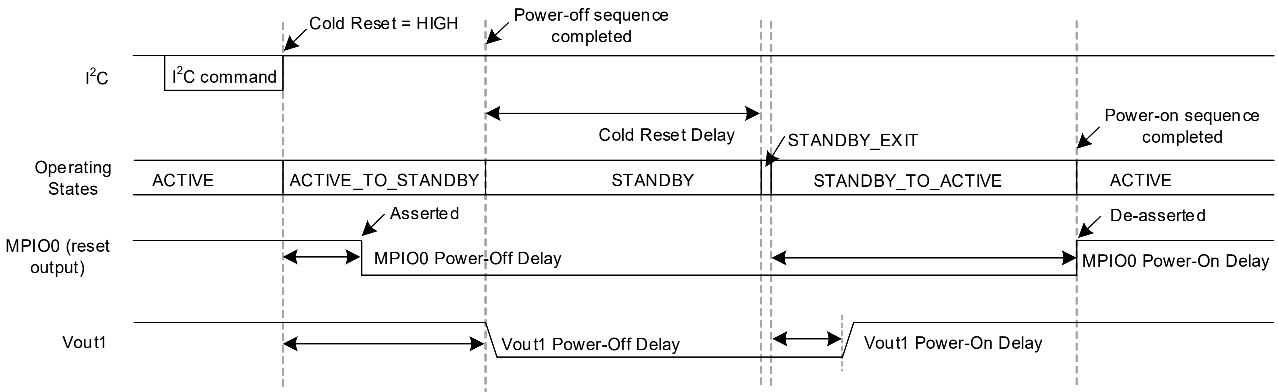


Figure 28. Cold Reset Operation

9.7 Output Discharge

There are four programmable options for the discharge of the buck rails:

- Set the regulator into Forced PWM (FPWM) mode and ramp down the reference following the programmed slew rate.
- Set the regulator into PFM/PWM mode and ramp down the reference following the programmed slew rate.
- Discharge the output rails using programmable discharge resistors. This option disables the regulator, turns the discharge switch on, and ramps down the reference following the programmed slew rate.
- Discharge the output rails using programmable discharge resistors. This option disables the regulator and turns the discharge switch on without ramping down the reference first - providing a simple RC discharge rate.

There are two programmable options for the discharge of the LDO rails:

- Discharge the output rails using programmable discharge resistors. This option disables the regulator, turns the discharge switch on, and ramps down the reference following the programmed slew rate.
- Discharge the output rails using programmable discharge resistors. This option disables the regulator and turns on the discharge switch without ramping down the reference first - providing a simple RC discharge rate.

During startup, there is no active discharge. Discharge functionality is disabled until after the state machine reaches {ACTIVE} or {ACTIVE_TO_STANDBY}. Active discharge is disabled in {RESET}.

Note: In VTT mode, check that the DDR manufacturer's recommendations are achieved during the discharge of VDDQ (typically Buck2) and VTT (Buck6).

9.8 DVS

The RAA215300 employs dynamic voltage scaling (DVS) to optimize power and efficiency in the system. The DVS features programmable DVS ramp-up/down slew rates for each rail that are applied when the output voltage(s) are changed. The common usage is to change the output voltages between {ACTIVE} and {SLEEP}. Exiting {SLEEP} often occurs to handle a real-time request; therefore, a fast slew rate is often required.

DVS is also used when changing the output voltage during {ACTIVE}. When the new output voltage is written into the register, the DVS block slews the output voltage to the new target based on the programmed rate.

Figure 29 illustrates the DVS between {ACTIVE} <-> {SLEEP} state transitions with delays.

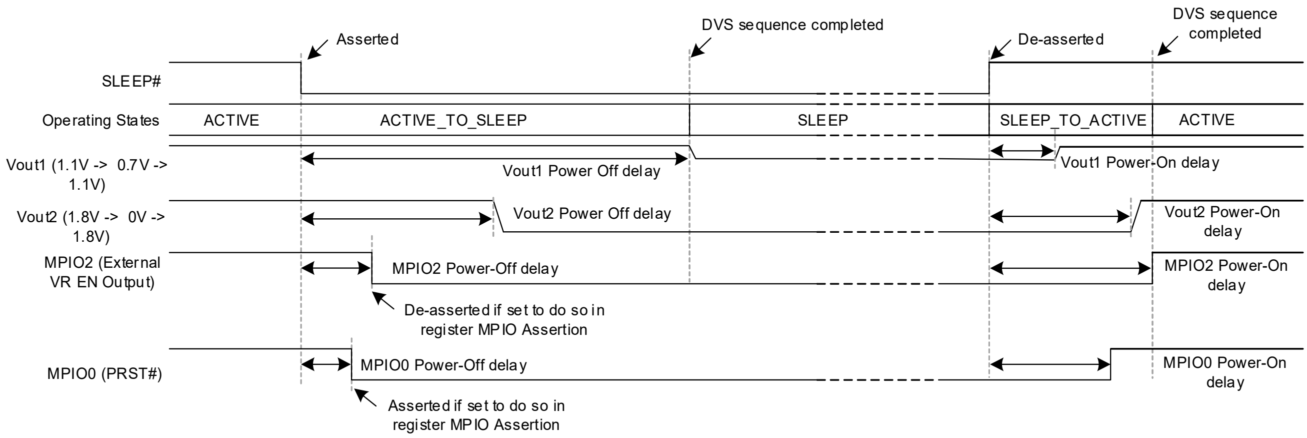


Figure 29. {ACTIVE} <-> {SLEEP} DVS Transition Example

Note: Not all DVS rate setting options (primarily the faster rate options) for the buck and LDO rails may be attainable in certain application configurations and conditions. DVS settings program a target for the rate of change of output voltage. The maximum rate of increase for the output voltage is limited by current limit, load current, and load capacitance. The maximum rate of decrease for the output voltage is limited by load current and load capacitance. The maximum and minimum rates of increase and decrease in the output voltage can be less than the DVS setting.

9.9 Real-Time Clock

The RTC is functionally the same as the Renesas ISL1208 RTC.

9.9.1 Clock

The RTC is a low-power real-time clock with timing and crystal compensation, clock/calendar, power fail indicator, periodic or polled alarm, intelligent battery backup switching, and battery-backed user SRAM. The oscillator uses either an external, low-cost 32.768kHz crystal or an external clock IC. The real-time clock tracks time with separate registers for hours, minutes, and seconds. The clock format can be set to either AM/PM or 24-hour. There are calendar registers for the date, month, year, and day of the week. The calendar is accurate until 2099, with automatic leap year correction.

The RTC clock/calendar portion is fully operational from 1.8V to 5.5V. See VCHG, VBAT, and VRTC for more details.

The accuracy of the real-time clock depends on the external 32.768KHz crystal or clock IC. The RAA215300 provides on-chip crystal compensation networks to adjust load capacitance to tune the crystal oscillator frequency. See Oscillator Frequency Accuracy for details.

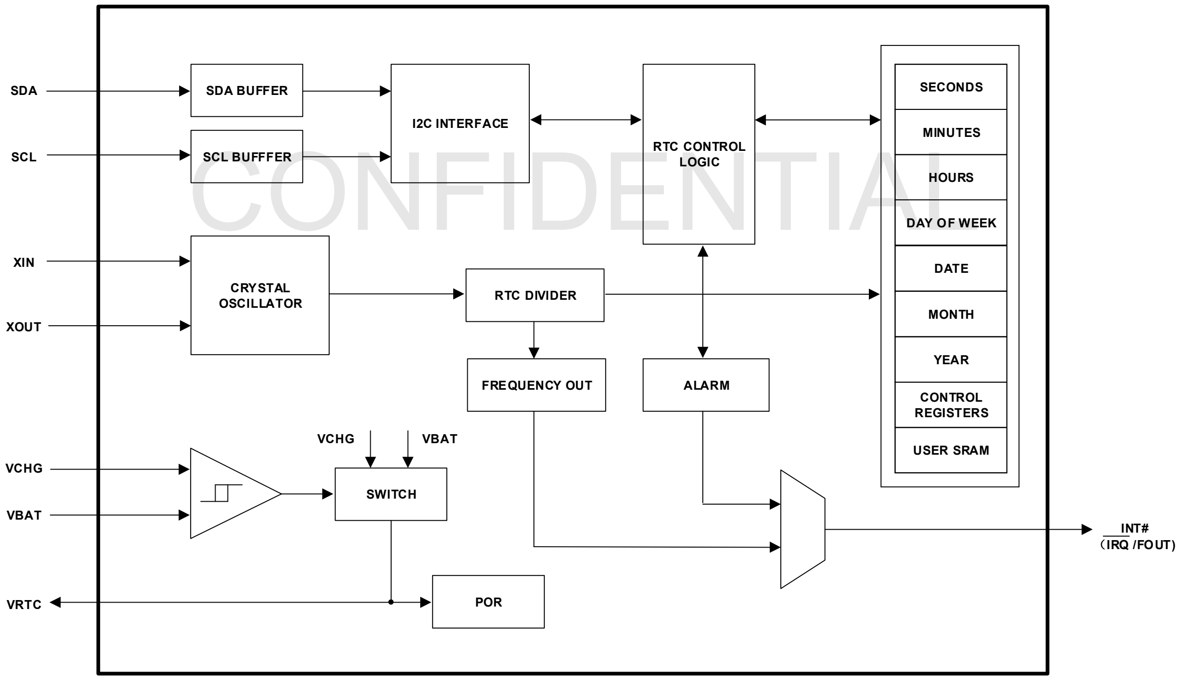


Figure 30. RTC Block Diagram

Note: To activate the RTC, the host must first set the RTC EN bit = 1 and the WRTC bit = 1. If using an external crystal, the XTOSCB bit needs to be set at 0 to enable the crystal oscillator. If using an external clock signal, set the XTOSCB bit as 1 to disable the crystal oscillator. Then, the date and time registers can be set accordingly, and the RTC is clocking and maintaining time. The clock does not increment until at least 1 byte is written to the clock/calendar registers.

INT# is a multi-functional output that can issue an interrupt or frequency signal. The function is selected by frequency out (FO) control bits. In interrupt mode, if an alarm condition occurs, the Interrupt Request (IRQ) is sent to the host processor. In Frequency Output (FOUT) mode, the output is a clock signal at a frequency generated from the crystal frequency.

The I²C interface is not functional if VIO_PGOOD is low. See VCHG, VBAT, and VRTC for more details.

9.9.2 Alarm

The flexible alarm of the RTC can be set to any clock/calendar value for a match. For example, every minute, every Tuesday, or at 5:23 AM on March 21. The alarm status is available by checking the Status Register, or the device can be configured to provide a hardware interrupt using INT#. A backup power input (VBAT) allows the device to be powered by a battery or supercapacitor with an automatic switchover between VCHG and VBAT.

The alarm compares the alarm registers with the RTC registers. As the RTC advances, the alarm is triggered when a match occurs. The alarm is enabled by the ALME bit. There are two alarm modes: single-event mode and periodic interrupt mode.

Single-event mode is enabled by setting the ALME bit to 1, the IM bit to 0, and the FO[3:0] bits to 0000. This mode detects a one-time match between the alarm registers and RTC registers. When this match occurs, the interrupt request ($\overline{IRQ}$) is sent to the host processor. The ALM bit is set to 1, and the INT# output is pulled low and remains low until the ALM bit is reset.

The periodic interrupt mode allows for repetitive or recurring alarm functionality. This mode is enabled by setting the ALME bit to 1, the IM bit to 1, and the FO[3:0] bits to 0000. There is an alarm each time there is a match of the alarm time and present time. Therefore, there is an alarm as often as every second (if only the nth second is set) or as infrequently as once a year (if at least the nth month is set). During Periodic Interrupt Mode, INT# is pulled low for 250ms, and the alarm status bit (ALM) is set to 1.

Note: The ALM bit can be reset by writing 0 to it or cleared by a valid read operation in the auto reset mode. The alarm function can be enabled/disabled during battery backup mode using the FOBATB bit.

9.9.3 Frequency Output

A clock signal related to the oscillator frequency can output from INT# or MPIO2.

FOUT from INT# is enabled by setting FO[3:0] bits to a non-zero value. The frequency is selected using the I²C bus. See Table 5.

Table 5. Frequency Selection of FOUT at INT#

FO3	FO2	FO1	FO0	FOUT from INT# (Hz)
0	0	0	0	0
0	0	0	1	32768
0	0	1	0	4096
0	0	1	1	1024
0	1	0	0	64
0	1	0	1	32
0	1	1	0	16
0	1	1	1	8
1	0	0	0	4
1	0	0	1	2
1	0	1	0	1
1	0	1	1	1/2
1	1	0	0	1/4
1	1	0	1	1/8
1	1	1	0	1/16
1	1	1	1	1/32

If enabled, a clock signal is outputted from MPIO2(see Table 6). For detailed information about MPIO2 frequency output, see 32kHz Clock (32K_CLK).

Table 6. Frequency Selection of Clock Signal at MPIO2

MPIO2 Power-Off Delay[2:0]	MPIO2 (Hz) - MPIO2 configured as 32K_CLK
000	32768
001	16384
010	8192
011	4096
100	2048
101	1024
110	512
111	256

9.9.4 General Purpose User SRAM

The RTC has 2 bytes of user SRAM, which continue to operate in battery backup mode. However, the I^2C bus is disabled if VCHG falls below the AVDD UVLO falling threshold.

9.9.5 Power Control Operation

There are two power supply inputs for the RTC circuit (VCHG and VBAT). The RAA215300 contains internal circuitry to automatically switch over to the backup battery when the main VCHG supply fails and switches back from the battery to VCHG when the main supply recovers. See VCHG, VBAT, and VRTC for details.

9.9.6 Power Failure Detection

The RAA215300 has a Real-Time Clock Failure (RTCF) bit to indicate total power failure. The RTCF bit is read-only and is set to 1 if the RTC has powered up after the failure of both VCHG and VBAT.

The bit is set regardless of whether VCHG or VBAT is applied first. At power-up after a total power failure, all registers are set to their default states, and the clock does not increment until at least 1 byte is written to the clock register. The first valid write to the RTC section resets the RTCF bit to 0.

9.9.7 Crystal Oscillator

A crystal can be used to generate the 32.768kHz clock and provide the time base for the RTC.

9.9.7.1 Oscillator Frequency Accuracy

The oscillator frequency accuracy primarily depends on the crystal accuracy and the match between the crystal and the load capacitance. If the load capacitance is too small or too large, the oscillator is too fast or too slow, respectively. RAA215300 provides an oscillator frequency adjustment mechanism that includes analog compensation in the RTC ATR register and digital compensation in the RTC DTR register. The combination of analog and digital trimming can give a maximum range of adjustment of -80ppm to +130ppm.

Note: Both of the frequency outputs on INT# and MPIO2 are affected by the setting in the RTC ATR register. The frequency on INT# is affected by the RTC DTR setting at all frequencies except the 32.768kHz setting. The frequency on MPIO2 is not affected by the RTC DTR setting.

9.9.7.2 Crystal Oscillator Frequency Trimming

The RAA215300 provides the option of timing correction of the crystal oscillator. Analog and digital compensation mechanisms are available as follows.

9.9.7.2.1 Analog Trimming with On-Chip Load Capacitance

The analog trimming register bits (ATR[5:0]) are used to trim oscillator frequency by selecting on-chip load capacitance. There are six bits for ATR, and the selectable range is from 4.5pF to 20.25pF. The available trim range of the oscillator frequency accuracy in ppm varies with crystals, operating temperature, and the stray capacitance of the PCB. As an example, the available PPM range for an ECX-.327-CDX-1293 crystal is -20ppm to 70ppm measured on the device evaluation board at 25°C.

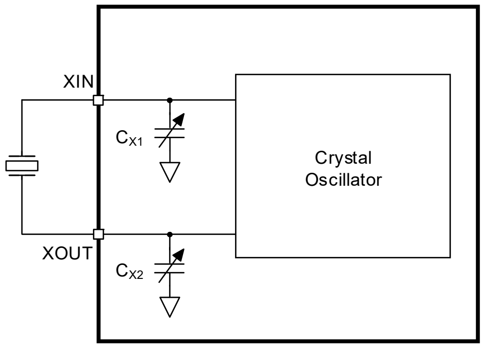


Figure 31. Diagram of On-Chip Load Capacitance

The on-chip load capacitance (C_{LOAD}) is the series combination of C_{X1} and C_{X2} shown in Figure 31. C_{X1} and C_{X2} range from 9pF to 40.5pF. The values of C_{X1} and C_{X2} are given in Equation 3:

(EQ. 3) $$C_X = (16 \cdot \overline{b5} + 8 \cdot b4 + 4 \cdot b3 + 2 \cdot b2 + 1 \cdot b1 + 0.5 \cdot b0 + 9)pF$$

The series load capacitance (C_{LOAD}) is derived by Equation 4:

(EQ. 4)

$$C_{LOAD} = \frac{1}{\left(\frac{1}{C_{X1}} + \frac{1}{C_{X2}}\right)}$$

$$C_{LOAD} = \left(\frac{16 \cdot \overline{b5} + 8 \cdot b4 + 4 \cdot b3 + 2 \cdot b2 + 1 \cdot b1 + 0.5 \cdot b0 + 9}{2}\right)pF$$

For example, C_{LOAD} = 12.5pF when ATR[5:0] = 00000, C_{LOAD} = 4.5pF when ATR[5:0] = 00000, and C_{LOAD} = 20.25pF when ATR[5:0] = 011111.

9.9.7.2.2 Battery Backup Mode Analog Trimming

The crystal oscillator frequency accuracy can change when the RTC is supplied by different power sources (VCHG or VBAT). The on-chip load capacitance offset between VCHG mode (VRTC supplied by VCHG) and battery backup mode (VRTC supplied by VBAT) is adjustable by BMATR[1:0]. The available range is from -0.5pF to 1pF.

9.9.7.2.3 Digital Trimming

The oscillator frequency is also affected by the digital trimming bits DTR[2:0] in the RTC DTR register. The DTR trim setting modifies the divider stage in the RTC digital block. The available trim range is from -60ppm to +60ppm. It is used for coarse adjustments of frequency drift over temperature or extending the adjustment range provided by the ATR settings.

9.9.7.2.4 Crystal Oscillator Frequency Adjustment

The Initial accuracy of the crystal oscillator can be adjusted by enabling the frequency output on INT# and monitoring it with a calibrated frequency counter. The gating time on the counter should be set long enough to ensure the accuracy of the reading. The ATR[5:0] bits can be set to 000000, to begin with. After the initial measurement is made, the RTC ATR register can be changed to tune the frequency. If the initial measurement shows the frequency is far off, then the DTR[2:0] can be used to do a coarse adjustment. Most crystal oscillators have tight enough accuracy at room temperature that the RTC ATR register adjustment should be all that is needed.

9.9.7.3 Temperature Compensation

The external crystal temperature drift is progressively worse as the crystal temperature deviates from +25°C. Figure 32 shows an example of temperature drift characteristics. There is a turnover temperature (T0) where the drift is near zero. The shape is parabolic because it varies with the square of the difference between the actual temperature and the turnover temperature.

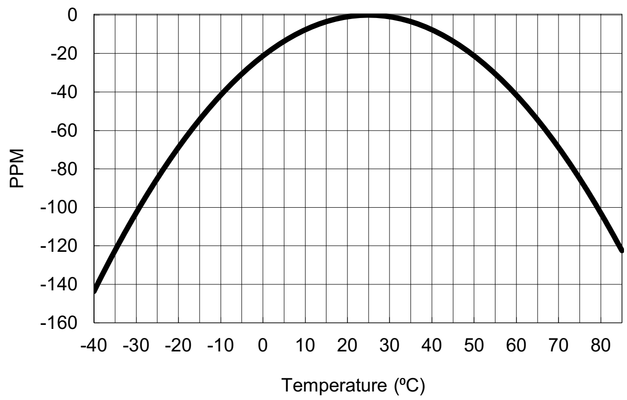


Figure 32. RTC Crystal Temperature Drift Example

A possible system to implement temperature compensation would consist of the RAA215300, a temperature sensor, and a microcontroller. These devices may already be in the system, so the function could just be a matter of implementing software and performing some calculations. Fairly accurate temperature compensation can be implemented just by using the crystal specifications for the turnover temperature T0 and the drift coefficient (β). Equation 5 is used to calculate the oscillator adjustment necessary,

(EQ. 5) $$\text{Adjustment(ppm)} = (T - T_0)^2 * \beta$$

When the temperature curve for a crystal is established, the designer should decide at what discrete temperatures the compensation changes.

A sample curve of the ATR[5:0] setting vs Frequency Adjustment for the RAA215300 and a typical RTC crystal is given in Figure 33. This curve may vary with different crystals and PCBs, so it is good practice to evaluate a given crystal in the RAA215300 circuit before establishing the adjustment values. The curve is then used to determine ATR[5:0] and DTR[2:0] settings. The results could be placed in a lookup table for the micro-controller to access.

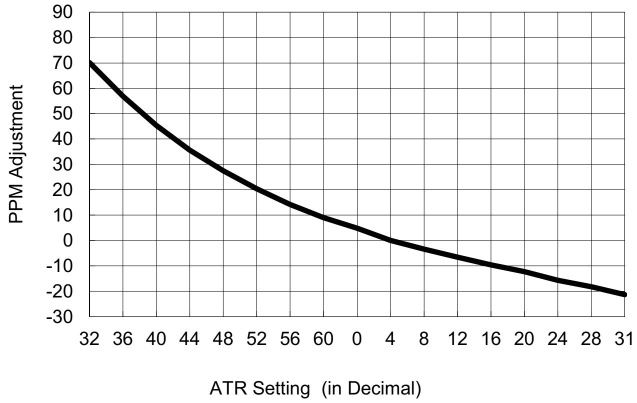


Figure 33. ATR Setting Vs. Crystal Oscillator Frequency Adjustment

9.9.8 Using an External Clock

The RTC can use either a standard 32.768kHz crystal or an external clock. XIN can be programmed for connection to an external clock input using the XTOSCB bit in the RTC SR register. When this bit is set to 1, the oscillator is disabled and XIN is a CMOS-compatible clock input.

The external clock input must be logic level CMOS (0.3 x VBAT LOW, 0.7 x VBAT HIGH), square wave preferred, frequency = 32.768KHz. The clock signal used for the XIN input must come from a source with the same voltage level as the VBAT of the RAA215300 device.

To check if the external clock is working properly, the following methods can be used to check the RTC function:

- Poll the time register to make sure the seconds are advancing at the correct rate.
- Enable the frequency on INT# or MPIO2: Clock and monitor the frequency for the correct value.

9.9.9 Real-Time Clock Registers

9.9.9.1 Clock and Calendar Registers [Address 0x00 to 0x06]

Time is set in BCD format by the following registers:

- RTC SC and RTC MN registers: Sets seconds and minutes that range from 0 to 59.
- RTC HR register: Sets hour that ranges from 0 to 23 or 1 to 12.
- RTC DT register: Sets date that ranges from 1 to 31.
- RTC MO register: Sets month that ranges from 1 to 12.
- RTC YR register: Sets year that ranges from 0 to 99.
- RTC DW register: Sets day of the week that ranges from 0 to 6.

See Register Map Detail for bits decoding.

A 12-hour or 24-hour format can be set by the MIL bit. If it is set to 1, the RTC uses a 24-hour format. If it is set to 0, the RTC uses a 12-hour format. In this case, the HR21 bit functions as an AM/PM indicator with 0 representing AM and 1 representing PM. The clock defaults to a 12-hour format time with HR21 = 0.

February 29 is added for leap years, which are defined as years that are divisible by 4. Years that are divisible by 100 are not considered leap years unless they are also divisible by 400. This means that the year 2000 is considered a leap year by the device, and the year 1900 is not.

9.9.9.2 Control and Status Registers [Address 0x07 to 0x0B]

9.9.9.2.1 RTC Status Register (RTC SR)

This is a volatile register that sets RTC functions and reports status. The following sections detail each bit.

Real-Time Clock Fail Bit (RTCF)

This read-only bit is set to 1 by the device after a power failure where both VCHG and VBAT lose power. After a power failure, all registers are set to their default states when the device powers up again. The host must reactivate the RTC. The first valid write operation to the RTC registers after a power failure resets the RTCF bit to 0.

Battery Bit (BAT)

This bit is set to 1 by the device when the RTC enters battery backup mode. When VCHG is valid again, this bit can be reset either by the host (by writing 0 to it) or automatically reset if ARST = 1.

Alarm Bit (ALM)

This bit is set to 1 if the alarm matches the real-time clock. It can be reset to 0 by the host (by writing 0 to it) or automatically reset if ARST = 1. Writing 1 to this bit is not accepted.

If the ALM bit is set during an RTC SR register reading operation, it remains set after the reading operation is complete.

Write RTC Enable Bit (WRTC)

The WRTC bit enables or disables writing capability into the RTC clock and calendar registers. The factory default setting of this bit is 0. On initialization or power-up, the WRTC bit must be set to 1 to enable the RTC. At the completion of a valid write command (STOP), the RTC starts to count. The RTC internal 1Hz signal is synchronized to the STOP condition during a valid write cycle.

Crystal Oscillator Enable Bit (XTOSCB)

This bit enables/disables the internal crystal oscillator. When XTOSCB is set to 1, the oscillator is disabled, and XIN allows for an external 32.768kHz clock signal to drive the RTC. The XTOSCB bit is set to 0 on power-up.

Auto Reset Enable Bit (ARST)

This bit enables/disables the automatic reset of the BAT and ALM status bits only. When the ARST bit is set to 1, these status bits are automatically reset to 0 after a valid read operation of the respective status register (with a valid STOP condition). When ARST is set to 0, the host must reset the BAT and ALM bits.

9.9.9.2.2 RTC Interrupt Control Register (RTC INT)

This register can be used to control the frequency output and alarm function.

Frequency Out Control Bits (FO[3:0])

These bits enable/disable the Frequency Output function (FOUT) and select the output frequency at INT#. The selectable frequency is listed in Table 5. When the frequency mode is enabled, it overrides the alarm mode at INT#.

Frequency Output and Interrupt Bit (FOBATB)

This bit enables/disables the $\overline{IRQ}$/FOUT function during battery backup mode (that is, VBAT power source active). When FOBATB is set to 0, both the Frequency Output and alarm output functions are disabled. When FOBATB is set to 1, the $\overline{IRQ}$/FOUT function is enabled during battery backup mode.

Oscillator Bias Current Control Bit (LPMODE)

With LPMODE = 0, the device works with a normal oscillator bias current. With LPMODE = 1, the device works with a reduced oscillator bias current. Renesas does not recommend setting this bit to 1.

Alarm Enable Bit (ALME)

This bit enables/disables the alarm function. When the ALME bit is set to 1, the alarm function is enabled. When ALME is set to 0, the alarm function is disabled. The alarm function can operate in either single-event mode or periodic interrupt mode. See Alarm for more details.

Note: When the frequency output mode is enabled, the alarm function is disabled.

Interrupt/Alarm Mode Bit (IM)

This bit is used to select single-event mode or periodic interrupt mode. See Alarm for more details.

9.9.9.2.3 Trimming Registers RTC ATR and RTC DTR

Analog Trimming (ATR[5:0])

ATR[5:0] bits are used to trim the oscillator frequency by adjusting the on-chip load capacitance value. The on-chip load capacitance value ranges from 4.5pF to 20.25pF in 0.25pF steps. See Analog Trimming with On-Chip Load Capacitance for more details.

Battery Mode ATR Selection (BMATR [1:0])

BMATR[1:0] bits are used to set the on-chip capacitance offset between VCHG mode and battery backup mode. See Battery Backup Mode Analog Trimming for more details.

Digital Trimming (DTR [2:0])

DTR[2:0] bits are used to trim the oscillator frequency by modifying the digital stage in RTC. See Digital Trimming for more details.

9.9.9.3 Alarm Registers Addresses [0x0C to 0x11]

The alarm register bytes are mapped identical to the RTC register bytes, except that the MSB of each byte functions as an enable bit (1 means enabled). These enable bits specify which alarm registers are used to make the comparison. *Note:* There is no alarm byte for year.

The followings are examples of using single-event mode and periodic Interrupt mode.

Example 1 – Alarm set to single-event mode (IM = 0)

A single-event alarm occurs on January 1 at 11:30 am.

Table 7. Register Settings in Example 1

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value	Description
RTC SCA	0	0	0	0	0	0	0	0	0×00	Seconds disabled
RTC MNA	1	0	1	1	0	0	0	0	0×B0	Minutes set to 30, enabled
RTC HRA	1	0	0	1	0	0	0	1	0×91	Hours set to 11, enabled
RTC DTA	1	0	0	0	0	0	0	1	0×81	Date set to 1, enabled
RTC MOA	1	0	0	0	0	0	0	1	0×81	Month set to 1, enabled
RTC DWA	0	0	0	0	0	0	0	0	0×00	Day of week disabled
RTC INT	0	1	X[1]	X[1]	0	0	0	0	0×X0	Enable single-event mode

1. X can be set to either 0 or 1 depending on the application.

After these registers are set, an alarm is generated when the RTC advances to exactly 11:30 am on January 1 (after seconds change from 59 to 00) by setting the ALM bit in the status register to 1 and also pulling the INT# output low.

Example 2 – Alarm set to periodic interrupt mode (IM = 1)

An interrupt occurs every minute when the value of the RTC SC register is at 30 seconds.

Table 8. Register Settings in Example 2

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value	Description
RTC SCA	1	0	1	1	0	0	0	0	0×B0	Seconds set to 30, enabled
RTC MNA	0	0	0	0	0	0	0	0	0×00	Minutes disabled
RTC HRA	0	0	0	0	0	0	0	0	0×00	Hours disabled
RTC DTA	0	0	0	0	0	0	0	0	0×00	Date disabled
RTC MOA	0	0	0	0	0	0	0	0	0×00	Month disabled
RTC DWA	0	0	0	0	0	0	0	0	0×00	Day of week disabled
RTC INT	1	1	X[1]	X[1]	0	0	0	0	0×X0	Enable periodic interrupt mode

1. X can be set to either 0 or 1 depending on the application.

When the registers are set, the following waveform is seen at INT#. The status register ALM bit is set each time the alarm is triggered and is cleared automatically.

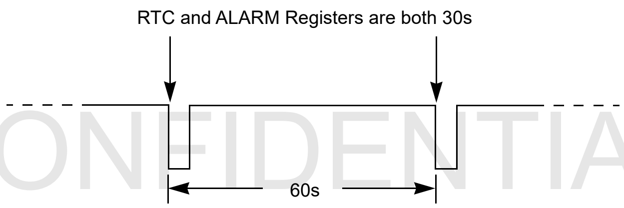


Figure 34. Periodic Interrupt Alarm Signal

9.10 Coin Cell Battery Charger

RAA215300 features a constant current charger to charge an external backup energy storage device to maintain power to the RTC when the VCHG supply falls. A typical energy storage device is a coin cell battery or supercapacitor connected to VBAT. The charger charges the external storage device when VCHG is higher than VBAT.

The charger is always off by default (after power-on or device reset) and must be enabled by I^2C.

The charger supports selectable 20µA or 60µA (typical) charge currents. If the charger is enabled and VCHG is higher than VBAT, the charge current is supplied through VBAT. The charging termination voltage is selectable by I^2C from 1.8V~3.3V in 100mV steps.

The device does not automatically re-enable the charger when the voltage on the external storage device falls. The host should monitor the PGOODCCBAT fault bits (poll the register using I^2C) to decide if and when the charger needs to be re-enabled to charge up the external storage device.

The battery sense comparator is disabled by default, and the PGOODCCBAT live bit stays at 0. The sense comparator is automatically enabled when the charger is enabled. The host can check the battery status by trying to enable the charger (writing 1 to CC Charger EN bit) every certain period of time (depending on the battery backup time), and the following occurs when the device receives the command:

- If VBAT voltage is above or at the target level (charging termination voltage), the charger is not turned on and CC Charger EN bit remains at 0.

- If VBAT voltage falls below the target level, the comparator and charger are enabled. The PGOODCCBAT live and latched bits are set. INT# is asserted if not masked.

The PGOODCCBAT latched bit can be cleared by writing 1 to it. This bit is edge sensitive. When cleared, it does not set until the next time VBAT falls below the target level. When VBAT reaches the target level, the charger and comparator are automatically disabled, and the PGOODCCBAT live bit is cleared, indicating VBAT PGOOD was attained.

9.10.1 Supercapacitor Backup Time

The supercapacitor backup time is calculated using Equation 6 where C_{BAT} is the capacitance value of the supercapacitor, V_{BAT1} is the battery voltage level when it is fully charged, V_{BAT2} is the voltage level when the battery needs to recharge, and I_{BAT} is the supply current drawn from the supercapacitor.

(EQ. 6) $$T_{Backup}(seconds) = C_{BAT} \times \frac{V_{BAT1} - V_{BAT2}}{I_{BAT}}$$

For example, if C_{BAT} = 0.1F, V_{BAT1} = 3.3V, V_{BAT2} = 1.8V, and I_{BAT} = 5µA when RTC is clocking, the battery backup time is 30000 seconds which equals 8.33 hours, which means that the host needs to check the battery status every 8 hours.

Charging time is calculated using Equation 7 where I_{Charge} is the charge current set in the register.

(EQ. 7) $$T_{Charge}(seconds) = C_{BAT} \times \frac{V_{BAT1} - V_{BAT2}}{I_{Charge} - I_{BAT}}$$

In the previous example, if I_{Charge} = 60µA, the charge time is 2727 seconds which equals 0.76 hours.

9.11 Buck Regulators

The RAA215300 has six synchronous buck regulators. Internal compensation is employed to simplify application design, reduce PCB space, and reduce the BOM cost. Each buck regulator has its own programmable output range, soft-start, power-up/down timing, switching frequency, and can be individually disabled by the register and EEPROM settings. Some of the buck regulators are optimized to support various DDR memory specifications but can also be used for general purposes. The buck regulators have various output voltage ranges and current ratings, allowing the system to be flexibly designed for improved performance, such as efficiency and voltage ripple. The buck regulators can be automatically reconfigured (by register settings) between {ACTIVE} and {SLEEP} for different applications or different power requirements.

The buck regulators have two operating modes: Auto PFM/PWM and FPWM. Each buck regulator can be set to the ultrasonic mode when operating in PFM (see Ultrasonic Mode) and can use a spread spectrum feature (see Spread Spectrum). A synchronous phase delay feature allows the switching of each buck regulator to be shifted in phase relative to the internal clock, which may improve EMC.

The buck regulators support Dynamic Voltage Scaling (DVS) with programmable ramp-up/down rates (see DVS), and offer various active discharge options (see Output Discharge). Various warnings and faults are monitored and reported (see Device Monitors, Warnings, and Protections).

Note: All buck supplies (BUCKx_VINx) = AVDD = VCHG.

9.11.1 Buck1

Buck1 supports the processor or SoC core power. It provides high efficiency, fast load transient response, and low ripple voltage. It can provide up to 5A. The output voltage can be set to 1.03V, and from 0.8V to 1.5Vin 50mV steps. *Note:* The switching frequency should be reduced when using outputs 1.03V and lower.

Buck1 supports high-current warning interrupt if the output current exceeds the programmable Buck1 High Current Threshold. It can be used as an early indicator for system thermal control. It is particularly helpful during the system design phase.

Buck1 configuration details are in registers 0x20 to 0x26.

9.11.2 Buck2

Buck2 supports DDR memory VDDQ rail. It can provide up to 1.5A. The output voltage can be set from 1.1V to 1.85V, in 50mV steps. If Buck2 powers DDR memory and VTT is required, connect VREFIN to the Buck2 output rail externally.

Buck2 configuration details are in registers 0x27 to 0x2D.

9.11.3 Buck3

Buck3 can provide up to 1.5A. The output voltage can be set from 1.8V to 3.3V, in 100mV steps. It can be used to power 1.8V or 3.3V I/O or other loads.

Buck3 configuration details are in registers 0x2E to 0x34.

9.11.4 Buck4

Buck4 can provide up to 3.5A. The output voltage can be set to 0.8V, 0.85V, 0.9V, 0.95V, 1.0V, 1.05V, 1.1V, 1.15V, 1.2V, 1.5V, 1.6V, 1.8V, 1.85V, 2.2V, 2.5V, or 3.3V. It can be used to power 1.8V or 3.3V I/O or other general loads. *Note:* Reduce the switching frequency when using outputs 1.6V and lower.

Buck4 configuration details are in registers 0x35 to 0x3B.

9.11.5 Buck5

Buck5 is a regulator for system peripherals such as WiFi or Ethernet. It can provide up to 0.6A. The output voltage can be set to 1.2V, 1.5V, 1.6V, 1.8V, 1.85V, 2.2V, 2.5V, or 3.3V. It can support up to 0.6A for outputs lower than 2.5V. When the set output voltage is 2.5V or 3.3V, the maximum load current capability derates.

Buck5 configuration details are in registers 0x3C to 0x42.

9.11.6 Buck6

Buck6 supports DDR VTT, which is required to sink (receive) and source (supply) currents up to ±1A. When the VTTREF EN bit = 1, Buck6 is configured for the DDR VTT application (VTT mode). The output voltage tracks the VREFIN input and the output voltage is fixed at VREFIN/2. The power-up/down sequence tracks the VREFIN per DDR memory specification. *Note:* Sink and source currents derate when the output voltage is 0.7V and higher. Also, sink currents and/or maximum input voltage derate when the output voltage is 0.575V or lower.

Buck6 configuration details are in registers 0x43 to 0x49.

9.11.7 Buck Operating Modes

The operating mode (Auto PFM/PWM and FPWM) is set by the Buckx_ACTIVE and Buckx_SLEEP registers.

In Auto PFM/PWM mode, the buck regulator transitions between PFM and PWM modes depending on load current. At light load, it enters PFM to reduce power consumption. As load current increases, the regulator transitions to PWM. PFM mode produces higher output voltage ripple than PWM mode. FPWM produces the lowest output voltage ripple at light load but it increases quiescent current.

FPWM mode makes the regulator operate at a fixed switching frequency, as programmed in EEPROM, irrespective of the load current. At light load, there is a negative inductor current (the current flows from output capacitance, through the inductor and low-side switch).

All bucks soft-start in PFM/PWM mode, irrespective of the mode setting. After soft-start completion, if selected, the device transitions to FPWM 300µs. The regulator is unable to create a negative inductor current until FPWM mode is established.

9.11.8 Ultrasonic Mode

Ultrasonic mode is an optional feature (set in EEPROM) of each buck regulator. Its purpose is to prevent PFM switching frequency from being within the audio frequency band.

9.11.9 Unused Buck

If a buck regulator is not required in a given application, configure that unused buck as follows:

- BUCKx_VINx = Always connect to the same supply as AVDD
- BUCKx_LXx = Open
- BUCKx_FB = GND
- Disable the BUCKx block in EEPROM by both Buckx_EN_ACTIVE and Buckx_EN_SLEEP bits.

A UV fault is triggered at startup if a buck regulator is enabled in the register settings but configured as unused on the board. The fault protection function is configured in the default settings to shut down all the outputs when a UV fault is detected. To avoid shutdown, disable the unused bucks in the EEPROM settings or before asserting PWRON.

When VTTREF_EN = Enabled and the register bit Link_Buck6_to_Buck2 is set to 1, Buck6 and Buck2 start up and shut down simultaneously, and settings of the following register bits are ignored: Buck6_EN_ACTIVE, Buck6_EN_SLEEP, Buck6_Power_On_Delay, and Buck6 Power_Off_Delay. When Link_Buck6_to_Buck2 is set to 0, sequencing of Buck6 and Buck2 is independent.

If VTTREF_EN = Enabled and Buck6 is unused, Link_Buck6_to_Buck2 must be set to 0.

9.11.10 Switching Frequency

The PWM switching frequency (f_{SW}) for each buck is programmable. Changing this setting on the fly using I^2C is not recommended. It is preferred to change the frequency only when the output is disabled, or before PWRON assertion. See the Register Map for the available options for each regulator and default selections.

At the load where control changes from PFM to PWM, the switching frequency is not as high as its setting. As load increases, the switching frequency increases. The setting is a maximum.

9.11.11 Spread Spectrum

To improve EMC, spread spectrum operation is optional in each buck regulator. The switching frequency is modulated to reduce peak noise power.

9.11.11.1 PFM mode

The switching frequency depends on load current and peak switch current limit. A 10-bit pseudo-random pattern is applied to the peak switch current limit code to modulate the PFM switching frequency. The PFM spread spectrum modulation rate is adjusted using the 2-bit code Buck#_PFM_AM[1:0].

Each buck regulator has a bit to enable/disable PFM spread spectrum operation.

9.11.11.2 PWM Mode

There are two spread spectrum modulation schemes in PWM mode: pseudo-random and triangular, set by the SS_PWM_Mod bit. The 2-bit code PWM_AM[1:0] sets the amplitude of modulation. The PWM_AM bits can also be set to disable the PWM spread spectrum. The selected modulation scheme and modulation amplitude are applied to all buck regulators.

The pseudo-random scheme is implemented similarly to PFM spread spectrum modulation, but instead of modulating PFM current limit it directly modulates switching frequency. The modulation frequency is set by the 2-bit code Freq_SS[1:0]. The modulation rate is adjusted using the 2-bit code PWM_AM[1:0].

When the triangular modulation profile is selected, the PWM switching frequency is the center frequency (f_{CENTER}). A maximum frequency (f_{MAX}) and minimum frequency (f_{MIN}) are adjusted by the modulation amplitude 2-bit code PWM_AM[1:0]. The modulation frequency (f_{MOD}) is set by the 2-bit code Freq_SS[1:0].

9.11.12 Phase Synchronization

The phase relationships between the starts of switching cycles of different buck regulators can be programmed. The programmed switching frequencies of synchronized buck regulators must be the same, double, or half. When programmed, synchronization occurs when the buck regulators are running at the full switching frequency, which occurs at all loads in FPWM mode and at moderate to high load in Auto PFM/PWM mode. Phase synchronization can be used to improve EMC.

9.12 LDO Regulators

The RAA215300 has three LDO regulators, each with programmable output voltage, soft-start timing, and power on/off delay. Each can be disabled by the register and EEPROM settings. The LDOs support various DDR memory specifications, but can also be used for general purposes. The LDOs can be reconfigured by programmed settings during transitions between {ACTIVE} and {SLEEP}. In {ACTIVE}, hardware inputs (see LDOx Selection Inputs) can change the output voltages of LDO1 and LDO2 at rates determined by DVS settings and limitations caused by current limit, load current, and load capacitance.

DVS settings program a target for the rate of change of output voltage. The maximum rate of increase of output voltage is limited by current limit, load current, and load capacitance.

The maximum rate of decrease of output voltage during DVS is limited by load current and load capacitance.

The maximum rates of increase and decrease in the output voltage can be less than the DVS setting.

The LDO regulators offer various active discharge options (see Output Discharge) at power-off. Various types of LDO regulator faults are monitored and reported, see Device Monitors, Warnings, and Protections.

The maximum rate of decrease of output voltage during a shutdown is limited by load current, load capacitance, and active discharge setting.

9.12.1 LDO1/2

LDO1 and LDO2 use the same design. The output voltages can be set to 0.8V, 0.9V, 1.2V, 1.5V, 1.8V, 2.5V, 3.0V, and 3.3V. The output voltages for {ACTIVE} and {SLEEP} are separately programmable. These LDOs support SD card interface applications.

- LDO1 configuration details are in registers 0x4A to 0x4E.
- LDO2 configuration details are in registers 0x4F to 0x53.

9.12.1.1 LDOx Selection Inputs

The LDO_SELx inputs can be used to change the output voltages while in {ACTIVE}. For example, this can be useful when the LDOs power an SD card interface.

- When LDO_SELx = HIGH, the LDOx_Vo_1_ACTIVE setting is selected.
- When LDO_SELx = LOW, the LDOx_Vo_0_ACTIVE setting is selected.

LDO_SELx inputs are ignored during {SLEEP}, when powering on, or during transitions from {STANDBY} to {ACTIVE}.

9.12.2 LDO3

LDO3 output voltage can be set to 0.8V, 0.9V, 1.2V, 1.5V, 1.8V, 2.5V, 3.0V, and 3.3V. The output voltages for {ACTIVE} and {SLEEP} are separately programmable. LDO3 can provide power for the DDR memory VPP rail.

9.12.3 LDOx Bypass

Each LDO can be set in bypass mode where the input and output are internally connected through the enhanced pass MOSFET.

The LDO cannot be switched in or out of bypass mode between {ACTIVE} and {SLEEP}.

9.12.4 Unused LDOx

If an LDO regulator is not required in a given application, configure that unused LDO as follows:

- LDOx_VIN = GND
- LDOx_OUT = GND
- LDO_SEL1 = GND if LDO1 is not used
- LDO_SEL2 = GND if LDO2 is not used
- Disable the LDOx block in EEPROM by both LDOx_EN_ACTIVE and LDOx_EN_SLEEP bits.

A UV fault is triggered at startup if an LDO is enabled in the register settings but configured as unused on the board. The fault protection function is configured in the default settings to shut down all the outputs when a UV fault is detected. To avoid shutdown, disable the unused LDOs in the EEPROM settings or before asserting PWRON.

9.13 VTTREF

The VTTREF block provides the VTT reference voltage in DDR applications. VREFOUT = VREFIN/2.

In DDR applications, VREFIN is connected to the VDDQ rail, which is typically generated by Buck2.

When Buck6 is set to VTT mode, Buck6 output provides an active tracking termination voltage (VTT) equal to VREFOUT.

If VTTREF_EN = Enabled, VTTREF is enabled when Buck2 starts up and is disabled when Buck2 shuts down. VREFIN (the input to VTTREF) can be connected to the output of any of the regulators, or to any voltage source. VREFIN UVLO detection is active only after Buck2 completes soft-start and before Buck2 starts power-down.

When VREFIN UVLO is active, UVLO latched fault and live fault bits are set and all outputs shut down if VREFIN is less than its falling UVLO threshold for longer than the VREFIN UVLO Falling Delay period. See VREFIN UVLO.

VTTREF is enabled and disabled simultaneously with Buck2. Therefore, Buck6 must not start up earlier than Buck2 and must not shut down later than Buck2. During startup, VREFIN must be greater than two times the Buck6 output voltage, or Buck6 OV could be triggered. Many things affect the rise times. In FPWM, constraints of minimum on-time and switching frequency can make Buck6 output voltage rise quickly. Therefore, it is necessary to make VREFIN establish quickly or before Buck6. During shutdown, the voltage source connected to VREFIN cannot shut down earlier than Buck6, or Buck6 OV could be triggered.

9.13.1 Unused VTTREF

If VTTREF is not going to be configured for use as a reference for Buck6, configure the schematic and board design as follows:

- VREFIN = GND
- VREFOUT = GND
- Disable the VTTREF block in EEPROM.

9.14 Pre-bias Startup

In some use cases, the output capacitor/load of the regulator may have residual charge and therefore a non-zero output voltage when the device is (re)started (that is, pre-biased). The RAA215300 supports pre-biased start-up.

9.15 Device Monitors, Warnings, and Protections

The RAA215300 has various monitors, warnings, and fault protection features.

If a fault is detected during normal operation, both a latched (sticky) and a live fault status bit are set. INT# is asserted if the fault interrupt is supported and not masked out. Certain fault events can be configured to shut down all rails (enter {FAULT_OUT}), or to keep all rails operating (do not enter {FAULT_OUT}). A latched fault bit remains set until cleared by the host writing a 1 to the latched register bit after the event has subsided. The live status bits show the real-time condition and are used to indicate if the fault has subsided or persists. For more information see Interrupt and Fault and Status Monitoring.

If a fault event shuts down the RAA215300 power rails, all the reset outputs are asserted and the output rails are powered down following the power-off sequence.

9.15.1 Input Voltage Monitor (AVDD Undervoltage Power Down)

To help prevent uncontrolled power-down due to input power loss, an AVDD voltage monitor option is included to provide the host an early warning. It is also called the AVDD Undervoltage Power Down (UVPD) feature, which has a programmable threshold and can be enabled/disabled in the EEPROM. When the programmed threshold is reached, after a delay the AVDD_UVPD_Latched and AVDD_UVPD_Live status bits are set and, if not masked, INT# is asserted. The device powers down according to the power-down sequence and then enters {FAULT_OUT}. At power-on, the device remains in {STANDBY} until AVDD exceeds the UVPD setting if the AVDD UVPD feature is enabled, and stays in this state indefinitely if AVDD remains below its UVPD setting.

The threshold options are:

- 4.25V (for 5V systems)
- 3.0V (for Li-Ion battery systems)
- 2.7V (for 3V systems)

9.15.2 AVDD UVLO

The AVDD input supply has UVLO protection. This checks the power supply is valid for normal operation. See the Electrical Specifications for detailed specifications. When AVDD is below its UVLO falling threshold, the device enters {RESET}. See Operating {States} and Transition Conditions for more details.

9.15.3 VREFIN UVLO

The VREFIN input has UVLO protection. When VREFIN is below its UVLO falling threshold, after a delay the VREFIN_UVLO_Latched and VREFIN_UVLO_Live fault bits are set and, if not masked, INT# is asserted. The device powers down according to the power-down sequence if it is configured to shut down all the rails by the VREFIN_UVLO_Disable bit and then enters {FAULT_OUT}.

Note: The device can be configured to either shut down all the rails or not shut down any rails by register bit VREFIN_UVLO_Disable. If the device is configured to not shut down any rails, the fault cannot be cleared until VREFIN exceeds its UVLO rising threshold. If the device is configured to shut down all the rails, the fault cannot be cleared until the power-off sequence completes.

The VREFIN UVLO Falling Delay timer is enabled after Buck2 finishes soft-start and before Buck2 starts shutdown.

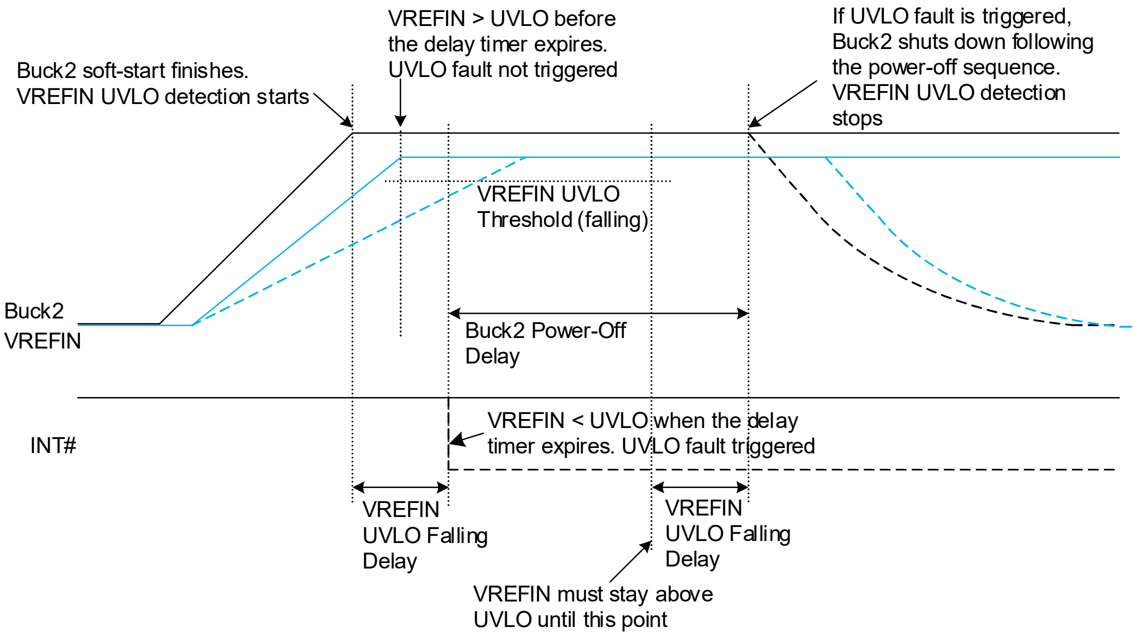


Figure 35. VREFIN UVLO Fault Detection at Power-On

9.15.4 Over-Temperature Warning and Protection

The RAA215300 continuously monitors its die temperature and responds at two thresholds. The lower threshold provides a warning that the temperature is near but less than the higher protection threshold.

The thermal warning threshold is programmable. When the warning threshold is reached, a latched fault flag and live status bit are set and if not masked, it asserts INT#. When the thermal shutdown threshold is reached, a latched fault flag and live status bit are set, INT# is asserted (if not masked), and the device powers down following the power-off sequence and it enters {FAULT_OUT}.

Note: OTP_WARN_Latched fault is edge triggered, that is, when the latched fault is cleared, it is only set again when the live fault goes LOW to HIGH. OTP_Latched fault is level triggered, that is, when the latched fault is cleared, it is set again if the live fault is high.

9.15.5 High Current Warning

Buck1 features a high-current warning with a programmable threshold. This can be used by the system, possibly in conjunction with the over-temperature warning, to moderate processor activity to avoid high-temperature operation. When Buck1 output current is higher than the threshold set in Buck1_High_Current_Threshold register bits, the Buck1_HC_Latched and Buck1_HC_Live bits are set, and INT# is asserted (if not masked). The device remains operating in this condition.

9.15.6 Overvoltage and Undervoltage Protection

All buck regulators have undervoltage (UV) and overvoltage (OV) fault protection. The LDOs have UV protection. PMIC response to a fault is configurable and can include assertion of INT#. When UV or OV protection threshold is reached, a latched fault flag and live status bit are set, and INT# is asserted (if not masked). If the UV_Disable or OV_Disable bit of the regulator is configured to shut down all the rails, the device powers down following the power-off sequence and enters {FAULT_OUT}. If it is configured to not shut down any rails, the device remains operating.

Note: The LDOx live status bits are PGOOD live status, and they are monitored when the related LDO is enabled and disabled. The LDOx latched status bits are UV latched status and are only monitored when the related LDO is enabled. Similarly, the BUCKx UV and OV status are only monitored when the related buck regulator is enabled. The INT# status depends on the latched fault status.

9.15.7 Interrupt

The RAA215300 has an interrupt (INT#) pin, which is an open-drain, active low output that can notify the system/host of a PMIC fault or alarm condition. Each latched fault can be configured to be unmasked or masked with respect to INT#. Unmasked faults assert INT#; masked faults do not. *Note:* The host can read latched and live faults from the status registers.

It is the responsibility of the host to de-assert/release INT# by clearing the latched fault bit(s). If INT# is not de-asserted, it is unable to notify the host of further qualifying events.

9.15.8 Fault and Status Monitoring

The RAA215300 supports numerous interrupt qualifying events and numerous status flags. Different fault events may have associated latched flags, live flags, and the ability to assert the INT# and power down all outputs (enter {FAULT_OUT}).

Note: Latched and live fault bits can be polled by the host at any time to check status. A latched fault sets the related flag to 1, and this remains until cleared by the host. The fault is re-triggered if the fault condition persists.

See Table 9 for a summary of all fault and status flags, see the Register Map for all details of the bits summarized.

Table 9. Fault and Status Flags: Behavior and Partitioning

Fault Register Partitioning	Fault/Status Name	Live Bit Status	Latched Bit Status	INT# Mask Option	Fault Response Option	Deglitch Time (ms)	Notes
Fault 1	Buck6 UV	Yes	Yes	Yes	Yes	1	
	Buck5 UV	Yes	Yes	Yes	Yes	1	
	Buck4 UV	Yes	Yes	Yes	Yes	1	
	Buck3 UV	Yes	Yes	Yes	Yes	1	
	Buck2 UV	Yes	Yes	Yes	Yes	1	
	Buck1 UV	Yes	Yes	Yes	Yes	1	
Fault 2	VIO_PGOOD	Yes	Yes	Yes	No	1	
	LDO3 UV	Yes	Yes	Yes	Yes	1	
	LDO2 UV	Yes	Yes	Yes	Yes	1	
	LDO1 UV	Yes	Yes	Yes	Yes	1	
Fault 3	Buck6 OV	Yes	Yes	Yes	Yes	1	
	Buck5 OV	Yes	Yes	Yes	Yes	1	
	Buck4 OV	Yes	Yes	Yes	Yes	1	
	Buck3 OV	Yes	Yes	Yes	Yes	1	
	Buck2 OV	Yes	Yes	Yes	Yes	1	
	Buck1 OV	Yes	Yes	Yes	Yes	1	
Fault 4	Buck1_HC	Yes	Yes	Yes	No	0.1	
Fault 5	NVM Read	No	Yes	No	No	-	Ok/good when bit = 1

Table 9. Fault and Status Flags: Behavior and Partitioning (Cont.)

Fault Register Partitioning	Fault/Status Name	Live Bit Status	Latched Bit Status	INT# Mask Option	Fault Response Option	Deglitch Time (ms)	Notes
Fault 6	PGOODCCBAT	Yes	Yes	Yes	No	0.1	
	VREFIN UVLO	Yes	Yes	Yes	Yes	1	Only monitored after Buck2 (VDDQ) rail soft-start is completed.
	AVDD UVPD	Yes	Yes	Yes	No	0.1	
	NVM_Error	No	Yes	Yes	No	-	
	CRST Triggered	Yes	Yes	Yes	No	-	
	WDT Error	Yes	Yes	Yes	No	-	
	OTP	Yes	Yes	Yes	No	-	
	OTP Warn	Yes	Yes	Yes	No	-	
ECC Detail 1	EE Bank 7 ECC Corrected	No	Yes	No	No	-	Clear latched flag by writing 1 to the bit location
	EE Bank 6 ECC Corrected	No	Yes	No	No	-	Clear latched flag by writing 1 to the bit location
	EE Bank 5 ECC Corrected	No	Yes	No	No	-	Clear latched flag by writing 1 to the bit location
	EE Bank 4 ECC Corrected	No	Yes	No	No	-	Clear latched flag by writing 1 to the bit location
	EE Bank 3 ECC Corrected	No	Yes	No	No	-	Clear latched flag by writing 1 to the bit location
	EE Bank 2 ECC Corrected	No	Yes	No	No	-	Clear latched flag by writing 1 to the bit location
	EE Bank 1 ECC Corrected	No	Yes	No	No	-	Clear latched flag by writing 1 to the bit location
	EE Bank 0 ECC Corrected	No	Yes	No	No	-	Clear latched flag by writing 1 to the bit location
ECC Detail 2	EE Bank 7 ECC Error	No	Yes	No	No	-	Clear latched flag by writing 1 to the bit location
	EE Bank 6 ECC Error	No	Yes	No	No	-	Clear latched flag by writing 1 to the bit location
	EE Bank 5 ECC Error	No	Yes	No	No	-	Clear latched flag by writing 1 to the bit location
	EE Bank 4 ECC Error	No	Yes	No	No	-	Clear latched flag by writing 1 to the bit location
	EE Bank 3ECC Error	No	Yes	No	No	-	Clear latched flag by writing 1 to the bit location
	EE Bank 2 ECC Error	No	Yes	No	No	-	Clear latched flag by writing 1 to the bit location
	EE Bank 1 ECC Error	No	Yes	No	No	-	Clear latched flag by writing 1 to the bit location
	EE Bank 0 ECC Error	No	Yes	No	No	-	Clear latched flag by writing 1 to the bit location

Table 9. Fault and Status Flags: Behavior and Partitioning (Cont.)

Fault Register Partitioning	Fault/Status Name	Live Bit Status	Latched Bit Status	INT# Mask Option	Fault Response Option	Deglitch Time (ms)	Notes
EE Detail	Valid EE Data	No	Yes	No	No	-	Clear latched flag by writing 1 to the bit location
	EE Error Latched	No	Yes	No	No	-	Clear latched flag by writing 1 to the bit location

9.16 Maximum Recommended Power Dissipation

The maximum power dissipation recommended in a package is calculated using Equation 8 where T_{JMAX} = Maximum junction temperature, T_{AMAX} = Maximum ambient temperature, θ_{JA} = Thermal resistance of the package, and P_{DMAX} = Maximum power dissipation recommended.

(EQ. 8)

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

An example of the maximum recommended power dissipation versus ambient temperature curve is shown in Figure 36. In this example, the maximum power dissipation across the temperature range is specified at 25°C and the maximum junction temperature is set to 125°C, which is the maximum recommended operating junction temperature.

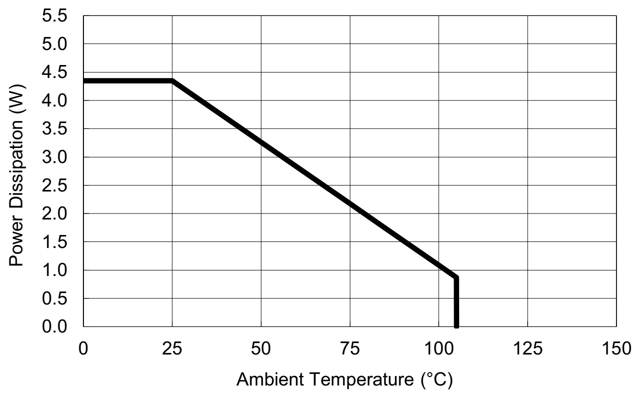


Figure 36. Power Dissipation vs Ambient Temperature

10. External Component Selection

The RAA215300 includes six synchronous buck regulators, three LDOs, and various features. It works with physically small components to reduce PCB assembly area and height. Switching MOSFETs are fully integrated and no external MOSFETs or diodes are needed.

10.1 Output Filters

The inductor and output capacitors are low-pass filters for the voltage at the buck switching node. Their characteristics influence the transfer function of the regulator and the control loop. It the transient load changes, the capacitors maintain output voltage with greater effective bandwidth than that achievable by the control loop alone. The permissible values of inductance and capacitance are dictated by PMIC design and settings. The values in Table 10 are consistent with stable operation and performance in accordance with Electrical Specifications.

10.1.1 Inductor Selection

At full load of the application, which is not necessarily the PMIC maximum rated load, inductors must have at least 90% of their low-current inductance. At 150% of PMIC maximum rated load, inductors must have at least 50% of their low-current inductance. For high efficiency, the inductors should have low resistance and low core loss. Choose molded or screened types for the best EMC.

Other similarly specified components may also be acceptable in the application, see Recommended External Components.

10.1.2 Output Capacitor Selection

Capacitors must be ceramic. When selecting for capacitance value, account for the effects of operating voltage and temperature.

Ceramic capacitors have temperature and voltage (bias) coefficients, which can significantly derate their effective capacitance value. When choosing capacitors, the effective capacitance rating for a given package size, voltage rating, and applied temperature and DC bias must be considered to ensure enough capacitance is used in the design. X5R and X7R types are recommended, depending on operating temperature. Other similarly specified components may also be acceptable in the application, see Recommended External Components.

10.2 Input Capacitor Selection

Ceramic input capacitors provide the high-frequency components of current flowing into the high-side MOSFETs. Place the capacitors close to the PMIC. If the power source is connected to the PMIC by long wires or traces, it may be necessary to add bulk capacitors near (not as close as the ceramic input capacitors) the PMIC to damp oscillation.

Other similarly specified components may also be acceptable in the application, see Recommended External Components.

10.3 Recommended External Components

Table 10. Recommended External Components

Name	Description	Qty	Part Number	Key Electrical Specifications	Imperial (Metric) Size	Manufacturer
All capacitors:[1]						
Supplies						
C_{AVDD}	AVDD Input capacitance, MLCC	1	GRM188R61A106MAAL	10µF±20%, 10V, X5R	0603 (1608)	Murata
C_{VIO}	Output capacitance, MLCC	1	GRM155R61A225KE01D	2.2µF±10%, 10V, X5R	0402 (1005)	Murata
C_{VCHG}	Input capacitance, MLCC	1	GRM155R61A225KE01D	2.2µF±10%, 10V, X5R	0402 (1005)	Murata
C_{VRTC}	Input capacitance, MLCC	DNP	GRM155R61A225KE01D	2.2µF±10%, 10V, X5R	0402 (1005)	Murata
C_{VPROG}	Optional: Input capacitance for EEPROM Programming, MLCC	1	GRM155R6YA225KE11	2.2µF±20%, 35V, X5R	0402 (1005)	Murata

Table 10. Recommended External Components (Cont.)

Name	Description	Qty	Part Number	Key Electrical Specifications	Imperial (Metric) Size	Manufacturer
C_{VBAT}	Output capacitance, supercapacitor	1	FMR0H104ZF	0.1F, 5.5V	-	Kemet
Buck1						
L_{BK1}	Inductor	1	HBED042T-1R0MS-99	1.0µH±20%, 8.2A I_{SAT}, 9mΩ DCR	(4.1x4.1 x2.0mm)	Cyntec
	Option A	1	FDSD0420-H-1R0M=P3	1.0µH±20%, 6.8A I_{SAT}, 29mΩ DCR	(4.0x4.0 x2.0mm)	Murata
	Option B	1	XGL4030-102ME	1.0µH±20%, 10.3A I_{SAT}, 7.2mΩ DCR	(4.0x4.0 x3.1mm)	Coilcraft
	Option C	1	SPM4020T-1R0M-LR	1.0µH±20%, 9A I_{SAT}, 28.1mΩ DCR	(4.4x4.1 x2.0mm)	TDK
C_{BK1_VIN}	Input capacitance, MLCC	2	GRM188R61A106MAAL	10µF±20%, 10V, X5R	0603 (1608)	Murata
C_{BK1_OUT}	Output capacitance, MLCC	5	GRM188R60J476ME15	47µF±20%, 6.3V, X5R	0603 (1608)	Murata
Buck2						
L_{BK2}	Inductor	1	DFE322512F-1R5M	1.5µH±20%, 3.9A I_{SAT}, 48mΩ DCR	(3.2x2.5 x1.2mm)	Murata
C_{BK2_VIN}	Input capacitance, MLCC	1	GRM188R61A106MAAL	10µF±20%, 10V, X5R	0603 (1608)	Murata
C_{BK2_OUT}	Output capacitance, MLCC	3	GRM188R60J476ME15	47µF±20%, 6.3V, X5R	0603 (1608)	Murata
Buck3						
L_{BK3}	Inductor	1	DFE322512F-1R5M	1.5µH±20%, 3.9A I_{SAT}, 48mΩ DCR	(3.2x2.5 x1.2mm)	Murata
C_{BK3_VIN}	Input capacitance, MLCC	1	GRM188R61A106MAAL	10µF±20%, 10V, X5R	0603 (1608)	Murata
C_{BK3_OUT}	Output capacitance, MLCC	2	LMK107BBJ226MA-T	22µF±20%, 10V, X5R	0603 (1608)	Taiyo Yuden
Buck4						
L_{BK4}	Inductor	1	HBED042T-1R5MS-99	1.5µH±20%, 6.8A I_{SAT}, 14mΩ DCR	(4.1x4.1 x2.0mm)	Cyntec
	Option A	1	FDSD0420-H-1R5M=P3	1.5µH±20%, 5.7A I_{SAT}, 36mΩ DCR	(4.0x4.0 x2.0mm)	Murata
	Option B	1	XGL4030-152ME	1.5µH±20%, 8.8A I_{SAT}, 10.5mΩ DCR	(4.0x4.0 x3.1mm)	Coilcraft
	Option C	1	SPM4020T-1R5M-LR	1.5µH±20%, 6.3A I_{SAT}, 40mΩ DCR	(4.4x4.1 x2.0mm)	TDK
C_{BK4_VIN}	Input capacitance, MLCC	2	GRM188R61A106MAAL	10µF±20%, 10V, X5R	0603 (1608)	Murata

Table 10. Recommended External Components (Cont.)

Name	Description	Qty	Part Number	Key Electrical Specifications	Imperial (Metric) Size	Manufacturer
C_{BK4_OUT}	Output capacitance, MLCC	4	GRM21BR61A226ME44	22µF±20%, 10V, X5R	0805 (2012)	Murata
Buck5						
L_{BK5}	Inductor	1	DFE252012F-1R5M	1.5µH±20%, 3.8A I_{SAT}, 58mΩ DCR	(2.5x2.0x1.2mm)	Murata
C_{BK5_VIN}	Input capacitance, MLCC	1	GRM188R61A106MAAL	10µF±20%, 10V, X5R	0603 (1608)	Murata
C_{BK5_OUT}	Output capacitance, MLCC	2	LMK107BBJ226MA-T	22µF±20%, 10V, X5R	0603 (1608)	Taiyo Yuden
Buck6 (supporting VTT Mode)						
L_{BK6}	Inductor	1	DFE252012F-R47M	0.47µH±20%, 6.7A I_{SAT}, 23mΩ DCR	(2.5x2.0 x1.2mm)	Murata
C_{BK6_VIN}	Input capacitance, MLCC	1	GRM188R61A106MAAL	10µF±20%, 10V, X5R	0603 (1608)	Murata
C_{BK6_OUT}	Output capacitance, MLCC	5	GRM188R60J476ME15	47µF±20%, 6.3V, X5R	0603 (1608)	Murata
LDO 1						
C_{LDO1_VIN}	Input capacitance, MLCC	1	GRM188R61A475KAAJ	4.7µF±10%, 10V, X5R	0603 (1608)	Murata
C_{LDO1_OUT}	Output capacitance, MLCC	2	LMK107BBJ226MA-T	22µF±20%, 10V, X5R	0603 (1608)	Taiyo Yuden
LDO 2						
C_{LDO2_VIN}	Input capacitance, MLCC	1	GRM188R61A475KAAJ	4.7µF±10%, 10V, X5R	0603 (1608)	Murata
C_{LDO2_OUT}	Output capacitance, MLCC	2	LMK107BBJ226MA-T	22µF±20%, 10V, X5R	0603 (1608)	Taiyo Yuden
LDO 3						
C_{LDO3_VIN}	Input capacitance, MLCC	1	GRM155R61A225KE01D	2.2µF±10%, 10V, X5R	0402 (1005)	Murata
C_{LDO3_OUT}	Output capacitance, MLCC	1	GRM155R61A475MEAA	4.7µF±20%, 10V, X5R	0402 (1005)	Murata
VTTREF						
C_{VREFIN}	Input capacitance, MLCC	1	GRM155R61A225KE01D	2.2µF±10%, 10V, X5R	0402 (1005)	Murata
$C_{VREFOUT}$	Output capacitance, MLCC	1	GRM155R61A475MEAA	4.7µF±20%, 10V, X5R	0402 (1005)	Murata

Table 10. Recommended External Components (Cont.)

Name	Description	Qty	Part Number	Key Electrical Specifications	Imperial (Metric) Size	Manufacturer
Crystal Oscillator						
XTAL	Crystal	1	ECX-.327-CDX-1293	32.768kHz, ±5ppm, 70kΩ max ESR, 12.5pF load capacitance	(3.2x1.5x 0.9mm)	ECS
	Option A	1	ECX-.327-CDX-2096	32.768kHz, ±5ppm, 50kΩ max ESR, 12.5pF load capacitance	(3.2x1.5x 0.9mm)	ECS
C_{XIN}[2]	Input capacitance	DNP		Up to 10pF, COG	0402 (1005)	
C_{XOUT}[2]	Output capacitance	DNP		Up to 10pF, COG	0402 (1005)	
Resistance						
R_{SDA}, R_{SCL}	I^{2}C Pull-up resistance	1	RC0402JR-0710KL	10kΩ±5%	0402 (1005)	Yageo
R_{INT}	INT# Pull-up resistance	1	RC0402FR-07100KL	100kΩ±5%	0402 (1005)	Yageo
R_{MPIO}	Optional: MPIOx Pull-up or Pull-down resistance	1	RC0402FR-074K75L	4.75kΩ±5%	0402 (1005)	Yageo

1. The capacitance listed in the above table is not derated. Refer to the capacitors datasheets for effective capacitance.
2. Do Not Populate capacitors by default. They are only needed for oscillator tuning. Renesas recommends placing footprints for these components in the system design in case they are needed.

10.4 Recommended Effective Capacitance

The effective capacitance of the ceramic capacitors changes with the DC bias voltage. When choosing the input capacitors or output capacitors for each regulator, the total capacitance needs to be equivalent to the recommended value as shown in Table 11.

Table 11. Recommended Effective Capacitance[1]

Regulator	Total Output Effective Capacitance (µF)	Total Input Effective Capacitance (µF)
Buck1	190	7.2
Buck2	110	3.6
Buck3	34	3.6
Buck4	59	7.2
Buck5	40	3.6
Buck6 (VTT mode)	222	3.6
LDO1	22	3.2
LDO2	22	3.2
LDO3	3	0.6
VIO	1.5	N/A

Table 11. Recommended Effective Capacitance[1]

Regulator	Total Output Effective Capacitance (µF)	Total Input Effective Capacitance (µF)
VREFIN	1.8	N/A
VREFOUT	4.6	N/A

1. The recommended effective capacitance is determined based on the RTKA215300DE0000BU BOM and the DC characteristics curves that are available on the capacitor vendor website. The DC bias voltages are the typical input and output voltages of each regulator as stated in Electrical Specifications.

11. Layout Guidelines

PCB design is crucial to proper performance of the PMIC and system. The following are recommendations to achieve proper device performance.

11.1 Power Ground (PGND)

PGND is the reference for all voltages of the power system. Many components must have low-impedance connections to PGND (most importantly the input and output capacitors). Create a PGND plane on at least one PCB layer and extend it to at least the connection points of all relevant components. The PGND plane is an important heatsink and it may also provide electrostatic screening. Aim to avoid interrupting the plane with non-PGND vias, especially if they are in a row and form a slit. The PGND plane is not perfect because it has impedance and there are unwanted voltages developed across it.

11.2 Analog Ground (AGND)

AGND is an electrically quiet reference for signals that could be corrupted if they were connected to PGND. These signals are the PMIC internal power supply and those associated with the RTC and its power supply. Create a small plane that connects these signals to Pin 26 and Pin 42. Connect this plane directly to PGND at the EPAD.

11.3 Digital Ground

Connect the grounds of digital signals to PGND.

11.4 Exposed Pad (EPAD)

Internal to the PMIC, all regulator power grounds are bonded to the EPAD. The EPAD is in close thermal contact with the PMIC die. Therefore, the connection between EPAD and PCB is important to both the grounding scheme and thermal management. Connect the EPAD to the PGND plane.

Place thermal vias, in a 1 to 1.2mm pitch grid formation, under the PMIC at least in the area of the EPAD, and connect them to the PGND plane. The vias must not wick solder from the EPAD joint.

11.5 Buck Regulators

The current through the MOSFETs is periodically and rapidly switched. The current generates a magnetic field that inductively couples current into nearby conductors. At some distance (dependent on frequency) from the source, the magnetic field becomes electromagnetic radiation (noise). Voltage (noise) develops across impedance in the current paths.

To mitigate the effects of switched current, make paths short and low impedance, make loop areas small and avoid sharing ground connections with sensitive circuits.

The MOSFETs are internal to the PMIC, so their current paths are predetermined. The main external high-frequency current path is through input capacitors. Place input capacitors close to their respective buck regulator input terminals, which usually means placing them on the same side as the PMIC. Connect the positive side with short wide copper. If the negative side needs to connect to an inner-layer PGND plane, do so with multiple vias. In some applications, it might be helpful to place a physically small capacitor with a lower high-frequency impedance closest to the PMIC. Current in the inductor has smaller high-frequency content than the MOSFETs; however, it is still necessary to connect the inductor to the switch node PMIC terminals with low-impedance copper and to make low-impedance connections to the output capacitors. The output capacitors must be intimately connected to the PGND plane so use multiple vias if the PGND plane is on an inner layer.

The voltage at the switch node is periodically and rapidly switched. The voltage generates an electric field that capacitively couples voltage into nearby conductors. At some distance (dependent on frequency) from the source, the electric field becomes electromagnetic radiation (noise).

To mitigate the effects of switched voltage, make the copper area of the switched node small. This partially contradicts the requirement to make a low-impedance connection between the switch node and inductor, but this is a compromise that must happen. Make the path short but only wide enough to carry the current. Do not add copper that does not have a high current density. Most of the generated electric field is perpendicular to the copper surface. The PGND plane is an effective shield. The inductor terminal also generates an electric field, in directions perpendicular to its surfaces.

11.6 Linear Regulators (LDOs)

The LDOs require good high-frequency decoupling of their inputs and outputs. Connections to input and output capacitors must be low impedance at high frequency. Place capacitors close to PMIC pins and connect with short wide copper. Connect capacitors to the PGND plane with multiple vias.

11.7 Crystal Oscillator

Place the crystal close to the PMIC. Pin 28, XIN, has very high impedance, and oscillator circuits operating at low frequencies are susceptible to noise if good layout practice is not followed. Erratic clocking and accuracy errors can be caused by adjacent noisy signals. Do not route noisy traces near the crystal. Add a guard ring around the crystal and connect one end to AGND. To avoid affecting load capacitance, keep all layers clear of copper in the area of the crystal and its connecting traces.

11.8 Device Specific Layout Guidelines

The following table provides layout guidelines (such as trace routing and size, and component placements) for the various pins of RAA215300. *Note:* All buck supplies (BUCKx_VINx) = AVDD = VCHG.

Pin Number	Pin Name	Layout Guideline
1, 2	MPIO4, MPIO3	Digital input/output pin. Route trace away from any buck switch node. Consider placing the trace such that the PGND plane is between the trace and any buck switch node.
3, 4, 5	BUCK1_LX3, BUCK1_LX2, BUCK1_LX1	Place the inductor close to the pins. Connect the pins together and to the inductor with short, wide copper, but keep the area small. Do not place sensitive signal traces (for example, feedback) near this copper on the same layer, or in the same area on inner layers unless shielded by the PGND plane.
6, 7, 8	BUCK1_VIN3, BUCK1_VIN2, BUCK1_VIN1	Place input capacitors close to the pins and connect with short, wide copper.
9	PGND	Connect the PGND pin directly to the top layer of copper under the exposed pad (EPAD). The PGND pin may also be connected to top layer copper - for example to nearby input capacitors for BUCK1
10	BUCK1_FB	Run a dedicated trace to BUCK1 output capacitors. Connect directly to a capacitor but away from the main path of output current. Route the trace away from any noisy signals, switch nodes, or output inductors. Consider placing the trace such that the PGND plane is between the trace and any buck switch node.
11	VPROG	Connect to PGND (if programming EEPROM is not required).

Pin Number	Pin Name	Layout Guideline
12	BUCK3_FB	Run a dedicated trace to BUCK3 output capacitors. Connect directly to a capacitor but away from the main path of output current. Route the trace away from any noisy signals, switch nodes, or output inductors. Consider placing the trace such that the PGND plane is between the trace and any buck switch node.
13	LDO_SEL2	Digital input pin. Should be isolated from the high di/dt and dv/dt signals to minimize any coupling. This signal should be placed on a quiet layer.
14	BUCK3_VIN	Place input capacitors close to the pin and connect with short, wide copper.
15	BUCK3_LX	Place the inductor close to the pin. Connect the pin to the inductor with short, wide copper, but keep the area small. Do not place sensitive signal traces (for example, feedback) near this copper on the same layer, or in the same area on inner layers unless shielded by the PGND plane.
16	INT#	Digital output pin. Should be isolated from the high di/dt and dv/dt signals to minimize any coupling. This signal should be placed on a quiet layer.
17	SCL	Digital input pins. Should be isolated from the high di/dt and dv/dt signals to minimize any coupling. These signals should be placed on a quiet layer. If not used, connect to VIO.
18	SDA	
19	LDO_SEL1	Digital input pin. Should be isolated from the high di/dt and dv/dt signals to minimize any coupling. This signal should be placed on a quiet layer.
20, 21	BUCK4_LX2, BUCK4_LX1	Place the inductor close to the pins. Connect the pins to the inductor with short, wide copper, but keep the area small. Do not place sensitive signal traces (for example, feedback) near this copper on the same layer, or in the same area on inner layers unless shielded by the PGND plane.
22, 23	BUCK4_VIN2, BUCK4_VIN1	Place input capacitors close to the pins and connect with short, wide copper.
24	VIO	Place the decoupling capacitor close to the pin and connect with short, wide copper. Connect the other side of the capacitor to pin 26 (AGND) with short, wide copper.
25	BUCK4_FB	Run a dedicated trace to BUCK4 output capacitors. Connect directly to a capacitor but away from the main path of output current. Route the trace away from any noisy signals, switch nodes, or output inductors. Consider placing the trace such that the PGND plane is between the trace and any buck switch node.
26, 42	AGND	Analog ground (AGND) and power ground (PGND) of the IC should be separated on the board, but connected directly to EPAD. To avoid unwanted noise coupling into the AGND plane, keep the plane localized to the area where AGND is required.
27	XOUT	Avoid routing serial bus lines, any high-speed logic lines, high dv/dt, or di/dt signals in the vicinity of crystal pins. These can induce noise in the oscillator circuit causing misclocking. Add a ground trace around the crystal with one end terminated at the chip analog ground, providing termination for emitted noise in the vicinity of the RTC device. Avoid ground plane in the layer(s) under these pins, traces, and external crystal, as this affects the load capacitance on the pins and therefore, the oscillator accuracy of the circuit. Connect to ground if not used.
28	XIN	
29	VRTC	When RTC is used, place a decoupling capacitor footprint close to the pin and connect with short, wide copper. Connect the other side of the capacitor footprint to AGND. This capacitor should be Do Not Populated by default.
30	VBAT	Connect to battery or supercapacitor with short trace. Connect to PGND if not used.
31	VCHG	AVDD, VCHG, and BUCKx_VINx must be the same voltage. Place the decoupling capacitor close to the pin and connect with short, wide copper. Connect the other side of the capacitor to PGND.
32, 35, 36	LDO1_OUT, LDO2_OUT, LDO3_OUT	Place decoupling capacitors close to their respective outputs and connect with wide traces.

Pin Number	Pin Name	Layout Guideline
33, 34, 37	LDO1_VIN, LDO2_VIN, LDO3_VIN	Place decoupling capacitors close to their respective inputs and connect with wide traces.
38	BUCK5_LX	Place the inductor close to the pin. Connect the pin to the inductor with short, wide copper, but keep the area small. Do not place sensitive signal traces (for example, feedback) near this copper on the same layer, or in the same area on inner layers unless shielded by the PGND plane.
39	BUCK5_VIN	Place input capacitors close to the pin and connect with short, wide copper.
40	AVDD	AVDD, VCHG, and BUCKx_VINx must be the same voltage. Place the decoupling capacitor close to the pin and connect with short, wide copper. Connect the other side of the capacitor to PGND.
41	BUCK5_FB	Run a dedicated trace to BUCK5 output capacitors. Connect directly to a capacitor but away from the main path of output current. Route the trace away from any noisy signals, switch nodes, or output inductors. Consider placing the trace such that the PGND plane is between the trace and any buck switch node.
43	VREFIN	Place the decoupling capacitor close to the pin and connect with short, wide copper. Connect the other side of the capacitor to PGND. *Note:* Pin has a 1MΩ (typical) internal resistor to GND.
44	VREFOUT	Place the decoupling capacitor close to the pin and connect with short, wide copper. Connect the other side of the capacitor to PGND.
45	MPIO5	Digital input/output pin. Route trace away from any buck switch node. Consider placing the trace such that the PGND plane is between the trace and any buck switch node.
46	BUCK6_FB	Run a dedicated trace to BUCK3 output capacitors. Connect directly to a capacitor but away from the main path of output current. Route the trace away from any noisy signals, switch nodes, or output inductors. Consider placing the trace such that the PGND plane is between the trace and any buck switch node.
47	CEN	Digital input pin. Route trace away from any buck switch node. Consider placing the trace such that the PGND plane is between the trace and any buck switch node.
48	BUCK6_VIN	Place input capacitors close to the pin and connect with short, wide copper.
49	BUCK6_LX	Place the inductor close to the pin. Connect the pin to the inductor with short, wide copper, but keep the area small. Do not place sensitive signal traces (for example, feedback) near this copper on the same layer, or in the same area on inner layers unless shielded by the PGND plane.
50	BUCK2_LX	Place the inductor close to the pin. Connect the pin to the inductor with short, wide copper, but keep the area small. Do not place sensitive signal traces (for example, feedback) near this copper on the same layer, or in the same area on inner layers unless shielded by the PGND plane.
51	BUCK2_VIN	Place input capacitors close to the pin and connect with short, wide copper.
52	PWRON	Digital input pin. Should be isolated from the high di/dt and dv/dt signals to minimize any coupling. This signal should be placed on a quiet layer.
53	BUCK2_FB	Run a dedicated trace to BUCK2 output capacitors. Connect directly to a capacitor but away from the main path of output current. Route the trace away from any noisy signals, switch nodes, or output inductors. Consider placing the trace such that the PGND plane is between the trace and any buck switch node.
54	MPIO0	Digital input/output pin. Route the trace away from any buck switch node. Consider placing the trace such that the PGND plane is between the trace and any buck switch node.
55	MPIO1	Digital input/output pin. Route the trace away from any buck switch node. Consider placing the trace such that the PGND plane is between the trace and any buck switch node.

Pin Number	Pin Name	Layout Guideline
56	MPIO2	Digital input/output pin. Route trace away from any buck switch node. Consider placing the trace such that the PGND plane is between the trace and any buck switch node.
-	EPAD	Connect to PGND with matching shape. Connect to the GND layer using an array of equidistant vias to achieve better thermal performance.

12. Register Map

Any register addresses (pointers) not indicated in the following section, Register Map Detail, are reserved and should not be used.

Register addresses 0x00~13 are read and write accessed using only the RTC Slave Address (set in register 0x1F).

All other register addresses are read and write accessed using the Main Slave Address (set in register 0x1E). See 7-bit Device Addresses.

12.1 Register Map Detail

The default values in the following table are for RAA215300A2GNP#HA0. Any differences with other part numbers are outlined in Part Number Differences.

Register Pointer	Register Bit(s)	Bit(s)/Function Name	Description	Setting/Range	Default
0x00	Register Name - RTC SC Type - (RW, Non EEPROM)				0x00 / 0
	[7]	not used			<0>
	[6]	SC22	Set seconds (0-59) in BCD format	RTC SC[6:0] BCD decode: 0000000: 0sec 0000001: 1sec 0000010: 2sec … 0001001: 9sec 0010000: 10sec 0010001: 11sec … 1010111: 57sec 1011000: 58sec 1011001: 59sec	<0>
	[5]	SC21			<0>
	[4]	SC20			<0>
	[3]	SC13			<0>
	[2]	SC12			<0>
	[1]	SC11			<0>
	[0]	SC10			<0>
0x01	Register Name - RTC MN Type - (RW, Non EEPROM)				0x00 / 0
	[7]	not used			<0>
	[6]	MN22	Set minutes (0-59) in BCD format	RTC MN[6:0] BCD decode: 0000000: 0min 0000001: 1min 0000010: 2min … 0001001: 9min 0010000: 10min 0010001: 11min … 1010111: 57min 1011000: 58min 1011001: 59min	<0>
	[5]	MN21			<0>
	[4]	MN20			<0>
	[3]	MN13			<0>
	[2]	MN12			<0>
	[1]	MN11			<0>
	[0]	MN10			<0>

0x02	Register Name - RTC HR Type - (RW, Non EEPROM)				0x00 / 0
	[7]	MIL	12-hour or 24-hour format selection bit	0: 12-hour format 1: 24-hour format	<0>
	[6]	not used			<0>
	[5]	HR21	Set hours in BCD format. If the MIL bit is "0", the RTC uses a 12-hour format and HR21 bit functions as an AM/PM indicator with a "1" representing PM.	If MIL = 1 RTC HR[5:0] decodes for 24-hour format: 000000: 0hr 000001: 1hr … 001001: 9hr 010000: 10hr … 011001: 19hr 100000: 20hr … 100011: 23hr If MIL = 0 RTC HR[4:0] decodes for 12-hour format with RTC HR [5] indicating AM/PM: 00000: INVALID 00001: 1 AM/PM 00010: 2 AM/PM … 01001: 9 AM/PM 10000: 10 AM/PM 10001: 11 AM/PM 10010: 12 AM/PM	<0>
	[4]	HR20			<0>
	[3]	HR13			<0>
	[2]	HR12			<0>
	[1]	HR11			<0>
	[0]	HR10			<0>
0x03	Register Name - RTC DT Type - (RW, Non EEPROM)				0x01 / 1
	[7:6]	not used			<00>
	[5]	DT21	Set date (1-31) in BCD format	RTC DT[5:0] BCD decode: 000000: INVALID 000001: date 1 000010: date 2 … 001001: date 9 010000: date 10 … 011001: date 19 100000: date 20 … 101001: date 29 110000: date 30 110001: date 31	<0>
	[4]	DT20			<0>
	[3]	DT13			<0>
	[2]	DT12			<0>
	[1]	DT11			<0>
	[0]	DT10			<1>
0x04	Register Name - RTC MO Type - (RW, Non EEPROM)				0x01 / 1
	[7:5]	not used			<000>
	[4]	MO20	Set month (1-12) in BCD format	RTC MO[4:0] BCD decode: 00000: INVALID 00001: 1st month (Jan) 00010: 2nd month (Feb) 00011: 3rd month (Mar) … 01001: 9th month (Sep) 10000: 10th month (Oct) 10001: 11th month (Nov) 10010: 12th month(Dec)	<0>
	[3]	MO13			<0>
	[2]	MO12			<0>
	[1]	MO11			<0>
	[0]	MO10			<1>

0x05	Register Name - RTC YR Type - (RW, Non EEPROM)				0x00 / 0
	[7]	YR23	Set year (0-99) in BCD format	RTC YR[7:0] decodes: 0000 0000: 0th year 0000 0001: 1st year … 0001 0000: 10th year 0001 0001: 11th year … 1000 0000: 80th year 1000 0001: 81st year … 1001 1000: 98th year 1001 1001: 99th year	<0>
	[6]	YR22			<0>
	[5]	YR21			<0>
	[4]	YR20			<0>
	[3]	YR13			<0>
	[2]	YR12			<0>
	[1]	YR11			<0>
	[0]	YR10			<0>
0x06	Register Name - RTC DW Type - (RW, Non EEPROM)				0x00 / 0
	[7:3]	not used			<00000>
	[2]	DW2	Set day of the week (1-7)	RTC DW[2:0] decodes: 000: 1st day of the week 001: 2nd day of the week 010: 3rd day of the week … 110: 7th day of the week	<0>
	[1]	DW1			<0>
	[0]	DW0			<0>
0x07	Register Name - RTC SR Type - (RW, Non EEPROM)				0x01 / 1
	[7]	ARST	Auto reset enable bit	0:Disable the automatic reset of the BAT and ALM status bits only 1: Enable the automatic reset of the BAT and ALM status bits only	<0>
	[6]	XTOSCB	Internal crystal oscillator enable bit. XTOSCB needs to be set to '0' when external crystal is used. XTOSCB needs to be set to 1' when external 32kHz clock signal is applied at XIN pin.	0: Enable internal crystal oscillator 1: Disable internal crystal oscillator	<0>
	[5]	not used			<0>
	[4]	WRTC	Write RTC enable bit	0: Disable write capability into the RTC timing registers 1: Enable write capability into the RTC timing registers	<0>
	[3]	not used			<0>
	[2]	ALM	Alarm bit	0: Alarm doesn't match the real time clock 1: Alarm matches the real time clock	<0>
	[1]	BAT	Battery bit	0: No battery 1: Battery backup mode	<0>
	[0]	RTCF	Real time clock fail bit	0: OK (normal) 1: RTC failure	<1>

0x08	Register Name - RTC INT Type - (RW, Non EEPROM)				0x10 / 16
	[7]	IM	Interrupt/alarm mode bit	0: Enable single event alarm mode 1: Enable periodic interrupt alarm mode	<0>
	[6]	ALME	Alarm enable bit	0: Disable the alarm function 1: Enable the alarm function	<0>
	[5]	LPMODE	Oscillator bias current control bit	0: Normal oscillator bias current 1: Reduced oscillator bias current	<0>
	[4]	FOBATB	Enable/disable the FOUT/IRQ function in battery backup mode	0: Disable the FOUT/IRQ function in battery backup mode 1: Enable the FOUT/IRQ function in battery backup mode	<1>
	[3:0]	FO	Enable/disable the frequency output function and select the output frequency at the INT# pin	0000: 0Hz 0001: 32768Hz 0010: 4096Hz 0011: 1024Hz 0100: 64Hz 0101: 32Hz 0110: 16Hz 0111: 8Hz 1000: 4Hz 1001: 2Hz 1010: 1Hz 1011: 1/2Hz 1100: 1/4Hz 1101: 1/8Hz 1110: 1/16Hz 1111: 1/32Hz	<0000>
0x09	Reserved for Renesas Internal Use				
0x0A	Register Name - RTC ATR Type - (RW, Non EEPROM)				0x00 / 0
	[7:6]	BMATR	Battery mode ATR selection. Adjust the on-chip capacitance when the RTC power source switches between VCHG and VBAT	00: 0pF 01: -0.5pF 10: +0.5pF 11: 1pF	<00>
	[5:0]	ATR	Adjust the on-chip load capacitance value for frequency compensation of the RTC	Cload = [16 x (~ATR[5]) + 8 x ATR[4] + 4 x ATR[3] + 2 x ATR[2] + 1 x ATR[1] + 0.5 x ATR[0] + 9]/2 (pF) RTC ATR[5:0] decode: 000000 : 12.5pF 000001 : 12.75pF 000010 : 13.0pF … 011110 : 20.0pF 011111 : 20.25pF 100000 : 4.5pF 100001 : 4.75pF … 111101 : 11.75pF 111110 : 12.0pF 111111 : 12.25pF	<000000>

0x0B	Register Name - RTC DTR Type - (RW, Non EEPROM)				0x00 / 0
	[7:3]	not used			<00000>
	[2:0]	DTR	Adjust the average number of counts per second and average the ppm error to achieve better accuracy	000: 0ppm 001: +20ppm 010: +40ppm 011: +60ppm 100: 0ppm 101: -20ppm 110: -40ppm 111: -60ppm	<000>
0x0C	Register Name - RTC SCA Type - (RW, Non EEPROM)				0x00 / 0
	[7]	ESCA	Enable or disable alarm register bytes for seconds	0: Disable the alarm register bytes for seconds 1: Enable the alarm register bytes for seconds	<0>
	[6]	ASC22	Set alarm seconds (0-59) in BCD format. The alarm will be triggered once a match occurs between the alarm registers and the RTC registers for seconds	RTC ASC[6:0] BCD decode: 0000000: 0sec 0000001: 1sec 0000010: 2sec … 0001001: 9sec 0010000: 10sec 0010001: 11sec … 1010111: 57sec 1011000: 58sec 1011001: 59sec	<0>
	[5]	ASC21			<0>
	[4]	ASC20			<0>
	[3]	ASC13			<0>
	[2]	ASC12			<0>
	[1]	ASC11			<0>
	[0]	ASC10			<0>
0x0D	Register Name - RTC MNA Type - (RW, Non EEPROM)				0x00 / 0
	[7]	EMNA	Enable or disable alarm register bytes for minutes	0: Disable the alarm register bytes for minutes 1: Enable the alarm register bytes for minutes	<0>
	[6]	AMN22	Set alarm minutes (0-59) in BCD format. The alarm will be triggered once a match occurs between the alarm registers and the RTC registers for minutes	RTC AMN[6:0] BCD decode: 0000000: 0min 0000001: 1min 0000010: 2min … 0001001: 9min 0010000: 10min 0010001: 11min … 1010111: 57min 1011000: 58min 1011001: 59min	<0>
	[5]	AMN21			<0>
	[4]	AMN20			<0>
	[3]	AMN13			<0>
	[2]	AMN12			<0>
	[1]	AMN11			<0>
	[0]	AMN10			<0>

0x0E	Register Name - RTC HRA Type - (RW, Non EEPROM)				0x00 / 0
	[7]	EHRA	Enable or disable alarm register bytes for hours	0: Disable the alarm register bytes for hours 1: Enable the alarm register bytes for hours	<0>
	[6]	not used			<0>
	[5]	AHR21	Set hours in BCD format. If the MIL bit is “0”, the RTC uses a 12-hour format and AHR21 bit functions as an AM/PM indicator with a “1” representing PM. The alarm will be triggered once a match occurs between the alarm registers and the RTC registers for hours	If MIL = 1 RTC AHR[5:0] decodes for 24-hour format: 000000: 0hr 000001: 1hr … 001001: 9hr 010000: 10hr … 011001: 19hr 100000: 20hr … 100011: 23hr If MIL = 0 RTC AHR[4:0] decodes for 12-hour format with RTC AHR[5] indicating AM/PM: 00000: INVALID 00001: 1 AM/PM 00010: 2 AM/PM … 01001: 9 AM/PM 10000: 10 AM/PM 10001: 11 AM/PM 10010: 12 AM/PM	<0>
	[4]	AHR20			<0>
	[3]	AHR13			<0>
	[2]	AHR12			<0>
	[1]	AHR11			<0>
	[0]	AHR10			<0>
0x0F	Register Name - RTC DTA Type - (RW, Non EEPROM)				0x00 / 0
	[7]	EDTA	Enable or disable alarm register bytes for date	0: Disable the alarm register bytes for date 1: Enable the alarm register bytes for date	<0>
	[6]	not used			<0>
	[5]	ADT21	Set alarm date (1-31) in BCD format. The alarm will be triggered once a match occurs between the alarm registers and the RTC registers for date	RTC ADT[5:0] BCD decode: 000000: INVALID 000001: date 1 000010: date 2 … 001001: date 9 010000: date 10 … 011001: date 19 100000: date 20 … 101001: date 29 110000: date 30 110001: date 31	<0>
	[4]	ADT20			<0>
	[3]	ADT13			<0>
	[2]	ADT12			<0>
	[1]	ADT11			<0>
	[0]	ADT10			<0>

0x10	Register Name - RTC MOA Type - (RW, Non EEPROM)				0x00 / 0
	[7]	EMOA	Enable or disable alarm register bytes for month	0: Disable the alarm register bytes for month 1: Enable the alarm register bytes for month	<0>
	[6:5]	not used			<00>
	[4]	AMO20	Set alarm month (1-12) in BCD format. The alarm will be triggered once a match occurs between the alarm registers and the RTC registers for month	RTC AMO[4:0] BCD decode: 00000: INVALID 00001: 1st month (Jan) 00010: 2nd month (Feb) 00011: 3rd month (Mar) … 01001: 9th month (Sep) 10000: 10th month (Oct) 10001: 11th month (Nov) 10010: 12th month(Dec)	<0>
	[3]	AMO13			<0>
	[2]	AMO12			<0>
	[1]	AMO11			<0>
	[0]	AMO10			<0>
0x11	Register Name - RTC DWA Type - (RW, Non EEPROM)				0x00 / 0
	[7]	EDWA	Enable or disable alarm register bytes for day of the week	0: Disable the alarm register bytes for day of the week 1: Enable the alarm register bytes for day of the week	<0>
	[6:3]	not used			<0000>
	[2]	ADW12	Set alarm day of the week (1-7). The alarm will be triggered once a match occurs between the alarm registers and the RTC registers for day of the week	RTC ADW[2:0] decodes: 000: 1st day of the week 001: 2nd day of the week 010: 3rd day of the week … 110: 7th day of the week	<0>
	[1]	ADW11			<0>
	[0]	ADW10			<0>
0x12	Register Name - RTC USR1 Type - (RW, Non EEPROM)				0x00 / 0
	[7]	USR17	Battery-backed user memory storage		<0>
	[6]	USR16			<0>
	[5]	USR15			<0>
	[4]	USR14			<0>
	[3]	USR13			<0>
	[2]	USR12			<0>
	[1]	USR11			<0>
	[0]	USR10			<0>
0x13	Register Name - RTC USR2 Type - (RW, Non EEPROM)				0x00 / 0
	[7]	USR27	Battery-backed user memory storage		<0>
	[6]	USR26			<0>
	[5]	USR25			<0>
	[4]	USR24			<0>
	[3]	USR23			<0>
	[2]	USR22			<0>
	[1]	USR21			<0>
	[0]	USR20			<0>

0x1E	Register Name - Main Slave Address Type - (RW, EEPROM)				0x00 / 0
	[7]	not used			<0>
	[6:0]	Main Slave Addr	Set the 7-bit main I2C slave address	0000000: slave address 0x12 0000001: slave address 0x01 0000010: slave address 0x02 … 1111111: slave address 0x7F	<0000000>
0x1F	Register Name - RTC Slave Address Type - (RW, EEPROM)				0x00 / 0
	[7]	not used			<0>
	[6:0]	RTC Slave Addr	Set the 7-bit RTC I2C slave address	0000000: slave address 0x6F 0000001: slave address 0x01 0000010: slave address 0x02 … 1111111: slave address 0x7F	<0000000>
0x20	Register Name - Buck1 Enable Type - (RW, EEPROM)				0x07 / 7
	[7:5]	not used			<000>
	[4]	Buck1 Phase Sync EN	Enable Buck1 Phase Synchronization function	0: Disabled 1: Enabled	<0>
	[3]	Buck1 SS EN	Enable Buck1 PFM Spread Spectrum function in PFM mode	0: Disabled 1: Enabled	<0>
	[2]	Buck1 ABS EN	Enable Buck1 ABS (Ultrasonic) mode	0: Disabled 1: Enabled	<1>
	[1]	Buck1 EN SLEEP	Enable Buck1 in SLEEP state	0: Disabled 1: Enabled	<1>
	[0]	Buck1 EN ACTIVE	Enable Buck1 in ACTIVE state	0: Disabled 1: Enabled	<1>
0x21	Register Name - Buck1 ACTIVE Type - (RW, EEPROM)				0x06 / 6
	[7:6]	not used			<00>
	[5:4]	Buck1 Mode ACTIVE	Set Buck1 operation mode in ACTIVE state	00: Auto PFM/PWM mode 01: Forced PWM mode 1x: Reserved	<00>
	[3:0]	Buck1 Vo ACTIVE	Set Buck1 output voltage in ACTIVE state	4'b0000 - 4'b1110: Buck1 = 0.8V + 0.05V x Buck1_Vo_ACTIVE[3:0] 4'b1111: 1.03V	<0110>
0x22	Register Name - Buck1 SLEEP Type - (RW, EEPROM)				0x06 / 6
	[7:6]	not used			<00>
	[5:4]	Buck1 Mode SLEEP	Set Buck1 operation mode in SLEEP state	00: Auto PFM/PWM mode 01: Forced PWM mode 1x: Reserved	<00>
	[3:0]	Buck1 Vo SLEEP	Set Buck1 output voltage in SLEEP state	4'b0000 - 4'b1110: Buck1 = 0.8V + 0.05V x Buck1_Vo_SLEEP[3:0] 4'b1111: 1.03V	<0110>

0x23	Register Name - Buck1 Power On Type - (RW, EEPROM)				0x02 / 2
	[7]	not used			<0>
	[6:0]	Buck1 Power On Delay	Delay timed from the beginning of power-on sequence	0: 0ms 1: 1ms … 127: 127ms	<0000010>
0x24	Register Name - Buck1 Power Off Type - (RW, EEPROM)				0x3C / 60
	[7]	not used			<0>
	[6:0]	Buck1 Power Off Delay	Delay timed from the beginning of power-off sequence	0: 0ms 1: 1ms … 127: 127ms	<0111100>
0x25	Register Name - Buck1 SR Type - (RW, EEPROM)				0x5A / 90
	[7:6]	Buck1 TSoftStart	Set Buck1 soft-start time	00: 4ms 01: 2ms 10: 1ms 11: 0.5ms	<01>
	[5:4]	Buck1 TShutDown	Set Buck1 shutdown period. Note: this setting sets the Shut Down SR when Shutdown Option Buck is set to 2b'00, 2b'01 or 2b'10. In addition, when CEN goes from high to low, the shutdown period starts to count from the time when the last rail is turned off. At the end of the shutdown period the FSM transitions to {STANDBY} then onward to {RESET}.	00: 4ms 01: 2ms 10: 1ms 11: 0.5ms	<01>
	[3:2]	Buck1 DVS SRup	Set Buck1 output ramp-up slew rate	00: 2mV/μs 01: 4mV/μs 10: 8mV/μs 11: 16mV/μs	<10>
	[1:0]	Buck1 DVS SRdn	Set Buck1 output ramp-down slew rate	00: 2mV/μs 01: 4mV/μs 10: 8mV/μs 11: 16mV/μs	<10>

0x26	Register Name - Buck1 Config Type - (RW, EEPROM)				0x12 / 18
	[7]	not used			<0>
	[6:5]	Buck1 Phase Sync Delay	Set Buck1 phase shift relative to the internal clock when Buck1 Phase Sync EN is enabled	00: 0deg 01: 90deg 10: 180deg 11: 270deg	<00>
	[4:2]	Buck1 SW Freq	Set Buck1 switching frequency when in PWM operation	000: 0.667MHz 001: 0.769MHz 010: 0.833MHz 011: 1MHz 100: 1.11MHz 101: 1.33MHz 110: 1.54MHz 111: 1.67MHz	<100>
	[1:0]	Buck1 Discharge	Set Buck1 output discharge resistance	00: Disabled 01: Slow 10: Medium 11: Fast	<10>
0x27	Register Name - Buck2 Enable Type - (RW, EEPROM)				0x07 / 7
	[7:5]	not used			<000>
	[4]	Buck2 Phase Sync EN	Enable Buck2 Phase Synchronization function	0: Disabled 1: Enabled	<0>
	[3]	Buck2 SS EN	Enable Buck2 PFM Spread Spectrum function in PFM mode	0: Disabled 1: Enabled	<0>
	[2]	Buck2 ABS EN	Enable Buck2 ABS (Ultrasonic) mode	0: Disabled 1: Enabled	<1>
	[1]	Buck2 EN SLEEP	Enable Buck2 in SLEEP state	0: Disabled 1: Enabled	<1>
	[0]	Buck2 EN ACTIVE	Enable Buck2 in ACTIVE state	0: Disabled 1: Enabled	<1>
0x28	Register Name - Buck2 ACTIVE Type - (RW, EEPROM)				0x02 / 2
	[7:6]	not used			<00>
	[5:4]	Buck2 Mode ACTIVE	Set Buck2 operation mode in ACTIVE state	00: Auto PFM/PWM mode 01: Forced PWM mode 1x: Reserved	<00>
	[3:0]	Buck2 Vo ACTIVE	Set Buck2 output voltage in ACTIVE state	Buck2 = 1.1V + 0.05V x Buck2_Vo_ACTIVE[3:0]	<0010>
0x29	Register Name - Buck2 SLEEP Type - (RW, EEPROM)				0x02 / 2
	[7:6]	not used			<00>
	[5:4]	Buck2 Mode SLEEP	Set Buck2 operation mode in SLEEP state	00: Auto PFM/PWM mode 01: Forced PWM mode 1x: Reserved	<00>
	[3:0]	Buck2 Vo SLEEP	Set Buck2 output voltage in SLEEP state	Buck2 = 1.1V + 0.05V x Buck2_Vo_SLEEP[3:0]	<0010>

0x2A	Register Name - Buck2 Power On Type - (RW, EEPROM)				0x03 / 3
	[7]	not used			<0>
	[6:0]	Buck2 Power On Delay	Delay timed from the beginning of power-on sequence	0: 0ms 1: 1ms … 127: 127ms	<0000011>
0x2B	Register Name - Buck2 Power Off Type - (RW, EEPROM)				0x3B / 59
	[7]	not used			<0>
	[6:0]	Buck2 Power Off Delay	Delay timed from the beginning of power-off sequence	0: 0ms 1: 1ms … 127: 127ms	<0111011>
0x2C	Register Name - Buck2 SR Type - (RW, EEPROM)				0x5A / 90
	[7:6]	Buck2 TSoftStart	Set Buck2 soft-start time	00: 4ms 01: 2ms 10: 1ms 11: 0.5ms	<01>
	[5:4]	Buck2 TShutDown	Set Buck2 shutdown period. Note: this setting sets the Shut Down SR when Shutdown Option Buck is set to 2b'00, 2b'01 or 2b'10. In addition, when CEN goes from high to low, the shutdown period starts to count from the time when the last rail is turned off. At the end of the shutdown period the FSM transitions to {STANDBY} then onward to {RESET}.	00: 4ms 01: 2ms 10: 1ms 11: 0.5ms	<01>
	[3:2]	Buck2 DVS SRup	Set Buck2 output ramp-up slew rate	00: 2mV/µs 01: 4mV/µs 10: 8mV/µs 11: 16mV/µs	<10>
	[1:0]	Buck2 DVS SRdn	Set Buck2 output ramp-down slew rate	00: 2mV/µs 01: 4mV/µs 10: 8mV/µs 11: 16mV/µs	<10>

0x2D	Register Name - Buck2 Config Type - (RW, EEPROM)				0x06 / 6
	[7]	not used			<0>
	[6:5]	Buck2 Phase Sync Delay	Set Buck2 phase shift relative to the internal clock when Buck1 Phase Sync EN is enabled	00: 0deg 01: 90deg 10: 180deg 11: 270deg	<00>
	[4:2]	Buck2 SW Freq	Set Buck2 switching frequency when in PWM operation	000: 0.667MHz 001: 0.769MHz 010: 0.833MHz 011: 1MHz 100: 1.11MHz 101: 1.33MHz 110: 1.54MHz 111: 1.67MHz	<001>
	[1:0]	Buck2 Discharge	Set Buck2 output discharge resistance	00: Disabled 01: Slow 10: Medium 11: Fast	<10>
0x2E	Register Name - Buck3 Enable Type - (RW, EEPROM)				0x07 / 7
	[7:5]	not used			<000>
	[4]	Buck3 Phase Sync EN	Enable Buck3 Phase Synchronization function	0: Disabled 1: Enabled	<0>
	[3]	Buck3 SS EN	Enable Buck3 PFM Spread Spectrum function in PFM mode	0: Disabled 1: Enabled	<0>
	[2]	Buck3 ABS EN	Enable Buck3 ABS (Ultrasonic) mode	0: Disabled 1: Enabled	<1>
	[1]	Buck3 EN SLEEP	Enable Buck3 in SLEEP state	0: Disabled 1: Enabled	<1>
	[0]	Buck3 EN ACTIVE	Enable Buck3 in ACTIVE state	0: Disabled 1: Enabled	<1>
0x2F	Register Name - Buck3 ACTIVE Type - (RW, EEPROM)				0x00 / 0
	[7:6]	not used			<00>
	[5:4]	Buck3 Mode ACTIVE	Set Buck3 operation mode in ACTIVE state	00: Auto PFM/PWM mode 01: Forced PWM mode 1x: Reserved	<00>
	[3:0]	Buck3 Vo ACTIVE	Set Buck3 output voltage in ACTIVE state	Buck3 = 1.8V + 0.1V x Buck3_Vo_ACTIVE[3:0]	<0000>
0x30	Register Name - Buck3 SLEEP Type - (RW, EEPROM)				0x00 / 0
	[7:6]	not used			<00>
	[5:4]	Buck3 Mode SLEEP	Set Buck3 operation mode in SLEEP state	00: Auto PFM/PWM mode 01: Forced PWM mode 1x: Reserved	<00>
	[3:0]	Buck3 Vo SLEEP	Set Buck3 output voltage in SLEEP state	Buck3 = 1.8V + 0.1V x Buck3_Vo_SLEEP[3:0]	<0000>

0x31	Register Name - Buck3 Power On Type - (RW, EEPROM)				0x02 / 2
	[7]	not used			<0>
	[6:0]	Buck3 Power On Delay	Delay timed from the beginning of power-on sequence	0: 0ms 1: 1ms … 127: 127ms	<0000010>
0x32	Register Name - Buck3 Power Off Type - (RW, EEPROM)				0x3C / 60
	[7]	not used			<0>
	[6:0]	Buck3 Power Off Delay	Delay timed from the beginning of power-off sequence	0: 0ms 1: 1ms … 127: 127ms	<0111100>
0x33	Register Name - Buck3 SR Type - (RW, EEPROM)				0x5A / 90
	[7:6]	Buck3 TSoftStart	Set Buck3 soft-start time	00: 4ms 01: 2ms 10: 1ms 11: 0.5ms	<01>
	[5:4]	Buck3 TShutDown	Set Buck3 shutdown period. Note: this setting sets the Shut Down SR when Shutdown Option Buck is set to 2b'00, 2b'01 or 2b'10. In addition, when CEN goes from high to low, the shutdown period starts to count from the time when the last rail is turned off. At the end of the shutdown period the FSM transitions to {STANDBY} then onward to {RESET}.	00: 4ms 01: 2ms 10: 1ms 11: 0.5ms	<01>
	[3:2]	Buck3 DVS SRup	Set Buck3 output ramp-up slew rate	00: 2mV/μs 01: 4mV/μs 10: 8mV/μs 11: 16mV/μs	<10>
	[1:0]	Buck3 DVS SRdn	Set Buck3 output ramp-down slew rate	00: 2mV/μs 01: 4mV/μs 10: 8mV/μs 11: 16mV/μs	<10>

0x34	Register Name - Buck3 Config Type - (RW, EEPROM)				0x1A / 26
	[7]	not used			<0>
	[6:5]	Buck3 Phase Sync Delay	Set Buck3 phase shift relative to the internal clock when Buck1 Phase Sync EN is enabled	00: 0deg 01: 90deg 10: 180deg 11: 270deg	<00>
	[4:2]	Buck3 SW Freq	Set Buck3 switching frequency when in PWM operation	000: 0.667MHz 001: 0.769MHz 010: 0.833MHz 011: 1MHz 100: 1.11MHz 101: 1.33MHz 110: 1.54MHz 111: 1.67MHz	<110>
	[1:0]	Buck3 Discharge	Set Buck3 output discharge resistance	00: Disabled 01: Slow 10: Medium 11: Fast	<10>
0x35	Register Name - Buck4 Enable Type - (RW, EEPROM)				0x07 / 7
	[7:5]	not used			<000>
	[4]	Buck4 Phase Sync EN	Enable Buck4 Phase Synchronization function	0: Disabled 1: Enabled	<0>
	[3]	Buck4 SS EN	Enable Buck4 PFM Spread Spectrum function in PFM mode	0: Disabled 1: Enabled	<0>
	[2]	Buck4 ABS EN	Enable Buck4 ABS (Ultrasonic) mode	0: Disabled 1: Enabled	<1>
	[1]	Buck4 EN SLEEP	Enable Buck4 in SLEEP state	0: Disabled 1: Enabled	<1>
	[0]	Buck4 EN ACTIVE	Enable Buck4 in ACTIVE state	0: Disabled 1: Enabled	<1>
0x36	Register Name - Buck4 ACTIVE Type - (RW, EEPROM)				0x0F / 15
	[7:6]	not used			<00>
	[5:4]	Buck4 Mode ACTIVE	Set Buck4 operation mode in ACTIVE state	00: Auto PFM/PWM mode 01: Forced PWM mode 1x: Reserved	<00>
	[3:0]	Buck4 Vo ACTIVE	Set Buck4 output voltage in ACTIVE state	A0: Vo=1.8V + 0.1V x Buck4_Vo_ACTIVE[3:0] A1: Codes 0-8 *decimal Vo= 0.8V + 0.05V x Buck4_Vo_ACTIVE[3:0] A1: Codes 9-15 decimal Vo= 1.5, 1.6, 1.8, 1.85, 2.2, 2.5, 3.3	<1111>

0x37	Register Name - Buck4 SLEEP Type - (RW, EEPROM)				0x0F / 15
	[7:6]	not used			<00>
	[5:4]	Buck4 Mode SLEEP	Set Buck4 operation mode in SLEEP state	00: Auto PFM/PWM mode 01: Forced PWM mode 1x: Reserved	<00>
	[3:0]	Buck4 Vo SLEEP	Set Buck4 output voltage in SLEEP state	A0: Vo=1.8V + 0.1V x Buck4_Vo_SLEEP[3:0] A1: Codes 0-8 *decimal Vo= 0.8V + 0.05V x Buck4_Vo_SLEEP[3:0] A1: Codes 9-15 decimal Vo= 1.5, 1.6, 1.8, 1.85, 2.2, 2.5, 3.3	<1111>
0x38	Register Name - Buck4 Power On Type - (RW, EEPROM)				0x0A / 10
	[7]	not used			<0>
	[6:0]	Buck4 Power On Delay	Delay timed from the beginning of power-on sequence	0: 0ms 1: 1ms … 127: 127ms	<0001010>
0x39	Register Name - Buck4 Power Off Type - (RW, EEPROM)				0x00 / 0
	[7]	not used			<0>
	[6:0]	Buck4 Power Off Delay	Delay timed from the beginning of power-off sequence	0: 0ms 1: 1ms … 127: 127ms	<0000000>
0x3A	Register Name - Buck4 SR Type - (RW, EEPROM)				0x5A / 90
	[7:6]	Buck4 TSoftStart	Set Buck4 soft-start time	00: 4ms 01: 2ms 10: 1ms 11: 0.5ms	<01>
	[5:4]	Buck4 TShutDown	Set Buck4 shutdown period. Note: this setting sets the Shut Down SR when Shutdown Option Buck is set to 2b'00, 2b'01 or 2b'10. In addition, when CEN goes from high to low, the shutdown period starts to count from the time when the last rail is turned off. At the end of the shutdown period the FSM transitions to {STANDBY} then onward to {RESET}.	00: 4ms 01: 2ms 10: 1ms 11: 0.5ms	<01>
	[3:2]	Buck4 DVS SRup	Set Buck4 output ramp-up slew rate	00: 2mV/µs 01: 4mV/µs 10: 8mV/µs 11: 16mV/µs	<10>
	[1:0]	Buck4 DVS SRdn	Set Buck4 output ramp-down slew rate	00: 2mV/µs 01: 4mV/µs 10: 8mV/µs 11: 16mV/µs	<10>

0x3B	Register Name - Buck4 Config Type - (RW, EEPROM)				0x1A / 26
	[7]	not used			<0>
	[6:5]	Buck4 Phase Sync Delay	Set Buck4 phase shift relative to the internal clock when Buck1 Phase Sync EN is enabled	00: 0deg 01: 90deg 10: 180deg 11: 270deg	<00>
	[4:2]	Buck4 SW Freq	Set Buck4 switching frequency when in PWM operation	000: 0.667MHz 001: 0.769MHz 010: 0.833MHz 011: 1MHz 100: 1.11MHz 101: 1.33MHz 110: 1.54MHz 111: 1.67MHz	<110>
	[1:0]	Buck4 Discharge	Set Buck4 output discharge resistance	00: Disabled 01: Slow 10: Medium 11: Fast	<10>
0x3C	Register Name - Buck5 Enable Type - (RW, EEPROM)				0x07 / 7
	[7:5]	not used			<000>
	[4]	Buck5 Phase Sync EN	Enable Buck5 Phase Synchronization function	0: Disabled 1: Enabled	<0>
	[3]	Buck5 SS EN	Enable Buck5 PFM Spread Spectrum function in PFM mode	0: Disabled 1: Enabled	<0>
	[2]	Buck5 ABS EN	Enable Buck5 ABS (Ultrasonic) mode	0: Disabled 1: Enabled	<1>
	[1]	Buck5 EN SLEEP	Enable Buck5 in SLEEP state	0: Disabled 1: Enabled	<1>
	[0]	Buck5 EN ACTIVE	Enable Buck5 in ACTIVE state	0: Disabled 1: Enabled	<1>
0x3D	Register Name - Buck5 ACTIVE Type - (RW, EEPROM)				0x00 / 0
	[7:5]	not used			<000>
	[4:3]	Buck5 Mode ACTIVE	Set Buck5 operation mode in ACTIVE state	00: Auto PFM/PWM mode 01: Forced PWM mode 1x: Reserved	<00>
	[2:0]	Buck5 Vo ACTIVE	Set Buck5 output voltage in ACTIVE state	000: 1.2V 001: 1.5V 010: 1.6V 011: 1.8V 100: 1.85V 101: 2.2V 110: 2.5V 111: 3.3V	<000>

0x3E	Register Name - Buck5 SLEEP Type - (RW, EEPROM)				0x00 / 0
	[7:5]	not used			<000>
	[4:3]	Buck5 Mode SLEEP	Set Buck5 operation mode in SLEEP state	00: Auto PFM/PWM mode 01: Forced PWM mode 1x: Reserved	<00>
	[2:0]	Buck5 Vo SLEEP	Set Buck5 output voltage in SLEEP state	000: 1.2V 001: 1.5V 010: 1.6V 011: 1.8V 100: 1.85V 101: 2.2V 110: 2.5V 111: 3.3V	<000>
0x3F	Register Name - Buck5 Power On Type - (RW, EEPROM)				0x0F / 15
	[7]	not used			<0>
	[6:0]	Buck5 Power On Delay	Delay timed from the beginning of power-on sequence	0: 0ms 1: 1ms … 127: 127ms	<0001111>
0x40	Register Name - Buck5 Power Off Type - (RW, EEPROM)				0x00 / 0
	[7]	not used			<0>
	[6:0]	Buck5 Power Off Delay	Delay timed from the beginning of power-off sequence	0: 0ms 1: 1ms … 127: 127ms	<0000000>
0x41	Register Name - Buck5 SR Type - (RW, EEPROM)				0x5A / 90
	[7:6]	Buck5 TSoftStart	Set Buck5 soft-start time	00: 4ms 01: 2ms 10: 1ms 11: 0.5ms	<01>
	[5:4]	Buck5 TShutDown	Set Buck5 shutdown period. Note: this setting sets the Shut Down SR when Shutdown Option Buck is set to 2b'00, 2b'01 or 2b'10. In addition, when CEN goes from high to low, the shutdown period starts to count from the time when the last rail is turned off. At the end of the shutdown period the FSM transitions to {STANDBY} then onward to {RESET}.	00: 4ms 01: 2ms 10: 1ms 11: 0.5ms	<01>
	[3:2]	Buck5 DVS SRup	Set Buck5 output ramp-up slew rate	00: 2mV/µs 01: 4mV/µs 10: 8mV/µs 11: 16mV/µs	<10>
	[1:0]	Buck5 DVS SRdn	Set Buck5 output ramp-down slew rate	00: 2mV/µs 01: 4mV/µs 10: 8mV/µs 11: 16mV/µs	<10>

0x42	Register Name - Buck5 Config Type - (RW, EEPROM)				0x1A / 26
	[7]	not used			<0>
	[6:5]	Buck5 Phase Sync Delay	Set Buck5 phase shift relative to the internal clock when Buck1 Phase Sync EN is enabled	00: 0deg 01: 90deg 10: 180deg 11: 270deg	<00>
	[4:2]	Buck5 SW Freq	Set Buck5 switching frequency when in PWM operation	000: 0.667MHz 001: 0.769MHz 010: 0.833MHz 011: 1MHz 100: 1.11MHz 101: 1.33MHz 110: 1.54MHz 111: 1.67MHz	<110>
	[1:0]	Buck5 Discharge	Set Buck5 output discharge resistance	00: Disabled 01: Slow 10: Medium 11: Fast	<10>
0x43	Register Name - Buck6 Enable Type - (RW, EEPROM)				0x07 / 7
	[7:5]	not used			<000>
	[4]	Buck6 Phase Sync EN	Enable Buck6 Phase Synchronization function	0: Disabled 1: Enabled	<0>
	[3]	Buck6 SS EN	Enable Buck6 PFM Spread Spectrum function in PFM mode	0: Disabled 1: Enabled	<0>
	[2]	Buck6 ABS EN	Enable Buck6 ABS (Ultrasonic) mode	0: Disabled 1: Enabled	<1>
	[1]	Buck6 EN SLEEP	Enable Buck6 in SLEEP state	0: Disabled 1: Enabled	<1>
	[0]	Buck6 EN ACTIVE	Enable Buck6 in ACTIVE state	0: Disabled 1: Enabled	<1>
0x44	Register Name - Buck6 ACTIVE Type - (RW, EEPROM)				0xD0 / 208
	[7]	Link Buck6 to Buck2	Link the sequencing of Buck 6 to Buck 2	0: Buck 6 and Buck 2 soft-start independently 1: Buck 6 and Buck 2 soft-start together	<1>
	[6]	VTTREF EN	When VTTREF EN is set to '1', buck6 (VTT) = VREFOUT	0: Disabled 1: Enabled	<1>
	[5:4]	Buck6 Mode ACTIVE	Set Buck6 operation mode in ACTIVE state	00: Auto PFM/PWM mode 01: Forced PWM mode 1x: Reserved	<01>
	[3:0]	reserved			<0000>
0x45	Register Name - Buck6 SLEEP Type - (RW, EEPROM)				0xC0 / 192
	[7:6]	EnPD VTTRef	Config the pull down resistor for VTTREF	00: Disabled 01: Slow 10: Medium 11: Fast	<11>
	[5:4]	Buck6 Mode SLEEP	Set Buck6 operation mode in SLEEP state	00: Auto PFM/PWM mode 01: Forced PWM mode 1x: Reserved	<00>
	[3:0]	reserved			<0000>

0x46	Register Name - Buck6 Power On Type - (RW, EEPROM)				0x0A / 10
	[7]	not used			<0>
	[6:0]	Buck6 Power On Delay	Delay timed from the beginning of power-on sequence	0: 0ms 1: 1ms … 127: 127ms	<0001010>
0x47	Register Name - Buck6 Power Off Type - (RW, EEPROM)				0x00 / 0
	[7]	not used			<0>
	[6:0]	Buck6 Power Off Delay	Delay timed from the beginning of power-off sequence	0: 0ms 1: 1ms … 127: 127ms	<0000000>
0x48	Register Name - Buck6 SR Type - (RW, EEPROM)				0x5A / 90
	[7:6]	Buck6 TSoftStart	Set Buck6 soft-start time	00: 4ms 01: 2ms 10: 1ms 11: 0.5ms	<01>
	[5:4]	Buck6 TShutDown	Set Buck6 shutdown period. Note: this setting sets the Shut Down SR when Shutdown Option Buck is set to 2b'00, 2b'01 or 2b'10. In addition, when CEN goes from high to low, the shutdown period starts to count from the time when the last rail is turned off. At the end of the shutdown period the FSM transitions to {STANDBY} then onward to {RESET}.	00: 4ms 01: 2ms 10: 1ms 11: 0.5ms	<01>
	[3:2]	Buck6 DVS SRup	Set Buck6 output ramp-up slew rate	00: 2mV/µs 01: 4mV/µs 10: 8mV/µs 11: 16mV/µs	<10>
	[1:0]	Buck6 DVS SRdn	Set Buck6 output ramp-down slew rate	00: 2mV/µs 01: 4mV/µs 10: 8mV/µs 11: 16mV/µs	<10>

0x49	Register Name - Buck6 Config Type - (RW, EEPROM)				0x03 / 3
	[7]	not used			<0>
	[6:5]	Buck6 Phase Sync Delay	Set Buck6 phase shift relative to the internal clock when Buck1 Phase Sync EN is enabled	00: 0deg 01: 90deg 10: 180deg 11: 270deg	<00>
	[4:2]	Buck6 SW Freq	Set Buck6 switching frequency when in PWM operation	000: 0.667MHz 001: 0.769MHz 010: 0.833MHz 011: 1MHz 100: 1.11MHz 101: 1.33MHz 110: 1.54MHz 111: 1.67MHz	<000>
	[1:0]	Buck6 Discharge	Set Buck6 output discharge resistance when it is configured as an individual regulator	00: Disabled 01: Slow 10: Medium 11: Fast	<11>
0x4A	Register Name - LDO1 ACTIVE Type - (RW, EEPROM)				0x7C / 124
	[7]	LDO1 Bypass	Set LDO1 to bypass mode	0: Normal LDO mode 1: Bypass mode	<0>
	[6]	LDO1 EN ACTIVE	Enable LDO1 in ACTIVE state	0: Disabled 1: Enabled	<1>
	[5:3]	LDO1 Vo 1 ACTIVE	Set LDO1 output voltage in ACTIVE state when LDO_SEL1 = HIGH	000: 0.8V 001: 0.9V 010: 1.2V 011: 1.5V 100: 1.8V 101: 2.5V 110: 3V 111: 3.3V	<111>
	[2:0]	LDO1 Vo 0 ACTIVE	Set LDO1 output voltage in ACTIVE state when LDO_SEL1 = LOW	000: 0.8V 001: 0.9V 010: 1.2V 011: 1.5V 100: 1.8V 101: 2.5V 110: 3V 111: 3.3V	<100>
0x4B	Register Name - LDO1 SLEEP Type - (RW, EEPROM)				0x0C / 12
	[7:4]	not used			<0000>
	[3]	LDO1 EN SLEEP	Enable LDO1 in SLEEP state	0: Disabled 1: Enabled	<1>
	[2:0]	LDO1 Vo SLEEP	Set LDO1 output voltage in SLEEP state (LDO_SEL1 pin change is ignored)	000: 0.8V 001: 0.9V 010: 1.2V 011: 1.5V 100: 1.8V 101: 2.5V 110: 3V 111: 3.3V	<100>

0x4C	Register Name - LDO1 Power On Type - (RW, EEPROM)				0x0A / 10
	[7]	not used			<0>
	[6:0]	LDO1 Power On Delay	Delay timed from the beginning of power-on sequence	0: 0ms 1: 1ms … 127: 127ms	<0001010>
0x4D	Register Name - LDO1 Power Off Type - (RW, EEPROM)				0x00 / 0
	[7]	not used			<0>
	[6:0]	LDO1 Power Off Delay	Delay timed from the beginning of power-off sequence	0: 0ms 1: 1ms … 127: 127ms	<0000000>
0x4E	Register Name - LDO1 SR Type - (RW, EEPROM)				0x5A / 90
	[7:6]	LDO1 TSoftStart	Set LDO1 soft-start time	00: 4ms 01: 2ms 10: 1ms 11: 0.5ms	<01>
	[5:4]	LDO1 TShutDown	Set LDO1 shutdown period. Note: this setting sets the Shut Down SR when Shutdown Option Buck is set to 2b'00, 2b'01 or 2b'10. In addition, when CEN goes from high to low, the shutdown period starts to count from the time when the last rail is turned off. At the end of the shutdown period the FSM transitions to {STANDBY} then onward to {RESET}.	00: 4ms 01: 2ms 10: 1ms 11: 0.5ms	<01>
	[3:2]	LDO1 DVS SRup	Set LDO1 output ramp-up slew rate	00: 2mV/µs 01: 4mV/µs 10: 8mV/µs 11: 16mV/µs	<10>
	[1:0]	LDO1 DVS SRdn	Set LDO1 output ramp-down slew rate	00: 2mV/µs 01: 4mV/µs 10: 8mV/µs 11: 16mV/µs	<10>

0x4F	Register Name - LDO2 ACTIVE Type - (RW, EEPROM)				0x7C / 124
	[7]	LDO2 Bypass	Set LDO2 to bypass mode	0: Normal LDO mode 1: Bypass mode	<0>
	[6]	LDO2 EN ACTIVE	Enable LDO2 in ACTIVE state	0: Disabled 1: Enabled	<1>
	[5:3]	LDO2 Vo 1 ACTIVE	Set LDO2 output voltage in ACTIVE state when LDO_SEL2 = HIGH	000: 0.8V 001: 0.9V 010: 1.2V 011: 1.5V 100: 1.8V 101: 2.5V 110: 3V 111: 3.3V	<111>
	[2:0]	LDO2 Vo 0 ACTIVE	Set LDO2 output voltage in ACTIVE state when LDO_SEL2 = LOW	000: 0.8V 001: 0.9V 010: 1.2V 011: 1.5V 100: 1.8V 101: 2.5V 110: 3V 111: 3.3V	<100>
0x50	Register Name - LDO2 SLEEP Type - (RW, EEPROM)				0x0C / 12
	[7:4]	not used			<0000>
	[3]	LDO2 EN SLEEP	Enable LDO2 in SLEEP state	0: Disabled 1: Enabled	<1>
	[2:0]	LDO2 Vo SLEEP	Set LDO2 output voltage in SLEEP state (LDO_SEL2 pin is ignored)	000: 0.8V 001: 0.9V 010: 1.2V 011: 1.5V 100: 1.8V 101: 2.5V 110: 3V 111: 3.3V	<100>
0x51	Register Name - LDO2 Power On Type - (RW, EEPROM)				0x0A / 10
	[7]	not used			<0>
	[6:0]	LDO2 Power On Delay	Delay timed from the beginning of power-on sequence	0: 0ms 1: 1ms … 127: 127ms	<0001010>
0x52	Register Name - LDO2 Power Off Type - (RW, EEPROM)				0x00 / 0
	[7]	not used			<0>
	[6:0]	LDO2 Power Off Delay	Delay timed from the beginning of power-off sequence	0: 0ms 1: 1ms … 127: 127ms	<0000000>

0x53	Register Name - LDO2 SR Type - (RW, EEPROM)				0x5A / 90
	[7:6]	LDO2 TSoftStart	Set LDO2 soft-start time	00: 4ms 01: 2ms 10: 1ms 11: 0.5ms	<01>
	[5:4]	LDO2 TShutDown	Set LDO2 shutdown period. Note: this setting sets the Shut Down SR when Shutdown Option Buck is set to 2b'00, 2b'01 or 2b'10. In addition, when CEN goes from high to low, the shutdown period starts to count from the time when the last rail is turned off. At the end of the shutdown period the FSM transitions to {STANDBY} then onward to {RESET}.	00: 4ms 01: 2ms 10: 1ms 11: 0.5ms	<01>
	[3:2]	LDO2 DVS SRup	Set LDO2 output ramp-up slew rate	00: 2mV/µs 01: 4mV/µs 10: 8mV/µs 11: 16mV/µs	<10>
	[1:0]	LDO2 DVS SRdn	Set LDO2 output ramp-down slew rate	00: 2mV/µs 01: 4mV/µs 10: 8mV/µs 11: 16mV/µs	<10>
0x54	Register Name - LDO3 ACTIVE SLEEP Type - (RW, EEPROM)				0xED / 237
	[7]	LDO3 EN SLEEP	Enable LDO3 in SLEEP state	0: Disabled 1: Enabled	<1>
	[6]	LDO3 EN ACTIVE	Enable LDO3 in ACTIVE state	0: Disabled 1: Enabled	<1>
	[5:3]	LDO3 Vo SLEEP	Set LDO3 output voltage in SLEEP state	000: 0.8V 001: 0.9V 010: 1.2V 011: 1.5V 100: 1.8V 101: 2.5V 110: 3V 111: 3.3V	<101>
	[2:0]	LDO3 Vo ACTIVE	Set LDO3 output voltage in ACTIVE state	000: 0.8V 001: 0.9V 010: 1.2V 011: 1.5V 100: 1.8V 101: 2.5V 110: 3V 111: 3.3V	<101>
0x55	Register Name - LDO3 Power On Type - (RW, EEPROM)				0x02 / 2
	[7]	not used			<0>
	[6:0]	LDO3 Power On Delay	Delay timed from the beginning of power-on sequence	0: 0ms 1: 1ms … 127: 127ms	<0000010>

0x56	Register Name - LDO3 Power Off Type - (RW, EEPROM)				0x46 / 70
	[7]	not used			<0>
	[6:0]	LDO3 Power Off Delay	Delay timed from the beginning of power-off sequence	0: 0ms 1: 1ms … 127: 127ms	<1000110>
0x57	Register Name - LDO3 SR Type - (RW, EEPROM)				0x5A / 90
	[7:6]	LDO3 TSoftStart	Set LDO3 soft-start time	00: 4ms 01: 2ms 10: 1ms 11: 0.5ms	<01>
	[5:4]	LDO3 TShutDown	Set LDO3 shutdown period. Note: this setting sets the Shut Down SR when Shutdown Option Buck is set to 2b'00, 2b'01 or 2b'10. In addition, when CEN goes from high to low, the shutdown period starts to count from the time when the last rail is turned off. At the end of the shutdown period the FSM transitions to {STANDBY} then onward to {RESET}.	00: 4ms 01: 2ms 10: 1ms 11: 0.5ms	<01>
	[3:2]	LDO3 DVS SRup	Set LDO3 output ramp-up slew rate	00: 2mV/µs 01: 4mV/µs 10: 8mV/µs 11: 16mV/µs	<10>
	[1:0]	LDO3 DVS SRdn	Set LDO3 output ramp-down slew rate	00: 2mV/µs 01: 4mV/µs 10: 8mV/µs 11: 16mV/µs	<10>
0x58	Register Name - LDOs Config Type - (RW, EEPROM)				0x2A / 42
	[7]	not used			<0>
	[6]	LDO3 Bypass	Set LDO3 to bypass mode	0: Normal LDO mode 1: Bypass mode	<0>
	[5:4]	LDO3 Discharge	Set LDO3 output discharge resistance	00: Disabled 01: Slow 10: Medium 11: Fast	<10>
	[3:2]	LDO2 Discharge	Set LDO2 output discharge resistance	00: Disabled 01: Slow 10: Medium 11: Fast	<10>
	[1:0]	LDO1 Discharge	Set LDO1 output discharge resistance	00: Disabled 01: Slow 10: Medium 11: Fast	<10>

0x59	Register Name - Fault Latched Status 1 Type - (RW, Non EEPROM)				0x00 / 0
	[7:6]	not used			<00>
	[5]	Buck6 UV Latched	Buck6 undervoltage fault latched bit. Write '1' to clear the fault	0: OK (normal) 1: Undervoltage fault occurs	<0>
	[4]	Buck5 UV Latched	Buck5 undervoltage fault latched bit. Write '1' to clear the fault	0: OK (normal) 1: Undervoltage fault occurs	<0>
	[3]	Buck4 UV Latched	Buck4 undervoltage fault latched bit. Write '1' to clear the fault	0: OK (normal) 1: Undervoltage fault occurs	<0>
	[2]	Buck3 UV Latched	Buck3 undervoltage fault latched bit. Write '1' to clear the fault	0: OK (normal) 1: Undervoltage fault occurs	<0>
	[1]	Buck2 UV Latched	Buck2 undervoltage fault latched bit. Write '1' to clear the fault	0: OK (normal) 1: Undervoltage fault occurs	<0>
	[0]	Buck1 UV Latched	Buck1 undervoltage fault latched bit. Write '1' to clear the fault	0: OK (normal) 1: Undervoltage fault occurs	<0>
0x5A	Register Name - Fault Latched Status 2 Type - (RW, Non EEPROM)				0x00 / 0
	[7:4]	not used			<0000>
	[3]	VIO Pgood Latched	VIO Pgood latched bit. Write '1' to clear the fault	0: OK (normal) 1: VIO level below its power-good threshold	<0>
	[2]	LDO3 UV Latched	LDO3 undervoltage fault latched bit. Write '1' to clear the fault	0: OK (normal) 1: Undervoltage fault occurs	<0>
	[1]	LDO2 UV Latched	LDO2 undervoltage fault latched bit. Write '1' to clear the fault	0: OK (normal) 1: Undervoltage fault occurs	<0>
	[0]	LDO1 UV Latched	LDO1 undervoltage fault latched bit. Write '1' to clear the fault	0: OK (normal) 1: undervoltage fault occurs	<0>
0x5B	Register Name - Fault Latched Status 3 Type - (RW, Non EEPROM)				0x00 / 0
	[7:6]	not used			<00>
	[5]	Buck6 OV Latched	Buck6 overvoltage fault latched bit. Write '1' to clear the fault	0: OK (normal) 1: Overvoltage fault occurs	<0>
	[4]	Buck5 OV Latched	Buck5 overvoltage fault latched bit. Write '1' to clear the fault	0: OK (normal) 1: Overvoltage fault occurs	<0>
	[3]	Buck4 OV Latched	Buck4 overvoltage fault latched bit. Write '1' to clear the fault	0: OK (normal) 1: Overvoltage fault occurs	<0>
	[2]	Buck3 OV Latched	Buck3 overvoltage fault latched bit. Write '1' to clear the fault	0: OK (normal) 1: Overvoltage fault occurs	<0>
	[1]	Buck2 OV Latched	Buck2 overvoltage fault latched bit. Write '1' to clear the fault	0: OK (normal) 1: Overvoltage fault occurs	<0>
	[0]	Buck1 OV Latched	Buck1 overvoltage fault latched bit. Write '1' to clear the fault	0: OK (normal) 1: Overvoltage fault occurs	<0>
0x5C	Register Name - Fault Latched Status 4 Type - (RW, Non EEPROM)				0x00 / 0
	[7:1]	not used			<0000000>
	[0]	Buck1 HC Latched	Buck1 high current warning latched bit. Write '1' to clear the fault	0: OK (normal) 1: High-current fault occurs	<0>
0x5D	Register Name - Fault Latched Status 5 Type - (RW, Non EEPROM)				0x01 / 1
	[7:1]	not used			<0000000>
	[0]	NVM Read Complete	This bit is set to '1' by the device at the end of {READ_EE} if EEPROM values are read into the registers successfully	0: Failed data loading 1: Completed data loading	<1>

0x5E	Register Name - Fault Latched Status 6 Type - (RW, Non EEPROM)				0x00 / 0
	[7]	PgoodCCBAT Latched	VBAT Pgood latched bit. Write '1' to clear the fault. This bit is edge sensitive.	0: OK (normal) 1: Battery voltage is below its power-good threshold	<0>
	[6]	VREFIN UVLO Latched	VREFIN UVLO fault latched bit. Write '1' to clear the fault.	0: OK (normal) 1: VREFIN UVLO occurs	<0>
	[5]	AVDD UVPD Latched	AVDD undervoltage power down fault latched bit. Write '1' to clear the fault.	0: OK (normal) 1: AVDD UVPD occurs	<0>
	[4]	NVM Error Latched	This bit gets set when any of the following conditions occurs: 1) There are ECC errors (both corrected and uncorrected). 2) The EEPROM voltage is not sufficient. 3) The EEPROM data is not valid. Write '1' to clear this bit which clears the detail bit(s) in 0x83/4/5.	0: OK (normal) 1: ECC error detected, insufficient EEPROM voltage or invalid EEPROM data	<0>
	[3]	CRST Triggered Latched	CRST Triggered latched bit. Write '1' to clear the fault	0: OK (normal) 1: CRST_IN# is asserted	<0>
	[2]	WDT Error Latched	WDT Error latched bit. Write '1' to clear the fault	0: OK (normal) 1: WDT Error occurs	<0>
	[1]	OTP Latched	Over temperature fault latched bit. Write '1' to clear the fault	0: OK (normal) 1: Over temperature fault occurs	<0>
	[0]	OTP WARN Latched	Over temperature warning latched bit. Write '1' to clear the fault	0: OK (normal) 1: Over temperature warning occurs	<0>
0x5F	Register Name - Fault Live Status 1 Type - (Read-Only)				0x00 / 0
	[7:6]	not used			<00>
	[5]	Buck6 UV Live	Buck6 undervoltage fault live bit. This bit is automatically cleared when the fault condition subsides.	0: OK (normal) 1: Undervoltage fault occurs	<0>
	[4]	Buck5 UV Live	Buck5 undervoltage fault live bit. This bit is automatically cleared when the fault condition subsides.	0: OK (normal) 1: Undervoltage fault occurs	<0>
	[3]	Buck4 UV Live	Buck4 undervoltage fault live bit. This bit is automatically cleared when the fault condition subsides.	0: OK (normal) 1: Undervoltage fault occurs	<0>
	[2]	Buck3 UV Live	Buck3 undervoltage fault live bit. This bit is automatically cleared when the fault condition subsides.	0: OK (normal) 1: Undervoltage fault occurs	<0>
	[1]	Buck2 UV Live	Buck2 undervoltage fault live bit. This bit is automatically cleared when the fault condition subsides.	0: OK (normal) 1: Undervoltage fault occurs	<0>
	[0]	Buck1 UV Live	Buck1 undervoltage fault live bit. This bit is automatically cleared when the fault condition subsides.	0: OK (normal) 1: Undervoltage fault occurs	<0>

0x60	Register Name - Fault Live Status 2 Type - (Read-Only)				0x00 / 0
	[7:3]	not used			<00000>
	[2]	LDO3 PGood Live	LDO3 Pgood live bit. This bit is monitored when the LDO is enabled and disabled.	0: PGood HIGH 1: PGood LOW	<0>
	[1]	LDO2 PGood Live	LDO2 Pgood live bit. This bit is monitored when the LDO is enabled and disabled.	0: PGood HIGH 1: PGood LOW	<0>
	[0]	LDO1 PGood Live	LDO1 Pgood live bit. This bit is monitored when the LDO is enabled and disabled.	0: PGood HIGH 1: PGood LOW	<0>
0x61	Register Name - Fault Live Status 3 Type - (Read-Only)				0x00 / 0
	[7:6]	not used			<00>
	[5]	Buck6 OV Live	Buck6 overvoltage fault live bit. This bit is automatically cleared when the fault condition subsides.	0: OK (normal) 1: Overvoltage fault occurs	<0>
	[4]	Buck5 OV Live	Buck5 overvoltage fault live bit. This bit is automatically cleared when the fault condition subsides.	0: OK (normal) 1: Overvoltage fault occurs	<0>
	[3]	Buck4 OV Live	Buck4 overvoltage fault live bit. This bit is automatically cleared when the fault condition subsides.	0: OK (normal) 1: Overvoltage fault occurs	<0>
	[2]	Buck3 OV Live	Buck3 overvoltage fault live bit. This bit is automatically cleared when the fault condition subsides.	0: OK (normal) 1: Overvoltage fault occurs	<0>
	[1]	Buck2 OV Live	Buck2 overvoltage fault live bit. This bit is automatically cleared when the fault condition subsides.	0: OK (normal) 1: Overvoltage fault occurs	<0>
	[0]	Buck1 OV Live	Buck1 overvoltage fault live bit. This bit is automatically cleared when the fault condition subsides.	0: OK (normal) 1: Overvoltage fault occurs	<0>
0x62	Register Name - Fault Live Status 4 Type - (Read-Only)				0x00 / 0
	[7:1]	not used			<0000000>
	[0]	Buck1 HC Live	Buck1 high current warning live bit. This bit is automatically cleared when the fault condition subsides.	0: OK (normal) 1: High-current fault occurs	<0>

0x63	Register Name - Fault Live Status 6 Type - (Read-Only)				0x00 / 0
	[7]	PgoodCCBAT Live	VBAT Pgood live bit. This bit is automatically cleared when the fault condition subsides.	0: OK (normal) 1: PgoodCCBAT fault occurs	<0>
	[6]	VREFIN UVLO Live	VREFIN UVLO fault live bit. This bit is automatically cleared when the fault condition subsides.	0: OK (normal) 1: VREFIN UVLO occurs	<0>
	[5]	AVDD UVPD Live	AVDD undervoltage power down live bit. This bit is automatically cleared when the fault condition subsides.	0: OK (normal) 1: AVDD UVPD occurs	<0>
	[4]	not used			<0>
	[3]	CRST Triggered Live	CRST Triggered live bit. This bit is automatically cleared when the fault condition subsides.	0: OK (normal) 1: The FSM is currently transitioning to either IORESET or FAULT_OUT	<0>
	[2]	WDT Error Live	WDT Error live bit. This bit is automatically cleared when the fault condition subsides.	0: OK (normal) 1: The watchdog timer has expired and is not currently counting	<0>
	[1]	OTP Live	Over temperature fault live bit. This bit is automatically cleared when the fault condition subsides.	0: OK (normal) 1: Over temperature fault occurs	<0>
	[0]	OTP WARN Live	Over temperature warning live bit. This bit is automatically cleared when the fault condition subsides.	0: OK (normal) 1: Over temperature warning occurs	<0>
0x64	Register Name - nINT Mask 1 Type - (RW, EEPROM)				0x00 / 0
	[7:6]	not used			<00>
	[5]	Buck6 UV nINT Mask	Configure INT# pin response to Buck6 UV fault	0: Unmask undervoltage fault from INT# pin 1: Mask undervoltage fault from INT# pin	<0>
	[4]	Buck5 UV nINT Mask	Configure INT# pin response to Buck5 UV fault	0: Unmask undervoltage fault from INT# pin 1: Mask undervoltage fault from INT# pin	<0>
	[3]	Buck4 UV nINT Mask	Configure INT# pin response to Buck4 UV fault	0: Unmask undervoltage fault from INT# pin 1: Mask undervoltage fault from INT# pin	<0>
	[2]	Buck3 UV nINT Mask	Configure INT# pin response to Buck3 UV fault	0: Unmask undervoltage fault from INT# pin 1: Mask undervoltage fault from INT# pin	<0>
	[1]	Buck2 UV nINT Mask	Configure INT# pin response to Buck2 UV fault	0: Unmask undervoltage fault from INT# pin 1: Mask undervoltage fault from INT# pin	<0>
	[0]	Buck1 UV nINT Mask	Configure INT# pin response to Buck1 UV fault	0: Unmask undervoltage fault from INT# pin 1: Mask undervoltage fault from INT# pin	<0>

0x65	Register Name - nINT Mask 2 Type - (RW, EEPROM)				0x00 / 0
	[7:4]	not used			<0000>
	[3]	VIO Pgood nINT mask	Configure INT# pin response to the loss of VIO Pgood	0: Unmask VIO Pgood fault from INT# pin 1: Mask VIO Pgood fault from INT# pin	<0>
	[2]	LDO3 UV nINT Mask	Configure INT# pin response to LDO3 UV fault	0: Unmask undervoltage fault from INT# pin 1: Mask undervoltage fault from INT# pin	<0>
	[1]	LDO2 UV nINT Mask	Configure INT# pin response to LDO2 UV fault	0: Unmask undervoltage fault from INT# pin 1: Mask undervoltage fault from INT# pin	<0>
	[0]	LDO1 UV nINT Mask	Configure INT# pin response to LDO1 UV fault	0: Unmask undervoltage fault from INT# pin 1: Mask undervoltage fault from INT# pin	<0>
0x66	Register Name - nINT Mask 3 Type - (RW, EEPROM)				0x00 / 0
	[7:6]	not used			<00>
	[5]	Buck6 OV nINT Mask	Configure INT# pin response to Buck6 OV fault	0: Unmask over-voltage fault from INT# pin 1: Mask over-voltage fault from INT# pin	<0>
	[4]	Buck5 OV nINT Mask	Configure INT# pin response to Buck5 OV fault	0: Unmask over-voltage fault from INT# pin 1: Mask over-voltage fault from INT# pin	<0>
	[3]	Buck4 OV nINT Mask	Configure INT# pin response to Buck4 OV fault	0: Unmask over-voltage fault from INT# pin 1: Mask over-voltage fault from INT# pin	<0>
	[2]	Buck3 OV nINT Mask	Configure INT# pin response to Buck3 OV fault	0: Unmask over-voltage fault from INT# pin 1: Mask over-voltage fault from INT# pin	<0>
	[1]	Buck2 OV nINT Mask	Configure INT# pin response to Buck2 OV fault	0: Unmask over-voltage fault from INT# pin 1: Mask over-voltage fault from INT# pin	<0>
	[0]	Buck1 OV nINT Mask	Configure INT# pin response to Buck1 OV fault	0: Unmask over-voltage fault from INT# pin 1: Mask over-voltage fault from INT# pin	<0>
0x67	Register Name - nINT Mask 4 Type - (RW, EEPROM)				0x00 / 0
	[7:1]	not used			<0000000>
	[0]	Buck1 HC nINT Mask	Configure INT# response to Buck1 high current warning event	0: Unmask high-current fault from INT# pin 1: Mask high-current fault from INT# pin	<0>

0x68	Register Name - nINT Mask 6 Type - (RW, EEPROM)				0x00 / 0
	[7]	PgoodCCBAT nINT Mask	Configure INT# response to the loss of VBAT Pgood	0: Unmask PgoodCCBAT fault from INT# pin 1: Mask PgoodCCBAT fault from INT# pin	<0>
	[6]	VREFIN UVLO nINT Mask	Configure INT# response to VREFIN UVLO fault	0: Unmask VREFIN UVLO fault from INT# pin 1: Mask VREFIN UVLO fault from INT# pin	<0>
	[5]	AVDD UVPD nINT Mask	Configure INT# response to AVDD UVPD fault	0: Unmask AVDD UVPD fault from INT# pin 1: Mask AVDD UVPD fault from INT# pin	<0>
	[4]	NVM Error nINT Mask	Configure INT# response to NVM Error	0: Unmask NVM Error from INT# pin 1: Mask NVM Error from INT# pin	<0>
	[3]	CRST Triggered nINT Mask	Configure INT# response to CRST Triggered event	0: Unmask CRST Triggered fault from INT# pin 1: Mask CRST Triggered fault from INT# pin	<0>
	[2]	WDT Error nINT Mask	Configure INT# response to WDT Error event	0: Unmask WDT Error from INT# pin 1: Mask WDT Error from INT# pin	<0>
	[1]	OTP nINT Mask	Configure INT# response to OTP fault	0: Unmask Over Temp fault from INT# pin 1: Mask Over Temp fault from INT# pin	<0>
	[0]	OTP WARN nINT Mask	Configure INT# response to OTP warning event	0: Unmask Over Temp Warning from INT# pin 1: Mask Over Temp Warning from INT# pin	<0>
0x69	Register Name - Fault Config 1 Type - (RW, EEPROM)				0x3F / 63
	[7:6]	not used			<00>
	[5]	Buck6 UV Disable	Configure the device response to Buck6 UV fault	0: UV fault does not shut down any rail 1: UV fault shuts down all the rails	<1>
	[4]	Buck5 UV Disable	Configure the device response to Buck5 UV fault	0: UV fault does not shut down any rail 1: UV fault shuts down all the rails	<1>
	[3]	Buck4 UV Disable	Configure the device response to Buck4 UV fault	0: UV fault does not shut down any rail 1: UV fault shuts down all the rails	<1>
	[2]	Buck3 UV Disable	Configure the device response to Buck3 UV fault	0: UV fault does not shut down any rail 1: UV fault shuts down all the rails	<1>
	[1]	Buck2 UV Disable	Configure the device response to Buck2 UV fault	0: UV fault does not shut down any rail 1: UV fault shuts down all the rails	<1>
	[0]	Buck1 UV Disable	Configure the device response to Buck1 UV fault	0: UV fault does not shut down any rail 1: UV fault shuts down all the rails	<1>

0x6A	Register Name - Fault Config 2 Type - (RW, EEPROM)				0x07 / 7
	[7:3]	not used			<00000>
	[2]	LDO3 UV Disable	Configure the device response to LDO3 UV fault	0: UV fault does not shut down any rail 1: UV fault shuts down all the rails	<1>
	[1]	LDO2 UV Disable	Configure the device response to LDO2 UV fault	0: UV fault does not shut down any rail 1: UV fault shuts down all the rails	<1>
	[0]	LDO1 UV Disable	Configure the device response to LDO1 UV fault	0: UV fault does not shut down any rail 1: UV fault shuts down all the rails	<1>
0x6B	Register Name - Fault Config 3 Type - (RW, EEPROM)				0x7F / 127
	[7]	not used			<0>
	[6]	VREFIN UVLO Disable	Configure the device response to VREFIN UVLO fault	0: VREFIN UVLO fault does not shut down any rail 1: VREFIN UVLO fault shuts down all the rails	<1>
	[5]	Buck6 OV Disable	Configure the device response to Buck6 OV fault	0: OV fault does not shut down any rail 1: OV fault shuts down all the rails	<1>
	[4]	Buck5 OV Disable	Configure the device response to Buck5 OV fault	0: OV fault does not shut down any rail 1: OV fault shuts down all the rails	<1>
	[3]	Buck4 OV Disable	Configure the device response to Buck4 OV fault	0: OV fault does not shut down any rail 1: OV fault shuts down all the rails	<1>
	[2]	Buck3 OV Disable	Configure the device response to Buck3 OV fault	0: OV fault does not shut down any rail 1: OV fault shuts down all the rails	<1>
	[1]	Buck2 OV Disable	Configure the device response to Buck2 OV fault	0: OV fault does not shut down any rail 1: OV fault shuts down all the rails	<1>
	[0]	Buck1 OV Disable	Configure the device response to Buck1 OV fault	0: OV fault does not shut down any rail 1: OV fault shuts down all the rails	<1>

0x6C	Register Name - Block EN Type - (RW, EEPROM)				0x00 / 0
	[7]	SLEEP State EN	Configure the device to enter {SLEEP}. This bit is not EEPROM backed	0: Exit SLEEP state 1: Enter SLEEP state	<0>
	[6]	RTC EN	Enable the RTC. This bit is battery backed	0: Disabled 1: Enabled	<0>
	[5]	CC Charger EN	Enable the coin cell battery charger. This bit is not EEPROM backed	0: Disabled 1: Enabled	<0>
	[4]	CCBAT COMP EN	Enable the VBAT comparator	0: Disabled 1: Enabled	<0>
	[3]	WD EN	Enable the watchdog timer	0: Disabled 1: Enabled	<0>
	[2]	WD PD EN	Enable the power-down feature when the watchdog timer expires	0: Disabled 1: Enabled	<0>
	[1]	WD RST EN	Enable the reset feature when the watch-dog timer expires	0: Disabled 1: Enabled	<0>
	[0]	CRST Fault EN	Enable the power-down feature when the CRST_IN# is asserted	0: Disabled 1: Enabled	<0>
0x6D	Register Name - Software Reset Type - (RW, Non EEPROM)				0x00 / 0
	[7:2]	not used			<000000>
	[1]	Warm Reset	Configure the device to do a warm reset	0: Normal 1: Warm reset	<0>
	[0]	Cold Reset	Configure the device to do a cold reset	0: Normal 1: Cold reset	<0>
0x6E	Register Name - I2C Trigger Power Off Type - (RW, Non EEPROM)				0xA8 / 168
	[7:0]	I2C Trigger Power Off key	Read-only. But when a data is written to this register, it will not ignore it. When the write data matches the read value, power off sequence starts.		<10101000>
0x6F	Register Name - Config 1 Type - (RW, EEPROM)				0xFB / 251
	[7]	Charge Current Level	Set the charge current level of the coin cell battery charger when it is enabled	0: 20μA 1: 60μA	<1>
	[6:5]	Thermal Warning Threshold	Set the thermal warning temperature ris-ing threshold	00: 105C 01: 110C 10: 115C 11: 120C	<11>
	[4:3]	Buck1 High Current Threshold	Set the buck1 high current warning thresh-old	00: 4A 01: 5A 10: 5.5A 11: 6A	<11>
	[2:1]	AVDD UVPD Config	Set the AVDD Under Voltage Power Down falling threshold	00: Disable AVDD monitoring 01: 2.7V 10: 3.0V 11: 4.25V	<01>
	[0]	PWRON Config	Set the PWRON configuration	0: On/off switch 1: Long push button	<1>

0x70	Register Name - Config 2 Type - (RW, EEPROM)				0xF8 / 248
	[7:4]	VCCBAT	Set the coin cell battery termination voltage	4'b0000 - 4'b1111: 1.8V + 0.1V*VCCBAT[3:0]	<1111>
	[3:2]	reserved			<10>
	[1:0]	PWRON Hold Period	Set the period in which the PWRON needs to stay high/low when it is configured as long push button	00: 1s 01: 1.5s 10: 2s 11: 3s	<00>
0x71	Register Name - Config 3 Type - (RW, EEPROM)				0x17 / 23
	[7:5]	not used			<000>
	[4:3]	VIO Timeout	Set the timeout period in which VIO_Pgood is monitored. If VIO_Pgood is asserted before the timer expires, then the FSM transitions to {STANDBY} before the end of the timeout period. If VIO_Pgood is not asserted when the timer expires, then the FSM transitions to {FAULT_OUT}.	00: Indefinite 01: 0.5ms 10: 1ms 11: 2ms	<10>
	[2:0]	Cold Reset Delay	Set the time delay from the completion of power-off sequence to the start of power-on	0: No delay 1: 15ms 2: 31ms 3: 63ms 4: 95ms 5: 127ms 6: 191ms 7: 255ms	<111>
0x72	Register Name - MPIO0 Power On Type - (RW, EEPROM)				0x46 / 70
	[7]	not used			<0>
	[6:0]	MPIO0 Power On Delay	Delay timed from the beginning of power-on sequence. The alternative function of bits[3:0] is to select which regulator is used for the PGood when MPIO0 is configured as PGood output. Refer to the settings for details	Bits[6:0] decodes: 0: 0ms 1: 1ms … 127: 127ms Alternative decodes of bits[3:0]: 0000: Buck1 0001: Buck2 0010: Buck3 0011: Buck4 0100: Buck5 0101: Buck6 0110: LDO1 0111: LDO2 1000: LDO3 1001: VTTREF 1010: AND of all regulators PGood	<1000110>
0x73	Register Name - MPIO0 Power Off Type - (RW, EEPROM)				0x00 / 0
	[7]	not used			<0>
	[6:0]	MPIO0 Power Off Delay	Delay timed from the beginning of power-off sequence	0: 0ms 1: 1ms … 127: 127ms	<0000000>

0x74	Register Name - MPIO1 Power On Type - (RW, EEPROM)				0x14 / 20
	[7]	not used			<0>
	[6:0]	MPIO1 Power On Delay	Delay timed from the beginning of power-on sequence. The alternative function of bits[3:0] is to select which regulator is used for the PGood when MPIO1 is configured as PGood output. Refer to the settings for details	Bits[6:0] decodes: 0: 0ms 1: 1ms … 127: 127ms Alternative decodes of bits[3:0]: 0000: Buck1 0001: Buck2 0010: Buck3 0011: Buck4 0100: Buck5 0101: Buck6 0110: LDO1 0111: LDO2 1000: LDO3 1001: VTTREF 1010: AND of all regulators PGood	<0010100>
0x75	Register Name - MPIO1 Power Off Type - (RW, EEPROM)				0x00 / 0
	[7]	not used			<0>
	[6:0]	MPIO1 Power Off Delay	Delay timed from the beginning of power-off sequence	0: 0ms 1: 1ms … 127: 127ms	<0000000>
0x76	Register Name - MPIO2 Power On Type - (RW, EEPROM)				0x04 / 4
	[7]	not used			<0>
	[6:0]	MPIO2 Power On Delay	Delay timed from the beginning of power-on sequence. The alternative function of bits[3:0] is to select which regulator is used for the PGood when MPIO2 is configured as PGood output. Refer to the settings for details	Bits[6:0] decodes: 0: 0ms 1: 1ms … 127: 127ms Alternative decodes of bits[3:0]: 0000: Buck1 0001: Buck2 0010: Buck3 0011: Buck4 0100: Buck5 0101: Buck6 0110: LDO1 0111: LDO2 1000: LDO3 1001: VTTREF 1010: AND of all regulators PGood	<0000100>

0x77	Register Name - MPIO2 Power Off Type - (RW, EEPROM)				0x00 / 0
	[7]	not used			<0>
	[6:0]	MPIO2 Power Off Delay	Delay timed from the beginning of power-off sequence. The alternative function of bits[2:0] is to set the frequency when MPIO2 is configured as 32K_CLK. Refer to the settings for details	Bits[6:0] decodes: 0: 0ms 1: 1ms … 127: 127ms Alternative decodes of bits[2:0]: 000: 32.768kHz 001: 16.384kHz 010: 8.192kHz 011: 4.096kHz 100: 2.048kHz 101: 1.024kHz 110: 512Hz 111: 256Hz	<0000000>
0x78	Register Name - MPIO3 Power On Type - (RW, EEPROM)				0x00 / 0
	[7]	not used			<0>
	[6:0]	MPIO3 Power On Delay	Delay timed from the beginning of power-on sequence. The alternative function of bits[3:0] is to select which regulator is used for the PGood when MPIO3 is configured as PGood output. Refer to the settings for details	Bits[6:0] decodes: 0: 0ms 1: 1ms … 127: 127ms Alternative decodes of bits[3:0]: 0000: Buck1 0001: Buck2 0010: Buck3 0011: Buck4 0100: Buck5 0101: Buck6 0110: LDO1 0111: LDO2 1000: LDO3 1001: VTTREF 1010: AND of all regulators PGood	<0000000>
0x79	Register Name - MPIO3 Power Off Type - (RW, EEPROM)				0x00 / 0
	[7]	not used			<0>
	[6:0]	MPIO3 Power Off Delay	Delay timed from the beginning of power-off sequence	0: 0ms 1: 1ms … 127: 127ms	<0000000>

0x7A	Register Name - MPIO4 Power On Type - (RW, EEPROM)				0x00 / 0
	[7]	not used			<0>
	[6:0]	MPIO4 Power On Delay	Delay timed from the beginning of power-on sequence. The alternative function of bits[3:0] is to select which regulator is used for the PGood when MPIO4 is configured as PGood output. Refer to the settings for details	Bits[6:0] decodes: 0: 0ms 1: 1ms … 127: 127ms Alternative decodes of bits[3:0]: 0000: Buck1 0001: Buck2 0010: Buck3 0011: Buck4 0100: Buck5 0101: Buck6 0110: LDO1 0111: LDO2 1000: LDO3 1001: VTTREF 1010: AND of all regulators PGood	<0000000>
0x7B	Register Name - MPIO4 Power Off Type - (RW, EEPROM)				0x00 / 0
	[7]	not used			<0>
	[6:0]	MPIO4 Power Off Delay	Delay timed from the beginning of power-off sequence. The alternative function of bits[3:0] is used to set the timeout period when MPIO4 is configured as Watchdog Timer Reset. Refer to the settings for details	Bits[6:0] decodes: 0: 0ms 1: 1ms … 127: 127ms Alternative decodes of bits[3:0]: 0000: 1ms 0001: 2ms 0010: 4ms 0011: 8ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 256ms 1001: 512ms 1010: 1.024s 1011: 2.048s 1100: 4.096s 1101: 8.192s 1110: 16.384s 1111: 32.768s	<0000000>

0x7C	Register Name - MPIO5 Power On Type - (RW, EEPROM)				0x00 / 0
	[7]	not used			<0>
	[6:0]	MPIO5 Power On Delay	Delay timed from the beginning of power-on sequence. The alternative function of bits[3:0] is used to select which regulator is used for the PGood when MPIO5 is configured as PGood output. Refer to the settings for details	Bits[6:0] decodes: 0: 0ms 1: 1ms … 127: 127ms Alternative decodes of bits[3:0]: 0000: Buck1 0001: Buck2 0010: Buck3 0011: Buck4 0100: Buck5 0101: Buck6 0110: LDO1 0111: LDO2 1000: LDO3 1001: VTTREF 1010: AND of all regulators PGood	<0000000>
0x7D	Register Name - MPIO5 Power Off Type - (RW, EEPROM)				0x00 / 0
	[7]	not used			<0>
	[6:0]	MPIO5 Power Off Delay	Delay timed from the beginning of power-off sequence	0: 0ms 1: 1ms … 127: 127ms	<0000000>
0x7E	Register Name - MPIO Input Status Type - (Read-Only)				0x00 / 0
	[7:6]	not used			<00>
	[5]	MPIO5 Status	Read back the live status of MPIO5	0: Low 1: High	<0>
	[4]	MPIO4 Status	Read back the live status of MPIO4	0: Low 1: High	<0>
	[3]	MPIO3 Status	Read back the live status of MPIO3	0: Low 1: High	<0>
	[2]	MPIO2 Status	Read back the live status of MPIO2	0: Low 1: High	<0>
	[1]	MPIO1 Status	Read back the live status of MPIO1	0: Low 1: High	<0>
	[0]	MPIO0 Status	Read back the live status of MPIO0	0: Low 1: High	<0>

0x7F	Register Name - MPIO I2C Output Type - (RW, Non EEPROM)				0x00 / 0
	[7:6]	not used			<00>
	[5]	MPIO5 I2C Output	Set the status of MPIO5 when its function is set to "Output from I2C output"	0: Set low 1: Set high	<0>
	[4]	MPIO4 I2C Output	Set the status of MPIO4 when its function is set to "Output from I2C output"	0: Set low 1: Set high	<0>
	[3]	MPIO3 I2C Output	Set the status of MPIO3 when its function is set to "Output from I2C output"	0: Set low 1: Set high	<0>
	[2]	MPIO2 I2C Output	Set the status of MPIO2 when its function is set to "Output from I2C output"	0: Set low 1: Set high	<0>
	[1]	MPIO1 I2C Output	Set the status of MPIO1 when its function is set to "Output from I2C output"	0: Set low 1: Set high	<0>
	[0]	MPIO0 I2C Output	Set the status of MPIO0 when its function is set to "Output from I2C output"	0: Set low 1: Set high	<0>

0x80	Register Name - MPIO Assertion Type - (RW, EEPROM)				0x3F / 63
	[7:6]	not used			<00>
	[5]	MPIO5 Assertion	Configure the MPIO5 operation during transition between {ACTIVE} and {SLEEP} when it is set to reset output or External VR EN output	0: A reset output will NOT be asserted (or an external VR enable will NOT be de-asserted) in SLEEP state 1: A reset output will be asserted (or an external VR enable be de-asserted) in SLEEP state	<1>
	[4]	MPIO4 Assertion	Configure the MPIO4 operation during transition between {ACTIVE} and {SLEEP} when it is set to reset output or External VR EN output	0: A reset output will NOT be asserted (or an external VR enable will NOT be de-asserted) in SLEEP state 1: A reset output will be asserted (or an external VR enable be de-asserted) in SLEEP state	<1>
	[3]	MPIO3 Assertion	Configure the MPIO3 operation during transition between {ACTIVE} and {SLEEP} when it is set to reset output or External VR EN output	0: A reset output will NOT be asserted (or an external VR enable will NOT be de-asserted) in SLEEP state 1: A reset output will be asserted (or an external VR enable be de-asserted) in SLEEP state	<1>
	[2]	MPIO2 Assertion	Configure the MPIO2 operation during transition between {ACTIVE} and {SLEEP} when it is set to reset output or External VR EN output	0: A reset output will NOT be asserted (or an external VR enable will NOT be de-asserted) in SLEEP state 1: A reset output will be asserted (or an external VR enable be de-asserted) in SLEEP state	<1>
	[1]	MPIO1 Assertion	Configure the MPIO1 operation during transition between {ACTIVE} and {SLEEP} when it is set to reset output or External VR EN output	0: A reset output will NOT be asserted (or an external VR enable will NOT be de-asserted) in SLEEP state 1: A reset output will be asserted (or an external VR enable be de-asserted) in SLEEP state	<1>
	[0]	MPIO0 Assertion	Configure the MPIO0 operation during transition between {ACTIVE} and {SLEEP} when it is set to reset output or External VR EN output	0: A reset output will NOT be asserted (or an external VR enable will NOT be de-asserted) in SLEEP state 1: A reset output will be asserted (or an external VR enable be de-asserted) in SLEEP state	<1>
0x81	Register Name - Input Pin Status Type - (Read-Only)				0x00 / 0
	[7:5]	not used			<000>
	[4]	VPROG Status	Read back the live status of VPROG	0: Low 1: High	<0>
	[3]	LDO2VSEL Status	Read back the live status of LDO2VSEL	0: Low 1: High	<0>
	[2]	LDO1VSEL Status	Read back the live status of LDO1VSEL	0: Low 1: High	<0>
	[1]	PWRON Status	Read back the live status of PWRON	0: Low 1: High	<0>
	[0]	CEN Status	Read back the live status of CEN	0: Low 1: High	<0>

0x82	Register Name - Report Buck Mode Type - (Read-Only)				0x00 / 0
	[7:6]	not used			<00>
	[5]	Buck6 Mode	Read back the operation status of buck6	0: PFM 1: PWM	<0>
	[4]	Buck5 Mode	Read back the operation status of buck5	0: PFM 1: PWM	<0>
	[3]	Buck4 Mode	Read back the operation status of buck4	0: PFM 1: PWM	<0>
	[2]	Buck3 Mode	Read back the operation status of buck3	0: PFM 1: PWM	<0>
	[1]	Buck2 Mode	Read back the operation status of buck2	0: PFM 1: PWM	<0>
	[0]	Buck1 Mode	Read back the operation status of buck1	0: PFM 1: PWM	<0>
0x83	Register Name - ECC Detail 1 Type - (RW, Non EEPROM)				0x00 / 0
	[7]	EE Bank7 ECC Corrected	Cleared by writing '1' to 0x5E[4] NVM Error bit	0: Bank7 ECC OK (normal) 1: Bank7 ECC corrected flag	<0>
	[6]	EE Bank6 ECC Corrected	Cleared by writing '1' to 0x5E[4] NVM Error bit	0: Bank6 ECC OK (normal) 1: Bank6 ECC corrected flag	<0>
	[5]	EE Bank5 ECC Corrected	Cleared by writing '1' to 0x5E[4] NVM Error bit	0: Bank5 ECC OK (normal) 1: Bank5 ECC corrected flag	<0>
	[4]	EE Bank4 ECC Corrected	Cleared by writing '1' to 0x5E[4] NVM Error bit	0: Bank4 ECC OK (normal) 1: Bank4 ECC corrected flag	<0>
	[3]	EE Bank3 ECC Corrected	Cleared by writing '1' to 0x5E[4] NVM Error bit	0: Bank3 ECC OK (normal) 1: Bank3 ECC corrected flag	<0>
	[2]	EE Bank2 ECC Corrected	Cleared by writing '1' to 0x5E[4] NVM Error bit	0: Bank2 ECC OK (normal) 1: Bank2 ECC corrected flag	<0>
	[1]	EE Bank1 ECC Corrected	Cleared by writing '1' to 0x5E[4] NVM Error bit	0: Bank1 ECC OK (normal) 1: Bank1 ECC corrected flag	<0>
	[0]	EE Bank0 ECC Corrected	Cleared by writing '1' to 0x5E[4] NVM Error bit	0: Bank0 ECC OK (normal) 1: Bank0 ECC corrected flag	<0>

0x84	Register Name - ECC Detail 2 Type - (RW, Non EEPROM)				0x00 / 0
	[7]	EE Bank7 ECC Error	Cleared by writing '1' to 0x5E[4] NVM Error bit	0: Bank7 ECC OK (normal) 1: Bank7 ECC uncorrectable error flag	<0>
	[6]	EE Bank6 ECC Error	Cleared by writing '1' to 0x5E[4] NVM Error bit	0: Bank6 ECC OK (normal) 1: Bank6 ECC uncorrectable error flag	<0>
	[5]	EE Bank5 ECC Error	Cleared by writing '1' to 0x5E[4] NVM Error bit	0: Bank5 ECC OK (normal) 1: Bank5 ECC uncorrectable error flag	<0>
	[4]	EE Bank4 ECC Error	Cleared by writing '1' to 0x5E[4] NVM Error bit	0: Bank4 ECC OK (normal) 1: Bank4 ECC uncorrectable error flag	<0>
	[3]	EE Bank3 ECC Error	Cleared by writing '1' to 0x5E[4] NVM Error bit	0: Bank3 ECC OK (normal) 1: Bank3 ECC uncorrectable error flag	<0>
	[2]	EE Bank2 ECC Error	Cleared by writing '1' to 0x5E[4] NVM Error bit	0: Bank2 ECC OK (normal) 1: Bank2 ECC uncorrectable error flag	<0>
	[1]	EE Bank1 ECC Error	Cleared by writing '1' to 0x5E[4] NVM Error bit	0: Bank1 ECC OK (normal) 1: Bank1 ECC uncorrectable error flag	<0>
	[0]	EE Bank0 ECC Error	Cleared by writing '1' to 0x5E[4] NVM Error bit	0: Bank0 ECC OK (normal) 1: Bank0 ECC uncorrectable error flag	<0>
0x85	Register Name - EE Detail Type - (RW, Non EEPROM)				0x00 / 0
	[7:2]	not used			<000000>
	[1]	Valid EE Data	Customer data is considered as valid if either of the EEPROM ID 1/2 registers are non-zero. Cleared by writing '1' to 0x5E[4] NVM Error bit	0: OK (normal) 1: EEPROM data is not valid	<0>
	[0]	EE Error Latched	Cleared by writing '1' to 0x5E[4] NVM Error bit	0: OK (normal) 1: Insufficient EEPROM voltage	<0>

0x86	Register Name - Spread Spectrum 1 Type - (RW, EEPROM)				0x00 / 0
	[7:6]	Freq SS	Spread spectrum modulation frequency	00: 17.5kHz 01: 20kHz 10: 22.5kHz 11: 25kHz	<00>
	[5:4]	PWM AM	Spread spectrum modulation amplitude in PWM mode. Setting these two bits to 2b'00 disables the spread spectrum function in PWM mode for all buck regulators	Pseudo random scheme: 00: 0, 0, 0, 0, 0, 0, 0, 0 01: -1, -1, 0, 0, 0, 0, +1, +1 10: -2, -1, -1, 0, 0, +1, +1, +2 11: -3, -2, -1, 0, 0, +1, +2, +3 Triangular scheme: 00: Disabled 01: -1%, 0, +1% 10: -2%, -1%, 0, +1%, +2% 11: -3%, -2%, -1%, 0, +1%, +2%, +3%	<00>
	[3:2]	Buck6 PFM AM	Buck6 spread spectrum modulation amplitude in PFM mode	00: -1, -1, 0, 0, 0, 0, +1, +1 01: -2, -1, -1, 0, 0, +1, +1, +2 10: -3, -2, -1, 0, 0, +1, +2, +3 11: -4, -3, -1, 0, 0, +1, +3, +4	<00>
	[1:0]	Buck5 PFM AM	Buck5 spread spectrum modulation amplitude in PFM mode	00: -1, -1, 0, 0, 0, 0, +1, +1 01: -2, -1, -1, 0, 0, +1, +1, +2 10: -3, -2, -1, 0, 0, +1, +2, +3 11: -4, -3, -1, 0, 0, +1, +3, +4	<00>
0x87	Register Name - Spread Spectrum 2 Type - (RW, EEPROM)				0x00 / 0
	[7:6]	Buck4 PFM AM	Buck4 spread spectrum modulation amplitude in PFM mode	00: -1, -1, 0, 0, 0, 0, +1, +1 01: -2, -1, -1, 0, 0, +1, +1, +2 10: -3, -2, -1, 0, 0, +1, +2, +3 11: -4, -3, -1, 0, 0, +1, +3, +4	<00>
	[5:4]	Buck3 PFM AM	Buck3 spread spectrum modulation amplitude in PFM mode	00: -1, -1, 0, 0, 0, 0, +1, +1 01: -2, -1, -1, 0, 0, +1, +1, +2 10: -3, -2, -1, 0, 0, +1, +2, +3 11: -4, -3, -1, 0, 0, +1, +3, +4	<00>
	[3:2]	Buck2 PFM AM	Buck2 spread spectrum modulation amplitude in PFM mode	00: -1, -1, 0, 0, 0, 0, +1, +1 01: -2, -1, -1, 0, 0, +1, +1, +2 10: -3, -2, -1, 0, 0, +1, +2, +3 11: -4, -3, -1, 0, 0, +1, +3, +4	<00>
	[1:0]	Buck1 PFM AM	Buck1 spread spectrum modulation amplitude in PFM mode	00: -1, -1, 0, 0, 0, 0, +1, +1 01: -2, -1, -1, 0, 0, +1, +1, +2 10: -3, -2, -1, 0, 0, +1, +2, +3 11: -4, -3, -1, 0, 0, +1, +3, +4	<00>
0x88	Register Name - Spread Spectrum 3 Type - (RW, EEPROM)				0x00 / 0
	[7:1]	not used			<0000000>
	[0]	SS PWM Mod	Set the spread spectrum modulation scheme in PWM mode	0: Triangular modulation 1: Pseudo random modulation	<0>

0x89	Register Name - Shutdown Config Type - (RW, EEPROM)				0x02 / 2
	[7:3]	not used			<00000>
	[2]	Shutdown Option LDO	Config the shutdown options for all LDOs	0: Shut down with discharge resistors using Shut Down SR 1: Shut down with discharge resistors, discharge rate set by RC	<0>
	[1:0]	Shutdown Option Buck	Config the shutdown options for all buck regulators	00: Shut down in forced PWM using Shut Down SR 01: Shut down in PFM/PWM using Shut Down SR 10: Shut down with discharge resistors using Shut Down SR 11: Shut down with discharge resistors, discharge rate set by RC	<10>
0x8A	Register Name - MPIO0 Config Type - (RW, EEPROM)				0x0D / 13
	[7:6]	not used			<00>
	[5]	MPIO0 Invert	Configure the polarity of MPIO0	0: Active low 1: Active high	<0>
	[4:3]	MPIO0 Type	If bits[4:3] = 00, then the respective MPIOx pin is high impedance, and the device will still use the MPIOx power on/off delays if bits[2:0] are not set to 3'b000	00: Disabled (high impedance) 01: Open drain NMOS output 10: Open drain PMOS output 11: Full CMOS output	<01>
	[2:0]	MPIO0 Function	Bits[2:0] = 000 disables the function of the respective MPIOx pin, and the device will ignore the MPIOx power on/off delay settings.	000: Disabled 001: Disabled 010: External VR PGood input 011: Input to I2C register 100: PGood output 101: Reset output 110: External VR EN output 111: Output from I2C output	<101>
0x8B	Register Name - MPIO1 Config Type - (RW, EEPROM)				0x0D / 13
	[7:6]	not used			<00>
	[5]	MPIO1 Invert	Configure the polarity of MPIO1	0: Active low 1: Active high	<0>
	[4:3]	MPIO1 Type	If bits[4:3] = 00, then the respective MPIOx pin is high impedance, and the device will still use the MPIOx power on/off delays if bits[2:0] are not set to 3'b000	00: Disabled (high impedance) 01: Open drain NMOS output 10: Open drain PMOS output 11: Full CMOS output	<01>
	[2:0]	MPIO1 Function	Bits[2:0] = 000 disables the function of the respective MPIOx pin, and the device will ignore the MPIOx power on/off delay settings.	000: Disabled 001: Disabled 010: External VR PGood input 011: Input to I2C register 100: PGood output 101: Reset output 110: External VR EN output 111: Output from I2C output	<101>

0x8C	Register Name - MPIO2 Config Type - (RW, EEPROM)				0x2C / 44
	[7:6]	not used			<00>
	[5]	MPIO2 Invert	Configure the polarity of MPIO2	0: Active low 1: Active high	<1>
	[4:3]	MPIO2 Type	If bits[4:3] = 00, then the respective MPIOx pin is high impedance, and the device will still use the MPIOx power on/off delays if bits[2:0] are not set to 3'b000	00: Disabled (high impedance) 01: Open drain NMOS output 10: Open drain PMOS output 11: Full CMOS output	<01>
	[2:0]	MPIO2 Function	Bits[2:0] = 000 disables the function of the respective MPIOx pin, and the device will ignore the MPIOx power on/off delay settings.	000: Disabled 001: 32K_CLK 010: External VR PGood input 011: Input to I2C register 100: PGood output 101: Reset output 110: External VR EN output 111: Output from I2C output	<100>
0x8D	Register Name - MPIO3 Config Type - (RW, EEPROM)				0x20 / 32
	[7:6]	not used			<00>
	[5]	MPIO3 Invert	Configure the polarity of MPIO3	0: Active low 1: Active high	<1>
	[4:3]	MPIO3 Type	If bits[4:3] = 00, then the respective MPIOx pin is high impedance, and the device will still use the MPIOx power on/off delays if bits[2:0] are not set to 3'b000	00: Disabled (high impedance) 01: Open drain NMOS output 10: Open drain PMOS output 11: Full CMOS output	<00>
	[2:0]	MPIO3 Function	Bits[2:0] = 000 disables the function of the respective MPIOx pin, and the device will ignore the MPIOx power on/off delay settings.	000: Disabled 001: SLEEP# 010: External VR PGood input 011: Input to I2C register 100: PGood output 101: Reset output 110: External VR EN output 111: Output from I2C output	<000>
0x8E	Register Name - MPIO4 Config Type - (RW, EEPROM)				0x00 / 0
	[7:6]	not used			<00>
	[5]	MPIO4 Invert	Configure the polarity of MPIO4	0: Active low 1: Active high	<0>
	[4:3]	MPIO4 Type	If bits[4:3] = 00, then the respective MPIOx pin is high impedance, and the device will still use the MPIOx power on/off delays if bits[2:0] are not set to 3'b000	00: Disabled (high impedance) 01: Open drain NMOS output 10: Open drain PMOS output 11: Full CMOS output	<00>
	[2:0]	MPIO4 Function	Bits[2:0] = 000 disables the function of the respective MPIOx pin, and the device will ignore the MPIOx power on/off delay settings.	000: Disabled 001: WDT_RST# 010: External VR PGood input 011: Input to I2C register 100: PGood output 101: Reset output 110: External VR EN output 111: Output from I2C output	<000>

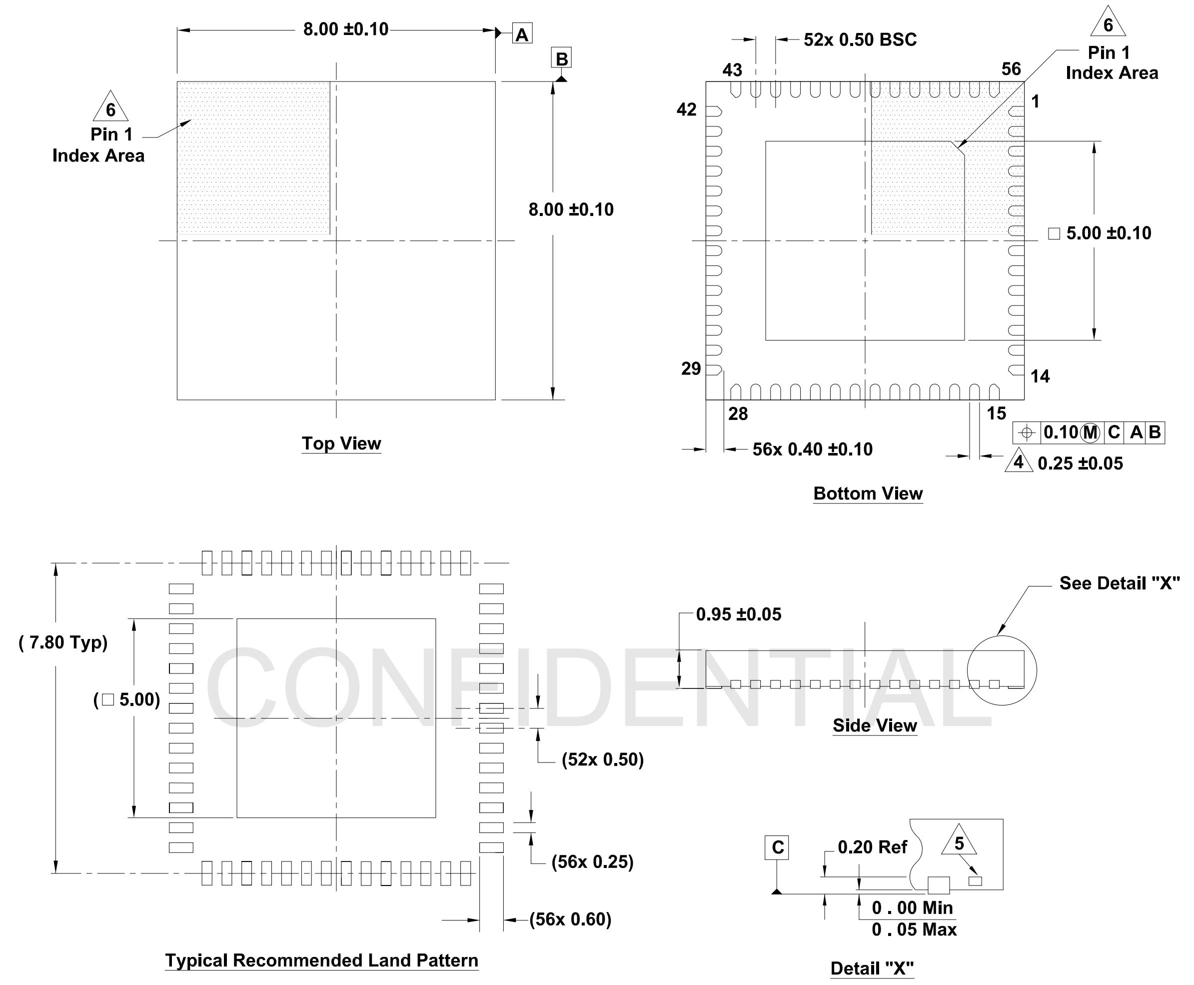
0x8F	Register Name - MPIO5 Config Type - (RW, EEPROM)				0x01 / 1
	[7:6]	not used			<00>
	[5]	MPIO5 Invert	Configure the polarity of MPIO5	0: Active low 1: Active high	<0>
	[4:3]	MPIO5 Type	If bits[4:3] = 00, then the respective MPIOx pin is high impedance, and the device will still use the MPIOx power on/off delays if bits[2:0] are not set to 3'b000	00: Disabled (high impedance) 01: Open drain NMOS output 10: Open drain PMOS output 11: Full CMOS output	<00>
	[2:0]	MPIO5 Function	Bits[2:0] = 000 disables the function of the respective MPIOx pin, and the device will ignore the MPIOx power on/off delay settings.	000: Disabled 001: CRST_IN# 010: External VR PGood input 011: Input to I2C register 100: PGood output 101: Reset output 110: External VR EN output 111: Output from I2C output	<001>
0x90	Register Name - PWRON Polarity Config Type - (RW, EEPROM)				0x01 / 1
	[7:1]	not used			<0000000>
	[0]	PWRON Polarity	Select the polarity of the PWRON input in both on/off switch and push button modes	0: Active low 1: Active high	<1>
0x95	Register Name - System Control Type - (RW, Non EEPROM)				0x00 / 0
	[7:2]	not used			<000000>
	[1]	reserved			<0>
	[0]	MPIO Config Lock	To prevent user from accidentally changing the MPIOx configurations. Once this bit is set to '1', it cannot be set back to '0' until POR	0: Unlock the MPIOx Config registers at 0x8A - 0x8F 1: Lock the MPIOx Config registers at 0x8A - 0x8F	<0>
0xAD	Reserved for Renesas Internal Use				
0xB0	Register Name - EEPROM ID 1 Type - (RW, EEPROM)				0x01 / 1
	[7:0]	NVM Ver 1	The EEPROM data is considered valid when EEPROM ID 1 or EEPROM ID 2 is programmed to non-zero value		<00000001>
0xB1	Register Name - EEPROM ID 2 Type - (RW, EEPROM)				0x01 / 1
	[7:0]	NVM Ver 2	The EEPROM data is considered valid when EEPROM ID 1 or EEPROM ID 2 is programmed to non-zero value		<00000001>
0xF7	Register Name - Chip ID Type - (Read-Only)				0x00 / 0
	[7:0]	PMIC ID			<00000000>

0xF8	Register Name - HW REV Type - (Read-Only)				0x12 / 18
	[7:4]	Major Rev	4-bit Major Revision	0x0 = x 0x1 = Rev A 0x2 = Rev B 0x3 = Rev C ….	<0001>
	[3:0]	Minor Rev	4-bit Minor Revision	0x0 = x 0x1 = 1st tape-out within a major revision 0x2 = 2nd tape-out within a major revision 0x3 = 3rd tape-out within a major revision …	<0010>
0xFF	Register Name - EEPROM Control Type - (RW, Non EEPROM)				0x00 / 0
	[7:4]	not used			<0000>
	[3]	reserved			<0>
	[2]	reserved			<0>
	[1]	Write EEPROM Customer	Write all customer registers to EEPROM	0: Do Nothing 1: Write reg data to EEPROM (customer banks), set bit LOW after write done	<0>
	[0]	EE Read	Reload EEPROM data to registers - (without resetting reg to all '0' first)	0: Do Nothing 1: Recall all the data from EEPROM and write to the registers, set bit LOW after loading done	<0>

13. Package Outline Drawing

For the most recent package outline drawing, see L56.8x8I.

L56.8x8I
56 Lead Quad Flat No-lead Plastic Package (5x5mm Exposed Paddle)
Rev 0, 11/20



Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier is either a mold or mark feature.

14. Part Number Differences

This document describes the base RAA215300A2GNP#HA0 device. The other part numbers have default, or other implementation *differences relative to this base part*. The detailed differences are outlined in the following sections.

14.1 RAA215300A2GNP#HA1

14.1.1 Register Map Detail

Summary of differences:

- PWRON Configuration: On/Off Switch

Register Pointer	Register Bit(S)	Bit(s)/Function Name	Description	Setting/Range	Default
0x6F	**Register Name - Config 1** **Type - (RW, EEPROM)**				0xFA / 250
	[0]	PWRON Config	Set the PWRON configuration	0: On/off switch 1: Long push button	<0>

15. Ordering Information

Part Number[1][2]	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	Temp. Range	Summary of Part Differences[4]
RAA215300A2GNP#HA0	215300B00	56 Lead, 8.8mm QFN	L56.8x8I	Reel, 1k	-40 to +105°C	▪ PWRON Config: Long Push Button
RAA215300A2GNP#HA1	215300B01					▪ PWRON Config: On/Off Switch
RTKA215300DE0000BU	Evaluation board for RAA215300A2GNP#HA0					
RTKA215300E00000BU	Socket board					

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the RAA215300 product page. For more information about MSL, see TB363.
3. See TB347 for details about reel specifications.
4. For a full detailed list of differences between parts, see Part Number Differences.

16. Revision History

Revision	Date	Description
1.01	Mar 20, 2023	Added description for VREFIN pin in the Pin Descriptions table and the Device Specific Layout Guidelines table. Updated Figures 9, 10, 11, 12 in section I2C Write Operation and I2C Read Operation. Added description in section {RESET}. Added description in section Output Discharge. Added description in section Unused Buck. Added description in section Unused LDOx. Updated VTTREF section. Added a figure and updated the description in section VREFIN UVLO. Updated External VR PGOOD Input section. Minor updates to the register map details table.
1.00	Sep 28, 2022	Initial release

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