

GENERAL DESCRIPTION

The 843004-01 is a 4 output LVPECL synthesizer optimized to generate Ethernet reference clock frequencies and is a member of the family of high performance clock solutions from IDT. Using a 25MHz 18pF parallel resonant crystal, the following frequencies can be generated based on the settings of 2 frequency select pins (F_SEL[1:0]): 156.25MHz, 125MHz, 62.5MHz. The 843004-01 uses IDT's 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Ethernet jitter requirements. The 843004-01 is packaged in a small 24-pin TSSOP package.

FEATURES

- Four 3.3V LVPECL outputs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- Supports the following output frequencies: 156.25MHz, 125MHz and 62.5MHz
- VCO range: 560MHz - 680MHz
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.57ps (typical)
- RMS phase noise at 156.25MHz (typical)

Phase noise:

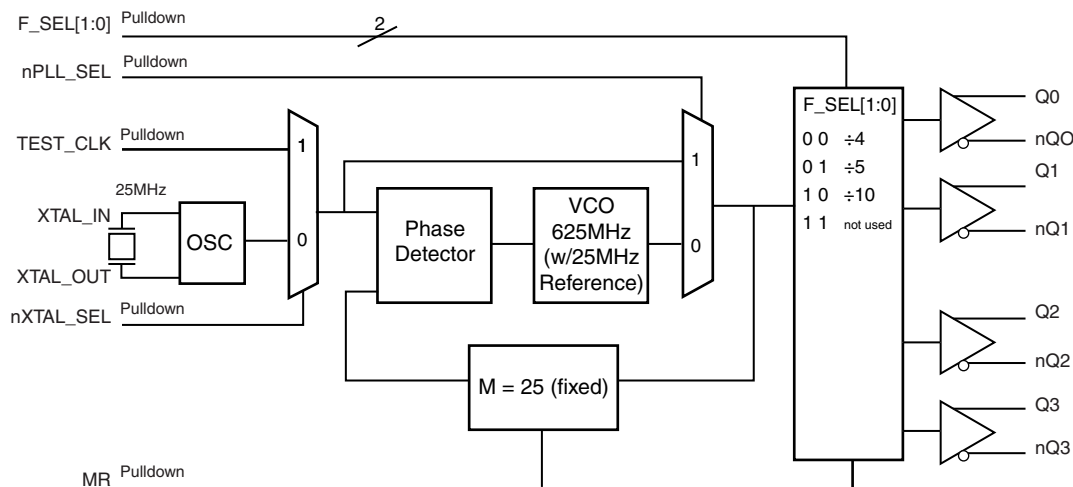
| Offset | Noise Power |
|--------|---------------|
| 100Hz | -95.5 dBc/Hz |
| 1kHz | -118 dBc/Hz |
| 10kHz | -126 dBc/Hz |
| 100kHz | -126.6 dBc/Hz |

- Full 3.3V supply mode
- -30°C to 85°C ambient operating temperature
- Available in lead-free RoHS compliant package

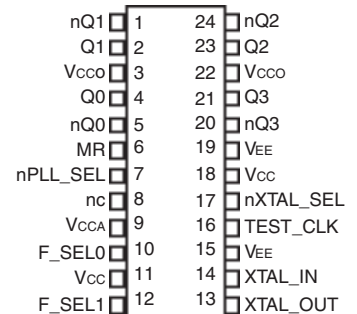
FREQUENCY SELECT FUNCTION TABLE

| Inputs | | | | | Output Frequency (25MHz Ref.) |
|--------|--------|-----------------|-----------------|-------------------|----------------------------------|
| F_SEL1 | F_SEL0 | M Divider Value | N Divider Value | M/N Divider Value | |
| 0 | 0 | 25 | 4 | 6.25 | 156.25 |
| 0 | 1 | 25 | 5 | 5 | 125 |
| 1 | 0 | 25 | 10 | 2.5 | 62.5 |
| 1 | 1 | 25 | not used | | not used |

BLOCK DIAGRAM



PIN ASSIGNMENT



843004-01

24-Lead TSSOP

4.40mm x 7.8mm x 0.92mm
package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|--------|-------------------|--------|----------|---|
| 1, 2 | nQ1, Q1 | Output | | Differential output pair. LVPECL interface levels. |
| 3, 22 | V _{CC0} | Power | | Output supply pins. |
| 4, 5 | Q0, nQ0 | Output | | Differential output pair. LVPECL interface levels. |
| 6 | MR | Input | Pulldown | Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels. |
| 7 | nPLL_SEL | Input | Pulldown | Selects between the PLL and TEST_CLK as input to the dividers. When LOW, selects PLL (PLL Enable). When HIGH, deselects the reference clock (PLL Bypass). LVCMOS/LVTTL interface levels. |
| 8 | nc | Unused | | No connect. |
| 9 | V _{CCA} | Power | | Analog supply pin. |
| 10, 12 | F_SEL0, F_SEL1 | Input | Pulldown | Frequency select pins. LVCMOS/LVTTL interface levels. |
| 11, 18 | V _{CC} | Power | | Core supply pin. |
| 13, 14 | XTAL_OUT, XTAL_IN | Input | | Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input. |
| 15, 19 | V _{EE} | Power | | Negative supply pins. |
| 16 | TEST_CLK | Input | Pulldown | LVCMOS/LVTTL clock input. |
| 17 | nXTAL_SEL | Input | Pulldown | Selects between crystal or TEST_CLK inputs as the the PLL Reference source. Selects XTAL inputs when LOW. Selects TEST_CLK when HIGH. LVCMOS/LVTTL interface levels. |
| 20, 21 | nQ3, Q3 | Output | | Differential output pair. LVPECL interface levels. |
| 23, 24 | Q2, nQ2 | Output | | Differential output pair. LVPECL interface levels. |

NOTE: refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 4 | | pF |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | kΩ |

ABSOLUTE MAXIMUM RATINGS

| | |
|--|--------------------------|
| Supply Voltage, V_{CC} | 4.6V |
| Inputs, V_I | -0.5V to $V_{CC} + 0.5V$ |
| Outputs, I_O | |
| Continuous Current | 50mA |
| Surge Current | 100mA |
| Package Thermal Impedance, θ_{JA} | 70°C/W (0 mps) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $T_A = -30^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------------|----------------------|---------|---------|---------|-------|
| V_{CC} | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{CCA} | Analog Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{CCO} | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| I_{EE} | Power Supply Current | | | | 135 | mA |
| I_{CCA} | Analog Supply Current | Included in I_{EE} | | | 15 | mA |

TABLE 3B. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $T_A = -30^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|---|---------|---------|----------------|---------|
| V_{IH} | Input High Voltage | | 2 | | $V_{CC} + 0.3$ | V |
| V_{IL} | Input Low Voltage | nPLL_SEL, nXTAL_SEL, F_SEL0, F_SEL1, MR | -0.3 | | 0.8 | V |
| | | TEST_CLK | -0.3 | | 1.3 | V |
| I_{IH} | Input High Current | TEST_CLK, MR, nPLL_SEL, nXTAL_SEL, F_SEL0, F_SEL1 $V_{CC} = V_{IN} = 3.465V$ | | | 150 | μA |
| I_{IL} | Input Low Current | TEST_CLK, MR, nPLL_SEL, nXTAL_SEL, F_SEL0, F_SEL1 $V_{CC} = 3.465V, V_{IN} = 0V$ | -5 | | | μA |

TABLE 3C. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $T_A = -30^\circ C$ TO $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-----------------------------------|-----------------|-----------------|---------|-----------------|-------|
| V_{OH} | Output High Voltage; NOTE 1 | | $V_{CCO} - 1.4$ | | $V_{CCO} - 0.9$ | V |
| V_{OL} | Output Low Voltage; NOTE 1 | | $V_{CCO} - 2.0$ | | $V_{CCO} - 1.7$ | V |
| V_{SWING} | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Outputs terminated with 50 to $V_{CCO} - 2V$.

TABLE 4. CRYSTAL CHARACTERISTICS

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | | 25 | | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 5. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $T_A = -30^\circ\text{C}$ TO 85°C

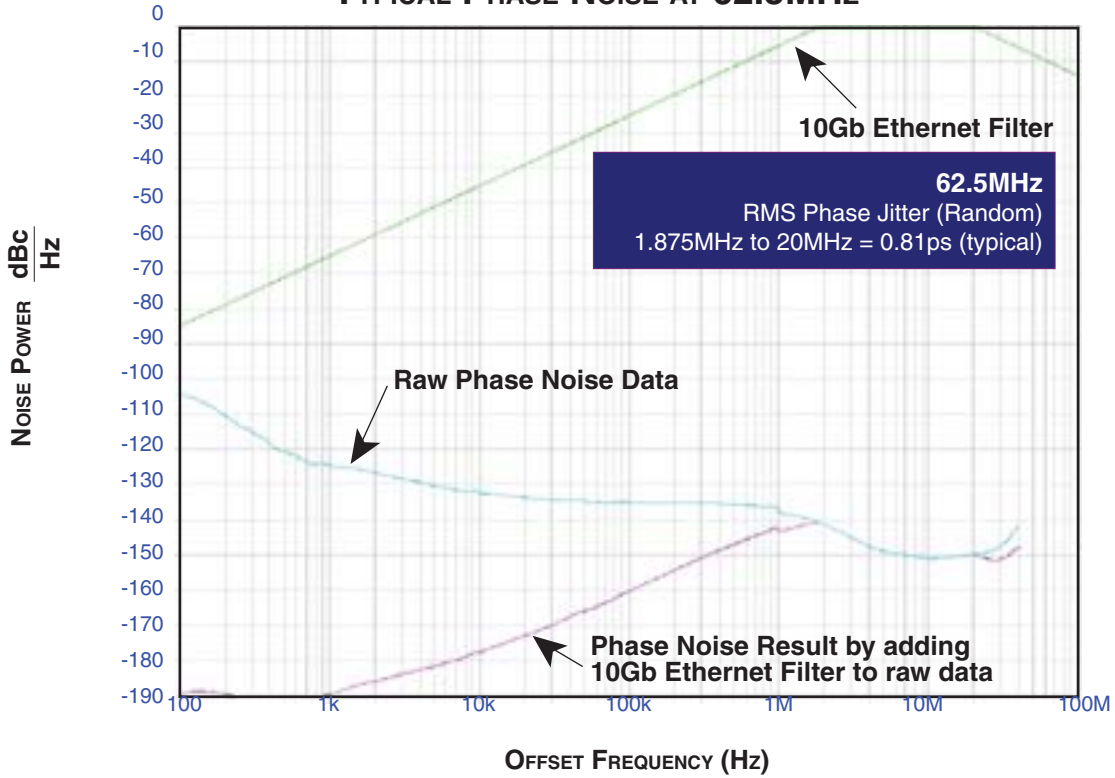
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---------------------|--------------------------|------------------------------|---------|---------|---------|-------|
| f_{OUT} | Output Frequency | F_SEL[1:0] = 00 | 140 | | 170 | MHz |
| | | F_SEL[1:0] = 01 | 112 | | 136 | MHz |
| | | F_SEL[1:0] = 10 | 56 | | 68 | MHz |
| tsk(o) | Output Skew; NOTE 1, 2 | | | 30 | ps | |
| tjit(\emptyset) | RMS Phase Jitter; NOTE 3 | 156.25MHz (1.875MHz - 20MHz) | | 0.57 | | ps |
| | | 125MHz (1.875MHz - 20MHz) | | 0.63 | | ps |
| | | 62.5MHz (1.875MHz - 20MHz) | | 0.81 | | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 300 | | 600 | ps |
| odc | Output Duty Cycle | | 49 | | 51 | % |

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{CCO}/2$.

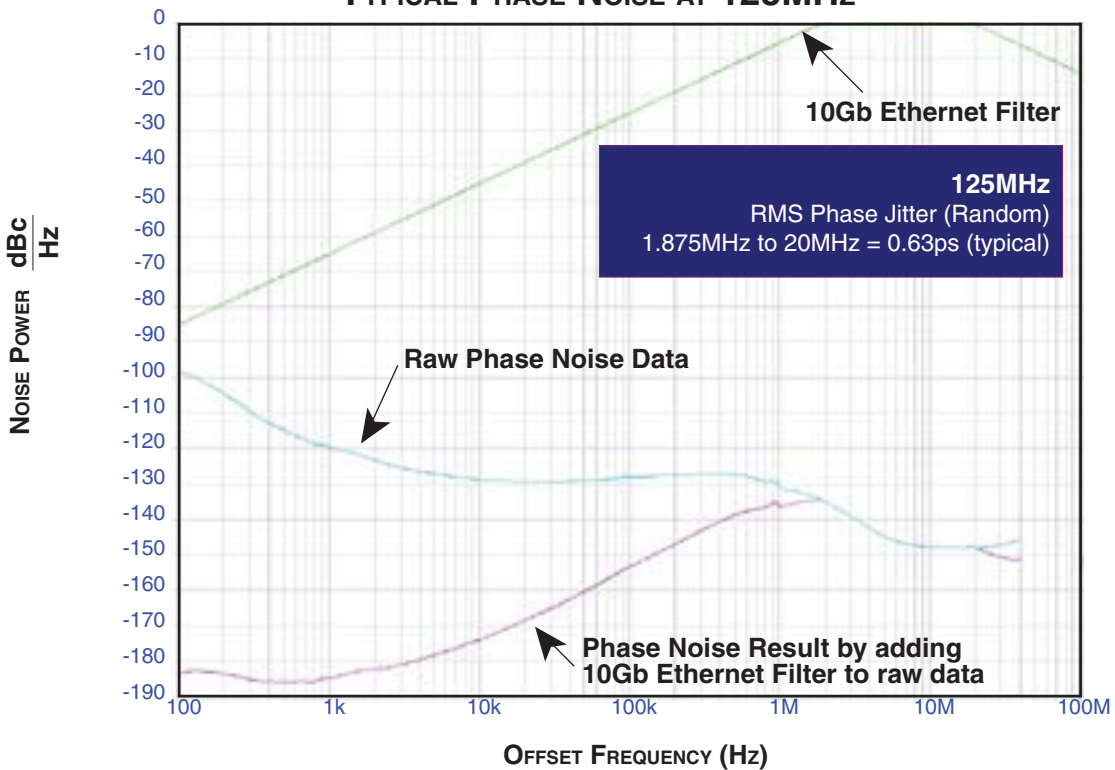
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Phase jitter is dependent on the input source used.

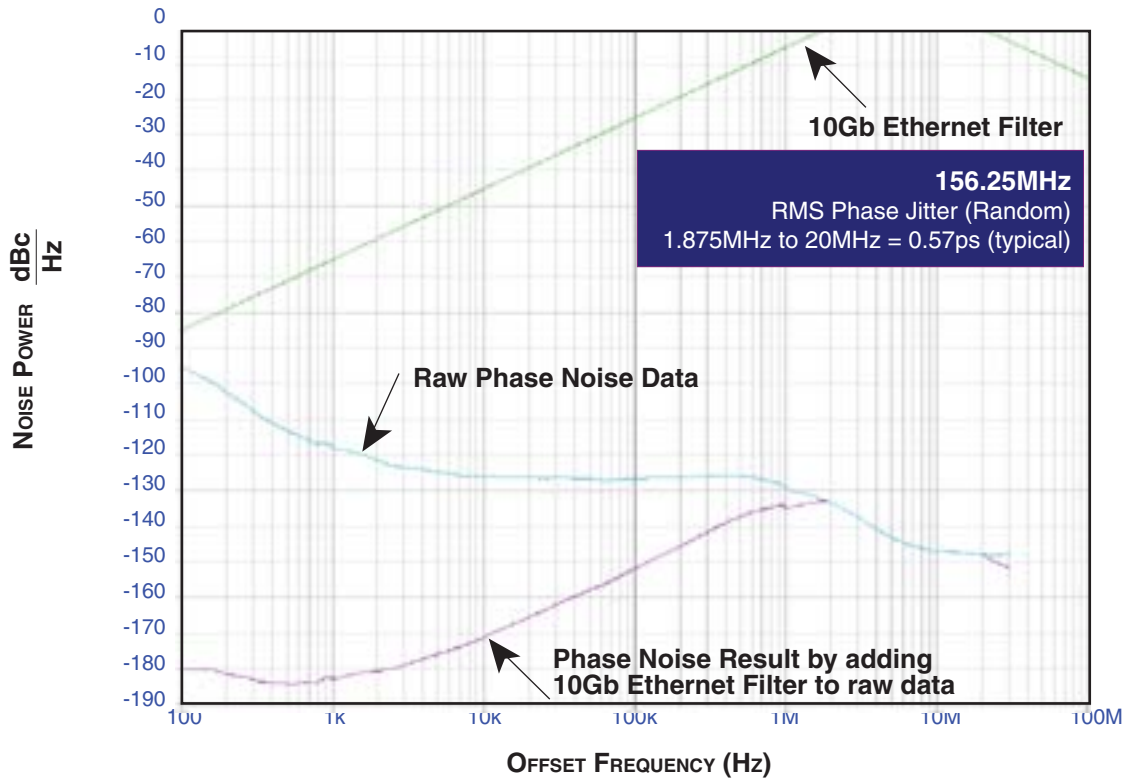
TYPICAL PHASE NOISE AT 62.5MHz



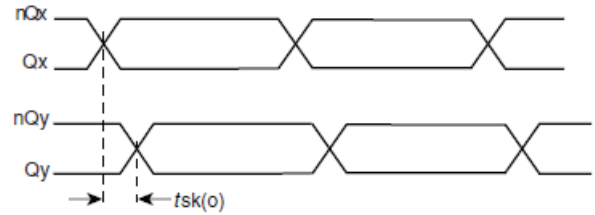
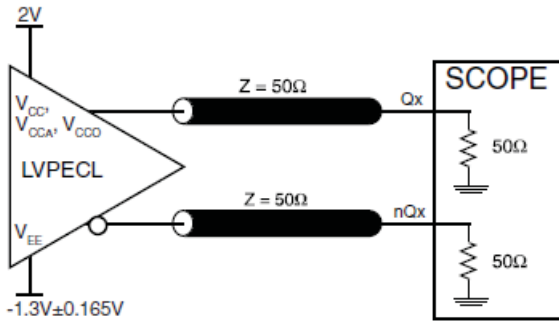
TYPICAL PHASE NOISE AT 125MHz



TYPICAL PHASE NOISE AT 156.25MHz

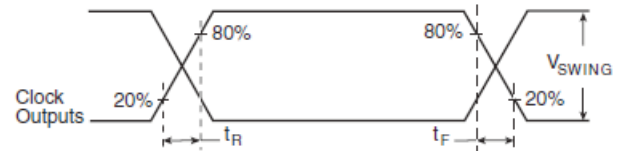
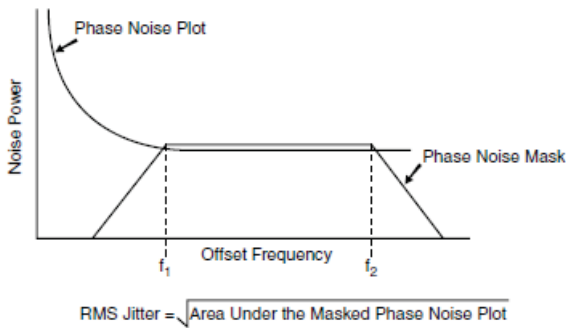


PARAMETER MEASUREMENT INFORMATION



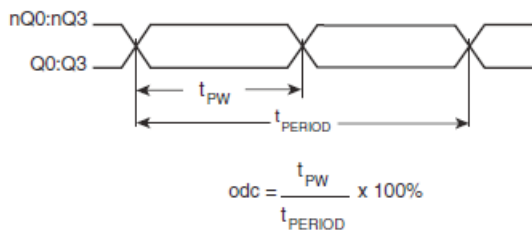
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT

OUTPUT SKEW



RMS PHASE JITTER

OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 843004-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} , V_{CCA} , and V_{CCO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a $10\mu\text{F}$ and a $.01\mu\text{F}$ bypass capacitor should be connected to each V_{CCA} .

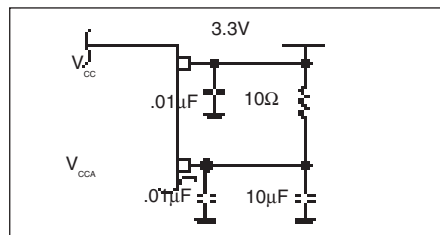


FIGURE 1. POWER SUPPLY FILTERING

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUT:

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a $1\text{k}\Omega$ resistor can be tied from XTAL_IN to ground.

TEST_CLK INPUT:

For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a $1\text{k}\Omega$ resistor can be tied from the TEST_CLK to ground.

LVC MOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A $1\text{k}\Omega$ resistor can be used.

OUTPUTS:

LVPECL OUTPUT

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

CRYSTAL INPUT INTERFACE

The 843004-01 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were

determined using a 25MHz , 18pF parallel resonant crystal and were chosen to minimize the ppm error.

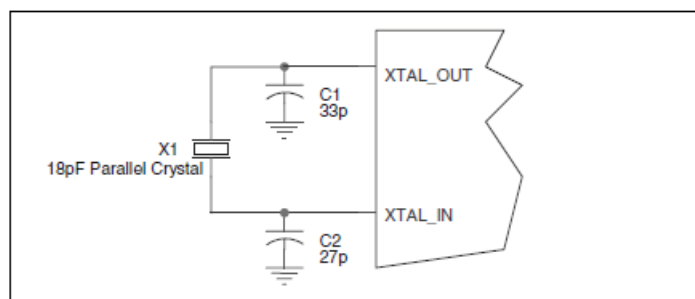


Figure 2. CRYSTAL INPUT INTERFACE

LVC MOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVC MOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure X*. The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVC MOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output

impedance of the driver (R_o) plus the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R_1 and R_2 in parallel should equal the transmission line impedance. For most 50Ω applications, R_1 and R_2 can be 100Ω. This can also be accomplished by removing R_1 and making R_2 50Ω.

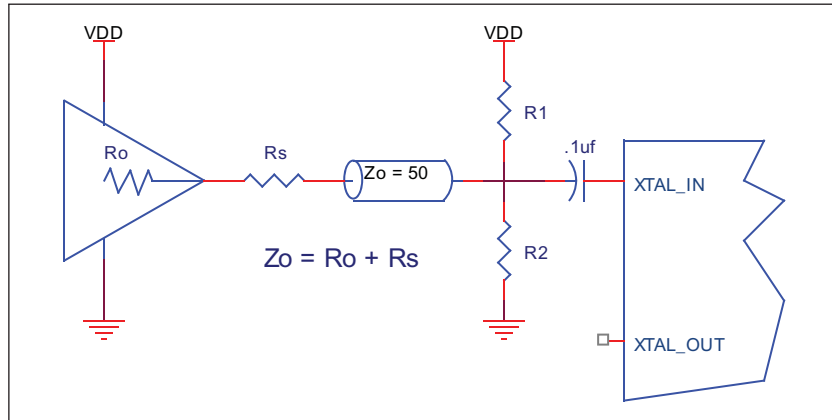


FIGURE 3. GENERAL DIAGRAM FOR LVC MOS DRIVER TO XTAL INPUT INTERFACE

TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission

lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

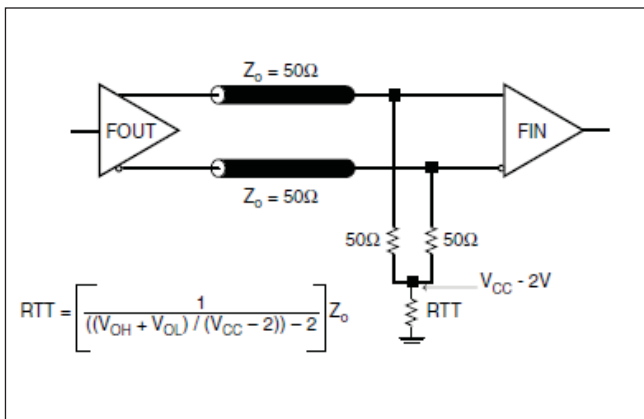


FIGURE 4A. LVPECL OUTPUT TERMINATION

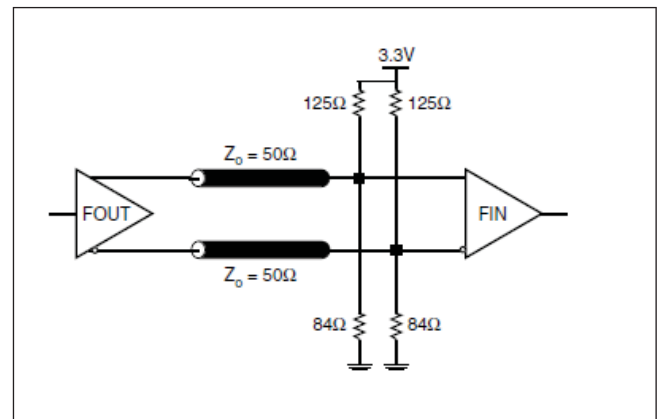


FIGURE 4B. LVPECL OUTPUT TERMINATION

LAYOUT GUIDELINE

Figure 5 shows a schematic example of the 843004-01. An example of LVEPCL termination is shown in this schematic. Additional LVPECL termination approaches are shown in the LVPECL Termination Application Note. In this example, an 18pF parallel

resonant 25MHz crystal is used. The C1=27pF and C2=33pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy.

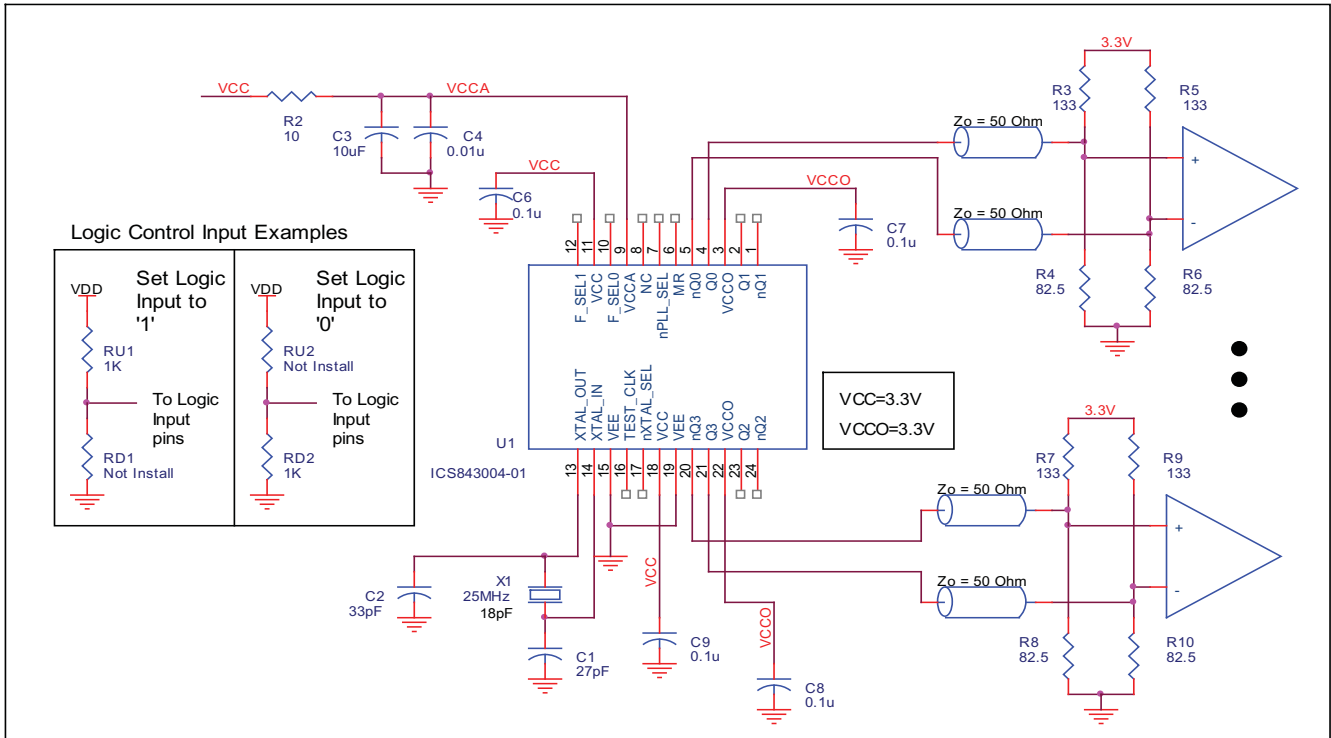


FIGURE 5. 843004-01 SCHEMATIC EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 843004-01. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 843004-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.465V * 135mA = 467.8mW$
- Power (outputs)_{MAX} = **30mW/Loaded Output pair**
If all outputs are loaded, the total power is $4 * 30mW = 120mW$

Total Power_{MAX} (3.465V, with all outputs switching) = $467.8mW + 120mW = 587.8mW$

2. Junction Temperature.

Junction temperature, T_j, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_{total} = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 65°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:
 $85°C + 0.588W * 65°C/W = 123.2°C$. This is below the limit of 125°C.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 24-PIN TSSOP, FORCED CONVECTION

| θ_{JA} by Velocity (Meters per Second) | | | |
|---|--------|--------|--------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 70°C/W | 65°C/W | 62°C/W |

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in Figure 6.

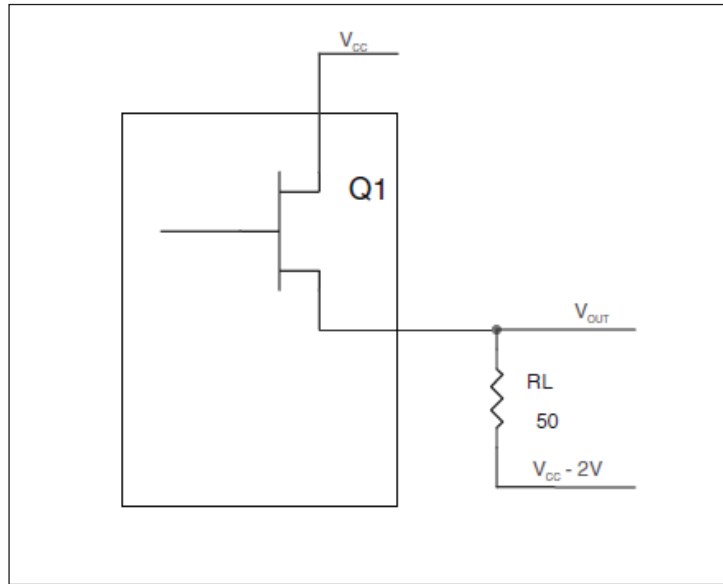


FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{cc} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CC_MAX} - 0.9V$

$$(V_{CC_MAX} - V_{OH_MAX}) = 0.9V$$

- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CC_MAX} - 1.7V$

$$(V_{CC_MAX} - V_{OL_MAX}) = 1.7V$$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - (V_{CC_MAX} - V_{OH_MAX}))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd_L = [(V_{OL_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - (V_{CC_MAX} - V_{OL_MAX}))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = 30mW$$

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

| θ_{JA} by Velocity (Meters per Second) | | | |
|---|--------|--------|--------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 70°C/W | 65°C/W | 62°C/W |

TRANSISTOR COUNT

The transistor count for 843004-01 is: 3183

PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

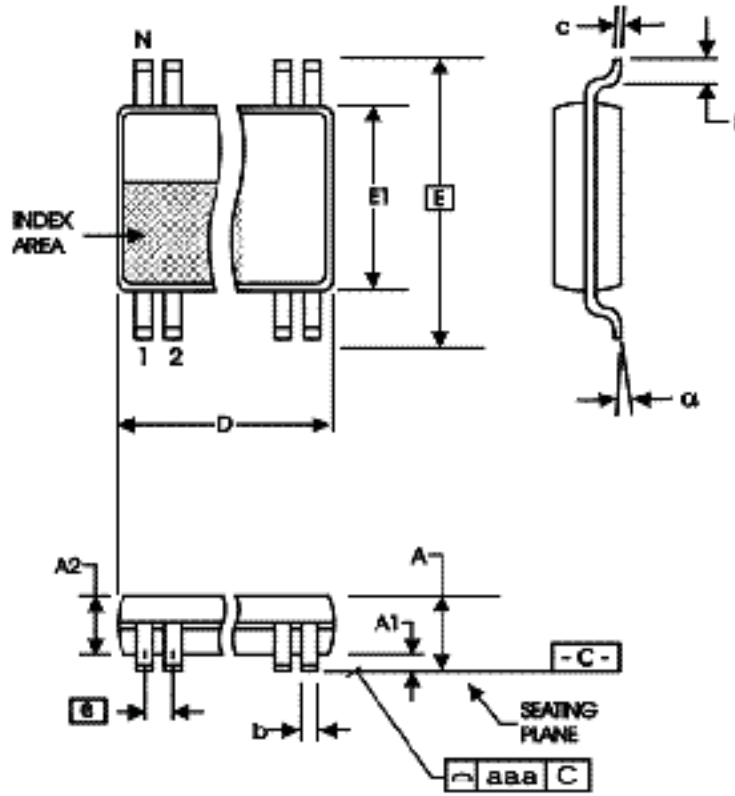


TABLE 8. PACKAGE DIMENSIONS

| SYMBOL | Millimeters | |
|----------|-------------|---------|
| | Minimum | Maximum |
| N | 24 | |
| A | -- | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 7.70 | 7.90 |
| E | 6.40 BASIC | |
| E1 | 4.30 | 4.50 |
| e | 0.65 BASIC | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | -- | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|--------------------------|----------------|---------------------------|---------------------------|--------------------|
| 843004AG-01LF | ICS43004A01L | 24 Lead "Lead-Free" TSSOP | tube | -30°C to 85°C |
| 843004AG-01LFT | ICS43004A01L | 24 Lead "Lead-Free" TSSOP | tape & reel | -30°C to 85°C |

| REVISION HISTORY SHEET | | | | |
|------------------------|-------|---------|--|---------|
| Rev | Table | Page | Description of Change | Date |
| B | T5 | 4 | AC Characteristics Table - deleted Propagation Delay row. | 5/6/05 |
| B | T9 | 1 | Features Section - added lead-free bullet. | 6/30/06 |
| | | 9 15 | Added - LVCMOS to XTAL Interface and Recommendations for Unused Input and Output Pins sections. Ordering Information Table - added lead-free part number, marking and note. | |
| B | T9 | 15 | Ordering Information Table - removed leaded devices - PDN CQ-13-02 expired. Updated datasheet format. | 12/9/14 |
| B | T9 | 1 | General Description - Removed Hiperlocks and changed ICS to IDT. | 1/18/16 |
| | | 15 | Ordering Information - Removed ICS in the Part/Order number and removed LF note below the table. Updated data sheet header and footer. | |

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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