

## IFP5020A, IFP5020B P-Channel JFET

### Features

- InterFET [P0032F Geometry](#)
- Typical Noise: 10 nV/√Hz
- Low Ciss: 3.2pF Typical
- Similar Characteristics to 2N5020,1
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

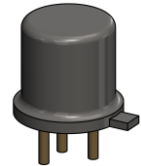
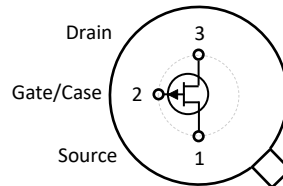
### Applications

- Analog Switches
- Choppers

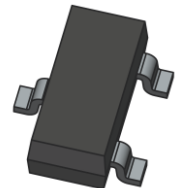
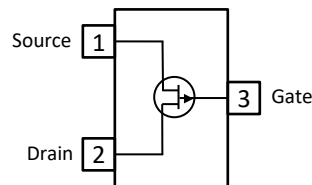
### Description

The 25V InterFET IFP5020A and IFP5020B are targeted for data switches and low-level chopper designs. Gate leakages are typically less than 1nA at room temperatures. The TO-18 package is hermetically sealed and suitable for military applications.

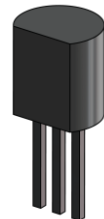
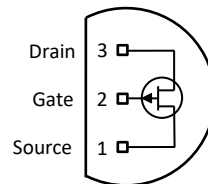
TO-18 Bottom View



SOT23 Top View



TO-92 Bottom View



### Product Summary

Parameters		IFP5020A Min	IFP5020B Min	Unit
BV <sub>GSS</sub>	Gate to Source Breakdown Voltage	25	25	V
I <sub>DSS</sub>	Drain to Source Saturation Current	-0.15	-0.3	mA
V <sub>GS(off)</sub>	Gate to Source Cutoff Voltage	0.3	0.3	V
G <sub>FS</sub>	Forward Transconductance	0.5	1	mS

### Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IFP5020A; IFP5020B	Through-Hole	TO-18	Bulk
PN5020A; PN5020B	Through-Hole	TO-92	Bulk
SMP5020A; SMP5020B	Surface Mount	SOT23	Bulk
SMP5020ATR; SMP5020BTR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
IFP5020ACOT; IFP5020BCOT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
IFP5020ACFT; IFP5020BCFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack



**Disclaimer:** It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

## Electrical Characteristics

### Maximum Ratings (@ T<sub>A</sub> = 25°C, Unless otherwise specified)

Parameters	Value	Unit
V <sub>RGS</sub> Reverse Gate Source and Gate Drain Voltage	25	V
I <sub>FG</sub> Continuous Forward Gate Current	50	mA
P <sub>D</sub> Continuous Device Power Dissipation	500	mW
P Power Derating	4	mW/°C
T <sub>J</sub> Operating Junction Temperature	-55 to 125	°C
T <sub>STG</sub> Storage Temperature	-65 to 200	°C

### Static Characteristics (@ T<sub>A</sub> = 25°C, Unless otherwise specified)

Parameters	Conditions	IFP5020A		IFP5020B		Unit
		Min	Max	Min	Max	
V <sub>(BR)GSS</sub> Gate to Source Breakdown Voltage	V <sub>DS</sub> = 0V, I <sub>G</sub> = -1μA	25		25		V
I <sub>GSS</sub> Gate to Source Reverse Current	V <sub>GS</sub> = 15V, V <sub>DS</sub> = 0V		1		1	nA
V <sub>GS(OFF)</sub> Gate to Source Cutoff Voltage	V <sub>DS</sub> = -15V, I <sub>D</sub> = 1nA	0.3	1.5	0.3	1.8	V
I <sub>DSS</sub> Drain to Source Saturation Current	V <sub>GS</sub> = 0V, V <sub>DS</sub> = -15V (Pulsed)	-0.15	-1.2	-0.3	-1.2	mA

### Dynamic Characteristics (@ T<sub>A</sub> = 25°C, Unless otherwise specified)

Parameters	Conditions	IFP5020A		IFP5020B		Unit
		Min	Max	Min	Max	
G <sub>FS</sub> Forward Transconductance	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0V	0.5	3.5	1.0	3.5	mS
G <sub>OS</sub> Output Conductance	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0V		20		20	μS
C <sub>ISS</sub> Input Capacitance	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0V, f = 1MHz		25		25	pF
C <sub>RSS</sub> Reverse Transfer Capacitance	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0V, f = 1MHz		7		7	pF

## SOT23 (TO-236AB) Mechanical and Layout Data

### Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

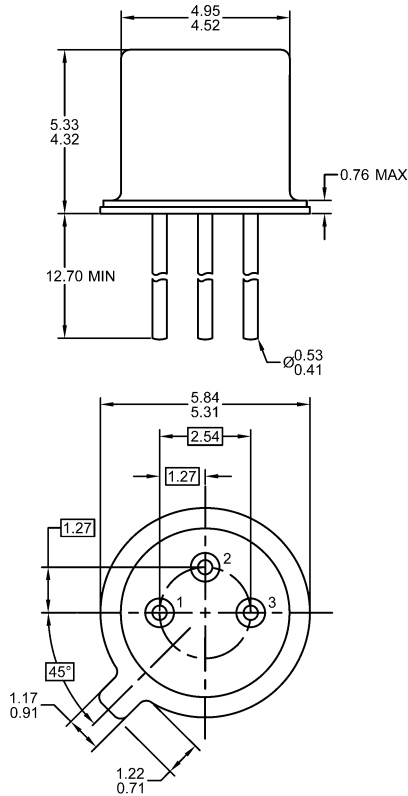
### Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

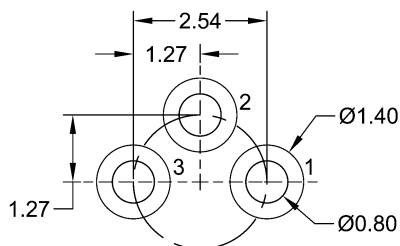
## TO-18 Mechanical and Layout Data

### Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.29 grams
3. Bulk product is shipped in standard ESD shipping material
4. Refer to JEDEC standards for additional information.

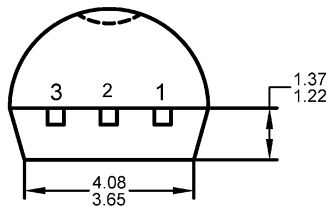
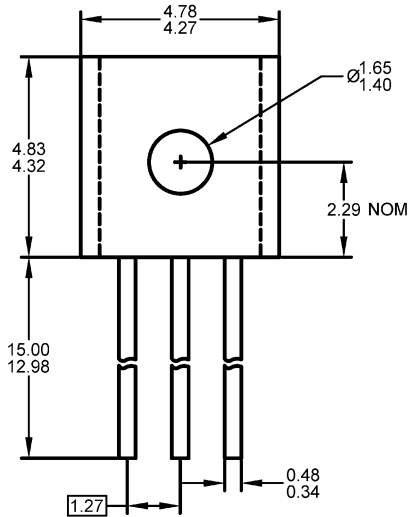
### Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.

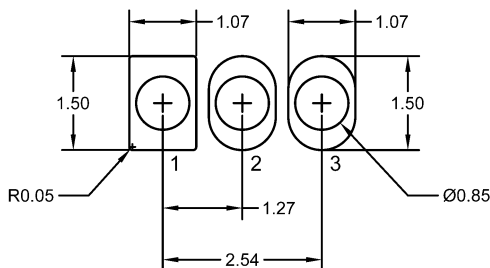
## TO-92 Mechanical and Layout Data

### Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.19 grams
3. Molded plastic case UL 94V-0 rated
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

### Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.

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