DDR5 SDRAM RDIMM Addendum

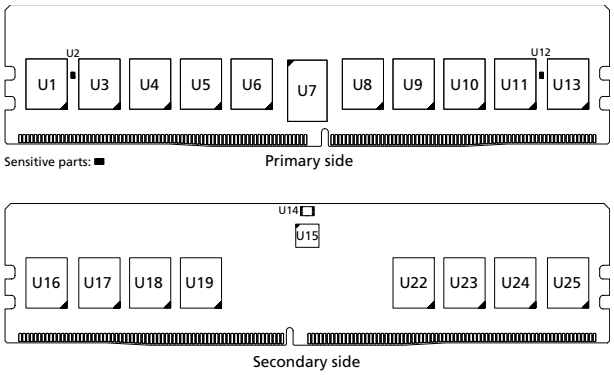
MTC18F1045S1PC – 32GB
16Gb Die Revision A

Features

Information provided here is in addition to or supersedes information provided in the Micron DDR5 RDIMM Core data sheet.

- DDR5 functionality and operations supported as defined in the component data sheet
- Features and specifications defined in the Micron DDR5 RDIMM core data sheet
- 288-pin, DDR5 registered dual in-line memory module (DDR5 RDIMM)
- Fast data transfer rate: PC5-4800
- 32GB (4Gig x 72)
- Single-rank
- 32 internal banks; 8 groups of 4 banks each

Figure 1: 288-Pin DDR5 RDIMM (R/C-F0)



Options — Marking

- Operating temperature
  - Commercial ($0°C \le T_{OPER} \le 95°C$) — C
- Frequency/CAS latency
  - 0.416ns @ CL = 40 (DDR5-4800) — 48B

Table 1: Addressing

Parameter	32GB
Row address[1]	64K (R0-R15)
Column address[1]	2K (C0-C10)
Device bank group address[1]	8 (BG0-BG2)
Device bank address per bank group[1]	4 (BA0-BA1)
Device configuration	16Gb (4Gb x 4), 32 banks
Module rank address	1 (CS0_n)

Notes: 1. These parameters represent the logical address state of the CA bus for different commands. Refer to the command truth table in the component data sheet.

Table 2: Part Numbers and Timing Parameters – 32GB Modules

Base device: MT60B4G4,[1] 16Gb DDR5 SDRAM Die Revision A

Part Number	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles ($CL-_nRCD-_nRP$)
MTC18F1045S1PC48BA2	32GB	4Gb x 72 (EC4)	38.4 GB/s	0.416ns/4800 MT/s	40-39-39

Notes: 1. The data sheet for the base device can be found on micron.com.

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DQ Map

Table 3: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	3A	154	U3	0	11A	165
	1	0A	7		1	8A	18
	2	1A	9		2	9A	20
	3	2A	152		3	10A	163
U4	0	19A	176	U5	0	27A	187
	1	16A	29		1	24A	40
	2	17A	31		2	25A	42
	3	18A	174		3	26A	185
U6	0	CB3A	198	U8	0	CB3B	243
	1	CB0A	51		1	CB0B	96
	2	CB1A	53		2	CB1B	98
	3	CB2A	196		3	CB2B	241
U9	0	7B	254	U10	0	15B	265
	1	4B	107		1	12B	118
	2	5B	109		2	13B	120
	3	6B	252		3	14B	263
U11	0	23B	276	U13	0	31B	287
	1	20B	129		1	28B	140
	2	21B	131		2	29B	142
	3	22B	274		3	30B	285
U16	0	24B	133	U17	0	16B	122
	1	27B	280		1	19B	269
	2	26B	278		2	18B	267
	3	25B	135		3	17B	124
U18	0	8B	111	U19	0	0B	100
	1	11B	258		1	3B	247
	2	10B	256		2	2B	245
	3	9B	113		3	1B	102
U22	0	28A	47	U23	0	20A	36
	1	31A	194		1	23A	183
	2	30A	192		2	22A	181
	3	29A	49		3	21A	38

Table 3: Component-to-Module DQ Map (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U24	0	12A	25	U25	0	4A	14
	1	15A	172		1	7A	161
	2	14A	170		2	6A	159
	3	13A	27		3	5A	16

I_{DD} Specifications

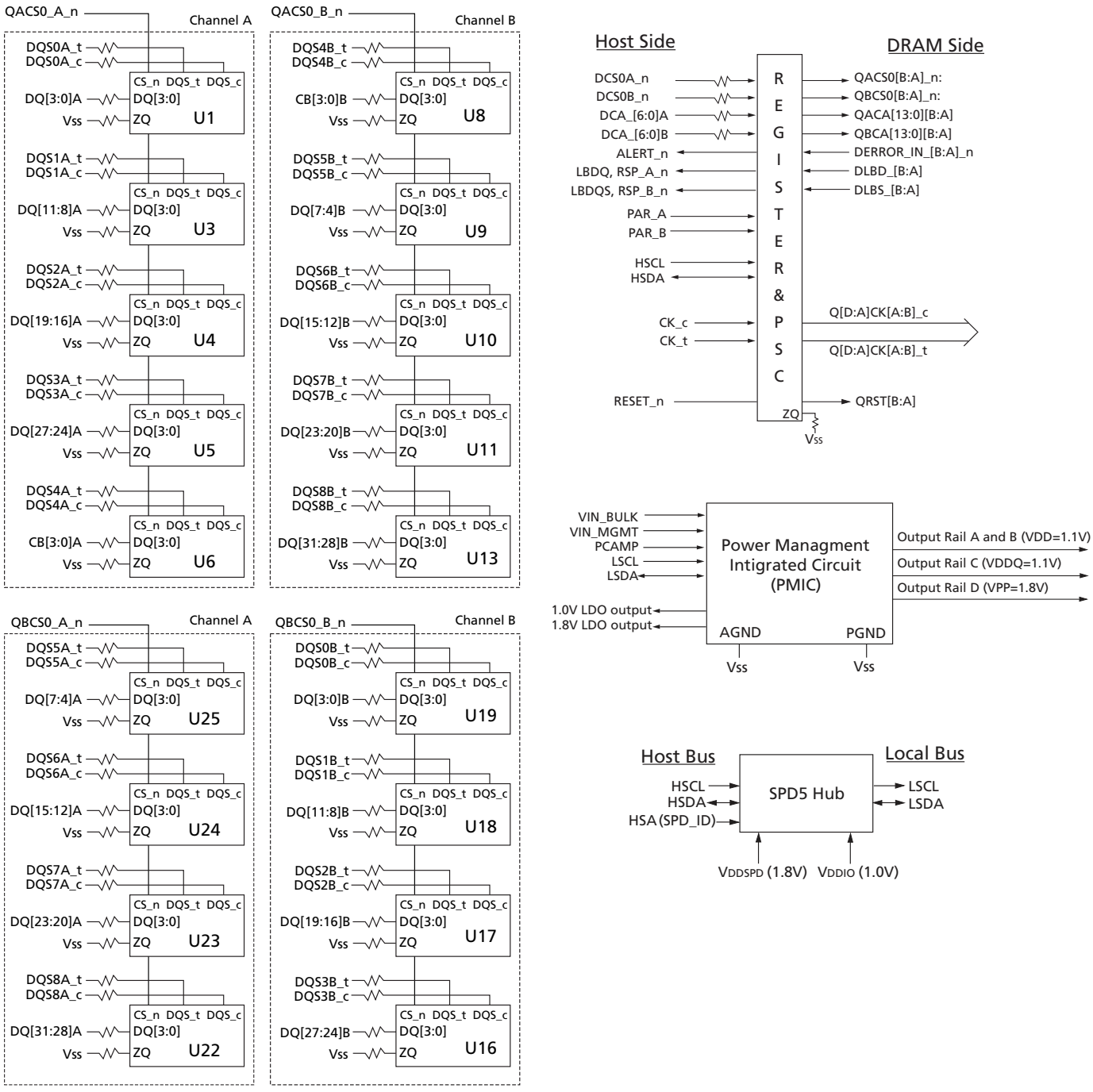
Table 4: DDR5 I_{DD} Specifications and Conditions – 32GB (Die Revision A)

Module I_{DD} is based on PMIC VIN_BULK 12V input current and typical operating range of temperature. Each I_{DD} parameter includes PMIC efficiency, RCD current and all DRAM current on all supplies (V_{DD}, V_{DDQ}, and V_{PP}).

Parameter	Symbol	4800	Units
Operating one bank ACTIVATE-PRECHARGE current	I_{DD0}	182	mA
Operating four bank ACTIVATE-PRECHARGE current	I_{DD0F}	261	mA
Precharge standby current	I_{DD2N}	152	mA
Precharge standby non-target command	I_{DD2NT}	294	mA
Precharge power-down current	I_{DD2P}	139	mA
Active standby current	I_{DD3N}	153	mA
Active power-down current	I_{DD3P}	153	mA
Operating burst read current	I_{DD4R}	574	mA
Operating burst write current	I_{DD4W}	729	mA
Operating burst write with write CRC current	I_{DD4WC}	748	mA
Burst refresh (normal refresh mode) current	I_{DD5B}	451	mA
Burst refresh (fine granularity refresh mode) current	I_{DD5F}	294	mA
Burst refresh (same bank refresh mode) current	I_{DD5C}	225	mA
Self refresh current	I_{DD6N}	63	mA
Operating bank interleave read current	I_{DD7}	674	mA
Maximum power saving deep power down mode current	I_{DD8}	65	mA

Functional Block Diagram

Figure 2: Functional Block Diagram



Notes: 1. The ZQ ball on each DDR5 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.
2. Functional block diagram is for reference only.

Revision History

Rev. C – 09/2021

- Production Release - MPN changed from MTC18F1045S1RC to MTC18F1045S1PC to indicate x72 I/O width

Rev. B – 06/2020

- Preliminary Release

Rev. A – 06/2020

- Preliminary Release

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