Technical Note

Transitioning Designs From DDR3 8Gb SDP 1CS to 8Gb DDP 1CS

Introduction

This technical note explains how to migrate a PCB design that uses a Micron 8Gb DDR3L product from a 90 series single-die 96-ball package to a 100 series dual-die 96-ball package.

For complete specifications, see the data sheet for each device. This technical note does not include memory controller firmware changes required to move from the single-die package (SDP) to the dual-die package (DDP). Customers are advised to resimulate the system for signal integrity (SI) confirmation.

The following table shows the single-die and dual-die part numbers and essential differences between the devices.

Table 1: DDR3L Device Details

Architecture	Device	
	MT41K512M16HA (SDP)	MT41K512M16VRN (DDP), MT41K512M16VRP (DDP)
Die configuration	64 Meg x 16 x 8 banks	64 Meg x 8 x 8 banks
Density per package	8Gb	8Gb
Die per package	1	2
Ranks (CS_n)	1	1
Refresh count	8K	8K
Row address	A[15:0]	A[15:0]
Bank address	BA[2:0]	BA[2:0]
Column address	A[9:0]	A[9:0]
Page size/die	2KB	1KB

Ball Assignments

Ballout and assignments are the same for the 8Gb DDR3L SDP and DDP devices; however, when replacing an SDP device with a DDP device on the same system board, we recommend resimulating the system and verifying all termination settings and values. A system firmware change to adjust the controller and DRAM DQ/DQS drive strength may be required depending on system SI simulation results.

For information on how to help verify these design changes and confirm SI, see Micron technical notes TN-41-13: Point to Point Design Support and TN-52-02: Point-to-Point System Design Layout and Routing Tips.

Block Diagrams

The block diagrams for the 8Gb DDR3L SDP and the DDP devices are shown in the figures below. Note that the DDP package has one internal RZQ resister and one ZQ pin out. External ballouts for both the SDP and DDP packages are the same.

Figure 1: Functional Block Diagram for 8Gb 1CS SDP (64 Meg x 16 x 8 Banks)

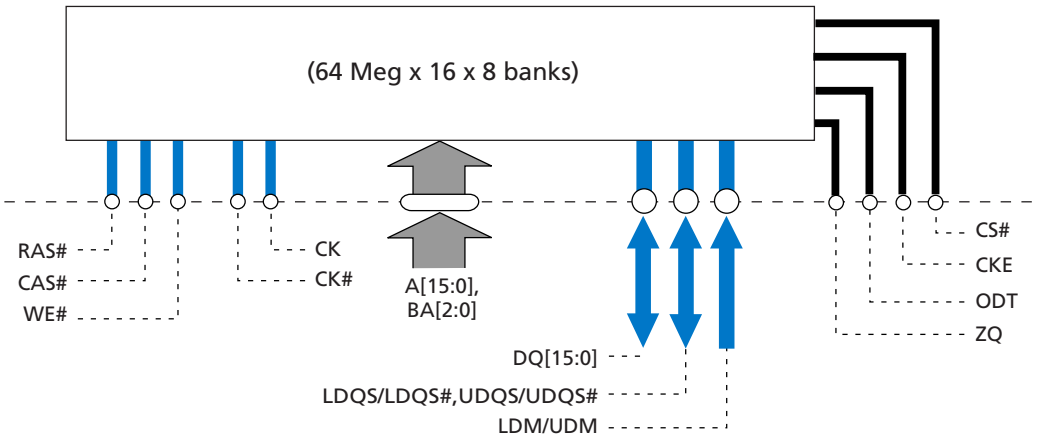
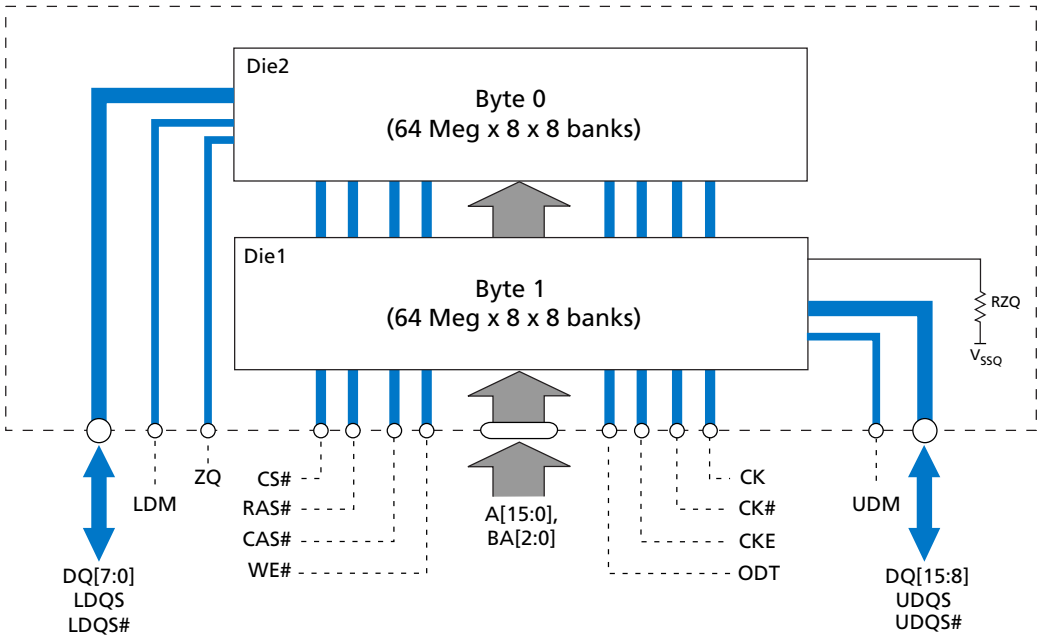


Figure 2: Functional Block Diagram for 8Gb 1CS DDP (2 x 64 Meg x 8 x 8 Banks)



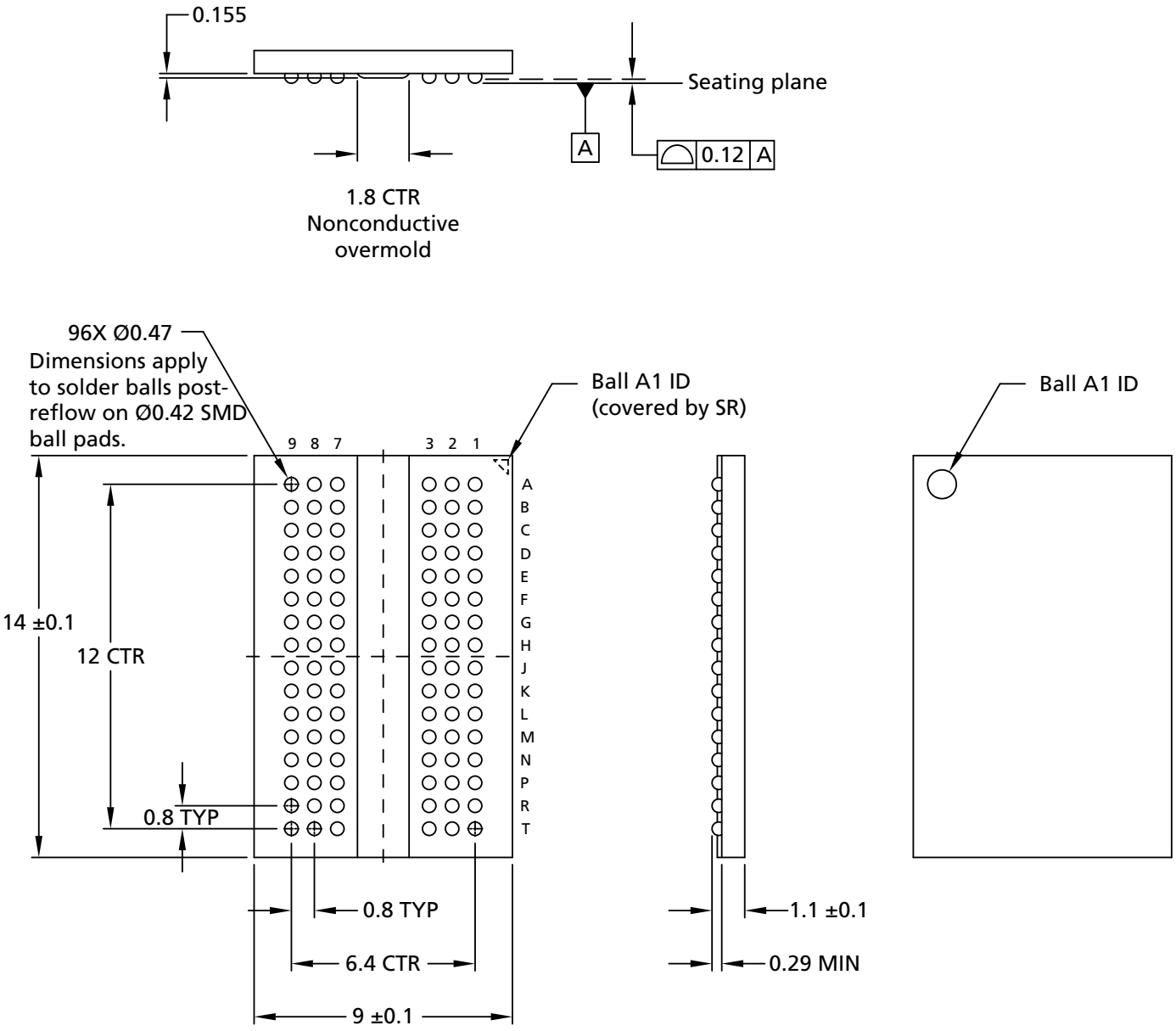
Package Dimensions

The package dimensions for the 8Gb DDR3L SDP and DDP devices are showed in the following figures, and the differences are summarized in the following table. The ball size increase for the DDP device is required to meet automotive solder join reliability (SJR) requirements. See Micron's customer service note CSN-33, a general BGA manufacturer's user guide, for information on how to easily integrate both leading-edge and legacy Micron ball grid array (BGA) packages into your manufacturing processes.

Table 2: Package Dimension Comparison

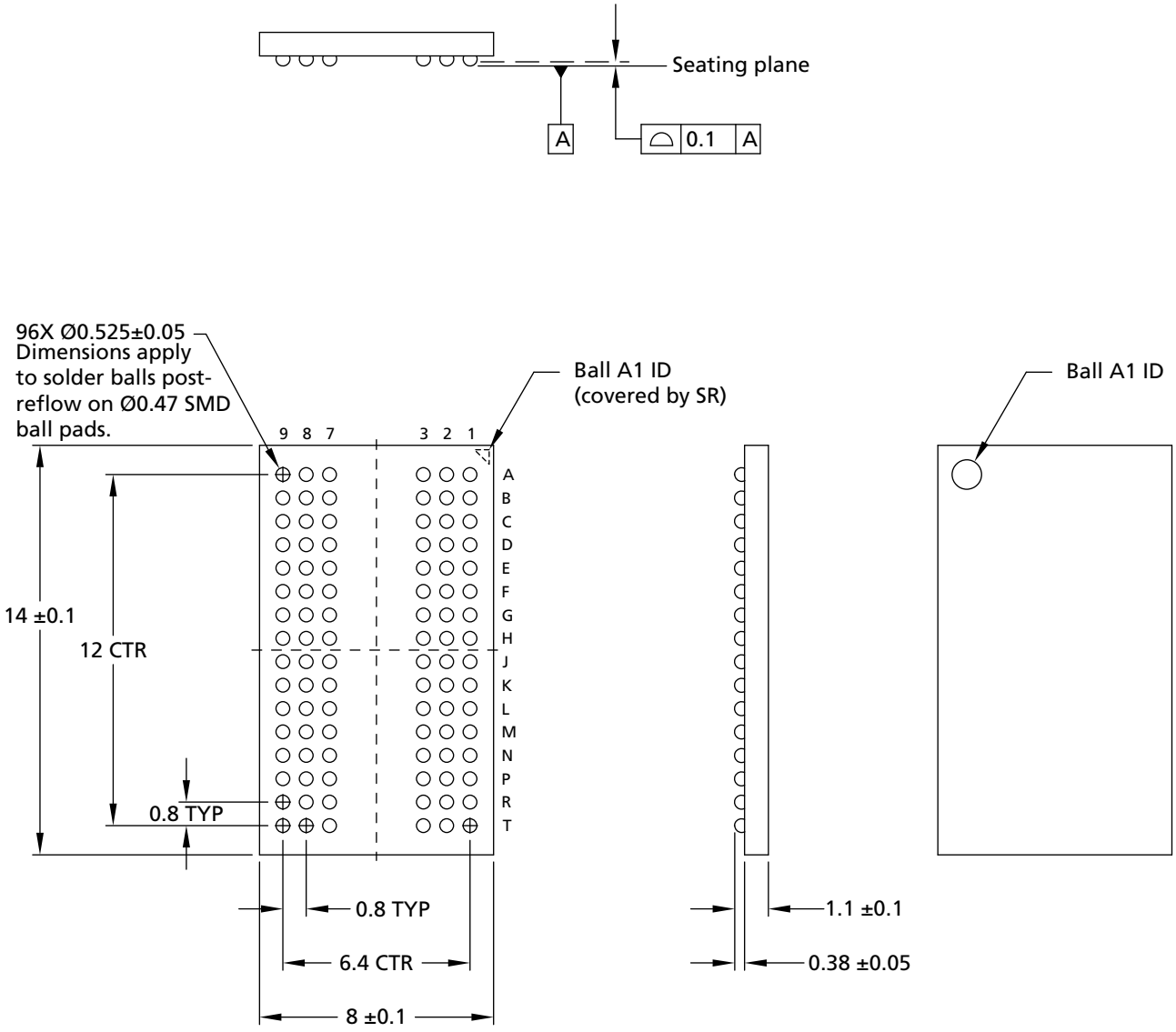
Package Code	Package (unit mm)	
	HA (SDP)	VRN (DDP) and VRP (DDP)
Dimension	9 x 14	8 x 14
Thickness (with ball)	1.1 ±0.1	1.1 ±0.1
Solder ball	96 x Ø0.47	96 x Ø0.525 ±0.05
SMD ball pad	Ø0.42	Ø0.47
Ball height	0.29 MIN	0.381 ±0.05

Figure 3: 8Gb SDP 96-Ball FBGA – x16 (HA)



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).

Figure 4: 8Gb DDP 96-Ball FBGA – x16 (VRN, VRP)



Notes:
1. All dimensions are in millimeters
2. VRN material composition: Pb-free SAC302 (96.8% Sn, 3% Ag, 0.2% Cu)
3. VRP material composition: Pb-free SAC Q (92.45% Sn, 4% Ag, 0.5% Cu, 3% Bi, 0.05%)

Electrical Specifications

The differences in thermal impedance, input/output capacitance and electrical specifications between the 8Gb DDR3 SDP and DDP devices are shown in the respective device data sheets. However, when migrating from the 8Gb DDR3L SDP device to the DDP device there are timing changes that should be noted. These changes are shown in the following tables.

DDR3L 8Gb Timing Changes

Table 3: Configurations and Page Size

Parameter	8Gb SDP	8Gb DDP
Die configuration	64 Meg x 16 x 8 banks	64 Meg x 8 x 8 banks
Refresh count	8K	8K
Row address	64K (A[15:0])	64K (A[15:0])
Bank address	8 (BA[2:0])	8 (BA[2:0])
Column address	1K (A[9:0])	1K (A[9:0])
Die page size	2KB	1KB

Table 4: Command Timing

Parameter	Symbol	SDP (DDR3L-1866)		DDP (DDR3L-1866)		Unit
		Min	Max	Min	Max	
ACTIVATE-to-ACTIVATE minimum command period	^{t}RRD	MIN = greater of 4CK or 6ns		MIN = greater of 4CK or 5ns		CK or ns
Four ACTIVATE windows	^{t}FAW	35	–	27	–	ns

Table 5: REFRESH Timing

Parameter	Symbol	DDR3L-1866		Unit
		Min	Max	
REFRESH-to-ACTIVATE or REFRESH command period	^{t}RFC – 4Gb	260	70,200	ns
	^{t}RFC – 8Gb	350	70,200	ns

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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