2048MB DDR2 SDRAM SO-DIMM

2048MB DDR2 SDRAM SO-DIMM based 128Mx8 , 8Banks, 1.8V DDR2 SDRAM with SPD

Features

Performance range (Bandwidth 6.4GB/sec)

Part No.	Max Freq. (Clock)	Speed Grade
78.A2G86.405	400MHz(2.5ns@CL6)	800 Mbps

- JEDECstandard 1.8V ± 0.1V Power Supply
- VDDQ = 1.8V± 0.1V
- Internal Bank: 8 Bank
- Posted CAS
- Programmable CAS Latency: 4, 5, 6
- Programmable Additive Latency: 0, 1 , 2 , 3 and 4
- Write Latency(WL) = Read Latency(RL) -1
- Burst Length: 4 , 8(Interleave/nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver(OCD) Impedance Adjustment
- On Die Termination
- Refresh and Self Refresh
  Average Refesh Period 7.8us
- Serial presence detect with EEPROM
- Compliance with RoHS
- Compliance with CE
- Operating Temperature Rang:
- Commercial 0°C ≦ TC ≦ 85°C
- Refresh: auto-refresh, self-refresh
- —Average refresh period
  7.8us at 0°C ≦ TC ≦ 85°C
  3.9us at 85°C ≦ TC ≦ 95°C

Description

This module is 256M x 64 bit Double Data Rate SDRAM high density memory modules based on first generation of 2048MB DDR2 SDRAM respectively.

It consists of sixteen CMOS 128M x8 bit with 8banks Double Data Rate SDRAMs in 60Ball FBGA packages mounted on a 200pin glass-epoxy substrate. Three 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each DDR2 SDRAM.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}	2	V_{SS}	51	DQS2	52	DM2	101	A1	102	A0	151	DQ42	152	DQ46
3	V_{SS}	4	DQ4	53	V_{SS}	54	V_{SS}	103	V_{DD}	104	V_{DD}	153	DQ43	154	DQ47
5	DQ0	6	DQ5	55	DQ18	56	DQ22	105	A10/AP	106	BA1	155	V_{SS}	156	V_{SS}
7	DQ1	8	V_{SS}	57	DQ19	58	DQ23	107	BA0	108	$\overline{RAS}$	157	DQ48	158	DQ52
9	V_{SS}	10	DM0	59	V_{SS}	60	V_{SS}	109	$\overline{WE}$	110	$\overline{S}0$	159	DQ49	160	DQ53
11	$\overline{DQS}0$	12	V_{SS}	61	DQ24	62	DQ28	111	V_{DD}	112	V_{DD}	161	V_{SS}	162	V_{SS}
13	DQS0	14	DQ6	63	DQ25	64	DQ29	113	$\overline{CAS}$	114	ODT0	163	NC, TEST	164	CK1
15	V_{SS}	16	DQ7	65	V_{SS}	66	V_{SS}	115	NC/$\overline{S}1$	116	A13	165	V_{SS}	166	$\overline{CK}1$
17	DQ2	18	V_{SS}	67	DM3	68	$\overline{DQS}3$	117	V_{DD}	118	V_{DD}	167	$\overline{DQS}6$	168	V_{SS}
19	DQ3	20	DQ12	69	NC	70	DQS3	119	NC/ODT1	120	NC	169	DQS6	170	DM6
21	V_{SS}	22	DQ13	71	V_{SS}	72	V_{SS}	121	V_{SS}	122	V_{SS}	171	V_{SS}	172	V_{SS}
23	DQ8	24	V_{SS}	73	DQ26	74	DQ30	123	DQ32	124	DQ36	173	DQ50	174	DQ54
25	DQ9	26	DM1	75	DQ27	76	DQ31	125	DQ33	126	DQ37	175	DQ51	176	DQ55
27	V_{SS}	28	V_{SS}	77	V_{SS}	78	V_{SS}	127	V_{SS}	128	V_{SS}	177	V_{SS}	178	V_{SS}
29	$\overline{DQS}1$	30	CK0	79	CKE0	80	NC/CKE1	129	$\overline{DQS}4$	130	DM4	179	DQ56	180	DQ60
31	DQS1	32	$\overline{CK}0$	81	V_{DD}	82	V_{DD}	131	DQS4	132	V_{SS}	181	DQ57	182	DQ61
33	V_{SS}	34	V_{SS}	83	NC	84	NC	133	V_{SS}	134	DQ38	183	V_{SS}	184	V_{SS}
35	DQ10	36	DQ14	85	BA2	86	NC	135	DQ34	136	DQ39	185	DM7	186	$\overline{DQS}7$
37	DQ11	38	DQ15	87	V_{DD}	88	V_{DD}	137	DQ35	138	V_{SS}	187	V_{SS}	188	DQS7
39	V_{SS}	40	V_{SS}	89	A12	90	A11	139	V_{SS}	140	DQ44	189	DQ58	190	V_{SS}
41	V_{SS}	42	V_{SS}	91	A9	92	A7	141	DQ40	142	DQ45	191	DQ59	192	DQ62
43	DQ16	44	DQ20	93	A8	94	A6	143	DQ41	144	V_{SS}	193	V_{SS}	194	DQ63
45	DQ17	46	DQ21	95	V_{DD}	96	V_{DD}	145	V_{SS}	146	$\overline{DQS}5$	195	SDA	196	V_{SS}
47	V_{SS}	48	V_{SS}	97	A5	98	A4	147	DM5	148	DQS5	197	SCL	198	SA0
49	$\overline{DQS}2$	50	NC	99	A3	100	A2	149	V_{SS}	150	V_{SS}	199	V_{DD}SPD	200	SA1

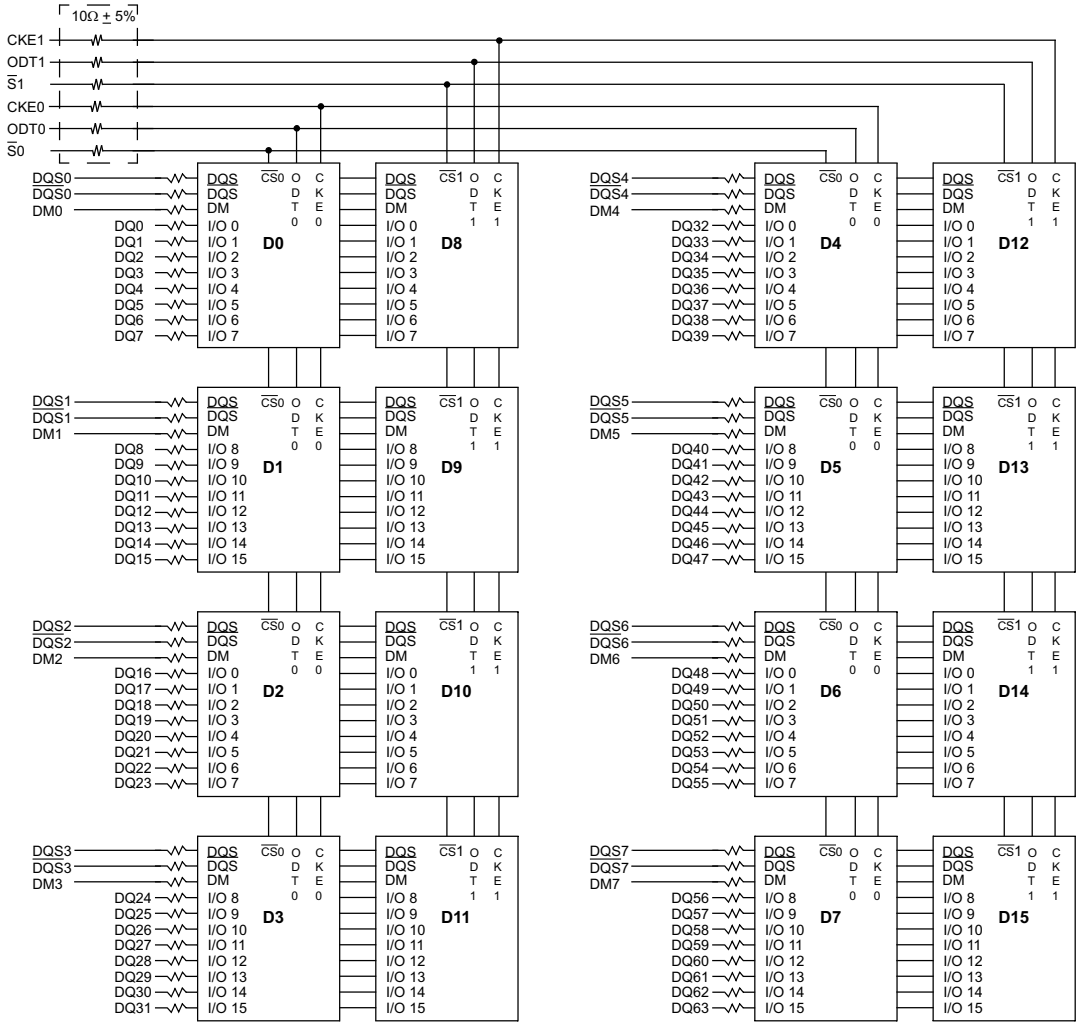
Pin Description

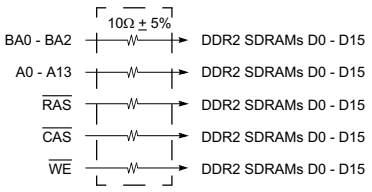
Pin Name	Function	Pin Name	Function
CK0,CK1	Clock Inputs, positive line	SDA	SPD Data Input/Output
$\overline{CK}0$,$\overline{CK}1$	Clock Inputs, negative line	SA1,SA0	SPD address
CKE0,CKE1	Clock Enables	DQ0~DQ63	Data Input/Output
$\overline{RAS}$	Row Address Strobe	DM0~DM7	Data Masks
$\overline{CAS}$	Column Address Strobe	DQS0~DQS7	Data strobes
$\overline{WE}$	Write Enable	$\overline{DQS}0$~$\overline{DQS}7$	Data strobes complement
$\overline{S}0$,$\overline{S}1$	Chip Selects	TEST	Logic Analyzer specific test pin (No connect on So-DIMM)
A0~A9, A11~A13	Address Inputs	V_{DD}	Core and I/O Power
A10/AP	Address Input/Autoprecharge	V_{SS}	Ground
BA0~BA2	SDRAM Bank Address	V_{REF}	Input/Output Reference
ODT0,ODT1	On-die termination control	V_{DD}SPD	SPD Power
SCL	Serial Presence Detect(SPD) Clock Input	NC	Spare pins, No connect

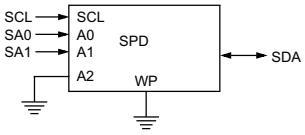
Input/Output Functional Description

Symbol	Type	Function
CK0-CK1 CK0-CK1	Input	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of CK . A Delay Locked Loop (DLL) circuit is driven from the clock input and output timing for read operations is synchronized to the input clock.
CKE0-CKE1	Input	Activates the DDR2 SDRAM CK signal when high and deactivates the CK signal when low, By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refesh mode.
S0-S1	Input	Enables the associated DDR2 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by S0, Rank 1 is selected by S1. Ranks are also called “Physical banks”.
RAS, CAS, WE	Input	When sampled at the cross point of the rising edge of CK and falling edge of CK, CAS, RAS, and WE define the operation to be executed by the SDRAM.
BA0~BA2	Input	Selects which DDR2 SDRAM internal bank is activated.
ODT0~ODT1	Input	Asserts on-die termination for DQ, DM, DQS, and DQS signals if enabled via the DDR2 SDRAM Extended Mode Register Set (EMRS).
A0~A9, A10/AP, A11~A13	Input	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of CK. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of CK. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be pecharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge.
DQ0~DQ63	In/Out	Data Input/Output pins.
DM0~DM7	Input	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
DQS0~DQS7 DQS0~DQS7	In/Out	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR2 SDRAMs and is sent at the leading edge of the data window. DQS signals are complements, and timing is relative to the crosspoint of respective DQS and DQS If the module is to be operated in single ended strobe mode, all DQS signals must be tied on the system board to VSS and DDR2 SDRAM mode registers programmed appropriately.
V_{DD},V_{DD} SPD,V_{SS}	Supply	Power supplies for core, I/O, Serial Presence Detect, and ground for the module.
SDA	In/Out	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected to V_{DD} to act as a pull up.
SCL	Input	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from SCL to V_{DD} to act as a pull up.
SA0~SA1	Input	Address pins used to select the Serial Presence Detect base address.
TEST	In/Out	The TEST pin is reserved for bus analysis tools and is not connected on normal memory modules(SO-DIMMs).

FUNCTIONAL BLOCK DIAGRAM

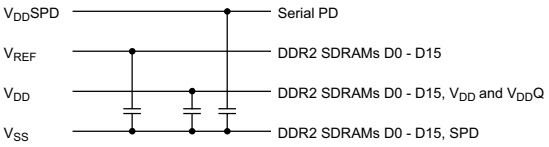






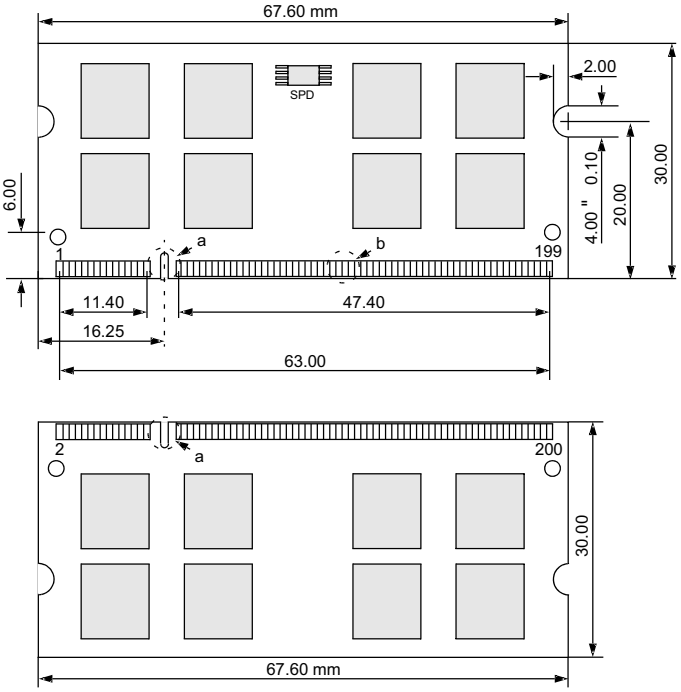
* Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/CK0	8 DDR2 SDRAMs
*CK1/CK1	8 DDR2 SDRAMs

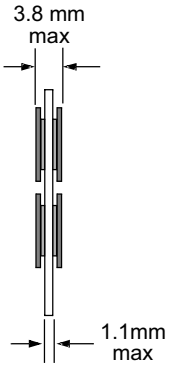
* Wire per Clock Loading Table/Wiring Diagrams



Notes :
1. DQ,DM, DQS/DQS resistors : 22 Ohms ± 5%.
2. BAx, Ax, RAS, CAS, WE resistors : 3.0 Ohms ± 5%.

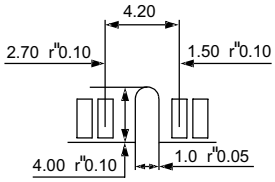
PACKAGE DIMENSIONS



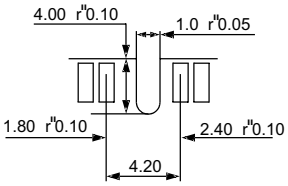


DETAIL a

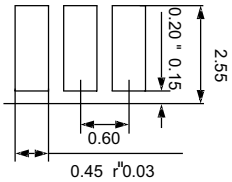
FRONT SIDE



BACK SIDE



DETAIL b



Tolerances:+-0.15mm unless otherwise specified

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