1GB DDR2 – SDRAM SO-DIMM

200 Pin SO-DIMM

SEN01G64D1BH1MT-25R

1GB PC2-6400 in FBGA Technology

RoHS compliant

Options:

- Data Rate / Latency — Marking
  - DDR2 800 MT/s CL6 — -25
  - DDR2 667 MT/s CL5 — -30
  - DDR2 533 MT/s CL4 — -37
- Module Density
  1GB with 8 dies and 1 rank
- Standard Grade (T_A) 0°C to 70°C
  (T_C) 0°C to 85°C
  Grade E (T_A) 0°C to 85°C
  (T_C) 0°C to 95°C
  Grade W (T_A) -40°C to 85°C
  (T_C) -40°C to 95°C

* The refresh rate has to be doubled when 85°C>T_C>95°C

Environmental Requirements:

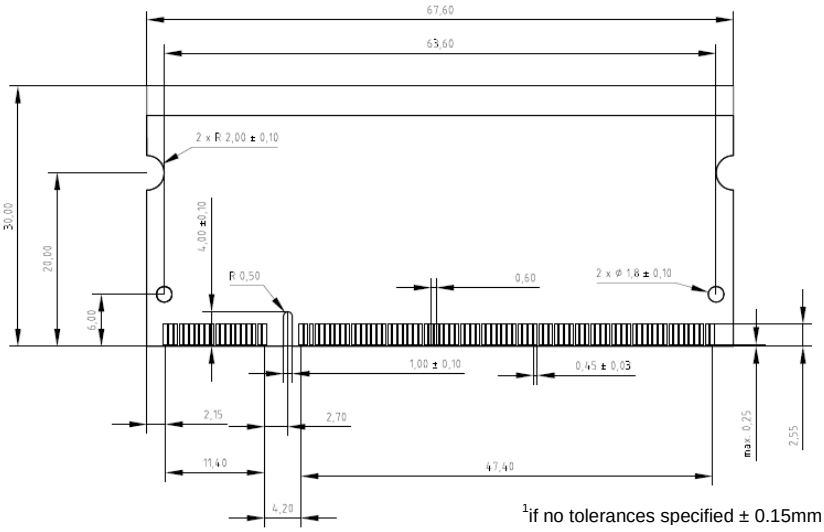
- Operating temperature (ambient)
  standard Grade 0°C to 70°C
  Grade E 0°C to 85°C
  Grade W -40°C to 85°C
- Operating Humidity
  10% to 90% relative humidity, noncondensing
- Operating Pressure
  105 to 69 kPa (up to 10000 ft.)
- Storage Temperature
  -55°C to 100°C
- Storage Humidity
  5% to 95% relative humidity, noncondensing
- Storage Pressure
  1682 PSI (up to 5000 ft.) at 50°C

Features:

- 200-pin 64-bit Small Outline, Dual-In-Line Double Data Rate Synchronous DRAM Module
- Module organization: single rank 128M x 64
- VDD = 1.8V ±0.1V, V_{DDQ} 1.8V ±0.1V
- 1.8V I/O (SSTL_18 compatible)
- Auto Refresh (CBR) and Self Refresh 8k Refresh every 64ms
- Serial Presence Detect with EEPROM
- Gold-contact pad
- This module is fully pin and functional compatible to the JEDEC PC2-6400 spec. and JEDEC- Standard MO-224. (see www.jedec.org)
- The pcb and all components are manufactured according to the RoHS compliance specification [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]

- **DDR2 - SDRAM component MICRON MT47H128M8CF-25 DIE-Revision H**
- 128Mx8 DDR2 SDRAM in FBGA-60 package
- Four bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Eight internal device banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency – 1 t_{CK}
- Programmable burst length: 4 or 8
- Adjustable data-output drive strength
- On-die termination (ODT)

Figure: mechanical dimensions[1]



[1]if no tolerances specified ± 0.15mm

This Swissbit module is an industry standard 200-pin 8-byte DDR2 SDRAM Small Outline Dual-In-line Memory Module (SO-DIMM) which is organized as x64 high speed CMOS memory arrays. The module uses internally configured octal-bank DDR2 SDRAM devices. The module uses double data rate architecture to achieve high-speed operation. DDR2 SDRAM modules operate from a differential clock (CK and CK#). READ and WRITE accesses to a DDR2 SDRAM module is burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. The burst length is either four or eight locations. An auto precharge function can be enabled to provide a self-timed row precharge that is initiated at the end of a burst access. The DDR2 SDRAM devices have a multibank architecture which allows a concurrent operation that is providing a high effective bandwidth. A self refresh mode is provided and a power-saving “power-down” mode. All inputs and all full drive-strength outputs are SSTL_18 compatible.
The DDR2 SDRAM module uses the optional serial presence detect (SPD) function implemented via serial EEPROM using the standard I^2C protocol. This nonvolatile storage device contains 256 bytes. The first 128 bytes are utilized by the SO-DIMM manufacturer (swissbit) to identify the module type, the module’s organization and several timing parameters. The second 128 bytes are available to the end user.

Module Configuration

Organization	DDR2 SDRAMs used	Row Addr.	Device Bank Select	Column Addr.	Refresh	Module Bank Select
128M x 64bit	8 x 128M x 8bit (1024Mbit)	14	BA0, BA1,BA2	10	8k	S0#

Module Dimensions in mm
67.60 (long) x 30 (high) x 3.80 [max] (thickness)

Timing Parameters

Part Number	Module Density	Transfer Rate	Clock Cycle/Data bit rate	Latency
SEN01G64D1BH1MT-25[E/W]R	1024 MB	6.4 GB/s	2.5ns/800MT/s	6-6-6
SEN01G64D1BH1MT-30[E/W]R	1024 MB	5.3 GB/s	3.0ns/667MT/s	5-5-5
SEN01G64D1BH1MT-37[E/W]R	1024 MB	4.26 GB/s	3.75ns/533MT/s	4-4-4

Pin Name

A0-9, A11 – A13	Address Inputs
A10/AP	Address Input / Autoprecharge Bit
BA0 – BA2	Bank Address Inputs
DQ0 – DQ63	Data Input / Output
DM0-DM7	Input Data Mask
DQS0 - DQS7	Data Strobe, positive line
DQS0# - DQS7#	Data Strobe, negative line (only used when differential data strobe mode is enabled)
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
CKE0	Clock Enable
CK0 – CK1	Clock Inputs, positive line

CK0# - CK1#	Clock Inputs, negative line
S0#	Chip Select
V_{DD}	Supply Voltage (1.8V± 0.1V)
V_{REF}	Input / Output Reference
V_{SS}	Ground
V_{DDSPD}	Serial EEPROM Positive Power Supply
SCL	Serial Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
SA0 – SA1	Presence Detect Address Inputs
ODT0	On-Die Termination
NC	No Connection

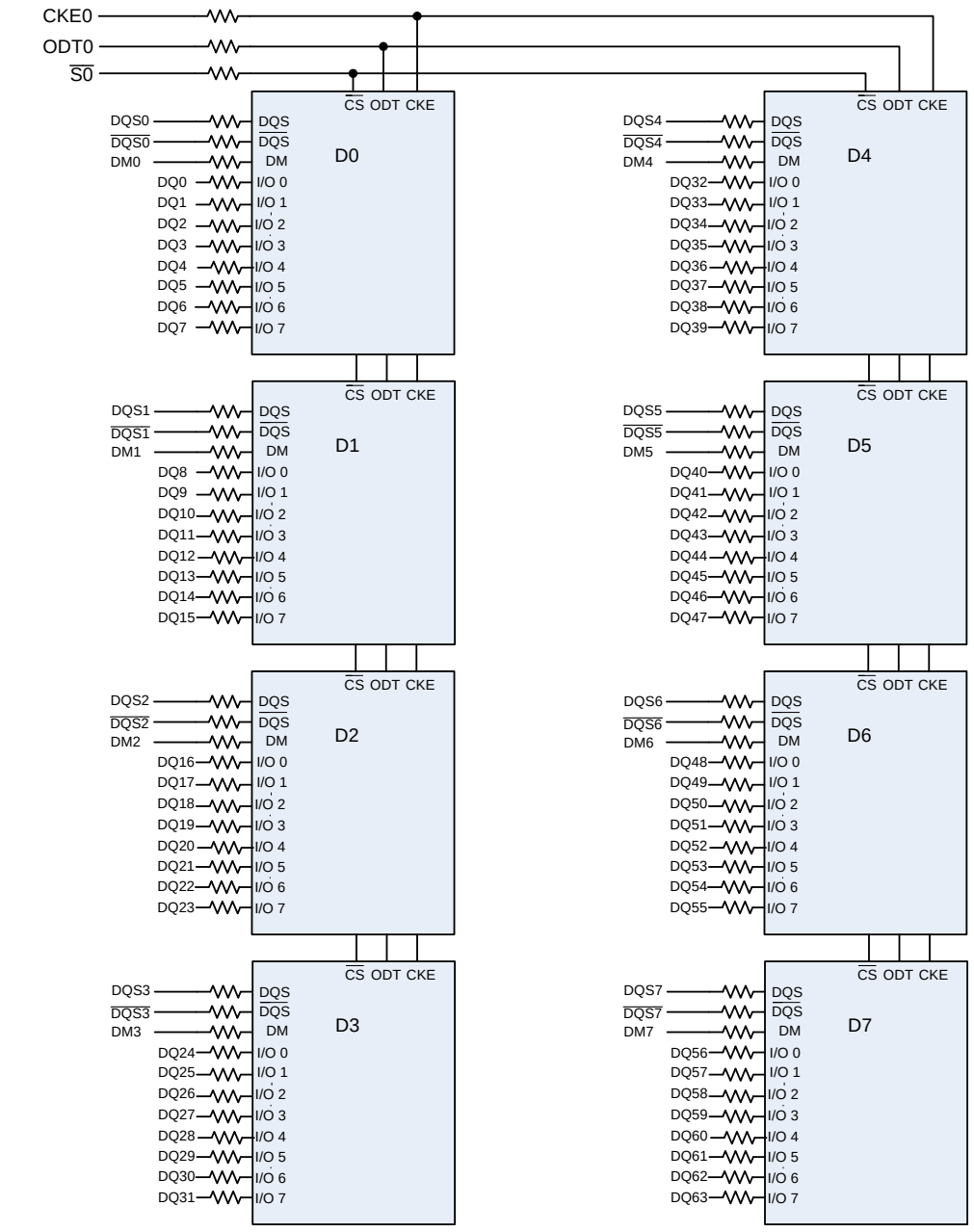
Pin Configuration

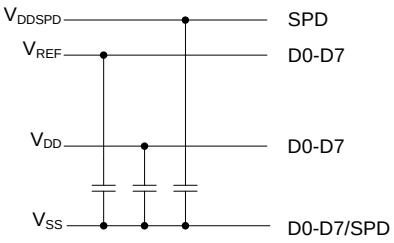
PIN #	Front Side	PIN #	Back Side	PIN #	Front Side	PIN #	Back Side
1	VREF	2	VSS	101	A1	102	A0
3	VSS	4	DQ4	103	VDD	104	VDD
5	DQ0	6	DQ5	105	A10/AP	106	BA1
7	DQ1	8	VSS	107	BA0	108	RAS#
9	VSS	10	DM0	109	WE#	110	S0#
11	DQS0#	12	VSS	111	VDD	112	VDD
13	DQS0	14	DQ6	113	CAS#	114	ODT0
15	VSS	16	DQ7	115	NC (S1#)	116	A13
17	DQ2	18	VSS	117	VDD	118	VDD
19	DQ3	20	DQ12	119	NC (ODT1)	120	NC (S3)
21	VSS	22	DQ13	121	VSS	122	VSS
23	DQ8	24	VSS	123	DQ32	124	DQ36
25	DQ9	26	DM1	125	DQ33	126	DQ37
27	VSS	28	VSS	127	VSS	128	VSS
29	DQS1#	30	CK0	129	DQS4#	130	DM4
31	DQS1	32	CK0#	131	DQS4	132	VSS
33	VSS	34	VSS	133	VSS	134	DQ38
35	DQ10	36	DQ14	135	DQ34	136	DQ39
37	DQ11	38	DQ15	137	DQ35	138	VSS
39	VSS	40	VSS	139	VSS	140	DQ44
41	VSS	42	VSS	141	DQ40	142	DQ45
43	DQ16	44	DQ20	143	DQ41	144	VSS
45	DQ17	46	DQ21	145	VSS	146	DQS5#
47	VSS	48	VSS	147	DM5	148	DQS5
49	DQS2#	50	NC (EVENT#)	149	VSS	150	VSS
51	DQS2	52	DM2	151	DQ42	152	DQ46

PIN #	Front Side	PIN #	Back Side	PIN #	Front Side	PIN #	Back Side
53	VSS	54	VSS	153	DQ43	154	DQ47
55	DQ18	56	DQ22	155	VSS	156	VSS
57	DQ19	58	DQ23	157	DQ48	158	DQ52
59	VSS	60	VSS	159	DQ49	160	DQ53
61	DQ24	62	DQ28	161	VSS	162	VSS
63	DQ25	64	DQ29	163	NC (TEST)	164	CK1
65	VSS	66	VSS	165	VSS	166	CK1#
67	DM3	68	DQS3#	167	DQS6#	168	VSS
69	NC (RESET#)	70	DQS3	169	DQS6	170	DM6
71	VSS	72	VSS	171	VSS	172	VSS
73	DQ26	74	DQ30	173	DQ50	174	DQ54
75	DQ27	76	DQ31	175	DQ51	176	DQ55
77	VSS	78	VSS	177	VSS	178	VSS
79	CKE0	80	NC (CKE1)	179	DQ56	180	DQ60
81	VDD	82	VDD	181	DQ57	182	DQ61
83	NC (S2#)	84	NC (A15)	183	VSS	184	VSS
85	BA2	86	NC (A14)	185	DM7	186	DQS7#
87	VDD	88	VDD	187	VSS	188	DQS7
89	A12	90	A11	189	DQ58	190	VSS
91	A9	92	A7	191	DQ59	192	DQ62
93	A8	94	A6	193	VSS	194	DQ63
95	VDD	96	VDD	195	SDA	196	VSS
97	A5	98	A4	197	SCL	198	SA0
99	A3	100	A2	199	VDDSPD	200	SA1

(Sig): Signal in brackets may be routed to the socket connector, but is not used on the module

FUNCTIONAL BLOCK DIAGRAMM 1GB DDR2 SDRAM SODIMM, 1 RANK AND 8 COMPONENTS





MAXIMUM ELECTRICAL DC CHARACTERISTICS

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD}	-1.0	2.3	V
I/O Supply Voltage	V_{DDQ}	-0.5	2.3	V
V_{DD}L Supply Voltage	V_{DDL}	-0.5	2.3	V
Voltage on any pin relative to V_{SS}	V_{in}, V_{out}	-0.5	2.3	V
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 0.95V (All other pins not under test = 0V)	I_I			µA
Command/Address RAS#, CAS#, WE#, S#, CKE		-40	40	
CK, CK#		-20	20	
DM		-5	5	
OUTPUT LEAKAGE CURRENT (DQ's and ODT are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ})	I_{OZ}	-5	5	µA
DQ, DQS, DQS#				
V_{REF} LEAKAGE CURRENT ; V_{REF} is on a valid level	I_{VREF}	-16	16	µA

DC OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
Supply Voltage	V_{DD}	1.7	1.8	1.9	V
I/O Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V
V_{DD}L Supply Voltage	V_{DDL}	1.7	1.8	1.9	V
I/O Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.50 x V_{DDQ}	0.51x V_{DDQ}	V
I/O Termination Voltage (system)	V_{TT}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
Input High (Logic 1) Voltage	$V_{IH\ (DC)}$	V_{REF} + 0.125		V_{DDQ} + 0.3	V
Input Low (Logic 0) Voltage	$V_{IL\ (DC)}$	-0.3		V_{REF} – 0.125	V

AC INPUT OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage	$V_{IH\ (AC)}$	V_{REF} + 0.25	-	V
Input Low (Logic 0) Voltage	$V_{IL\ (AC)}$	-	V_{REF} - 0.25	V

CAPACITANCE

At DDR2 data rates, it is recommended to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

I_{DD} Specifications and Conditions

(0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.8V ± 0.1V, V_{DD} = +1.8V ± 0.1V)

Parameter & Test Condition		Symbol	max.			Unit
			6400-666	5300-555	4200-444	
OPERATING CURRENT *) : One device bank Active-Precharge; t_{RC}= t_{RC} (I_{DD}); t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; DQ inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		I_{DD0}	720	680	560	mA
OPERATING CURRENT *) : One device bank; Active-Read-Precharge; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; t_{CK} = t_{CK} (I_{DD}), t_{RC}= t_{RC} (I_{DD}), t_{RAS} = t_{RAS} MIN (I_{DD}), t_{RCD} = t_{RCD} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address inputs changing once every two clock cycles; Data Pattern is same as I_{DD4W}		I_{DD1}	880	800	760	mA
PRECHARGE POWER-DOWN CURRENT: All device banks idle; Power-down mode; t_{CK} = t_{CK} (I_{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF}		I_{DD2P}	56	56	56	mA
PRECHARGE QUIET STANDBY CURRENT: All device banks idle; t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF}		I_{DD2Q}	400	320	320	mA
PRECHARGE STANDBY CURRENT: All device banks idle; t_{CK} = t_{CK} (I_{DD}); CKE is HIGH, CS# is HIGH; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle		I_{DD2N}	400	320	320	mA
ACTIVE POWER-DOWN CURRENT: All device banks open; t_{CK} = t_{CK} (I_{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V_{REF}	Fast PDN Exit MR[12] = 0	I_{DD3P}	320	240	240	mA
	Slow PDN Exit MR[12] = 1		80	80	80	mA
ACTIVE STANDBY CURRENT: All device banks open; t_{CK} = t_{CK} (I_{DD}), t_{RAS} = t_{RAS} MAX (I_{DD}), t_{RP} = t_{RP} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle		I_{DD3N}	480	440	360	mA

Parameter & Test Condition	Symbol	max.			Unit
		6400-666	5300-555	4200-444	
OPERATING READ CURRENT: All device banks open, Continuous burst reads; One module rank active; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; t_{CK} = t_{CK} (I_{DD}), t_{RAS} = t_{RAS} MAX (I_{DD}), t_{RP} = t_{RP} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I_{DD4R}	1280	1080	1000	mA
OPERATING WRITE CURRENT: All device banks open, Continuous burst writes; One module rank active; BL = 4, CL = CL (I_{DD}), AL = 0; t_{CK} = t_{CK} (I_{DD}), t_{RAS} = t_{RAS} MAX (I_{DD}), t_{RP} = t_{RP} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I_{DD4W}	1280	1080	1000	mA
BURST REFRESH CURRENT: t_{CK} = t_{CK} (I_{DD}); refresh command at every t_{RFC} (I_{DD}) interval, CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I_{DD5}	1880	1720	1680	mA
SELF REFRESH CURRENT: CK and CK# at 0V; CKE $\leq 0.2V$; All other Control and Address bus inputs are floating at V_{REF}; DQ's are floating at V_{REF}	I_{DD6}	56	56	56	mA
OPERATING CURRENT*) : Four device bank interleaving READs, I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = t_{RCD} (I_{DD}) – 1 x t_{CK} (I_{DD}); t_{CK} = t_{CK} (I_{DD}), t_{RC} = t_{RC} (I_{DD}), t_{RRD} = t_{RRD} (I_{DD}), t_{RCD} = t_{RCD} (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are not changing during DESELECT; DQ inputs changing once per clock cycle	I_{DD7}	2680	2240	2160	mA

TIMING VALUES USED FOR I_{DD} MEASUREMENT

I_{DD} MEASUREMENT CONDITIONS				
SYMBOL	**6400-666**	**5300-555**	**4200-444**	**Unit**
CL (I_{DD})	6	5	4	t_{CK}
t_{RCD} (I_{DD})	15	15	15	ns
t_{RC} (I_{DD})	60	60	60	ns
t_{RRD} (I_{DD})	7.5	7.5	7.5	ns
t_{CK} (I_{DD})	2.5	3.0	3.75	ns
t_{RAS} MIN (I_{DD})	45	45	45	ns
t_{RAS} MAX (I_{DD})	70'000	70'000	70'000	ns
t_{RP} (I_{DD})	15	15	15	ns
t_{RFC} (I_{DD})	127.5	127.5	127.5	ns

DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.8V ± 0.1V, V_{DD} = +1.8V ± 0.1V)

AC CHARACTERISTICS			6400-666		5300-555		4200-444		Unit
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	
Clock cycle time	CL = 6	t_{CK} (6)	2.5	8.0	-	+	-	-	ns
	CL = 5	t_{CK} (5)	3.0-	8.0-	3.0	8.0	-	-	ns
	CL = 4	t_{CK} (4)	3.75	8.0	3.75	8.0	3.75	8.0	ns
	CL = 3	t_{CK} (3)	-	-	5.0	8.0	5.0	8.0	ns
CK high-level width		t_{CH}	0.48	0.52	0.45	0.55	0.45	0.55	t_{CK}
CK low-level width		t_{CL}	0.48	0.52	0.45	0.55	0.45	0.55	t_{CK}
Half clock period		t_{HP}	min (t_{CH}, t_{CL})		min (t_{CH}, t_{CL})		min (t_{CH}, t_{CL})		ps
Access window (output) of DQ_S from CK/CK#		t_{AC}	-0.40	+0.40	-0.45	+0.45	-0.50	+0.50	ns
Data-out high-impedance window from CK/CK#		t_{HZ}		t_{AC} max		+0.45 (= t_{AC} max)		+0.50 (= t_{AC} max)	ns
Data-out low-impedance window from CK/CK#		t_{LZ}	t_{AC} min	t_{AC} max	-0.45 (= t_{AC} min)	+0.45 (= t_{AC} max)	-0.50 (= t_{AC} min)	+0.50 (= t_{AC} max)	ns
DQ and DM input setup time relative to DQS		t_{DS}	0.05		0.10		0.10		ns
DQ and DM input hold time relative to DQS		t_{DH}	0.125		0.30		0.35		ns
DQ and DM input pulse width (for each input)		t_{DIPW}	0.35		0.35		0.35		t_{CK}
Data hold skew factor		t_{QHS}		0.3		0.34		0.4	ns
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t_{QH}	t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		ns
Data valid output window		t_{DVW}	t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		ns
DQS input high pulse width		t_{DQSH}	0.35		0.35		0.35		t_{CK}
DQS input low pulse width		t_{DQSL}	0.35		0.35		0.35		t_{CK}
DQS falling edge to CK rising - setup time		t_{DSS}	0.2		0.2		0.2		t_{CK}
DQS falling edge from CK rising - hold time		t_{DSH}	0.2		0.2		0.2		t_{CK}
DQS –DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}		0.2		0.24		0.30	ns
DQS read preamble		t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}
DQS read postamble		t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
DQS write preamble		t_{WPRE}	0.35		0.35		0.25		t_{CK}
DQS write preamble setup time		t_{WPRES}	0		0		0		ns
DQS write postamble		t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
Positive DQS latching edge to associated clock edge		t_{DQSS}	- 0.25	+ 0.25	- 0.25	+ 0.25	- 0.25	+ 0.25	t_{CK}
Write command to first DQS latching transition		-	WL- t_{DQSS}	WL+ t_{DQSS}	WL- t_{DQSS}	WL+ t_{DQSS}	WL- t_{DQSS}	WL+ t_{DQSS}	t_{CK}
Address and control input pulse width (for each input)		t_{IPW}	0.6		0.6		0.6		t_{CK}
Address and control input setup time		t_{ISa}	0.175		0.4		0.5		ns

DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

(0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.8V ± 0.1V, V_{DD} = +1.8V ± 0.1V)

AC CHARACTERISTICS		6400-666		5300-555		4200-444		Unit
PARAMETER	SYMBOL	Min	Max	MIN	MAX	MIN	MAX	
Address and control input hold time	t_{IH}	0.25		0.4		0.5		ns
CAS# to CAS# command delay	t_{CCD}	2		2		2		t_{CK}
ACTIVE to ACTIVE (same bank) command period	t_{RC}	60		60		60		ns
ACTIVE bank *a* to ACTIVE bank *b* command	t_{RRD}	7.5		7.5		7.5		ns
ACTIVE to READ or WRITE delay	t_{RCD}	15		15		15		ns
Four bank Activate period	t_{FAW}	37.5		37.5		37.5		ns
ACTIVE to PRECHARGE command	t_{RAS}	45	70,000	45	70,000	45	70,000	ns
Internal READ to precharge command delay	t_{RTP}	7.5		7.5		7.5		ns
Write recovery time	t_{WR}	15		15		15		ns
Auto precharge write recovery + precharge time	t_{DAL}	$t_{WR} + t_{RP}$		$t_{WR} + t_{RP}$		$t_{WR} + t_{RP}$		ns
Internal WRITE to READ command delay	t_{WTR}	7.5		7.5		7.5		ns
PRECHARGE command period	t_{RP}	15		15		15		ns
PRECHARGE ALL command period	t_{RPA}	$t_{RP} + t_{CK}$		$t_{RP} + t_{CK}$		$t_{RP} + t_{CK}$		ns
LOAD MODE command cycle time	t_{MRD}	2		2		2		t_{CK}
CKE low to CK, CK# uncertainty	t_{DELAY}	$t_{IS} + t_{CK} + t_{IH}$		$t_{IS} + t_{CK} + t_{IH}$		$t_{IS} + t_{CK} + t_{IH}$		t_{CK}
REFRESH to ACTIVE or REFRESH to REFRESH command interval	t_{RFC}	127.5	70,000	127.5	70,000	127.5	70,000	ns
Average periodic refresh interval (0°C<= T_{CASE} <= 85 °C)	t_{REFI}		7.8		7.8		7.8	µs
(85°C<= T_{CASE} <= 95 °C)	$t_{REFI\ (IT)}$		3.9		3.9		3.9	µs
Exit SELF REFRESH to non-READ command	t_{XSNR}	t_{RFC}(min) + 10		t_{RFC}(min) + 10		t_{RFC}(min) + 10		ns
Exit SELF REFRESH to READ command	t_{XSRD}	200		200		200		t_{CK}
Exit SELF REFRESH timing reference	t_{ISXR}	t_{IS}		t_{IS}		t_{IS}		ps
ODT turn-on delay	t_{AOND}	2	2	2	2	2	2	t_{CK}
ODT turn-on	t_{AON}	t_{AC}(min)	t_{AC}(max) + 1,000	t_{AC}(min)	t_{AC}(max) + 1,000	t_{AC}(min)	t_{AC}(max) + 1,000	ps
ODT turn-off delay	t_{AOFD}	2.5	2.5	2.5	2.5	2.5	2.5	t_{CK}
ODT turn-off	t_{AOF}	t_{AC}(min)	t_{AC}(max) + 600	t_{AC}(min)	t_{AC}(max) + 600	t_{AC}(min)	t_{AC}(max) + 600	ps
ODT turn-on (power-down mode)	t_{AONPD}	t_{AC}(min) + 2,000	2 x t_{CK} + t_{AC}(max) + 1,000	t_{AC}(min) + 2,000	2 x t_{CK} + t_{AC}(max) + 1,000	t_{AC}(min) + 2,000	2 x t_{CK} + t_{AC}(max) + 1,000	ps
ODT turn-off (power-down mode)	t_{AOFPD}	t_{AC}(min) + 2,000	2.5 x t_{CK} + t_{AC}(max) + 1,000	t_{AC}(min) + 2,000	2.5 x t_{CK} + t_{AC}(max) + 1,000	t_{AC}(min) + 2,000	2.5 x t_{CK} + t_{AC}(max) + 1,000	ps
ODT to power-down entry latency	t_{ANPD}	3		3		3		t_{CK}

DDR2 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

(0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.8V ± 0.1V, V_{DD} = +1.8V ± 0.1V)

AC CHARACTERISTICS		6400-666		5300-555		4200-444		Unit
PARAMETER	SYMBOL	Min	Max	MIN	MAX	MIN	MAX	
ODT power-down exit latency	t_{AXPD}	8		8		8		t_{CK}
ODT enable from MRS command	t_{MOD}	12		12		12		ns
Exit active power-down to READ command, MR [bit 12 = 0]	t_{XARD}	2		2		2		t_{CK}
Exit active power-down to READ command, MR [bit 12 = 1]	t_{XARDS}	8 – AL		7 – AL		6 – AL		t_{CK}
Exit precharge power-down to any non-READ command	t_{XP}	2		2		2		t_{CK}
CKE minimum high/low time	t_{CKE}	3		3		3		t_{CK}

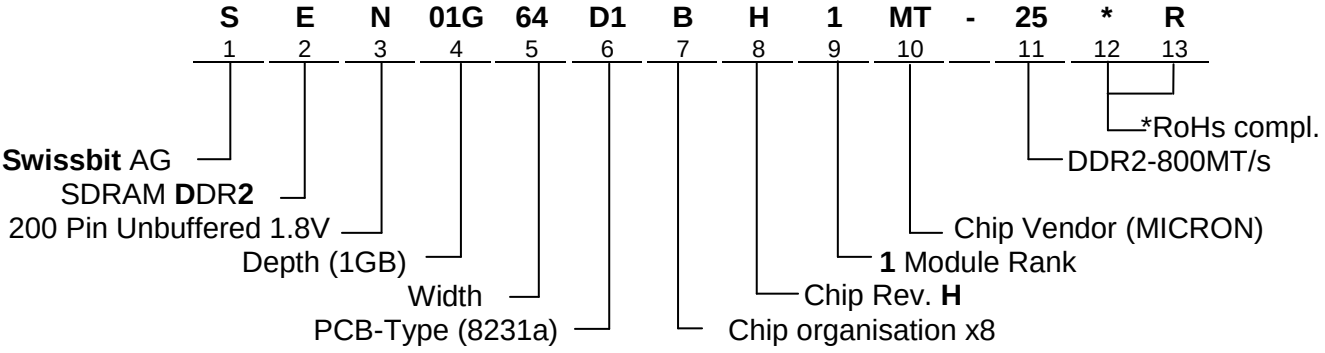
SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	6400-666	5300-555	4200-444
0	NUMBER OF SPD BYTES USED	0x80		
1	TOTAL NUMBER OF BYTES IN SPD DEVICE	0x08		
2	FUNDAMENTAL MEMORY TYPE	0x08		
3	NUMBER OF ROW ADDRESSES ON ASSEMBLY	0x0E		
4	NUMBER OF COLUMN ADDRESSES ON ASSEMBLY	0x0A		
5	DIMM HIGHT AND MODULE RANKS	0x60		
6	MODULE DATA WIDTH	0x40		
7	MODULE DATA WIDTH (continued)	0x00		
8	MODULE VOLTAGE INTERFACE LEVELS (V_{DDQ})	0x05		
9	SDRAM CYCLE TIME, (t_{CK}) [max CL] CL = 6 (6400), CL = 5 (5300), CL = 4 (4200)	0x25	0x30	0x3D
10	SDRAM ACCESS FROM CLOCK, (t_{AC}) [max CL] CL = 6 (6400), CL = 5 (5300), CL = 4 (4200)	0x40	0x45	0x50
11	MODULE CONFIGURATION TYPE	0x00		
12	REFRESH RATE / TYPE	0x82		
13	SDRAM DEVICE WIDTH (PRIMARY SDRAM)	0x08		
14	ERROR- CHECKING SDRAM DATA WIDTH	0x00		
15	MINIMUM CLOCK DELAY, BACK-TO-BACK RANDOM COLUMN ACCESS	0x00		
16	BURST LENGTHS SUPPORTED	0x0C		
17	NUMBER OF BANKS ON SDRAM DEVICE	0x08		
18	CAS LATENCIES SUPPORTED	0x70	0x38	0x18
19	MODULE THICKNESS	0x01		
20	DDR2 DIMM TYPE	0x04		
21	SDRAM MODULE ATTRIBUTES	0x00		
22	SDRAM DEVICE ATTRIBUTES: Weak Driver and 50Ω ODT	0x03		0x01
23	SDRAM CYCLE TIME, (t_{CK}) [max CL – 1] CL = 5 (6400), CL = 4 (5300), CL = 3 (4200)	0x30	0x3D	0x50
24	SDRAM ACCESS FROM CK, (t_{AC}) [max CL – 1] CL = 5 (6400), CL = 4 (5300), CL = 3 (4200)	0x40	0x45	0x50
25	SDRAM CYCLE TIME, (t_{CK}) [max CL – 2] CL = 4 (6400), CL = 3 (5300)	0x3D	0x50	0x00
26	SDRAM ACCESS FROM CK, (t_{AC}) [max CL – 2] CL = 4 (6400), CL = 3 (5300)	0x40	0x45	0x00
27	MINIMUM ROW PRECHARGE TIME, (t_{RP})	0x3C		
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, (t_{RRD})	0x1E		
29	MINIMUM RAS# TO CAS# DELAY, (t_{RCD})	0x3C		
30	MINIMUM RAS# PULSE WIDTH, (t_{RAS})	0x2D		
31	MODULE BANK DENSITY	0x01		

SERIAL PRESENCE-DTECT MATRIX (continued)

BYTE	DESCRIPTION	6400-666	5300-555	4200-444
32	ADDRESS AND COMMAND SETUP TIME, (t_{ISb})	0x17	0x20	0x25
33	ADDRESS AND COMMAND HOLD TIME, (t_{IHb})	0x25	0x27	0x37
34	DATA / DATA MASK INPUT SETUP TIME, (t_{DSb})	0x05	0x10	
35	DATA / DATA MASK INPUT HOLD TIME, (t_{DHb})	0x12	0x17	0x22
36	WRITE RECOVERY TIME, (t_{WR})	0x3C		
37	WRITE to READ Command Delay, (t_{WTR})	0x1E		
38	READ to PRECHARGE Command Delay, (t_{RTP})	0x1E		
39	Mem Analysis Probe	0x00		
40	Extension for Bytes 41 and 42	0x06		
41	MIN ACTIVE AUTO REFRESH TIME, (t_{RC})	0x3C		
42	MINIMUM AUTO REFRESH TO ACTIVE / AUTO REFRESH COMMAND PERIOD, (t_{RFC})	0x7F		
43	SDRAM DEVICE MAX CYCLE TIME, (t_{CKMAX})	0x80		
44	SDRAM DEVICE MAX DQS-DQ SKEW TIME, (t_{DQSQ})	0x14	0x18	0x1E
45	SDRAM DEVICE MAX READ DATA HOLD SKEW FACTOR, (t_{QHS})	0x1E	0x22	0x28
46	PLL Relock Time	0x00		
47-61	Optional Features, not supported	0x00		
62	SPD REVISION	0x13		
63	CHECKSUM FOR BYTES 0-62	0xCA	0xEF	0x9A
64-66	MANUFACTURER`S JEDEC ID CODE	0x7F		
67	MANUFACTURER`S JEDEC ID CODE (continued)	0xDA		
68-71	RESERVED	0x00		
72	MANUFACTURING LOCATION	0x01 (Switzerland) | 0x02 (Germany) | 0x03 (USA)		
73-90	MODULE PART NUMBER (ASCII)	"SEN01G64D1BH1MT-xx"		
91	PCB IDENTIFICATION CODE	x		
92	IDENTIFICATION CODE (continued)	x		
93	YEAR OF MANUFACTURE IN BCD	x		
94	WEEK OF MANUFACTURE IN BCD	x		
95-98	MODULE SERIAL NUMBER	x		
99-127	MANUFACTURER-SPECIFIC DATA (RSVD)	0x00		
128-255	Open for customer use	0xff		

Part Number Code



* optional / additional information

Locations

Swissbit AG
Industriestrasse 4 – 8
CH – 9552 Bronschhofen
Switzerland
Phone: +41 (0)71 913 03 03
Fax: +41 (0)71 913 03 15

Swissbit Germany GmbH
Wolfener Strasse 36
D – 12681 Berlin
Germany
Phone: +49 (0)30 93 69 54 – 0
Fax: +49 (0)30 93 69 54 – 55

Swissbit NA, Inc.
14 Willett Avenue, Suite 301A
Port Chester, NY 10573
USA
Phone: +1 914 935 1400
Fax: +1 914 935 9865

Swissbit NA, Inc.
3913 Todd Lane, Suite – 307
Austin, TX 78744
USA
Phone: +1 512 302 9001
Fax: +1 512 302 4808

Swissbit Japan, Inc.
3F Core Koenji,
2-1-24 Koenji-Kita, Suginami-Ku,
Tokyo 166-0002
Japan
Phone: +81 3 5356 3511
Fax: +81 3 5356 3512

Mouser Electronics

Authorized Distributor

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Swissbit:
SEN01G64D1BH1MT-25WR