Home Bus System (HBS) Compatible Transceiver

MAX22288

General Description

The MAX22288 Home Bus System (HBS) compatible transceiver can be used in the Home Bus System, where data and power are passed on a single pair of wires while minimizing the need for external components.

The MAX22288 provides robust communication by using dynamic cable termination that improves the signal quality with longer cables and higher data rates. The device data outputs AIO/BIO do not load the bus when the MAX22288 is not powered. The MAX22288 supports passing data with speed up to 200kbps.

The MAX22288 features adjustable receiver thresholds and driver slew rates that allow the MAX22288 to be used in a wide variety of systems. Integrated protection ensures robust communication in harsh industrial environments.

The MAX22288 is pin-to-pin compatible with the MAX22088, the Home Bus System (HBS) Compatible Transceiver with Active Inductor. The MAX22288 is recommended for use in an HBS system where an external power supply is typically available.

The MAX22288 is specified for operation over the -40°C to +125°C temperature range and is available in a compact 24-pin 4mm x 4mm TQFN package.

Benefits and Features

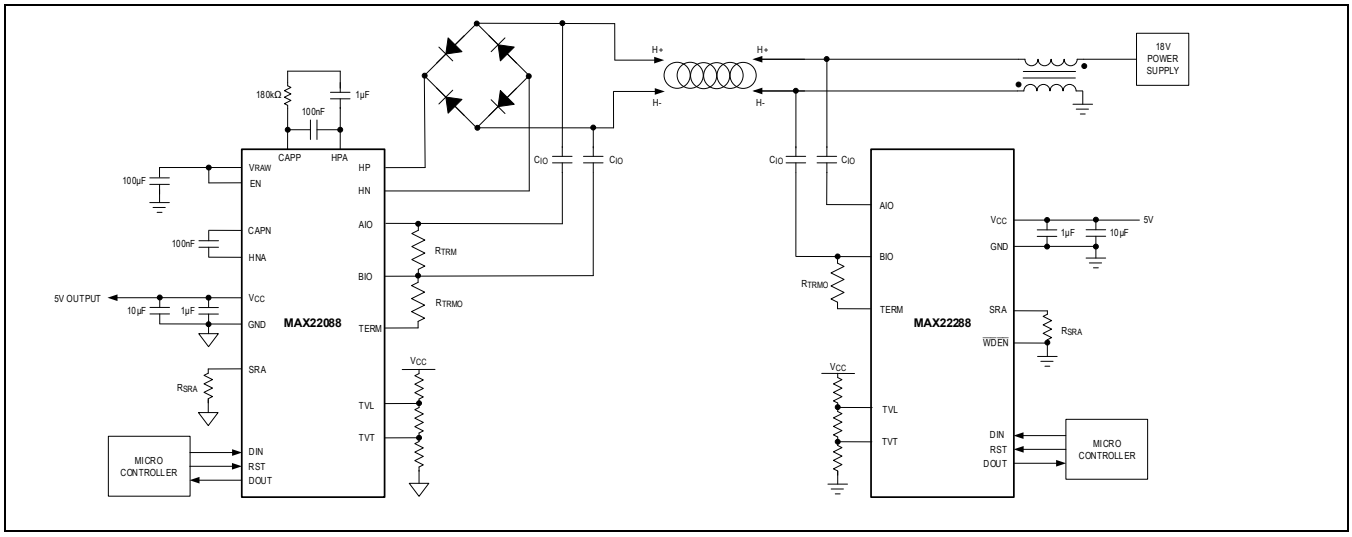
- Robust Communication with Configurability
- Dynamic Cable Termination Improves Signal Quality for High-Speed Applications
- Adjustable Slew Rates for Low EMI
- Maximum Data Rate up to 200kbps over 1000m UTP Cable
- Programmable Receiver Thresholds
- Space Saving
  - 4mm x 4mm TQFN package
  - Pin-to-pin Compatible with the MAX22088
- Integrated Protection
  - IEC 61000-4-2 ±8kV Contact and ±15kV Air-Gap ESD Protection
  - IEC 61000-4-5 ±1kV Transient Surge Protection with Selected External Components
  - -40°C to +125°C Operating Temperature Range

Applications

- HVAC
- Building Controllers
- Industrial IoT

***Ordering Information* appears at end of data sheet.**

Simplified Home Bus System (HBS)



19-101199; Rev 1; 09/23

Absolute Maximum Ratings

V_{CC} to GND ..... -0.3V to +6.0V

AIO, BIO, TERM to GND ..... -0.3V to +6.0V

SRA to GND ..... -0.3V to (V_{CC} + 0.3)V

$\overline{WDEN}$, $\overline{HPEN}$, TVL, TVT to GND ..... -0.3V to +6.0V

DIN, DOUT, RST to GND ..... -0.3V to +6.0V

Continuous Current Into Any Pin

V_{CC}, AIO, BIO, TERM ..... ±100mA

All Other Pins ..... ±50mA

Continuous Power Dissipation

Single-Layer Board (T_A = +70°C, derate 20.8mW/°C above +70°C) 1666.70mW

Multilayer Board (T_A = +70°C, derate 27.8mW/°C above +70°C) 2222.20mW

Temperature Ratings

Operating Temperature Range ..... -40°C to +125°C

Junction Temperature ..... +150°C

Storage Temperature Range ..... -40°C to +150°C

Lead Temperature (soldering, 10s) ..... +300°C

Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

24-Pin TQFN

Package Code	T2444+4C
Outline Number	*21-0139*
Land Pattern Number	*90-0022*
Thermal Resistance, Single-Layer Board:	
Junction-to-Ambient (θ_{JA})	48°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	3°C/W
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	36°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	3°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics

(R_{SRA} = 120kΩ, V_{CC} = 4.5V to 5.5V, V_{TVL} = 1V, V_{TVT} = 0.5V, T_A = -40°C to +125°C. Typical values are at V_{CC} = 5V, T_A = +25°C, unless otherwise noted.) (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER						
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Supply Current	I_{CC}	V_{RST} = GND, DIN at 57.6kbps, R_{LOAD} = 200Ω between AIO/BIO		14	18	mA
Undervoltage-Lockout Threshold	V_{UVLO}	V_{CC} rising	3.8		4.3	V
Undervoltage-Lockout Threshold Hysteresis	V_{UVHYST}			140		mV
DC CHARACTERISTICS / TRANSMITTER (AIO, BIO, TERM)						
Output Voltage High	V_{TOH}	AIO, BIO to GND, R_{LOAD} = 200Ω between AIO/BIO	V_{CC} - 0.6			V
Output Voltage Low	V_{TOL}	AIO, BIO to GND, R_{LOAD} = 200Ω between AIO/BIO			0.6	V
Termination Switch On Resistance	R_{TERM}	TERM to AIO	2.5	5	10	Ω
Bias Voltage Ratio Matching	V_{AIO} / V_{BIO}	AIO, BIO unconnected	-1		+1	%
AIO, BIO Loading Current	I_{IOLD}	V_{CC} = 0V, V_{AIO} = 5.5V, V_{BIO} = 5.5V			250	µA
AIO, BIO Input Resistance	R_{IN}	Input resistance of AIO and BIO when they are unconnected, DIN = V_{CC}	15			kΩ
DC CHARACTERISTICS / RECEIVER (TVL, TVT)						
Receive Threshold Leading Edge	V_{LEAD}	V_{TVL} = 1.0V, $\overline{HPEN}$ = V_{CC}	0.85	1	1.15	V
Receive Threshold Trailing Edge	V_{TRAIL}	V_{TVT} = 0.5V, $\overline{HPEN}$ = V_{CC}	0.35	0.5	0.65	V
TVL and TVT Input Leakage Current	I_{THLEAK}	V_{TVT} = V_{TVL} = 2.5V	-1		+1	µA
TVL and TVT Input Voltage	V_{TH}				V_{CC} – 1.5	V
DC CHARACTERISTICS / DIGITAL IO (DIN, DOUT, $\overline{WDEN}$, $\overline{HPEN}$)						
Input Logic High	V_{IH}		1.4			V
Input Logic Low	V_{IL}				0.4	V
Input Leakage Current	I_{LEAK}	Leakage at DIN and $\overline{HPEN}$	-1		+1	µA
$\overline{WDEN}$ Pull-Down Resistance	$R_{\overline{WDEN}}$	Internal pull-down resistance from $\overline{WDEN}$ to GND	100	176	300	kΩ
Open-Drain Logic-Low	V_{OL}	DOUT, I_{SINK} = 2mA			0.3	V
Open-Drain Leakage	I_{ODL}	V_{OD} = V_{CC}, output not asserted			1	µA
AC CHARACTERISTICS / TRANSMITTER (Note 2)						
Output Rise Time Leading Edge	t_{RLD}	R_{SRA} = 120kΩ, R_{LOAD} = 200Ω, *Figure 1*	0.9	1.5	2.5	µs

(R_{SRA} = 120kΩ, V_{CC} = 4.5V to 5.5V, V_{TVL} = 1V, V_{TVT} = 0.5V, T_A = -40°C to +125°C. Typical values are at V_{CC} = 5V, T_A = +25°C, unless otherwise noted.) (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Fall Time Leading Edge	t_{FLD}	R_{SRA} = 120kΩ, R_{LOAD} = 200Ω, *Figure 1*	0.9	1.5	2.5	µs
Output Rise Time Trailing Edge	t_{RTR}	R_{SRA} = 120kΩ, R_{LOAD} = 200Ω, *Figure 1*	0.9	1.5	2.5	µs
Output Fall Time Trailing Edge	t_{FTR}	R_{SRA} = 120kΩ, R_{LOAD} = 200Ω, *Figure 1*	0.9	1.5	2.5	µs
Transmit Propagation Delay	t_{TPROP}	R_{SRA} = 120kΩ, R_{LOAD} = 200Ω, *Figure 1*			1.4	µs
Transmission Output Symmetry	t_{SYM}	R_{SRA} = 120kΩ, R_{LOAD} = 200Ω, *Figure 1*	-0.5	0	+0.5	µs
Termination Switching Delay	t_{TERM}	R_{SRA} = 120kΩ, R_{LOAD} = 200Ω, *Figure 2*			0.5	µs
Termination On-Time	t_{TRMON}	R_{SRA} = 120kΩ, R_{LOAD} = 200Ω, *Figure 2*	19	34	63	µs
AC CHARACTERISTICS / RECEIVER (Note 2)						
Receiver Propagation Delay	t_{RPROP}	$\overline{HPEN}$ = V_{CC}, *Figure 3*			1	µs
Receiver High Pass Filter Time Constant	t_{HP}	$\overline{HPEN}$ = GND		1200		µs
Watchdog Timeout	t_{WDTO}	*Figure 4*	8	21	44	ms
PROTECTION						
ESD Protection AIO, BIO, TERM to GND (Note 3)		IEC 61000-4-2 air-gap discharge		±15		kV
ESD Protection AIO, BIO, TERM to GND (Note 3)		IEC 61000-4-2 contact discharge		±8		kV
ESD Protection (All Pins)		Human Body Model		±4		kV

Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Note 2: Not production tested. Guaranteed by design.

Note 3: Guaranteed by design. Both air-gap and contact ESD are tested with no power connected to V_{CC}.

Timing Diagrams and Test Circuits

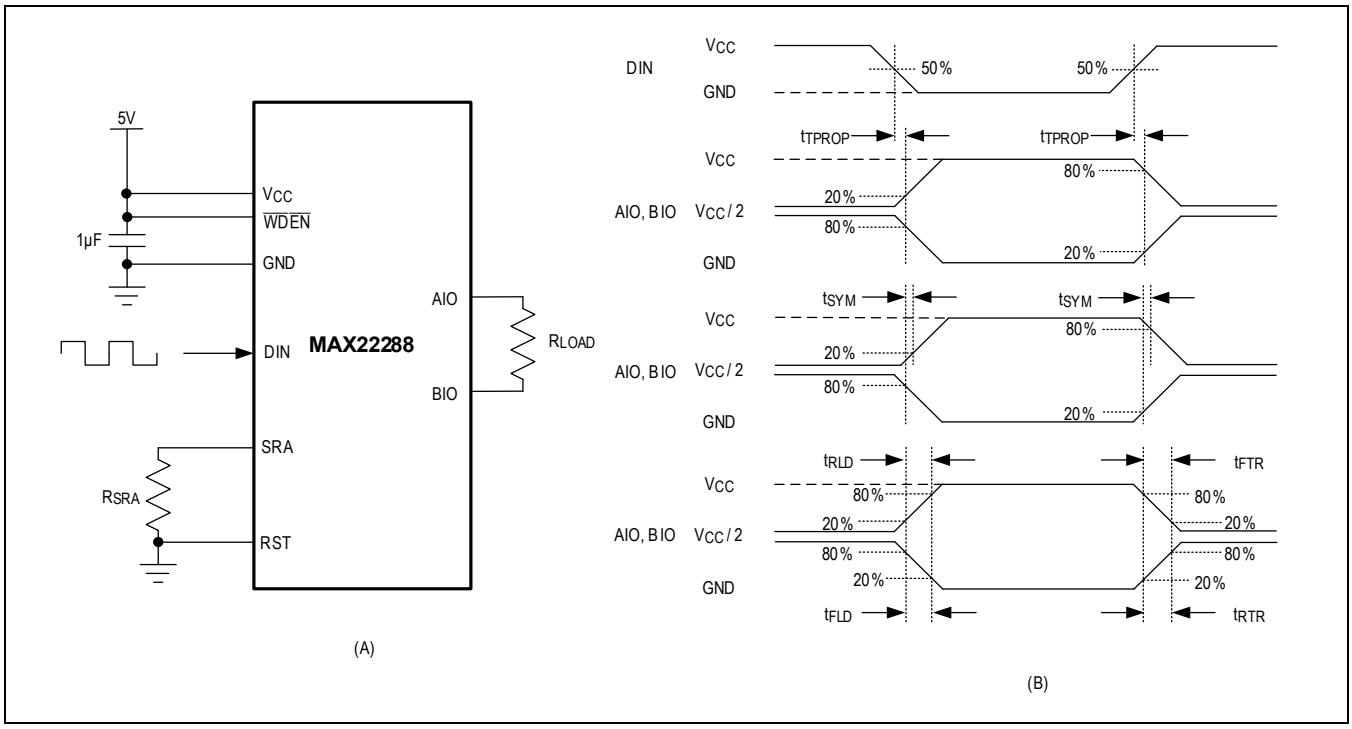


Figure 1. Transmit Channel Timing Diagram

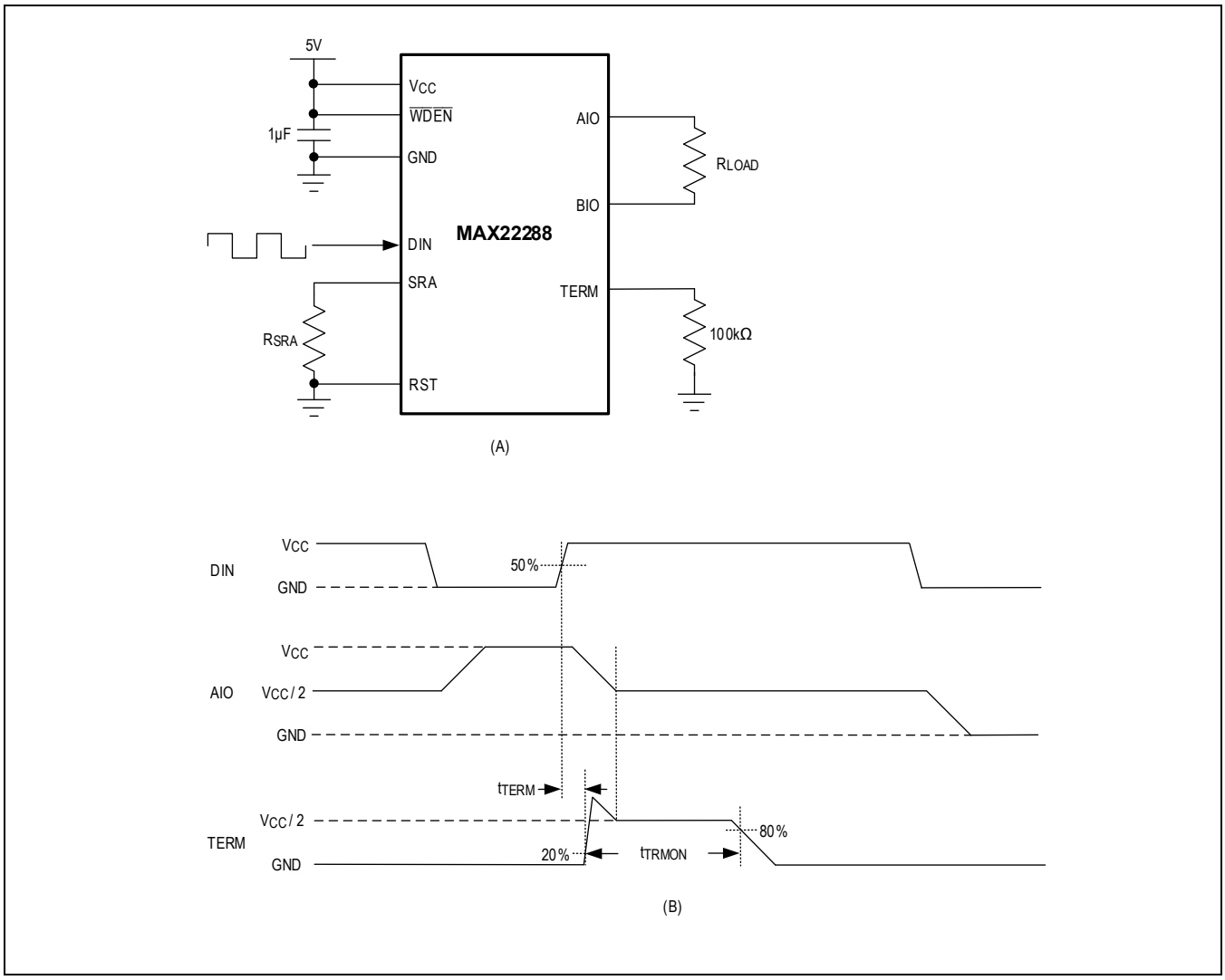


Figure 2. Transmission Switch Delay and Termination On-Time

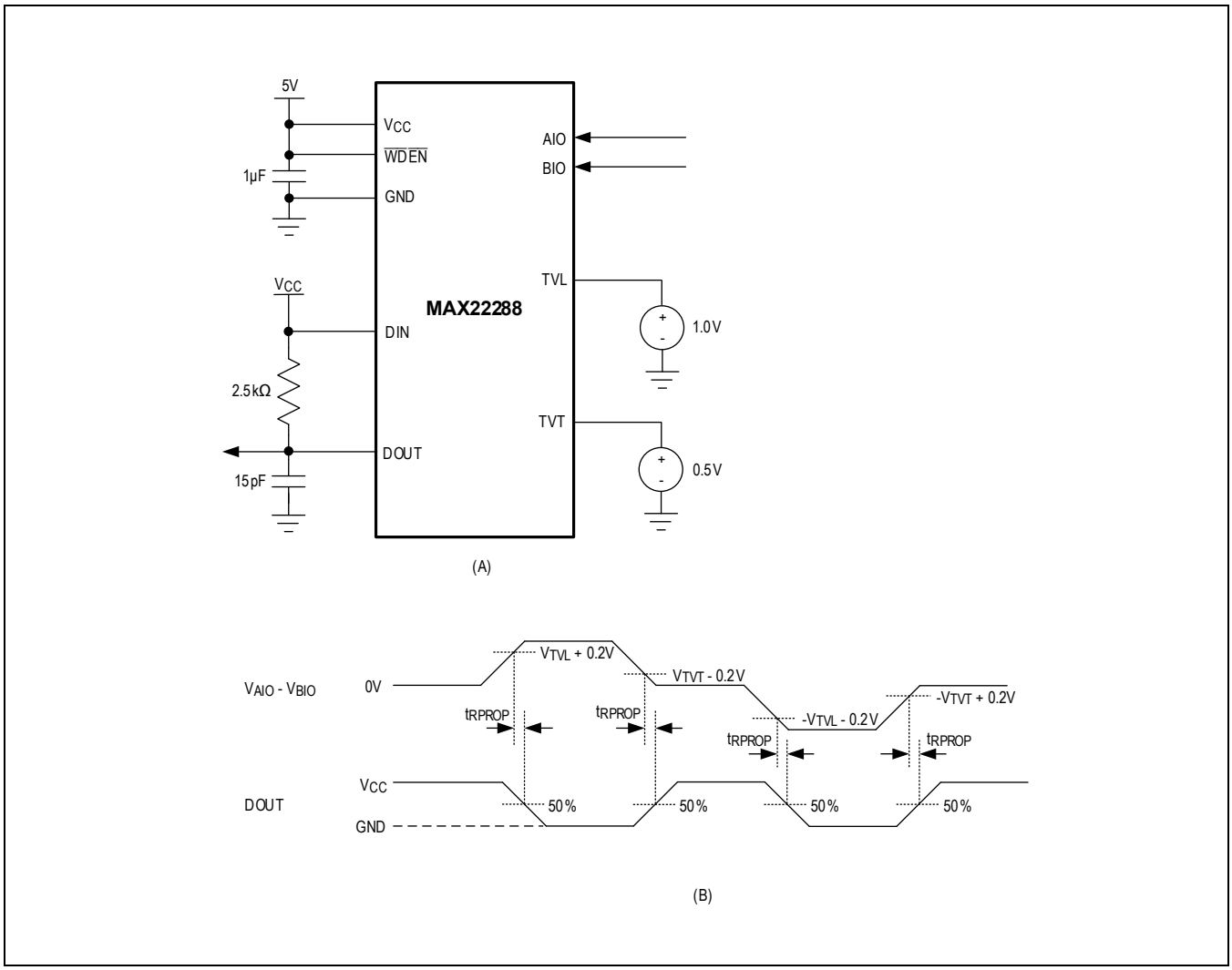


Figure 3. Receiver Propagation Delay

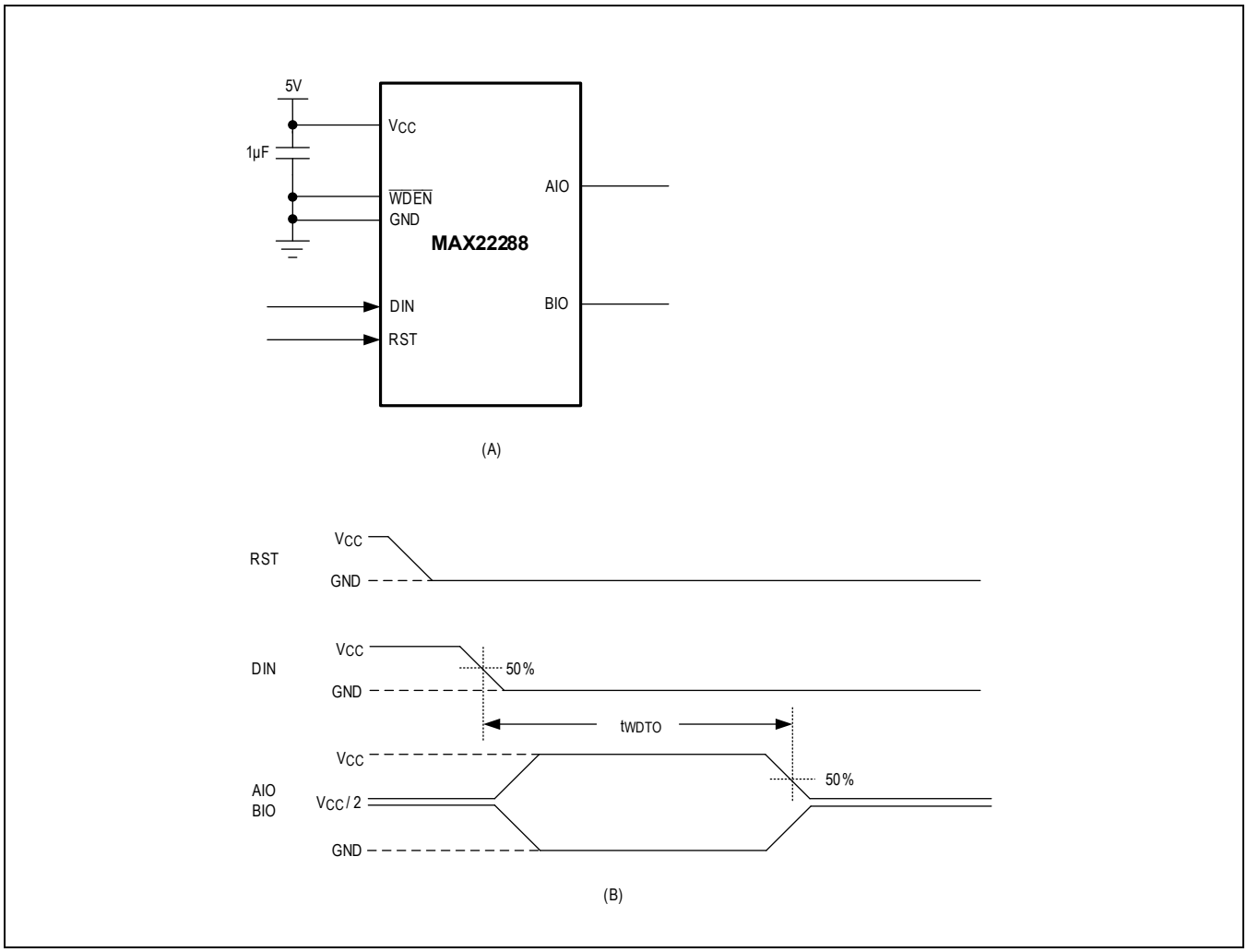
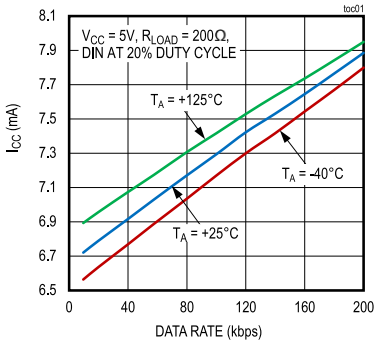


Figure 4. Watchdog Timeout

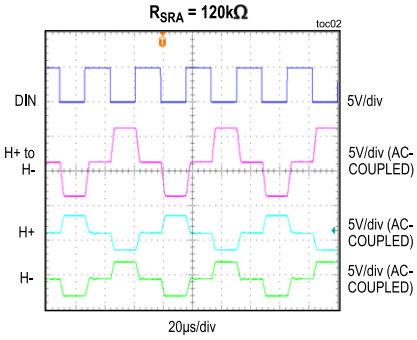
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

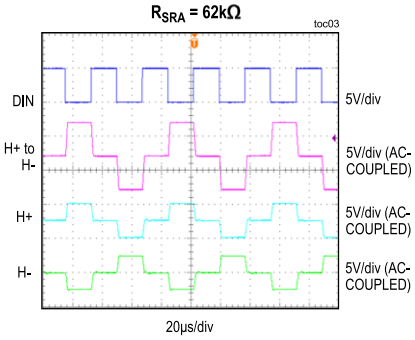
I_{CC} vs DATA RATE



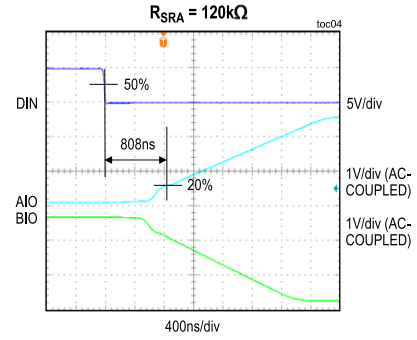
TRANSMITTER WAVEFORM
R_{SRA} = 120kΩ



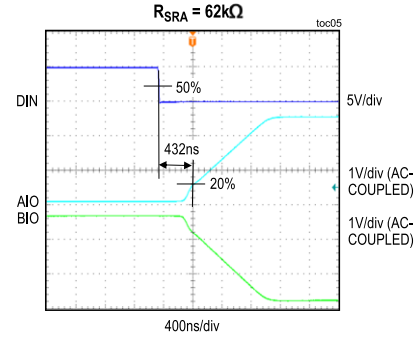
TRANSMITTER WAVEFORM
R_{SRA} = 62kΩ



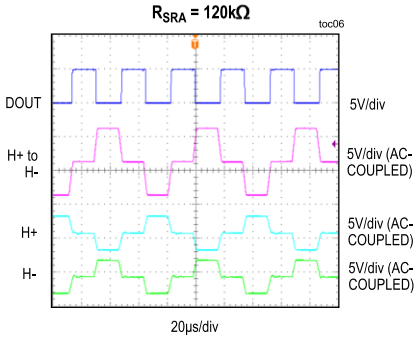
TRANSMITTER PROPAGATION DELAY
R_{SRA} = 120kΩ



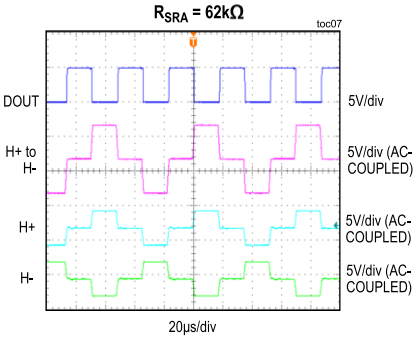
TRANSMITTER PROPAGATION DELAY
R_{SRA} = 62kΩ



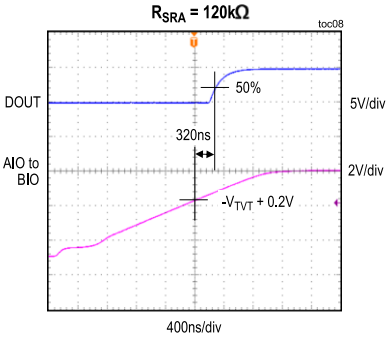
RECEIVER WAVEFORM
R_{SRA} = 120kΩ



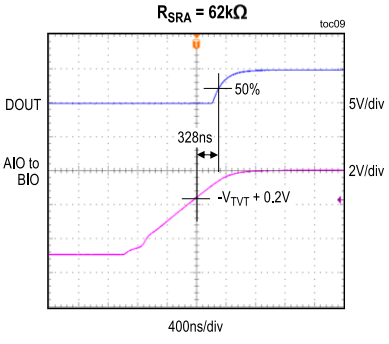
RECEIVER WAVEFORM
R_{SRA} = 62kΩ



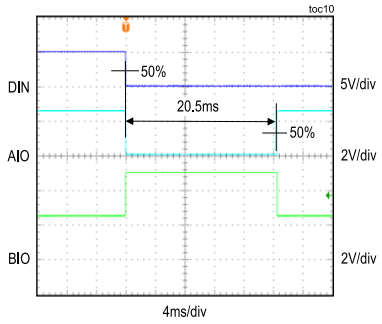
RECEIVER PROPAGATION DELAY
R_{SRA} = 120kΩ



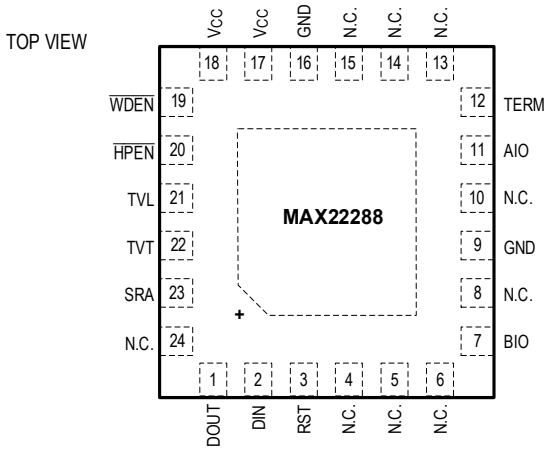
RECEIVER PROPAGATION DELAY
R_{SRA} = 62kΩ



WATCHDOG TIMEOUT



Pin Configuration

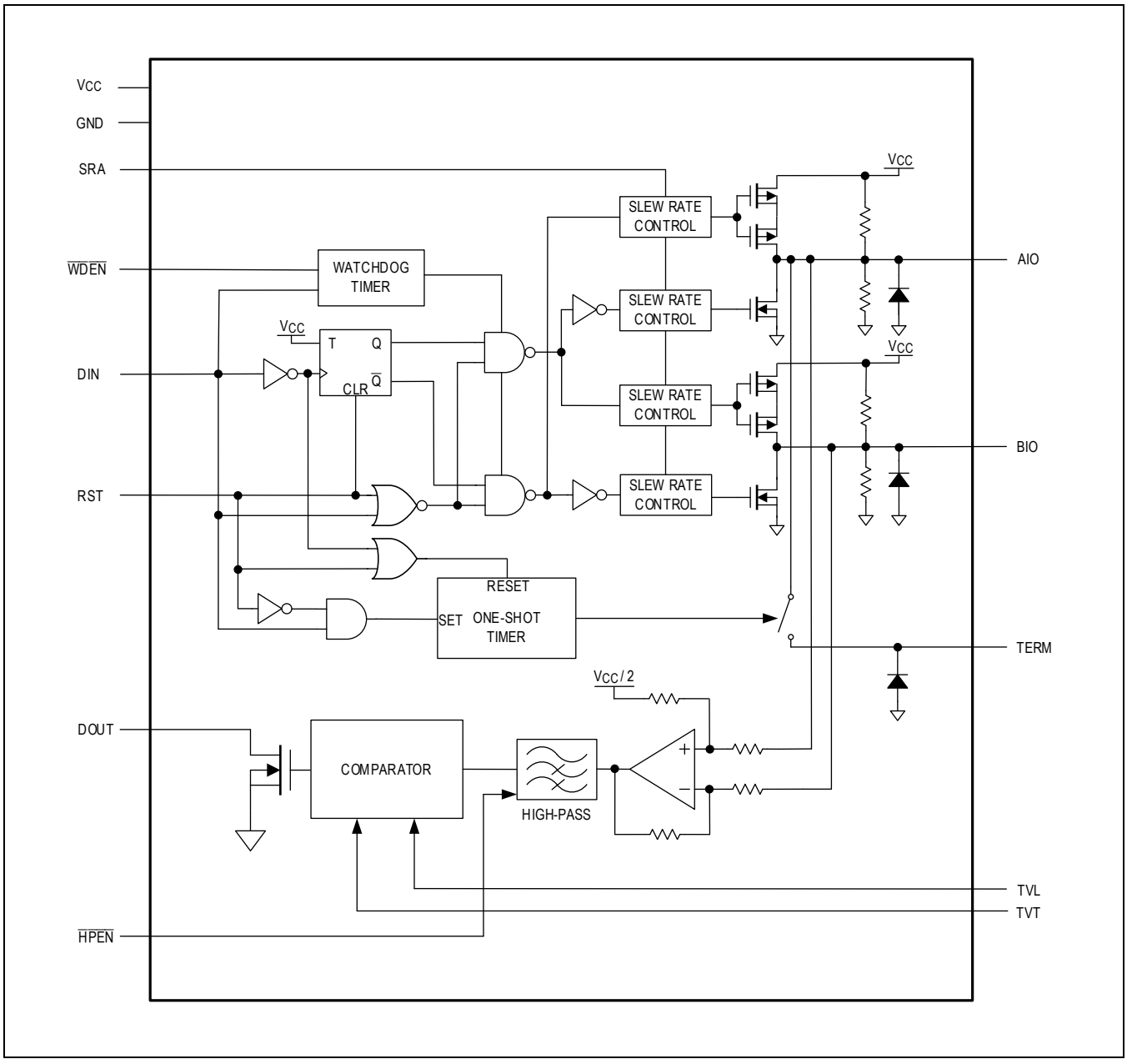


TQFN
4mm x 4mm

Pin Descriptions

PIN	NAME	FUNCTION
17, 18	V_{CC}	Power Supply. Bypass V_{CC} to GND with a 1µF (min) ceramic capacitor as close to the pin as possible.
EP	EP	Exposed Pad. Connect EP to GND.
9, 16	GND	Ground Reference
7	BIO	HBS Data Input and Output. Connect BIO to HBS through an external capacitor. See the *Operation of MAX22288 Transceiver* section for more information.
11	AIO	HBS Data Input and Output. Connect AIO to HBS through an external capacitor. See the *Operation of MAX22288 Transceiver* section for more information.
12	TERM	Switched Bus Termination. Connect a resistor between TERM and BIO to adjust Home Bus cable termination for better signal quality. See the *Dynamic Cable Termination* section for more information.
21	TVL	Leading Edge Data Threshold. See the *Receiver Threshold Adjustment* section for more information.
22	TVT	Trailing Edge Data Threshold. See the *Receiver Threshold Adjustment* section for more information.
1	DOUT	Open-Drain Data Output. Connect a pullup resistor to the logic voltage supply.
2	DIN	Data Input
3	RST	Bus Reset Control Input. See the *RST (Reset) Functionality* section for more information.
20	$\overline{HPEN}$	High Pass Filter Enable Input. Connect $\overline{HPEN}$ to GND to enable the internal high pass filter on receiver input. Connect $\overline{HPEN}$ to V_{CC} to disable the internal high pass filter. Do not leave $\overline{HPEN}$ unconnected. See the *High Pass Filter* section for more information.
23	SRA	Slew Rate Adjustment Input. Connect SRA to GND through a resistor to adjust the slew rate of the AIO and BIO transmit edges. See the *Transmit Slew Rate Adjustment* section for more information.
19	$\overline{WDEN}$	Watchdog Timer Enable Input. Connect $\overline{WDEN}$ to GND to enable the internal watchdog timer on AIO and BIO. Connect $\overline{WDEN}$ to V_{CC} to disable the watchdog timer. $\overline{WDEN}$ has a weak internal pulldown to ground. See the *Watchdog Timer Functionality* section for more information.
4, 5, 6, 8, 10, 13, 14, 15, 24	N.C.	Not Connected.

Functional Diagram



Detailed Description

The MAX22288 can be used in the Home Bus System (HBS), where power and data are carried on a single pair of wires.

The MAX22288 operates with data rates up to 200kbps for bus-powered applications. The MAX22288 is used in HBS applications where external power supplies are sourced. In HBS applications where power is consumed, the MAX22088, a HBS compatible transceiver with active inductor, can be used. Refer to the *MAX22088* data sheet for more information.

The MAX22288 features dynamic cable termination, configurable receiver thresholds, and transmit driver slew rate adjustment for better signal quality and flexible design.

Power Supply

The MAX22288 is powered by the external 5V (typ) supplied at V_{CC}. An external inductor and coupling capacitors are required to superimpose the data on the HBS cable.

Operation of MAX22288 Transceiver

The MAX22288 uses three pins for the logic interface: RST, DIN, and DOUT. AIO, BIO, and TERM are connected to the HBS network. RST is the bus reset control input. Drive RST low to enable the transmitter on AIO and BIO. Drive RST high to disable the transmitter. The MAX22288 HBS receiver is always enabled.

DIN is the logic input of the MAX22288. DOUT is the logic output. When DIN goes from high to low, the polarities of AIO and BIO invert. When DIN goes from low to high, AIO and BIO are set to high-impedance (*Figure 5*).

DOUT asserts low when the leading edge of V_{AIO} - V_{BIO} crosses V_{TVL} or $-V_{TVL}$. DOUT is high-impedance when the trailing edge of V_{AIO} - V_{BIO} crosses V_{TVT} or $-V_{TVT}$. See the *Receiver Threshold Adjustment* section for more information.

To improve signal quality, the MAX22288 features an internal switch that connects TERM to AIO for 34µs (typ) after the driver transitions to high-impedance. See the *Dynamic Cable Termination* section for more information.

For a typical data rate of 57.6kbps, the recommended value for coupling capacitors is 2.2µF (min).

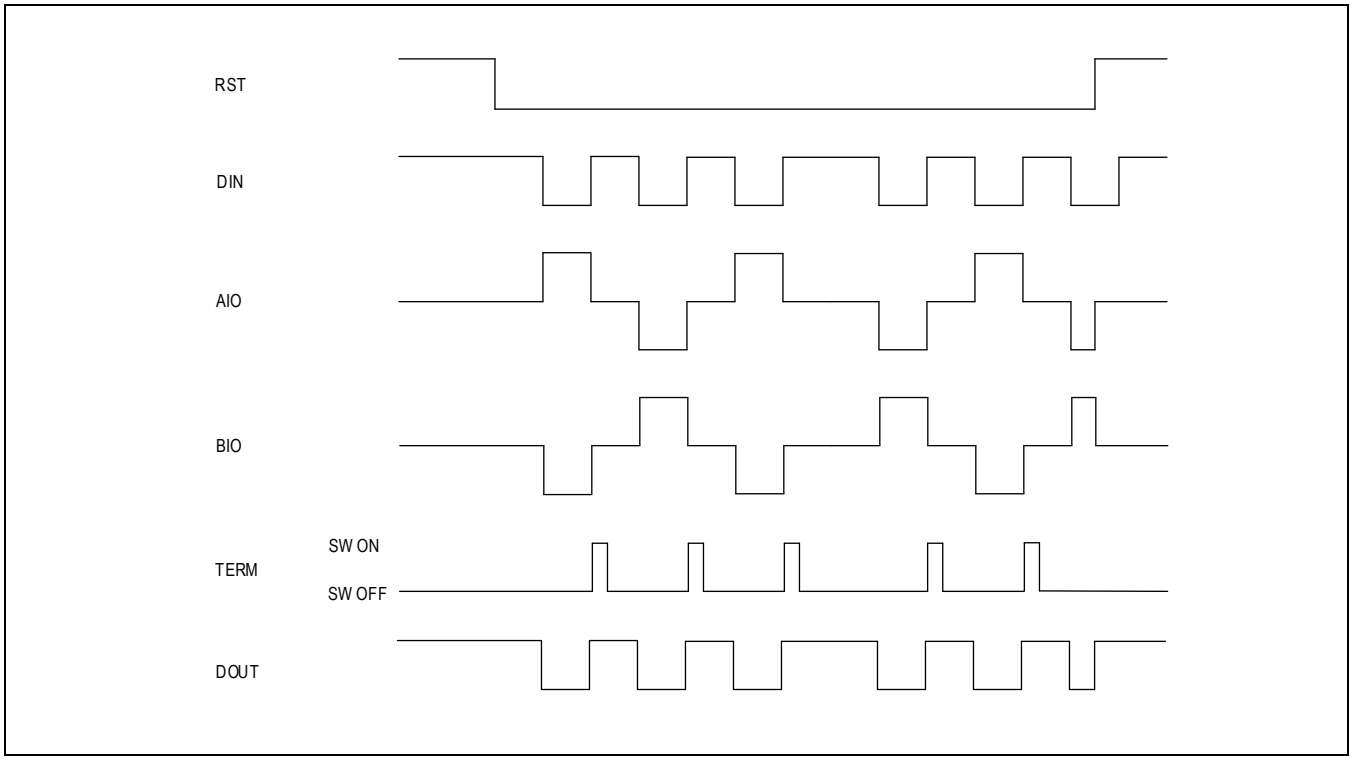


Figure 5. Operation of the MAX22288

Dynamic Cable Termination

The MAX22288 supports HBS signals at data rates up to 200kbps. When operating at high data rates, the mismatch between the HBS cable impedance and cable termination resistor can negatively affect the signal quality. The MAX22288 features dynamic cable termination to improve the signal quality with longer cables. When the driver transitions to high-impedance, an internal switch connects AIO to TERM. The external termination resistor at TERM is then connected between AIO and BIO in parallel with the static cable termination resistor. The internal switch opens after 34µs (typ), when DIN is driven low, or when RST is driven high. The optimized value of the dynamic termination resistor depends on the application. For typical applications, the value of the dynamic termination resistor is between 50Ω and 240Ω.

Transmit Slew Rate Adjustment

Connect an external resistor R_{SRA} from SRA to GND to control the slew rate of the transmit signals at AIO and BIO. The transmit rise/fall time (t_{RLD}, t_{FLD}, t_{RTR}, t_{FTR}) is proportional to R_{SRA} and is calculated using the following equation:

$$t_{rise/fall}\ (ns) = 17pF \times R_{SRA}\ (k\Omega)$$

For most applications, it is recommended to use R_{SRA} = 62kΩ resulting in 1µs (typ) output rise/fall time. Ensure that

R_{SRA} is in the range from 33kΩ to 470kΩ.

Receiver Threshold Adjustment

The threshold levels for the receiving signals are set by the voltages at TVL and TVT. The voltage at TVL sets the threshold for the leading edge of the pulse on the Home Bus signal (V_{AIO} - V_{BIO}). The voltage at TVT sets the threshold for the trailing edge of the pulse. Ensure that $V_{TVL} > V_{TVT}$.

DOUT asserts low when V_{AIO} - V_{BIO} crosses V_{TVL} or $-V_{TVL}$. DOUT is high-impedance when V_{AIO} - V_{BIO} crosses V_{TVT} or $-V_{TVT}$ (*Figure 6*). Connect a pullup resistor from DOUT to a logic voltage supply of the microcontroller. Ensure the pullup resistor is in the range from 1kΩ to 100kΩ.

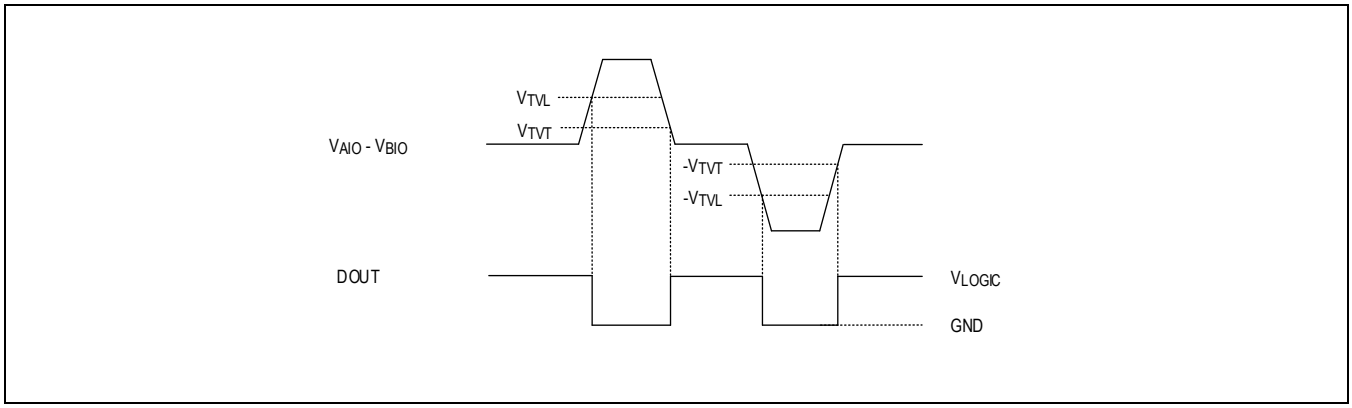


Figure 6. Receiver Threshold

RST (Reset) Functionality

The MAX22288 features a bus reset control input. Drive RST low to enable the transmitter. Drive RST high to disable the transmitter. RST also controls the internal switch used for dynamic cable termination. Ensure that RST remains low for at least 34µs (typ) after the internal switch is closed when the driver transitions to high-impedance. The internal switch opens when RST is driven high.

High Pass Filter

The MAX22288 features an internal high-pass filter on the receiver to filter out the low frequency voltage fluctuations at AIO and BIO. Connect $\overline{HPEN}$ to GND to enable the internal high-pass filter on the receiver input. Connect $\overline{HPEN}$ to V_{CC} to disable the internal high pass filter. Ensure that $\overline{HPEN}$ is always connected.

Watchdog Timer Functionality

The MAX22288 features an internal watchdog timer to avoid the bus being blocked by a long zero. This feature is enabled by setting $\overline{WDEN}$ to low. The internal watchdog timer monitors the logic input DIN and if any long zero condition persists for more than 21ms (typ) and blocks the bus, it sets the AIO and BIO outputs to high-impedance states. Any transition resets the watchdog timer. $\overline{WDEN}$ has a weak internal pulldown to ground.

Applications Information

Surge Protection

External components are required to protect the MAX22288 Home Bus pins (AIO, BIO, and TERM) from high-voltage transient events. The *Typical Application Circuit* shows a recommended protection scheme.

AIO, BIO, and TERM Surge Protection

AIO, BIO, and TERM must be protected with external components from surge transients. Connect TVS diodes with a 5.8V (max) standoff voltage from AIO and BIO to GND. Connect a 4.7Ω serial resistor between each TVS diode and AIO/BIO to limit the current flows into AIO/BIO during the surge transients. Depending on the surge transient polarities, the residual current after the 4.7Ω resistor flows from AIO/BIO through the internal ESD clamping diodes to V_{CC} or GND. Connect a 1µF (min) ceramic capacitor as close to V_{CC} as possible, and a 10µF (min) bulk capacitor on the V_{CC} bus to absorb this current and limit the voltage overshoot on V_{CC} during surge transients.

Layout Recommendations

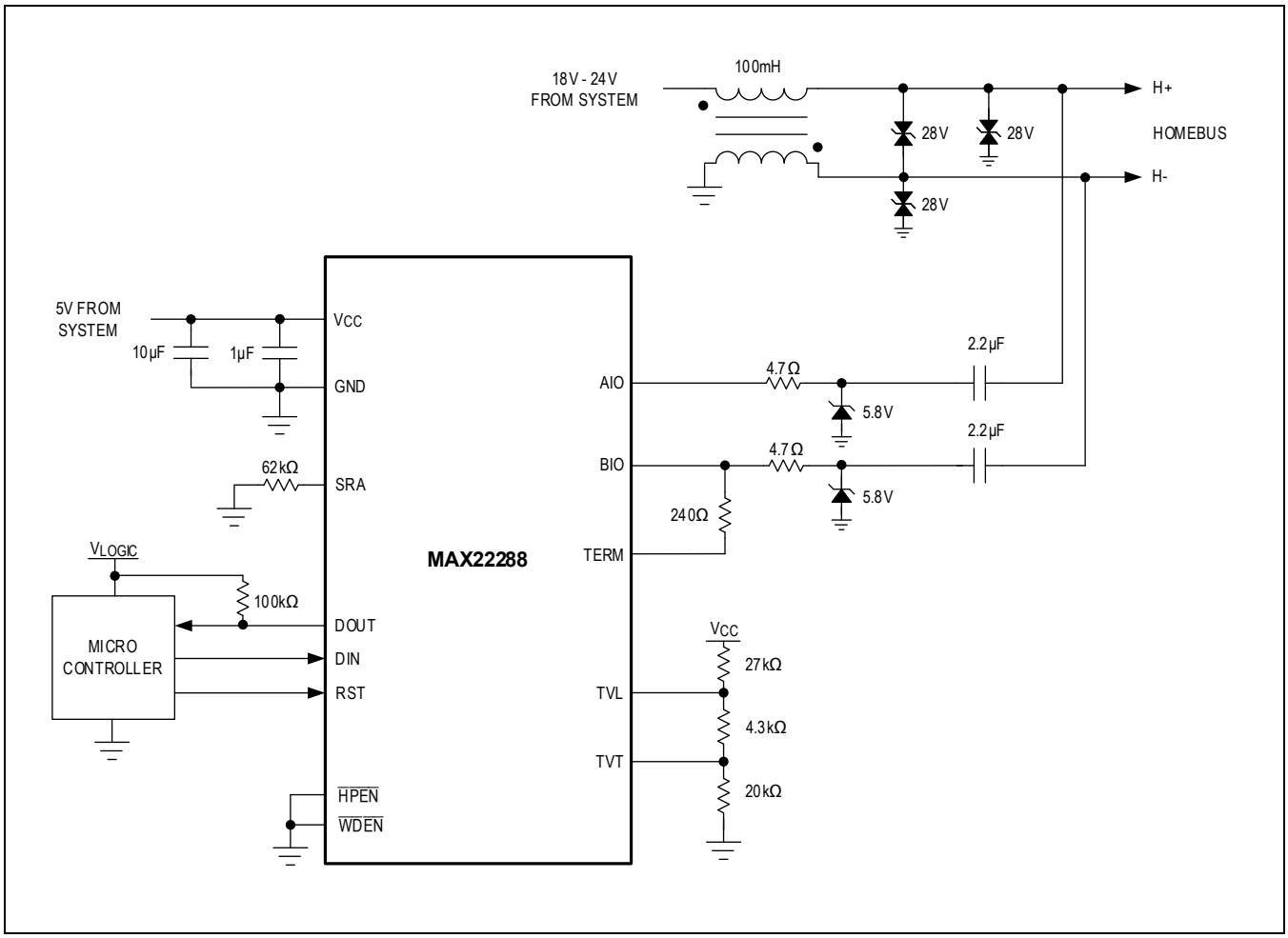
To ensure proper protection, connect the ground return of the protection diodes directly to the ground plane. Use a star configuration to connect all grounds together as close to the GND (pin 9) as possible. Place the external protection TVS diodes and the diode bridge as close to the Home Bus connector as possible.

Application Notes

Refer to *AN7224*, *Introduction to Home Bus*, for Home Bus System (HBS) standard and communication protocols.

Refer to *AN7226*, *How to Transmit UART Packets Using Home Bus System (HBS) Compatible Transceiver*, for data packet processing examples in a microcontroller in the Home Bus System.

Typical Application Circuit for 57.6kbps Operation



Ordering Information

PART	TEMPERATURE RANGE
MAX22288ATG+	-40°C to +125°C
MAX22288ATG+T	-40°C to +125°C

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/21	Release for Market Intro	—
1	9/23	Updated the Dynamic Cable Termination section and updated the entire document according to ADI Format.	1–18

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