

## Integrated, Step-Down Switching Regulator with Selectable Applications Configurations

## MAX16425/MAX16425A

### General Description

The MAX16425/MAX16425A are fully-integrated, highly efficient switching regulators for applications operating from 4.5V to 16V input supplies that require up to 25A maximum load. These single-chip regulators provide a compact high-efficiency, power-delivery solution for precision outputs that demand fast transient response.

The two devices have different programmability options (see [Table 3a](#) and [3b](#) for details) to enable a wide range of configurations. The programmable features include: internal/external reference voltage, output voltage set-point, switching frequency, overcurrent protection level (OCP), and soft-start timing. Discontinuous current mode (DCM) operation can be enabled through pin-strapping to improve light-load efficiency.

The MAX16425/MAX16425A include multiple protection and measurement features. Positive and negative cycle-by-cycle OCP, short-circuit protection and overtemperature protection (OTP) ensure robust design. Input undervoltage and overvoltage lockout shut down the regulator to prevent damage when the input voltage is out of specification. Regulation is halted in case of an output overvoltage (OVP) event. A status pin indicates that the output voltage is within range and the output voltage is in regulation. The device has an analog output that can be configured to report output current or junction temperature with  $\pm 5\%$  and  $\pm 8^\circ\text{C}$  accuracy, respectively.

The devices are available in a 27-bump (2.2mm x 3.8mm) WLCSP package that provides low thermal resistance and minimizes the PCB area.

### Applications

- Servers/ $\mu$ Servers
- I/O and Chipset Supplies
- GPU Core Supply
- DDR Memory:  $V_{DDQ}$ ,  $V_{PP}$  and  $V_{TT}$
- Point-of-Load (PoL) Applications

DEVICE TYPE	CURRENT RATING	INPUT VOLTAGE	OUTPUT VOLTAGE
MAX16425	25A	4.5V to 16V	0.6V to 3.3V
MAX16425A			

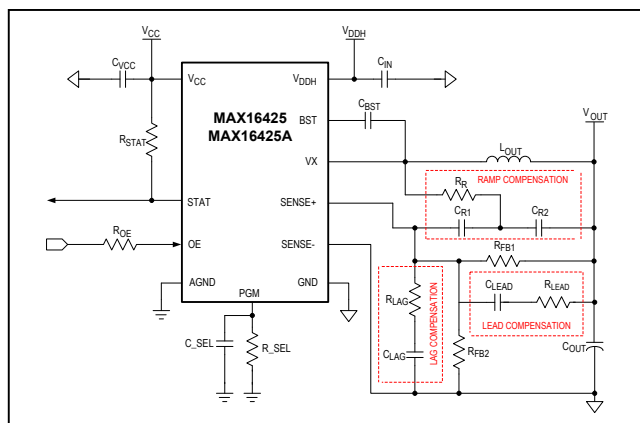
Quick-PWM is a trademark of Maxim Integrated Products, Inc.

### Benefits and Features

- High-Efficiency Solution
  - Up to 97% Peak
  - Up to 87% Full-Load
  - Up to 96% Light-Load Efficiency at 1A with DCM Enabled
- Flexible Design Allows Early PCB Definition
  - Footprint Compatible with VT2491 (15A) and Related Scalable Products
  - Programmable Switching Frequency Up to 1MHz
  - Programmable Soft-Start and STAT Delay Timings
  - Programmable Reference Voltage with External Input Option
  - Programmable Positive and Negative OCP Limit
- Advanced Architecture, Protection and Reporting Guarantees Reliable Designs
  - Analog Current or Temperature Reporting
  - Differential Remote Sense with Open-Circuit Detection
  - Fast Transient Response with Quick-PWM™ Architecture
  - Percentage-Based Output Power Good and OVP
  - Open-Drain Status Indicator (STAT) Pin
  - Input Undervoltage and Overvoltage Lockout
  - Adaptive Dead Time Control
- Saves Board Space
  - Integrated Boost Switch
  - 27-Bump WLCSP (2.2mm x 3.8mm) Footprint
  - Operation Using Ceramic Input and Output Capacitors

[Ordering Information](#) appears at end of data sheet.

### Basic Application Circuit



## Absolute Maximum Rating

VDDH to GND (Note 1).....	-0.3V to +23V	VCC to AGND.....	-0.3V to +2.5V
VX to GND (DC).....	-0.3V to +23V	OE to GND.....	-0.3V to +2.5V
VX to GND (AC) (Notes 1, 2).....	-10V to +23V	PGM, SENSE+, SENSE- to GND.....	-0.3V to VCC +0.3V
VDDH to VX (DC).....	-0.3V to +23V	STAT to AGND.....	-0.3V to +4V
VDDH to VX (AC) (Notes 1, 2).....	-10V to +23V	Junction Temperature (T <sub>J</sub> ).....	+150°C
BST to GND (DC).....	-0.3V to +25.5V	Storage Temperature Range.....	-65°C to +150°C
BST to GND (AC) (Notes 1, 2).....	-7V to +25.5V	Peak Reflow Temperature Lead-Free.....	+260°C
BST to VX Differential.....	-0.3V to +2.5V		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Operating Ratings

Input Voltage (V <sub>DDH</sub> ).....	4.5V to 16V	Junction Temperature (T <sub>J</sub> ).....	0°C to 125°C
Bias-Supply Voltage (V <sub>CC</sub> ).....	1.71V to 1.89V	Peak Output Current (I <sub>PK+,MAX</sub> ).....	40A
Output Current (I <sub>OUT</sub> ).....	25A		

## Package Information

27 WLCSP	
Package Code	C272C3+1
Outline Number	<a href="#">21-0928</a>
Land Pattern Number	Refer to <a href="#">Application Note 1891</a>
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ <sub>JA</sub> )	19°C/W (Note 3)
Junction to Case (θ <sub>JC</sub> )	0.75°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

**Note 1:** Input HF capacitors placed not more than 60 mils away from the V<sub>DDH</sub> pin are required to keep inductive voltage spikes within Absolute Maximum Ratings limits.

**Note 2:** AC is limited to 25ns.

**Note 3:** Data taken using Analog Devices' evaluation kit with no air flow and no heatsink.

## Electrical Characteristics

( $V_{CC} = 1.8V \pm 5\%$ ,  $V_{DDH} = 12V$  unless otherwise specified. The \* symbol denotes specifications that apply over the temperature range of  $T_J = 0^\circ C$  to  $125^\circ C$ . Otherwise, specifications are for  $T_J = 32^\circ C$ . The # denotes parameters that are programmable. Limits are 100% tested at  $T_A = +32^\circ C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGES, SUPPLY CURRENT, TEMPERATURE RANGE						
12V Supply Voltage Range	V <sub>DDH</sub>	*	4.5		16	V
1.8V Supply Voltage Range	V <sub>CC</sub>	*	1.71	1.8	1.89	V
V <sub>CC</sub> Supply Current	I <sub>CC</sub>	CCM *			35	mA
		DCM *			25	
		Shutdown *		32	132	μA
V <sub>REF</sub>						
Programmable Reference Voltage	V <sub>REF</sub>	# (See Table 3)	0.6			V
0.95						
V <sub>REF</sub> Tolerance (V <sub>REF_TOL</sub> )			T = 35°C (Note 4)	-0.5		+0.5
V <sub>REF</sub> Tolerance Temperature Coefficient (V <sub>REF_T_COEFF</sub> )		0°C < T <sub>J</sub> < 100°C (Note 4)			0.0106	%/°C
FEEDBACK LOOP						
R <sub>SENSE</sub> GAIN	Gain	# (See Table 3)	1.4			mV/A
			2.8			
			5.4			
SWITCHING FREQUENCY						
Switching Frequency Accuracy	f <sub>SW</sub>	Relative to the nominal value (see Figure 4). 0A < I <sub>LOAD</sub> < Full Load V <sub>CC</sub> , V <sub>DDH</sub> ±10% *	-20		+20	%
Low f <sub>SW</sub> Threshold		DCM enabled		30		kHz
Forced Minimum f <sub>SW</sub>		DCM enabled. The low f <sub>SW</sub> threshold has been crossed.		60		kHz
INPUT PROTECTION						
Rising V <sub>DDH</sub> UVLO Threshold	V <sub>DDH</sub> UVLO	*	3.85	4.15	4.40	V
Falling V <sub>DDH</sub> UVLO Threshold			3.70	3.98	4.25	V
Rising V <sub>DDH</sub> OVLO Threshold	V <sub>DDH</sub> OVLO	*	16.6	17.3	17.8	V
Falling V <sub>DDH</sub> OVLO Threshold			16.1	16.7	17.3	V
Rising V <sub>CC</sub> UVLO Threshold	V <sub>CC</sub> UVLO	*	1.49	1.62	1.70	V
Falling V <sub>CC</sub> UVLO Threshold			1.46	1.57	1.65	V
Rising V <sub>BST</sub> UVLO Threshold	V <sub>BST</sub> UVLO	*	1.48	1.57	1.70	V
Falling V <sub>BST</sub> UVLO Threshold			1.33	1.52	1.65	V

**Electrical Characteristics (continued)**

( $V_{CC} = 1.8V \pm 5\%$ ,  $V_{DDH} = 12V$  unless otherwise specified. The \* symbol denotes specifications that apply over the temperature range of  $T_J = 0^\circ C$  to  $125^\circ C$ . Otherwise, specifications are for  $T_J = 32^\circ C$ . The # denotes parameters that are programmable. Limits are 100% tested at  $T_A = +32^\circ C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE PROTECTION (OVP)						
Overvoltage-Protection Rising Threshold	OVP	(Note 5)	9.5	13	16.5	%
Overvoltage-Protection Deglitch Filter Time			25	30	36	μs
Power Good Protection Falling Threshold	PWRGD	(Note 5)	-12	-9	-4.5	%
Power Good Protection Rising Threshold		(Note 5)	-9	-6	-2	%
Power Good Deglitch Filter Time			25	30	36	μs
OVERCURRENT PROTECTION (OCP)						
Positive Overcurrent-Protection Threshold (POCP)	OCP	Valley current #	16			A
			20			
			24			
-16			A			
-20						
-24						
POCP Threshold Tolerance		Referenced to nominal value (Note 5) *	-20		20	%
Hysteresis (Note 6)		Referenced to inception value (Note 5)*	12	15	18	%
OVERTEMPERATURE PROTECTION (OTP)						
Overtemperature-Protection Inception Threshold	OTP	*	130	140	150	°C
Hysteresis			-30		-10	°C
TEMPERATURE REPORTING						
Temperature-Reporting Range	T <sub>J</sub>		0		125	°C
Temperature-Reporting Tolerance		*	-4		+4	°C
CURRENT REPORTING						
Current-Reporting Range	I <sub>LOAD</sub>		0		25	A
Current-Reporting Tolerance		From no load to full load *	-2		+2	A
		Full load *	-8		+8	%

## Electrical Characteristics (continued)

( $V_{CC} = 1.8V \pm 5\%$ ,  $V_{DDH} = 12V$  unless otherwise specified. The \* symbol denotes specifications that apply over the temperature range of  $T_J = 0^\circ C$  to  $125^\circ C$ . Otherwise, specifications are for  $T_J = 32^\circ C$ . The # denotes parameters that are programmable. Limits are 100% tested at  $T_A = +32^\circ C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OE PIN						
Input Range	—	*	0		1.89	V
Rising Threshold	V <sub>OE(H)</sub>	Full V <sub>CC</sub> supply range. Measured at OE Pin *	0.89	1.09	1.3	V
Falling Threshold	V <sub>OE(L)</sub>		0.44	0.65	0.83	V
Hysteresis	—	*	0.34	0.44	0.61	V
Deglintch Filter Time			230		520	ns
OE Pin Input Resistance		UVLO < V <sub>CC</sub> < OVLO *	250	435	490	kΩ
STARTUP TIMING						
Enable Time from OE Rise to Start of Regulation	t <sub>EN</sub>		200	300	500	μs
Soft-Start Ramp Time	t <sub>SS</sub>	# (see Table 3)	1.5			ms
			3			
			6			
Dwell Time at V <sub>OUT</sub> (DCM Not Allowed)	t <sub>SETTLE</sub>		14		35	μs
Timing to Charge Boost Capacitor	t <sub>BST</sub>		8			μs
STAT PIN						
Pullup Voltage	VOH <sub>STAT</sub>		3.6			V
Status Output Low	VOL <sub>STAT</sub>	I <sub>STAT</sub> = 4mA *	0.4			V
		I <sub>STAT</sub> = 0.2mA, 0V < V <sub>CC</sub> < UVLO and 0V < V <sub>DDH</sub> < UVLO *	0.67			
		I <sub>STAT</sub> = 1.3mA, 0V < V <sub>CC</sub> < UVLO and 0V < V <sub>DDH</sub> < UVLO *	0.76			
Status Output High Leakage Current	I <sub>STAT</sub>	STAT pull to 3.3V through 20kΩ *	7			μA
Time from V <sub>OUT</sub> Ramp Completion to STAT Pin Released	t <sub>STAT</sub>	STAT output low to high # (See Table 3)	128			μs
			2000			
Fault Clearing		Bad-to-good delay	1.8	2	2.2	ms

**Electrical Characteristics (continued)**

( $V_{CC} = 1.8V \pm 5\%$ ,  $V_{DDH} = 12V$  unless otherwise specified. The \* symbol denotes specifications that apply over the temperature range of  $T_J = 0^\circ C$  to  $125^\circ C$ . Otherwise, specifications are for  $T_J = 32^\circ C$ . The # denotes parameters that are programmable. Limits are 100% tested at  $T_A = +32^\circ C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PGM PIN						
Reporting Voltage Range	V <sub>PGM</sub>	System regulating	0.5		1	V
Resistor Range	R_SEL	Twelve options	1.78		162	kΩ
Resistor Accuracy		EIA standard resistor values only	-1		+1	%
Capacitor Range	C_SEL	Three options	0		820	pF
C_SEL Capacitor Accuracy			-20		+20	%
External Capacitance		Load and stray capacitance in addition to C_SEL			20	pF
SYSTEM SPECIFICATIONS (Note 6)						
Peak-to-Peak Output Ripple Voltage, DCM Disabled	V <sub>OUT-RIPL</sub>		-1		+1	%
Peak-to-Peak Input Ripple Voltage	V <sub>IN-RIPL</sub>	V <sub>DDH</sub> = 10.8V - 13.2V	-1		+1	%
Line Regulation	V <sub>OUT</sub>	V <sub>DDH</sub> = 10.8V - 13.2V			0.15	%
Load Regulation (Static)		I <sub>OUT</sub> = 0A - I <sub>MAX</sub>	-0.5		+0.5	%
Load Regulation (Dynamic)		V <sub>DDH</sub> = 10.8V - 13.2V, I <sub>OUT</sub> step 6A at 36A/μs, 1kHz - 1MHz repetition rate, 10% - 90% duty cycle	-3		+3	%

**Note 4:** To calculate the total  $V_{REF}$  tolerance over a temperature variation of  $\Delta T$ :

$$V_{REF\_TOL\_TOT} = V_{REF\_TOL} + |\Delta T| \times V_{REF\_T\_COEFF}$$

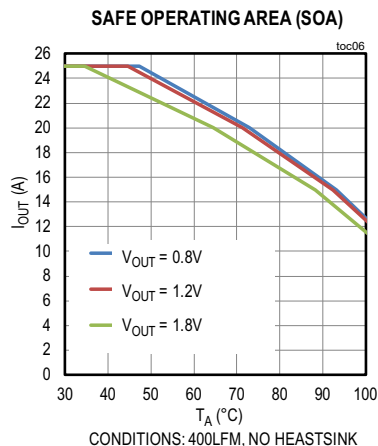
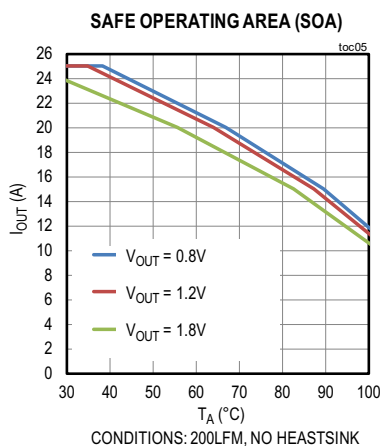
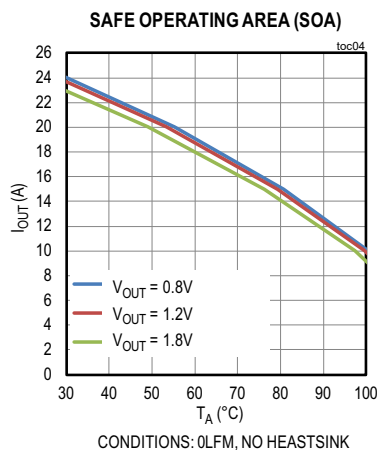
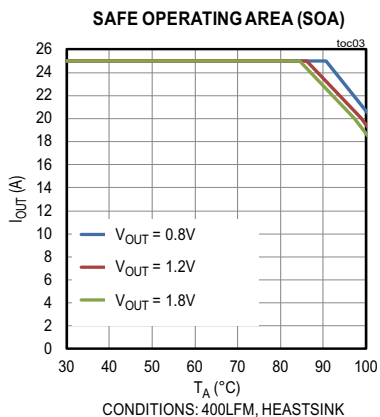
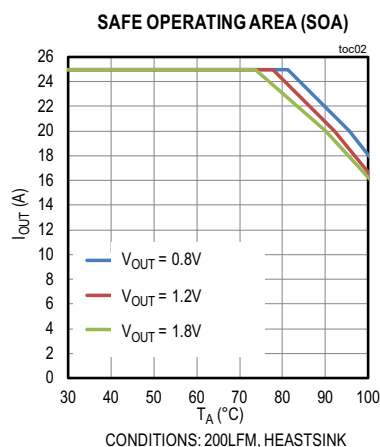
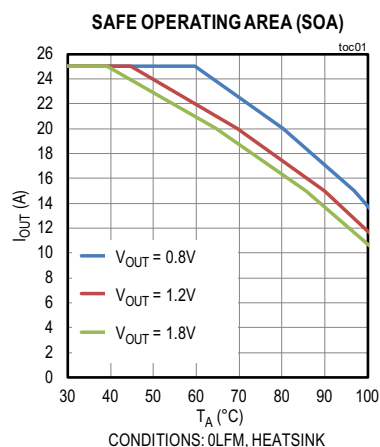
**Note 5:** Min/max limits are  $\geq 4\sigma$  about the mean.

**Note 6:** The OCP hysteresis is for positive current OCP only, negative current OCP hysteresis is always 0.

**Note 7:** Tested using circuit of Reference Schematic (Figure 9) with  $C_{OUT} = 15 \times 22\mu F$ .  $V_{OUT} = 1.05V$ . Not guaranteed; for reference only.

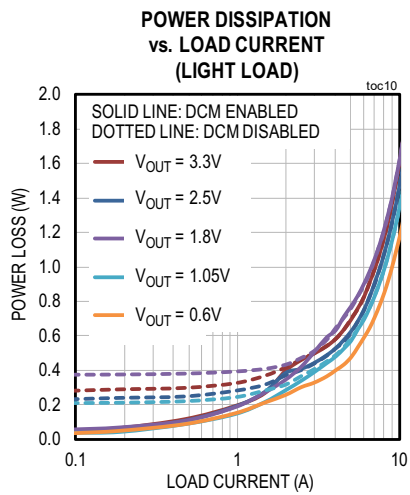
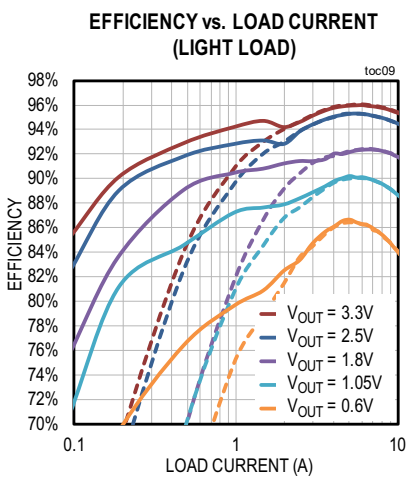
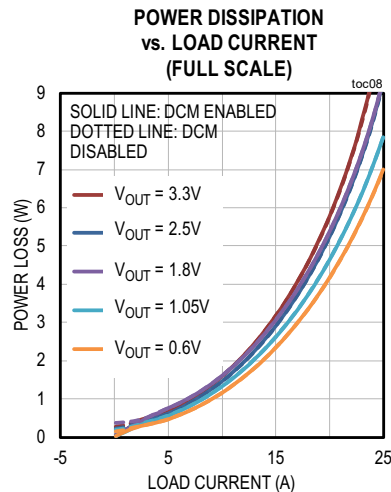
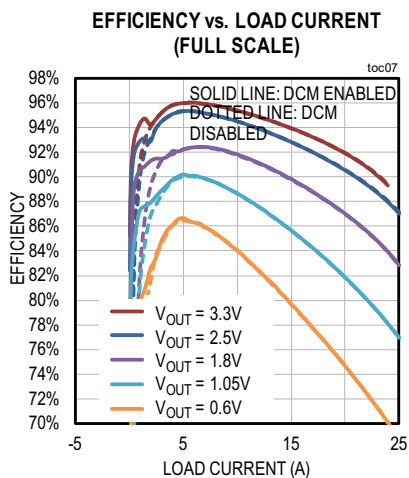
## Typical Operating Characteristics

( $V_{DDH} = 12V$ ,  $V_{CC} = 1.8V$ . Curve indicates  $T_{CASE} = 125^{\circ}C$  or  $I_{OUT} = I_{MAX}$ , whichever happens first.)



### Typical Operating Characteristics (continued)

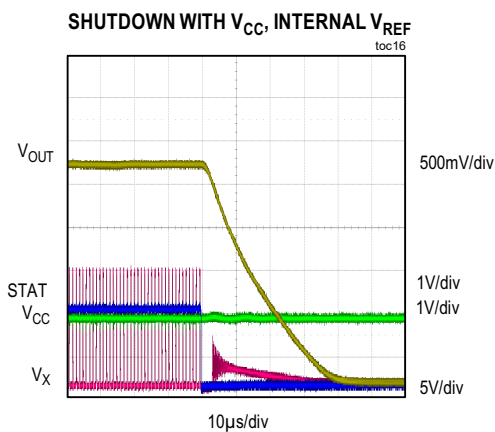
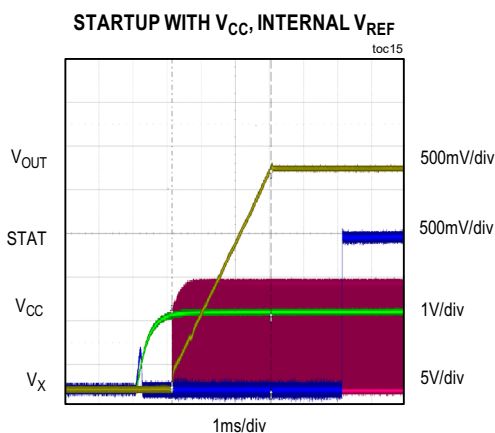
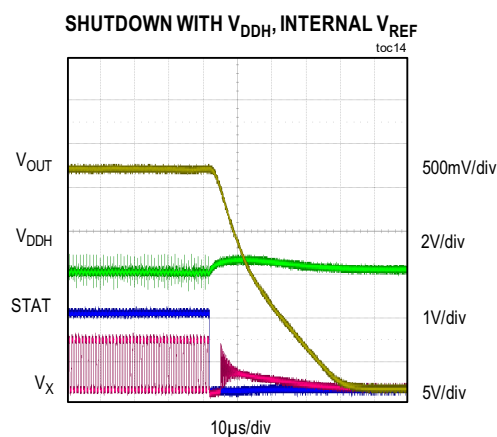
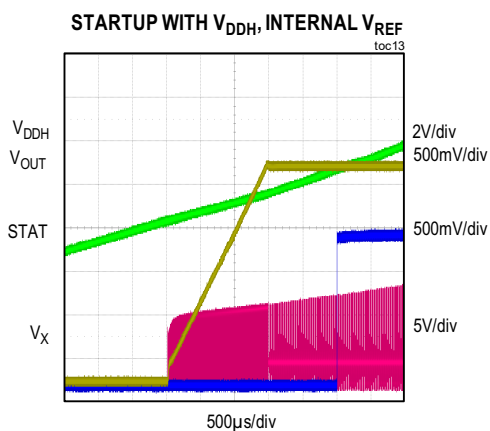
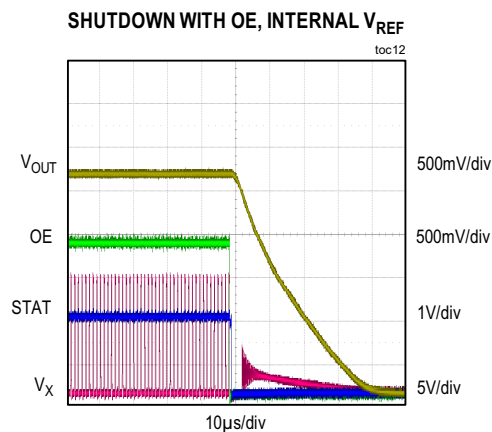
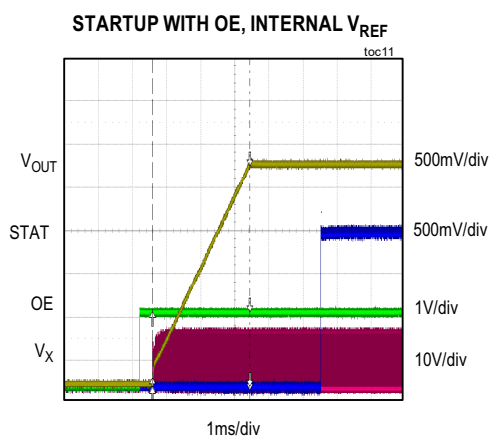
( $V_{DDH} = 12V$ ,  $V_{CC} = 1.8V$ ,  $f_{sw}$  Setting #6,  $C_{OUT} = 5 \times 22\mu F + 4 \times 47\mu F$ ,  $L_{OUT} = 680nH$  for  $V_{OUT} \geq 2.5V$ ,  $L_{OUT} = 200nH$  for  $V_{OUT} \leq 1.8V$ )





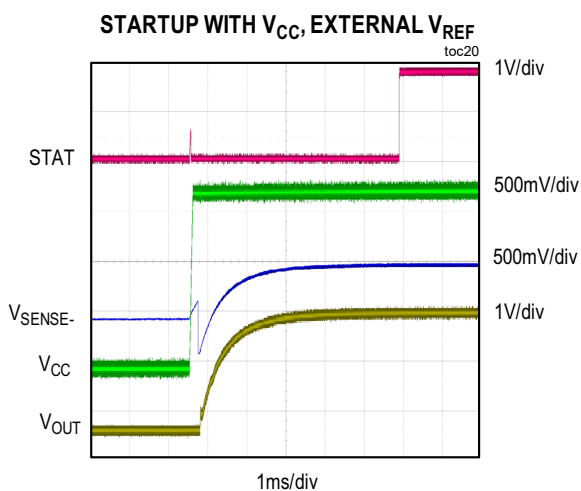
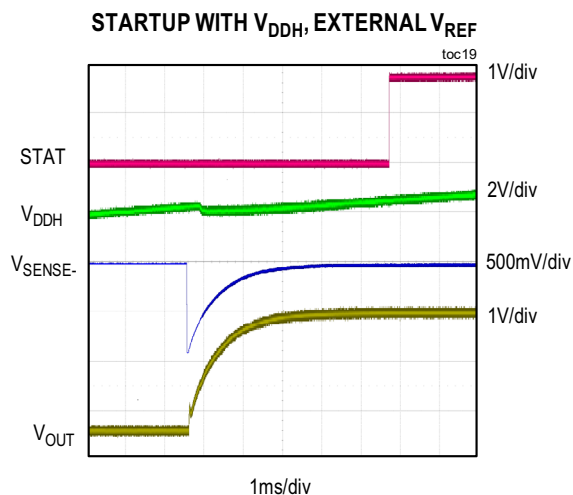
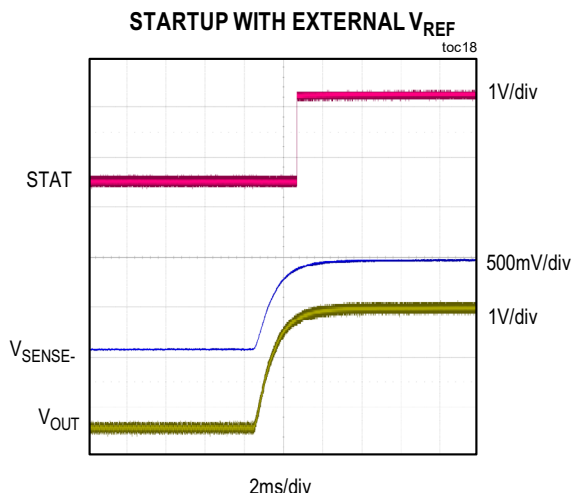
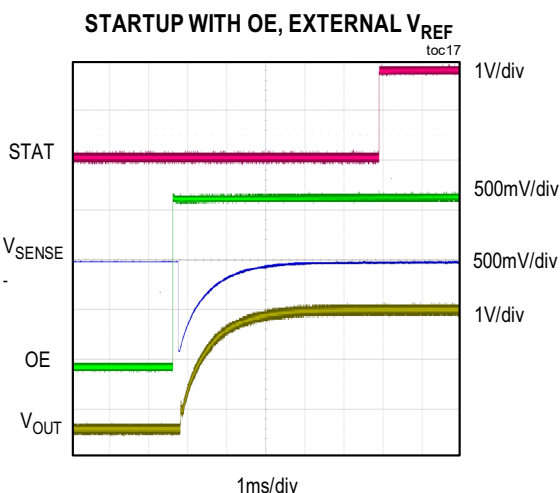
### Typical Operating Characteristics (continued)

( $V_{DDH} = 12V$ ,  $V_{CC} = 1.8V$ ,  $V_{OUT} = 2.5V$ , Circuit of [Figure 3](#),  $R_{SEL} = 6.04k\Omega$ ,  $R_{FB1} = 4.32k\Omega$ ,  $R_{FB2} = 2.61k\Omega$ , No heatsink,  $I_{LOAD} = 15A$ , unless otherwise noted.)



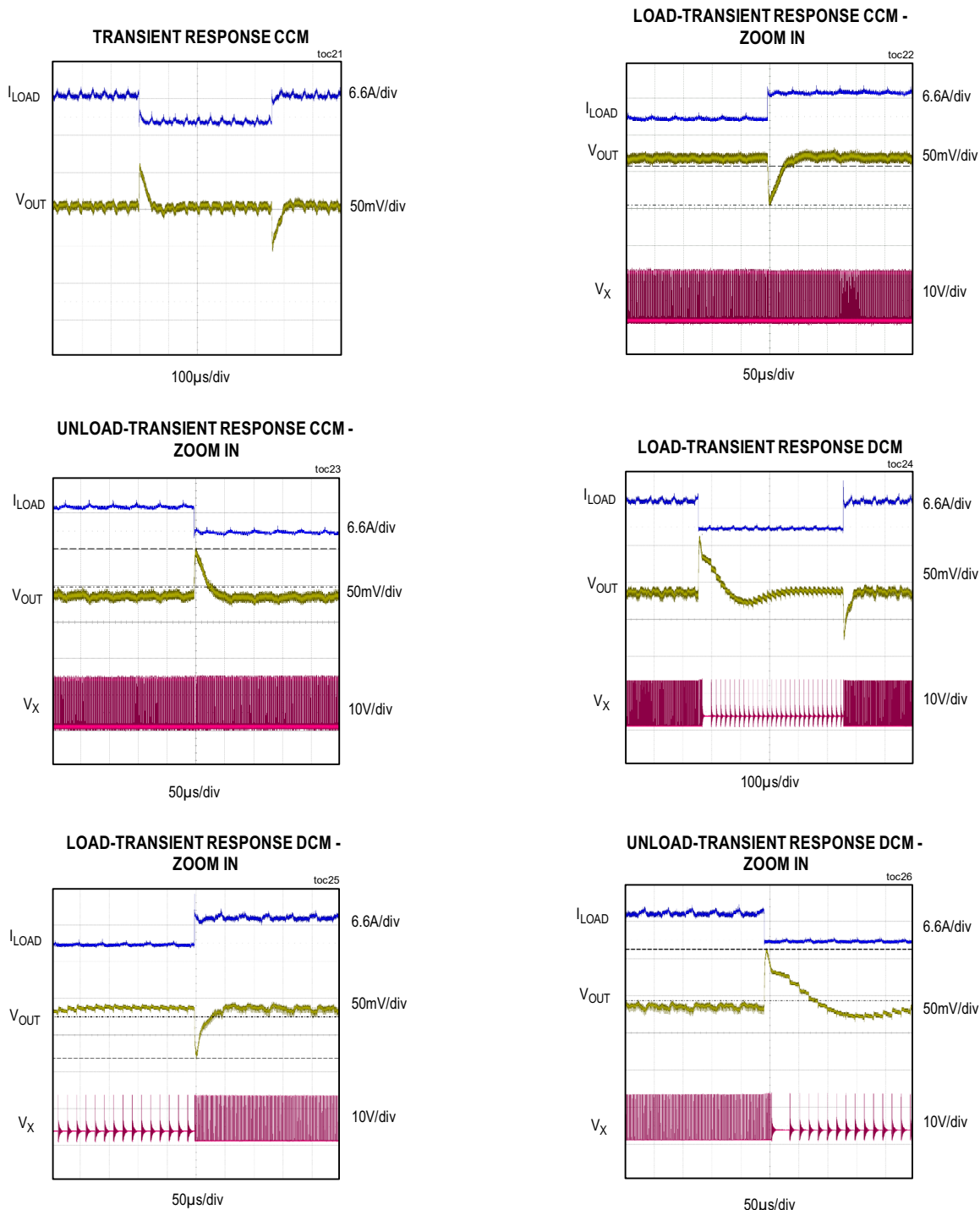
### Typical Operating Characteristics (continued)

( $V_{DDH} = 12V$ ,  $V_{CC} = 1.8V$ ,  $V_{OUT} = 2.5V$ , Circuit of [Figure 6](#),  $R_{SEL} = 9.09k\Omega$ ,  $R_{FB1} = 4.32k\Omega$ ,  $R_{FB2} = 2.61k\Omega$ , External  $V_{REF} = 0.95V$ . No heatsink, unless otherwise noted.)



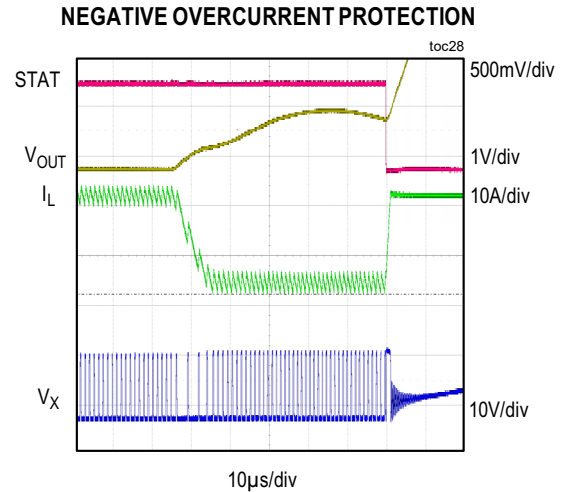
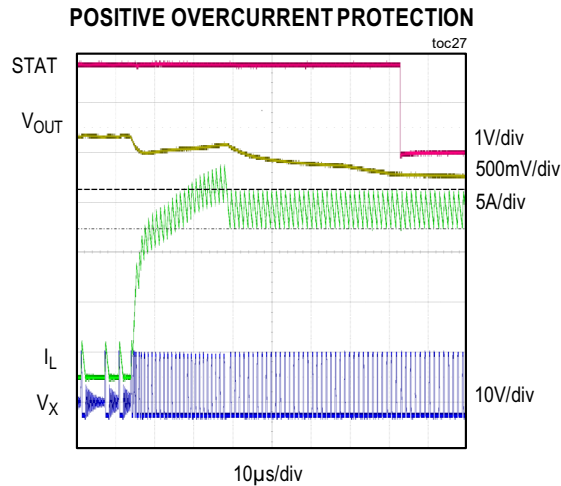
### Typical Operating Characteristics (continued)

( $V_{DDH} = 12V$ ,  $V_{CC} = 1.8V$ ,  $V_{OUT} = 2.5V$ , Circuit of [Figure 3](#),  $C_{OUT} = 5 \times 22\mu F + 4 \times 47\mu F$ ,  $L = 680nH$ ,  $f_{SW}$  Setting #6, Load Step = 6A at 36A/ $\mu s$ .)

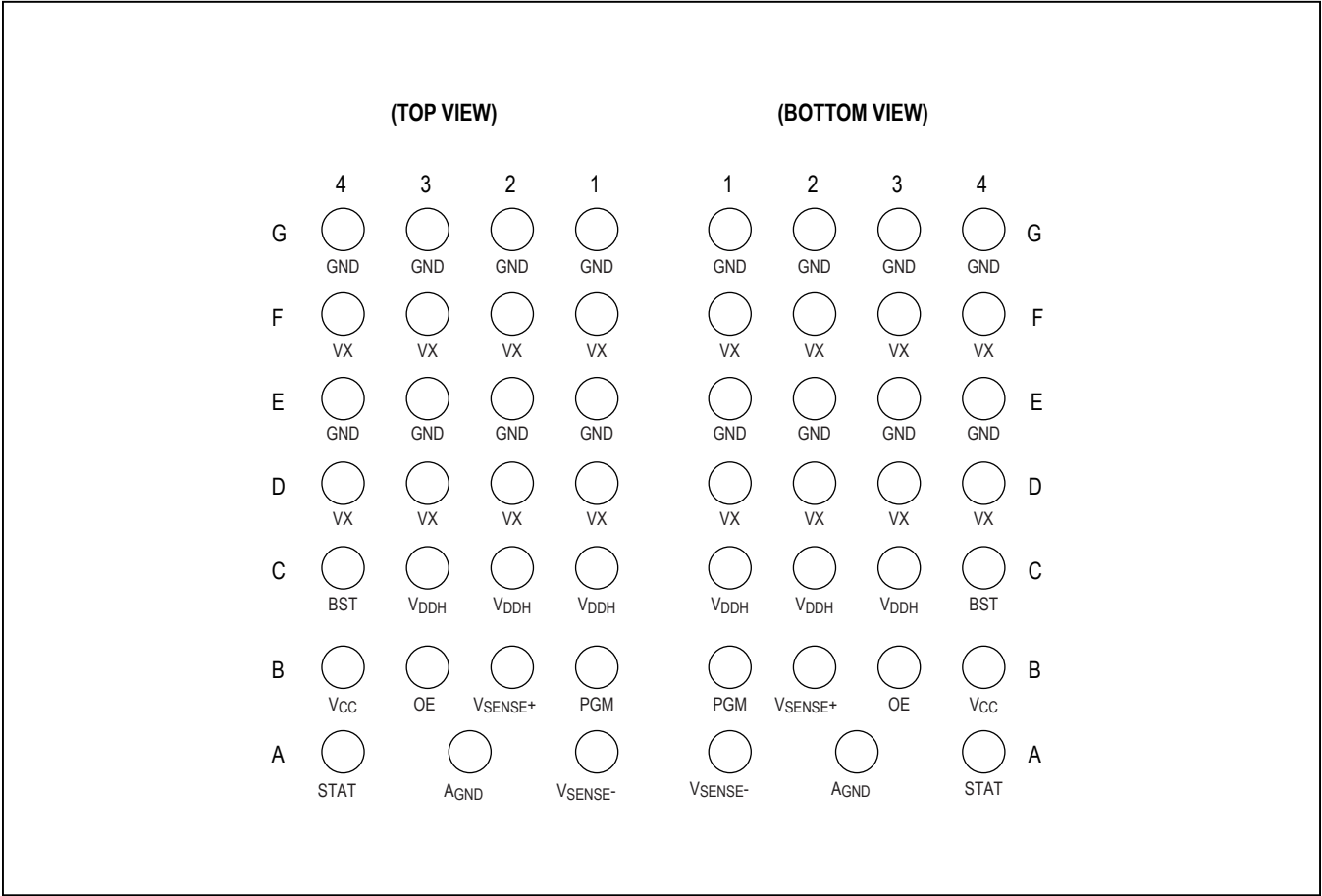


**Typical Operating Characteristics (continued)**

( $V_{DDH} = 12V$ ,  $V_{CC} = 1.8V$ ,  $V_{OUT} = 2.5V$ , Circuit of [Figure 3](#),  $C_{OUT} = 5 \times 22\mu F + 4 \times 47\mu F$ ,  $L = 680nH$ ,  $f_{SW}$  Setting #6, OCP = 16A.  
No heatsink, unless otherwise noted.)



Pin Configuration



## Pin Description

PIN	NAME	FUNCTION
A1	SENSE-	Negative Remote-Sense/External-Reference Input. Connect the SENSE- pin to ground at the load with a Kelvin connection to use the internal voltage reference, or connect the pin to an external reference voltage as shown in Figure 6.
A2	AGND	Analog/Signal Ground. Connect to ground plane following the recommendations mentioned in the <i>Printed Circuit Board Layout</i> section.
A4	STAT	Open-Drain Status Output. This pin is pulled low to indicate a fault or output-undervoltage and output-overvoltage events.
B1	PGM	Programming Input/Telemetry Output. Connect PGM to analog ground using a programming resistor and capacitor. The resistance and capacitance values are measured at startup to determine the desired regulator settings (see Table 3a and 3b). Refer to the <i>Current/Temperature Reporting and Programming Options</i> sections for more information.
B2	SENSE+	Positive Remote-Sense Input. Connect SENSE+ to V <sub>OUT</sub> at the load using a Kelvin connection. A resistive voltage-divider can be inserted between the output and SENSE+ to regulate the output above the reference voltage.
B3	OE	Output-Enable Input. Connect to enable signal through a 20k $\Omega$ resistor. When OE is low, the VX node is high-impedance. Toggle OE to clear the fault-protection latch.
B4	V <sub>CC</sub>	Supply-Voltage Input. Use this pin for the regulator's analog, digital and gate drive circuits. Connect V <sub>CC</sub> to 1.8V and closely bypass the pin to power ground with a 1 $\mu$ F or greater ceramic capacitor.
C1–C3	V <sub>DDH</sub>	Power-Input Voltage. Connect V <sub>DDH</sub> to the input power supply source. High-frequency ceramic decoupling capacitors must be placed in close proximity to the pin. Refer to Table 4 for decoupling recommendations.
C4	BST	Bootstrap Supply Input. Connect a 0.47 $\mu$ F ceramic capacitor in close proximity to the IC between BST and VX, as specified in Table 4 and the <i>Printed Circuit Board Layout</i> section.
D1–D4, F1–F4	VX	Switching Node. Connect to the switching node of the power inductor.
E1–E4, G1–G4	GND	Power Ground. Connect to the return path of the output load.



The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage (Equation 1). Another one-shot sets a minimum off-time of 100ns (typ).

Under normal operating conditions, the on-time one-shot is triggered if the sum of the feedback voltage and the valley current-sense signal falls below the control voltage, and the minimum off-time one-shot has timed out. The  $t_{ON}$  pulse width is clamped to a maximum of 2.5µs.

#### Equation 1

$$t_{ON} = \frac{V_{X_{AVE}}}{f_{SW} \times V_{DDH}}$$

where:

- $f_{SW}$  = Switching frequency (MHz)
- $t_{ON}$  = On-time period for high-side switch (µs)
- $V_{X_{AVE}}$  = Average VX voltage (V)
- $V_{DDH}$  = Input voltage (V)

### Voltage Regulator Enable and Turn-On Sequencing

The startup sequence is shown in [Figure 1](#). Once the OE pin rises above the  $V_{OE(H)}$  threshold, the control circuits wait for a 300µs  $t_{EN}$  time to allow the bias circuits, analog blocks, and other circuits to settle to their proper states before beginning the regulation.

The OE pin has a voltage rating of 1.8V. For control signal voltages higher than 1.8V, a resistor-divider network must be used to drive the OE pin.

In addition, the impedance of the OE pin is reduced when the  $V_{CC}$  is below UVLO. To prevent any damage to the part due to lowering the impedance, a resistor is used to limit the current. For 1.8V control signals, this resistor has a value of 20kΩ and it is placed in series with the OE pin. For higher drive voltages to OE that require a resistive voltage-divider, choose 20kΩ for the bottom resistor to ground. The top resistor is given by Equation 2. Use closest higher resistor value available.

#### Equation 2

$$R_{TOP} = 20k\Omega \times \left[ \left( \frac{V_{SIG}}{1.8V} \right) - 1 \right]$$

Output enable delay timing can be added using an RC network connected between control signal and OE pin. R-C delay networks are designed based on desired turn on/off timings and the  $V_{OE(H)}/V_{OE(L)}$  thresholds.

The OE pin has nominal input impedance, which should be included in calculations for the divider network (see the [Electrical Characteristics](#) table for nominal impedance).

When the system pulls OE low, the MAX16425/MAX16425A enter low-power shutdown mode. STAT is pulled low immediately. The MAX16425/MAX16425A discharge the inductor by keeping the low-side FET enabled until the current reaches zero. Under these conditions, both power FETs are in high-impedance and the regulator enters shutdown.

### Soft-Start Control

Once the OE reaches its threshold and the  $t_{EN}$  has elapsed, the regulator performs the bootstrap capacitor charging sequence. After bootstrap capacitor is fully charged, the internal reference voltage starts ramping to the target voltage with the appropriate soft-start time ( $t_{SS}$ ). Both soft-start timing, and target voltage can be programmed (see the [Programming Options](#) section, and [Table 3a](#) and [3b](#)).

If the regulator is enabled with a prebiased output voltage, the system does not regulate until the reference voltage ramps above the SENSE+ node voltage. Upon reaching the SENSE+ voltage, the regulator performs the  $C_{BST}$  charging sequence and starts normal operation. If, at the end of  $t_{SS}$ , the SENSE+ pin voltage is still higher than the internal reference, continuous conduction mode (CCM) operation is forced for a short period of time ( $t_{SETTLE}$ ) to discharge the output to the desired voltage. After this period, discontinuous conduction mode (DCM) is allowed, if selected, and the OVP/UVLP circuitry becomes active.



## Remote Output Voltage Sensing

Remote output-voltage sensing is implemented to improve output-voltage regulation accuracy at the load. This technique reduces errors due to voltage drops in the plane impedance between the load and the MAX16425/MAX16425A, particularly in cases where the load is placed away from the MAX16425/MAX16425A. Remote output-voltage sensing is implemented by using the SENSE- node as a reference for the internal voltage reference  $V_{REF}$ .

## Switching Operation Modes

The MAX16425/MAX16425A support both CCM and DCM. The mode of operation can be programmed as indicated in the [Programming Options](#) section, and [Table 3a](#) and [3b](#).

If DCM is enabled, MAX16425/MAX16425A transition seamlessly to DCM at light loads to improve efficiency. Once in DCM, the switching frequency decreases as load decreases until a minimum frequency of 30kHz is reached. The purpose of this minimum switching frequency limitation is to prevent operation in the audible frequency range to reduce audible noise.

If the load is such that no  $t_{ON}$  pulse is generated for  $\sim 33\mu s$  ( $1/30kHz$ ) since the last pulse was issued, the low-side FET is turned ON until the error comparator commutates, and a  $t_{ON}$  pulse is issued. Once this minimum frequency mode is entered, the IC operates with a minimum switching frequency of 60kHz, to provide proper hysteresis and prevent the IC from moving in and out of this mode.

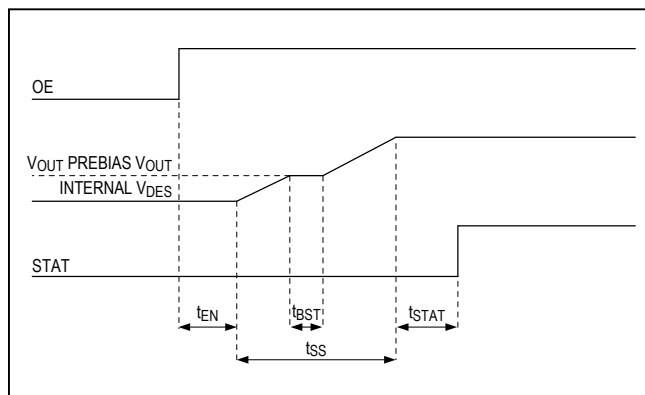


Figure 1. Startup Timing

## Protection And Status Features

### Output Voltage Protection (OVP)

The SENSE+ pin is continuously monitored for both undervoltage and overvoltage conditions. If the output voltage falls below the PWRGD threshold (9% of programmed output voltage) for more than 30 $\mu s$  (typ), the STAT pin is driven low while the MAX16425/MAX16425A continue to operate, attempting to maintain regulation. If the output voltage rises above the overvoltage protection threshold (13% of programmed output voltage) for more than 30 $\mu s$  (typ), the STAT pin is driven low and the MAX16425/MAX16425A latch off (high-side and low-side FETs turn off). Toggle OE or cycling  $V_{CC}$  supply is required to reset fault conditions.

### Current Limiting

The MAX16425/MAX16425A have a current limit that can be programmed using the appropriate R\_SEL value (see [Table 3a](#) and [3b](#)). The overcurrent protection (OCP) monitors and limits the low-side FET current on a cycle-by-cycle basis. If the minimum instantaneous “valley” low-side switch current level exceeds the OCP (source) level, the IC delays the next on-time pulse until the current falls below the threshold level ([Figure 2](#)). Since the regulator responds to the inductor valley current, the DC current delivered during positive (source) current limit is the programmed valley current ( $I_{OCP}$  - hysteresis) plus half of the inductor ripple. During the current limit event (source), the output voltage drops and if the voltage reaches the PWRGD threshold, the STAT pin is driven low.

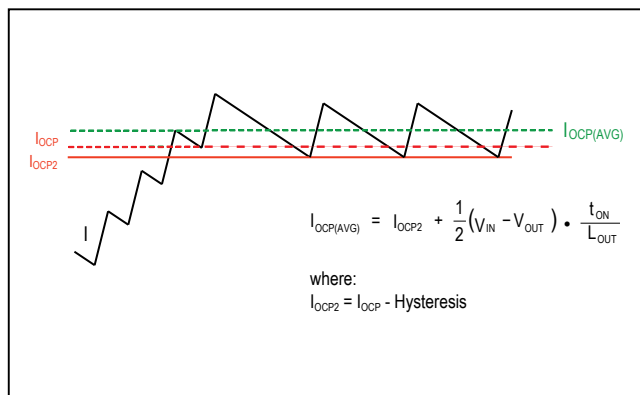


Figure 2. Inductor Current During Current Limit Event

The MAX16425/MAX16425A also have negative OCP limits (Sink). When this threshold is reached, the IC issues an on-time pulse to limit the negative current. This on-time pulse is issued regardless of the error comparator state. Therefore, it is possible to cause an overvoltage protection (OVP) event if the negative load exceeds the negative current limit.

### UVLO and OVLO Protection

The regulator monitors  $V_{DDH}$  with both undervoltage lockout (UVLO) and overvoltage lockout (OVLO) circuits. UVLO protection is also present on BST and  $V_{CC}$  supplies. When any of the supply voltages is below the UVLO threshold or  $V_{DDH}$  is above the OVLO threshold, the regulator stops switching, and the STAT pin is driven low (refer to the [Electrical Characteristics](#) table for UVLO and OVLO levels).

### Overtemperature Protection (OTP)

If the die temperature exceeds the overtemperature threshold during operation, the MAX16425/MAX16425A stop regulation and the STAT pin is driven low. Regulation starts again once the die temperature falls below the new overtemperature threshold (overtemperature threshold - hysteresis) value. The STAT pin eventually goes high again once the output voltage reaches the expected value.

### Regulator Status

The regulator status (STAT) signal provides an open-drain output (4V max, refer to the [Absolute Maximum Rating](#) section) that indicates whether the MAX16425/MAX16425A are functioning properly. An external pullup resistor is required.

After the startup ramp is completed ( $t_{STAT}$ ), if the output voltage is within the PWRGD/OVP regulation window, the STAT pin goes high impedance. The STAT pin is driven low when one or more of the following conditions exist:

- OE is low
- $V_{DDH}$  or  $V_{CC}$  are not present or below/above the respective UVLO/OVLO thresholds.
- A PWRGD fault is present (see the [Output Voltage Protection \(OVP\)](#) section).
- The SENSE- or SENSE+ pin is left unconnected at startup.
- The die temperature is above the maximum allowed temperature.
- The OVP circuit has detected that the output voltage is above the tolerance limit.
- UVLO is detected on bootstrap supply (BST-VX), indicating possible short or open bootstrap capacitor.

### Current/Temperature Reporting

During regulation, an analog voltage is produced on the PGM pin that represents either average output current or chip temperature (see [Table 3a](#) and [3b](#) for proper settings). The PGM pin has an output-voltage range of 0.5V to 1V. The PGM output is designed to drive the R\_SEL/C\_SEL network with an additional 20pF external load (including parasitics), which allows this node to be connected to external circuitry, such as a voltage buffer or ADC.

The conversion equations for temperature and current reporting are shown in Equation 3 and Equation 4.

#### Equation 3

$$T_{REPORTED} = (V_{PGM} - T_{OFFSET}) \times T_{SLOPE}$$

$$T_{OFFSET} = 0.592V$$

$$T_{SLOPE} = 611 \frac{^{\circ}C}{V}$$

#### Equation 4

$$I_{REPORTED} = (V_{PGM} - I_{OFFSET}) \times I_{SLOPE}$$

$$I_{OFFSET} = 0.495V$$

$$I_{SLOPE} = 86.2 \frac{A}{V}$$

**Table 1. Summary of Fault Actions**

FAULT TYPE	REGULATOR RESPONSE	STAT	DESCRIPTION
Power Good (PWRGD)	Continue Operation	LOW	$V_{OUT} < (1 - 9\%) V_{OUTNOM}$
Overvoltage Protection (OVP)	Shutdown and Latchoff	LOW	$V_{OUT} > (1 + 13\%) V_{OUTNOM}$
Overtemperature Protection (OTP)	Shutdown	LOW	$T_J > 140^{\circ}C$
Overcurrent Protection (OCP)	Clamping	$V_{OUT}$ Drop, LOW	Valley current higher than selected limit
Boost Undervoltage	Shutdown	LOW	$(BST - VX) < 1.52V$
$V_{DDH}$ Supply	Shutdown	LOW	$V_{DDH} < 4.5V$ or $V_{DDH} > 16V$
$V_{CC}$ Supply	Shutdown	LOW	$V_{CC} < 1.57V$
SENSE-/SENSE+ Disconnected	Do Not Start	LOW	Open Sense Lines

## Reference Design

The typical application circuit is shown in [Figure 3](#).

## Programming Options

The MAX16425/MAX16425A allow programming of several key parameters to allow optimization for specific applications. The parameters that are programmable are shown in [Table 2](#). A resistor and capacitor connected from the programming pin to ground select a set of parameters.

By selecting the appropriate values of resistor and capacitor, the desired set of parameters (scenario) can be programmed, as shown in [Table 3a](#) and [3b](#).

C\_SEL selects the  $f_{SW}$  setting. There are six options available (from #1 to #6), indicating six different nominal switching frequencies, from lowest to highest. Since the actual value of  $f_{SW}$  also depends on  $V_{OUT}$ , refer to [Figure 4](#) to select the proper  $f_{SW}$  setting for a specific application.

The MAX16425/MAX16425A feature two different configuration tables to provide a wider range of options. [Table 3a](#) and [3b](#) show the scenario options for the MAX16425/MAX16425A, respectively.

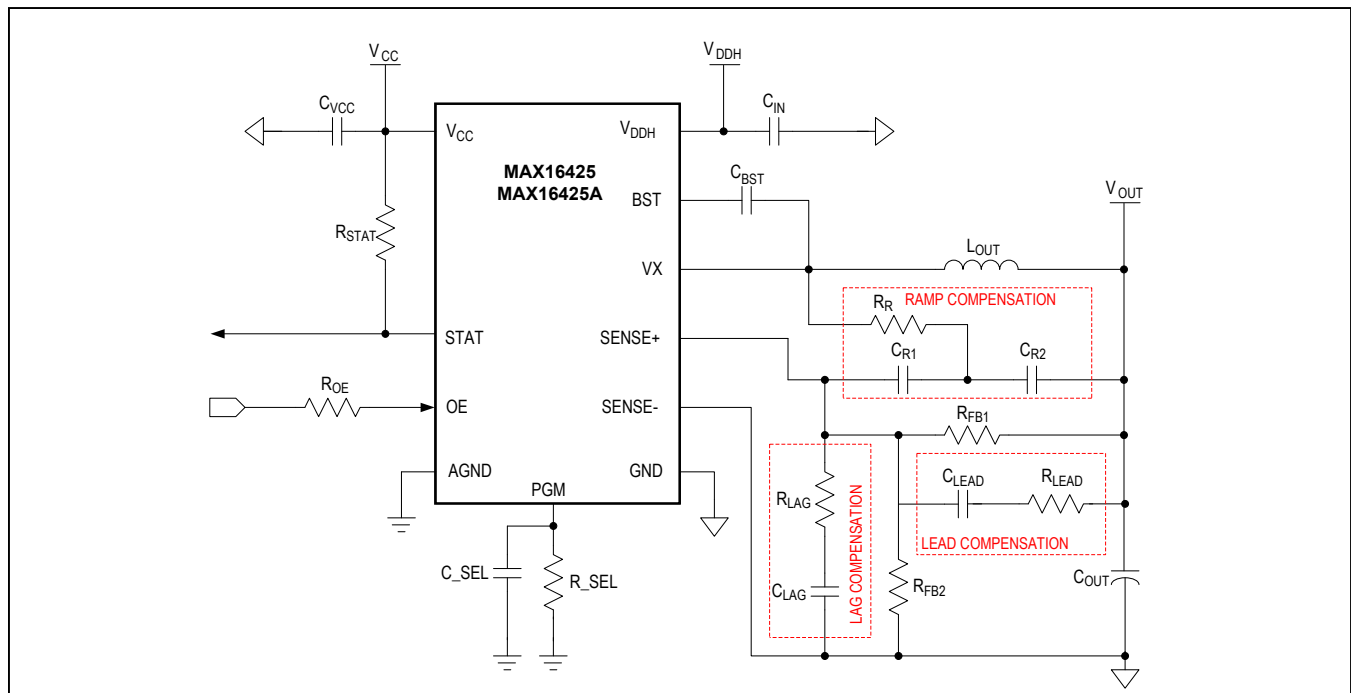


Figure 3. Typical Application Circuit

Table 2. Programmable Options

PARAMETER	DESCRIPTION
V <sub>REF</sub>	Selects internal or external voltage reference. For internal V <sub>REF</sub> two values are available.
Soft-Start Time	The time required to ramp the reference voltage to its final value
OCF Inception	The valley current at which the overcurrent protection is tripped (see the <i>Current Limiting</i> section).
Operation Modes	Selects whether DCM is allowed. If allowed the IC transitions to DCM mode for light loads
Reporting	Selects the parameter reported through the analog output voltage on the PGM pin during regulation.
R <sub>SENSE</sub> Gain	Selects the sense loop gain. By changing this value, the operation and components selection can be optimized.
$f_{SW}$	Switching frequency setting.
t <sub>STAT</sub>	Time delay between the completion of the soft-start ramp and the STAT pin output is valid.

**Table 3a. MAX16425 Configuration Table**

R_SEL (kΩ)	V <sub>REF</sub> (V)	SOFT-START TIME (t <sub>SS</sub> ) (ms)	VALLEY OCP INCEPTION (A)	OPERATION MODES	REPORTING (CURRENT/TEMP)	R <sub>SENSE</sub> (GAIN) (mΩ)	f <sub>SW</sub> SETTING			t <sub>STAT</sub> (μs)
							C_SEL			
							0pF	200pF	820pF	
1.78	0.95	6	16	CCM	Current	2.8	f <sub>SW</sub> #4	f <sub>SW</sub> #5	f <sub>SW</sub> #6	2000
2.67				CCM/DCM						
4.02		3		CCM						
6.04				CCM/DCM						
9.09	Ext.	1.5		CCM						
13.3										
20	0.6	6	24	CCM/DCM	Temp	1.4	f <sub>SW</sub> #1	f <sub>SW</sub> #2	f <sub>SW</sub> #3	128
30.9			16	CCM						
46.4				CCM/DCM						
71.5										
107										
162	Ext.	1.5	20	CCM	Temp		f <sub>SW</sub> #1	f <sub>SW</sub> #2	f <sub>SW</sub> #3	

**Table 3b. MAX16425A Configuration Table**

R_SEL (kΩ)	V <sub>REF</sub> (V)	SOFT-START TIME (t <sub>SS</sub> ) (ms)	VALLEY OCP INCEPTION (A)	OPERATION MODES	REPORTING (CURRENT/TEMP)	R <sub>SENSE</sub> (GAIN) (mΩ)	f <sub>SW</sub> SETTING			t <sub>STAT</sub> (μs)
							C_SEL			
							0pF	200pF	820pF	
1.78	0.95	1.5	16	CCM	Current	2.8	f <sub>SW</sub> #4	f <sub>SW</sub> #5	f <sub>SW</sub> #6	2000
2.67				CCM/DCM						
4.02		3		CCM		5.4				
6.04				CCM/DCM						
9.09	Ext.			CCM		2.8				
13.3				CCM/DCM						
20	0.6	3	24	Temp	5.4					
30.9			CCM							
46.4			16		CCM/DCM					
71.5					CCM					
107	Ext.	1.5	20	CCM	Temp	1.4	f <sub>SW</sub> #1	f <sub>SW</sub> #2	f <sub>SW</sub> #3	128
162										

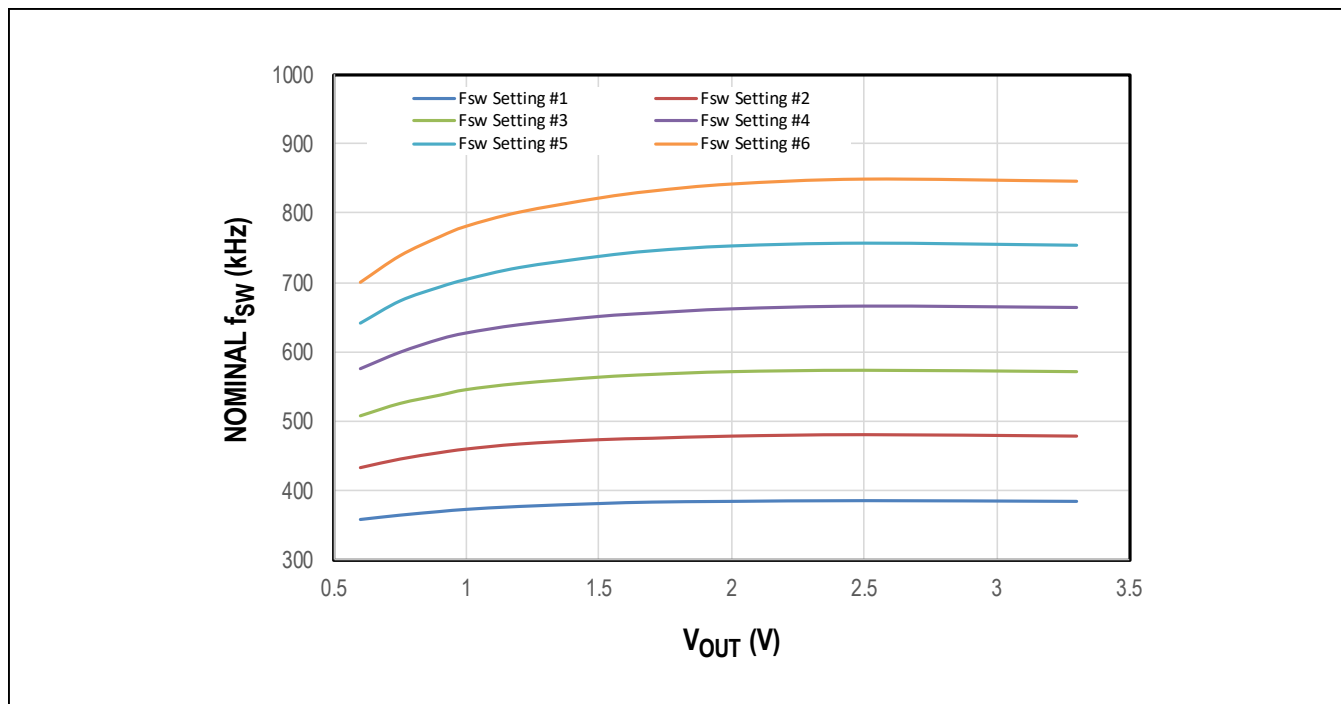


Figure 4. Nominal Switching Frequency vs.  $V_{OUT}$  and  $f_{sw}$  Setting

### Setting the Output Voltage

The output voltage of the MAX16425/MAX16425A is set by selecting a reference voltage and using an appropriate resistive voltage-divider, as shown in Equation 5.

The reference voltage is selected using  $R_{SEL}$  (see [Table 3a](#) and [3b](#)) and can be either internal or external (refer to the [Operation with External  \$V\_{REF}\$](#)  section for more details). In order to improve the DC output voltage accuracy, use the highest  $V_{REF}$  value available and suitable for the application.

For instance, use  $V_{REF} = 0.6V$  for  $0.6V \leq V_{OUT} < 0.95V$  and  $V_{REF} = 0.95V$  for  $0.95V \leq V_{OUT} < 3.3V$ .

To optimize the common-mode rejection of the error amplifier, choose the voltage-divider resistors so that their parallel resistance is as close as possible to  $2k\Omega$  (Equation 6).

#### Equation 5

$$V_{OUT} = V_{REF} \times \left( 1 + \frac{R_{FB1}}{R_{FB2}} \right)$$

Refer to [Table 3a](#) and [3b](#) for  $V_{REF}$  values.

#### Equation 6

$$R_{FB1} = V_{OUT} \times \left( \frac{R_{PAR}}{V_{REF}} \right)$$

$$R_{FB2} = R_{FB1} \times \left( \frac{R_{PAR}}{R_{FB1} - R_{PAR}} \right)$$

where:

- $R_{FB1}$  = Top voltage-divider resistor
- $R_{FB2}$  = Bottom voltage-divider resistor
- $R_{PAR}$  = Desired parallel resistance of  $R_{FB1}$  and  $R_{FB2}$
- $V_{OUT}$  = Output voltage
- $V_{REF}$  = Reference voltage

### The Effect of Resistor Selection on DC Output Voltage Accuracy

$R_{FB1}$  and  $R_{FB2}$  set the output voltage as described in Equation 5. The tolerance of these resistors affects the accuracy of the programmed output voltage.

#### Equation 7

$$\epsilon_{RV_{OUT}} = \frac{2\epsilon_R}{1 - \epsilon_R} \left( \frac{V_{OUT} - V_{REF}}{V_{OUT}} \right)$$

Figure 5 shows the effect of 1% tolerance resistors over a range of output voltages. To ensure accuracy over temperature, the temperature coefficients must also be included in the error calculation (i.e., for 25ppm/°C resistors over a 50°C excursion, add 0.125% to the 25°C tolerance).

The error due to the voltage-feedback resistors' tolerance,  $R_{FB1}$  and  $R_{FB2}$  should be added to the output voltage tolerance due to the IC's  $V_{REF}$  tolerance listed in the [Electrical Characteristics](#) table.

#### Equation 8

$$\varepsilon_{V_{OUT}} = \varepsilon_{V_{REF}} + \varepsilon_{RV_{OUT}}$$

#### Voltage Margining

Voltage margining can be implemented by changing the effective feedback divider ratio. FET switches can be used to introduce or remove parallel resistors to  $R_{FB2}$ , to increase or decrease the output voltage respectively. In order to avoid triggering OVP or UVP faults, the circuits used to introduce resistive divider changes should have switching time constants greater than the response time of the MAX16425/MAX16425A.

#### Operation with External $V_{REF}$

When using an external reference, adopt the configuration shown in [Figure 6](#). The MAX16425/MAX16425A employ a specialized soft-start sequence. Once OE is asserted, the regulator briefly discharges the SENSE- node and releases it as regulation begins. The resulting soft-start ramp timing is determined by the external low-pass filter time constant. The external filter time constant needs to be lower than  $t_{SS}/3$  in order to avoid premature assertion of the STAT pin while the output voltage is still ramping.

The external reference voltage should be limited between 0.8V and 1.1V and can be applied prior to enabling the regulator, or ramped up right after enable is asserted. In both cases, the low-pass filtered reference voltage at the SENSE- pin must reach its final value within  $t_{SS}$ .

Typical values for the filter components are:

- $R_F = 2.2k\Omega$
- $C_F = 0.22\mu F$

When changing the external reference voltage during normal operation (after the part has powered up, and reached regulation level), the regulator must be able to

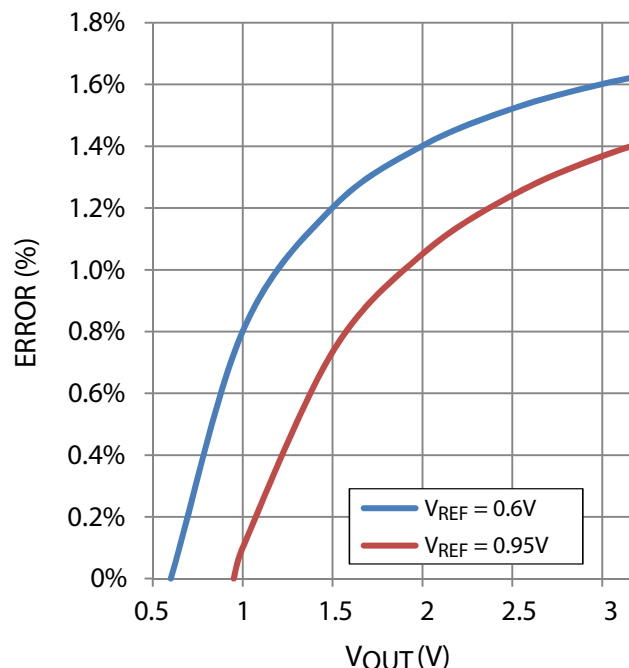


Figure 5. Contribution of 1% Tolerance Resistors on  $V_{OUT}$  Error

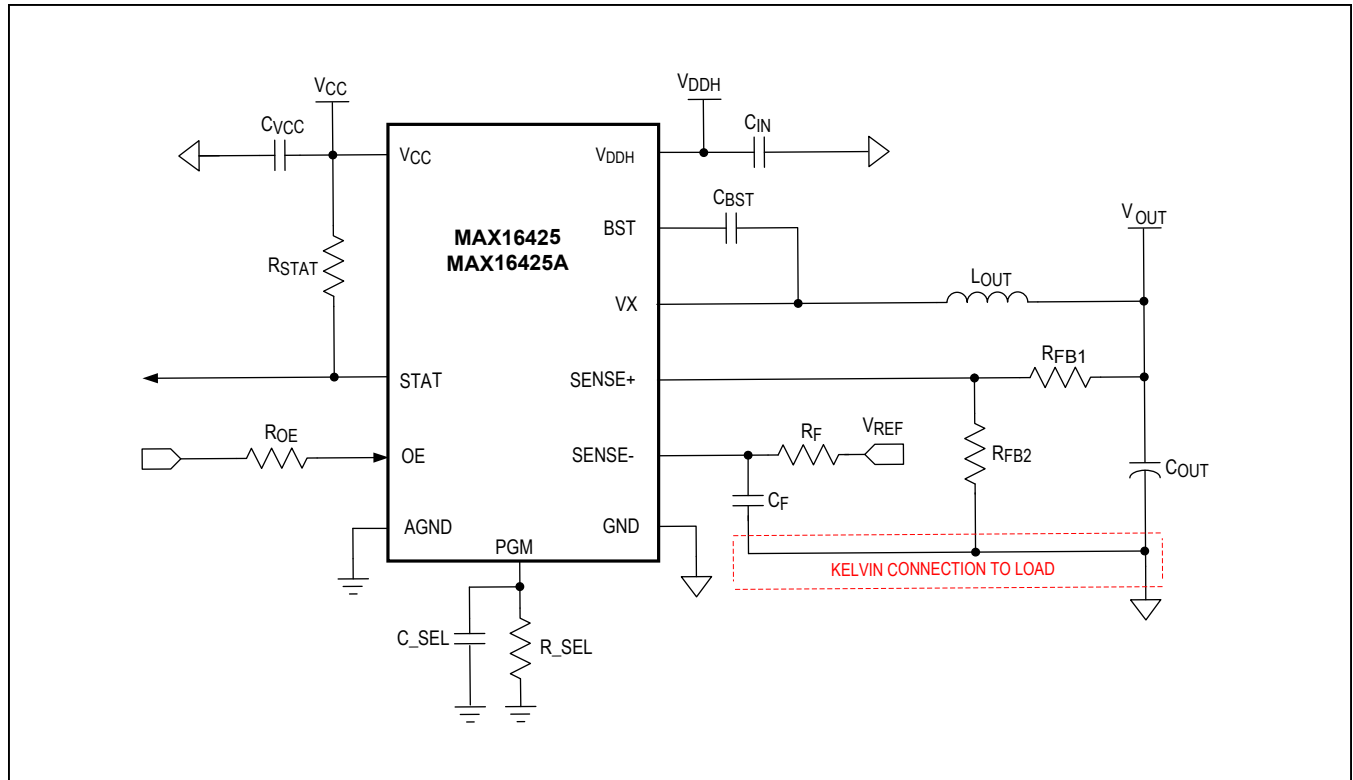


Figure 6. Electrical Connections to Use the External Voltage Reference Feature

follow the reference-voltage change fast enough as to avoid OVP and PWRGD faults. Please make sure that reference-voltage change timing from the initial to the final value does not exceed  $1/(2 \times BW)$ , where BW is the bandwidth of the regulator in Hertz (Hz).

### Control Loop

The MAX16425/MAX16425A use Quick PWM architecture with current-sense signal added to feedback. Hence, without additional compensation, the voltage-loop gain consists of the following terms:

- The IC's current-mode control scheme has an effective transconductance gain of  $1/R_{SENSE(GAIN)}$ . See [Table 3a](#) and [3b](#) for correct  $R_{SENSE(GAIN)}$  values.
- The output capacitors contribute an impedance gain of  $1/(2 \times \pi \times C_{OUT} \times f)$ .
- The feedback divider contributes an attenuation of  $K_{DIV} = R_{FB2}/(R_{FB1} + R_{FB2})$ .

Thus, when the ramp injection components ( $R_R$ ,  $C_{R1}$ ,  $C_{R2}$ ), lead compensation components ( $C_{LEAD}$ ,  $R_{LEAD}$ ) and lag compensation components ( $R_{LAG}$ ,  $C_{LAG}$ ) are not used, the approximate loop gain and bandwidth (BW) are given by the following equations.

### Equation 9

$$|Loop\_Gain(f)| = \frac{K_{DIV}}{2 \times \pi \times R_{SENSE(GAIN)} \times C_{OUT} \times f}$$

$$BW = \frac{K_{DIV}}{2 \times \pi \times R_{SENSE(GAIN)} \times C_{OUT}}$$

$$\text{or } BW = \frac{1}{2 \times \pi \times R_{GAIN\_EFF} \times C_{OUT}}$$

where,  $R_{GAIN\_EFF}$  equals  $R_{SENSE(GAIN)}/K_{DIV}$ .

For stability,  $C_{OUT}$  should be chosen so that  $BW < f_{SW}/3$ . Designing with no loop compensation can result in fairly large  $C_{OUT}$ ; compensation schemes such as Lead, Lag and Ramp Injection can be used to allow  $C_{OUT}$  reduction.



These compensations impact the transient performance as they change the BW of the system. This should be included in design analysis.

### Integrator

The IC has an integrator included in its error amplifier to improve load regulation. The integrator only adds gain at low frequencies, so it does not affect the loop BW; therefore, it was not considered in previous equations. With the integrator, the loop gain from Equation 9 is multiplied by a factor of

$$(1/\tau_{\text{REC}} + s)/s$$

where,  $\tau_{\text{REC}} = 20\mu\text{s}$ .

### Step Response

$R_{\text{GAIN\_EFF}}$  determines the small-signal transient response of the regulator. When a load step is applied that does not exceed the slew rate capability of the inductor current, the regulator responds linearly and  $V_{\text{OUT}}$  temporarily changes by the amount of  $V_{\text{OUT\_ERROR}}$  (Equation 10a). If the load step applied exceeds the slew rate capability of the inductor current, the voltage deviation ( $V_{\text{OUT\_ERROR}}$ ) is solely determined by output filter values (Equation 10a).

The actual voltage deviation ( $V_{\text{OUT\_ERROR}}$ ) is given by the largest of the values calculated using Equation 10a and Equation 10b

#### Equation 10.

$$\begin{aligned} \text{a) } V_{\text{OUT\_ERROR}} &= I_{\text{STEP}} \times R_{\text{GAIN\_EFF}} \\ \text{b) } V_{\text{OUT\_ERROR}} &\approx \frac{(I_{\text{STEP}} \times L)}{2 \times V_{\text{OUT}} \times C_{\text{OUT}}} \end{aligned}$$

After a transient event,  $V_{\text{OUT}}$  returns to the nominal value with a  $20\mu\text{s}$  time constant, due to the integrator circuit. A first order average small-signal model of the regulator is shown in [Figure 7](#).  $V_{\text{EQ}}$  is an ideal voltage source equal to  $V_{\text{OUT}}$ ,  $R_{\text{EQ}}$  ( $R_{\text{GAIN\_EFF}}$ ) is an emulated lossless resistance created by the control-loop action and  $L_{\text{EQ}}$  ( $\tau_{\text{REC}} \times R_{\text{GAIN\_EFF}}$ ) is an emulated inductance. Note that  $L_{\text{EQ}}$  is not the same as the actual  $L_{\text{OUT}}$  inductor, which has been absorbed into the model.  $C_{\text{OUT}}$  is the actual output capacitance.

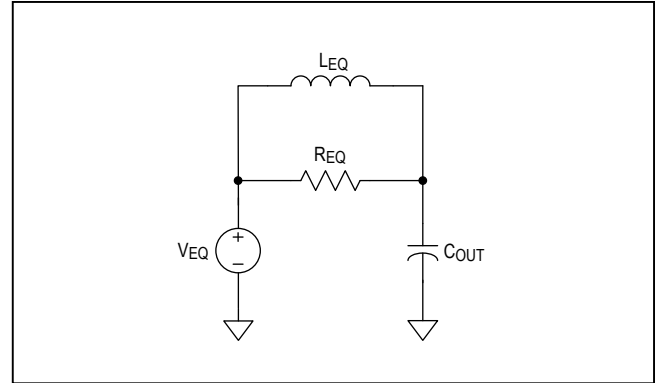


Figure 7. Averaged Small-Signal Equivalent Circuit of Regulator

### Lag Compensation

In cases where the response is faster than desired, the lag compensation network ( $R_{\text{LAG}}$ ,  $C_{\text{LAG}}$ ) can be used to decrease the BW. This has the effect of lowering the gain contribution of the feedback network at higher frequencies, by effectively placing  $R_{\text{LAG}}$  in parallel with  $R_{\text{FB2}}$ . For the lag network to be effective and to achieve optimal phase margin, the zero at  $1/(2 \times \pi \times R_{\text{LAG}} \times C_{\text{LAG}})$  should be placed at least a decade below the crossover frequency ( $\text{BW}/10$ ). With lag,  $K_{\text{DIV}}$  near the crossover frequency becomes Equation 11.

#### Equation 11

$$\begin{aligned} K_{\text{DIV\_LAG}} &= \frac{(R_{\text{FB2}} \parallel R_{\text{LAG}})}{(R_{\text{FB1}} + R_{\text{FB2}} \parallel R_{\text{LAG}})} \\ R_{\text{GAIN\_EFF}} &= \frac{R_{\text{GAIN}}}{K_{\text{DIV\_LAG}}} \end{aligned}$$

Lag compensation increases  $R_{\text{GAIN\_EFF}}$  and  $V_{\text{OUT\_ERROR}}$  while decreasing BW. An increase in  $V_{\text{OUT\_ERROR}}$  can also result in higher overshoot at startup especially when the system recovers after hitting OCP. To avoid this, make sure that Equation 12 is satisfied.

#### Equation 12

$$C_{\text{LAG}} < \frac{V_{\text{OUT}} \times C_{\text{OUT}}}{I_{\text{OCP}} \times (R_{\text{LAG}} + R_{\text{FB1}} \parallel R_{\text{FB2}}) \times 3}$$

### Lead Compensation

In cases where the response is slower than desired, the lead compensation network ( $R_{\text{LEAD}}$ ,  $C_{\text{LEAD}}$ ) can be used to increase the bandwidth. This has the effect of increasing the gain contribution of the feedback network at higher frequencies, by effectively placing  $R_{\text{LEAD}}$  in parallel with  $R_{\text{FB1}}$ .



For the lead network to be effective and to achieve optimal phase margin, the zero at  $1/(2 \times \pi \times R_{LEAD} \times C_{LEAD})$  should be placed below the crossover frequency ( $BW/10 < f_z < BW$ ).

With lead compensation,  $K_{DIV}$  near the crossover frequency becomes Equation 13.

**Equation 13**

$$K_{DIV\_LEAD} = \frac{R_{FB2}}{(R_{FB1} \parallel R_{LEAD} + R_{FB2})}$$

$$R_{GAIN\_EFF} = \frac{R_{GAIN}}{K_{DIV\_LEAD}}$$

Lead compensation decreases  $R_{GAIN\_EFF}$  and  $V_{OUT\_ERROR}$  while increasing BW accordingly.

**External Ramp**

The ramp compensation stabilizes the converter if the ESR of the output capacitor bank is low. The ramp is added to the internal current-sense signal at the error comparator inputs, which improves the signal-to-noise ratio and reduces the offtime jitter.

The amplitude of the external ramp is determined by  $R_R$  and  $C_{R2}$  (Figure 8). A voltage signal, which approximates the inductor current appears across  $C_{R2}$  and it is injected to the feedback node through  $C_{R1}$ .

Values of ramp compensation network are selected as follows:

- 1)  $C_{R1}$  is chosen to maximize the coupling of the ramp signal on the feedback node:  
 $C_{R1} \times R_{FB1} \parallel R_{FB2} \parallel R_{LEAD} \parallel R_{LAG} \approx 10 \times t_{SW}$
- 2)  $C_{R2}$  is chosen such that the ramp signal is unaffected by the value of  $C_{R1}$ :  $C_{R2} \approx 10 \times C_{R1}$ .
- 3)  $R_R$  is chosen to achieve the desired ramp injection signal. Use Equation 14 to calculate proper  $R_R$  value.

The approximate amplitude of the external ramp at the SENSE+ pin is given by Equation 14.

**Equation 14**

$$V_{RAMP\_EXT} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{(V_{IN} \times R_R \times C_{R2} \times f_{SW})}$$

The sensed inductor current ramp at the comparator input is given in Equation 15.

**Equation 15**

$$V_{RAMP\_IND} = \frac{R_{GAIN} \times V_{OUT} \times (V_{IN} - V_{OUT})}{(V_{IN} \times L_{OUT} \times f_{SW})}$$

where,  $R_{GAIN}$  equals the internal current sense gain (see [Electrical Characteristics](#) table)

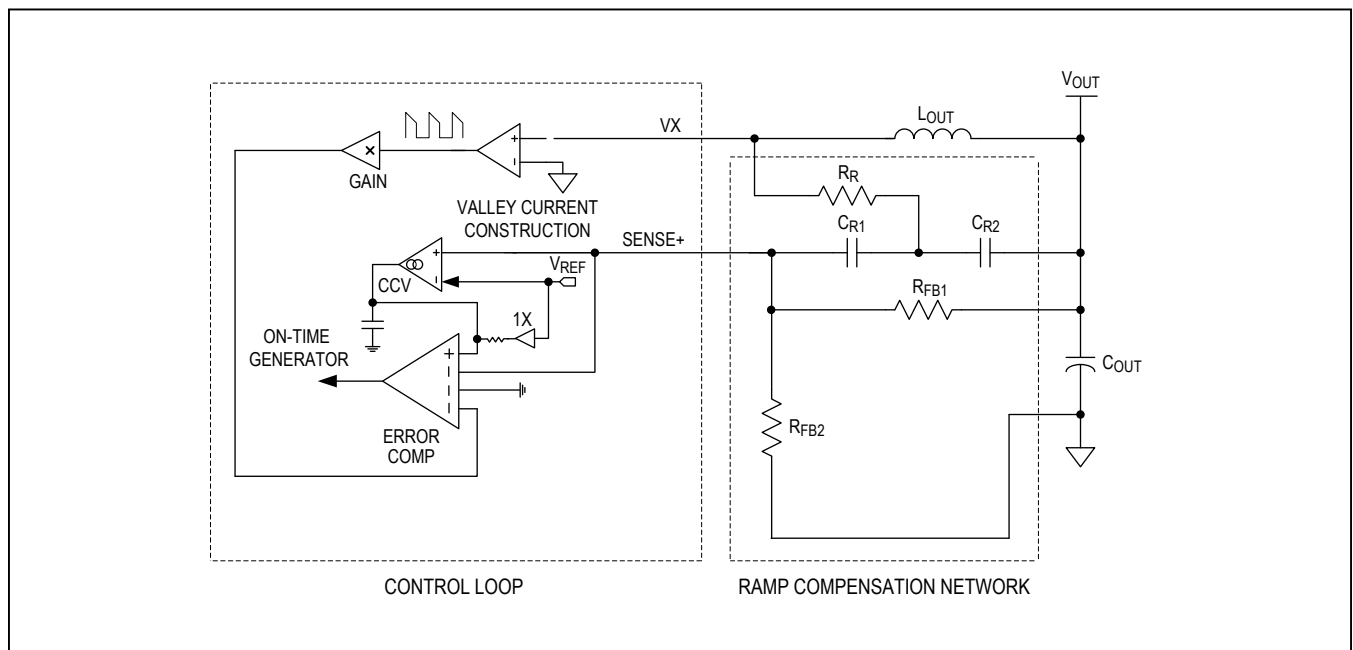


Figure 8. Ramp Compensation Diagram

The high-frequency gain from SENSE+ to the comparator input is unity. Therefore, with the external ramp, the comparator sees an effective ramp given in Equation 16.

**Equation 16**

$$V_{\text{RAMP\_EFF}} = V_{\text{RAMP\_IND}} + V_{\text{RAMP\_EXT}} \\ = V_{\text{OUT}} \times \frac{(V_{\text{IN}} - V_{\text{OUT}})}{(V_{\text{IN}} \times L_{\text{OUT}} \times f_{\text{SW}})} \times \left[ R_{\text{GAIN}} + \frac{L_{\text{OUT}}}{(R_{\text{R}} \times C_{\text{R2}})} \right]$$

For best results, it is recommended that  $V_{\text{RAMP\_EFF}}$  be at least 15mV.

The effective  $R_{\text{GAIN}}$  with external ramp is given in Equation 17.

**Equation 17**

$$R_{\text{GAIN\_EFF}} = R_{\text{GAIN}} + \frac{L_{\text{OUT}}}{(R_{\text{R}} \times C_{\text{R2}})}$$

The ramp injection capacitors effectively bypass the divider near the cross-over frequency, so in this case  $K_{\text{DIV}}$  is approximately 1 and drops out of the loop gain equation.

Similar to lag compensation, ramp injection increases  $R_{\text{GAIN\_EFF}}$  and  $V_{\text{OUT\_ERR}}$ .

**Inductor Selection**

The inductor value is selected based on the switching frequency and the percentage ratio of the inductor ripple to the peak load current (LIR - inductor current ratio).

**Equation 18**

$$L = \left[ \frac{(V_{\text{IN}} - V_{\text{OUT}})}{f_{\text{SW}} \times I_{\text{LOAD(MAX)}} \times \text{LIR}} \right] \times \frac{V_{\text{OUT}}}{V_{\text{IN}}}$$

where:

LIR = Inductor current ratio

$I_{\text{LOAD(MAX)}}$  = Peak load current

A lower LIR results in lower RMS losses in passive and active components, which improves the regulator efficiency. A higher LIR results in faster inductor current slew rate, better transient performance and lower inductor value/size. Optimal inductor selection is performed by evaluating these trade-offs according to design requirements.

The inductor must have a saturation current higher than the peak current during OCP event. The highest peak current is reached when a hard  $V_{\text{OUT}}$  short circuit is applied during operation (See Equation 19). In addition, the application circuit design must ensure that the peak current never exceeds the maximum operating current ( $I_{\text{PK}}$ ) listed in the [Operating Ratings](#) section.

**Equation 19**

$$I_{\text{SAT}} > I_{\text{PK(MAX)}} = I_{\text{OCP}} + \frac{V_{\text{OUT}}}{L \times f_{\text{SW}}}$$

where:

$I_{\text{SAT}}$  = Inductor saturation current

$I_{\text{OCP}}$  = Overcurrent protection threshold (see [Table 3a](#) and [3b](#))

**Output Capacitor Selection**

Output capacitor selection is based on output-ripple and load-transient requirements. Low ESR capacitors (MLCCs) are recommended to minimize ripple.

The output ripple is affected by three components: a resistive component due to effective ESR of the output capacitor bank, an inductive component due to parasitic inductance of the capacitor package (ESL) and capacitive component based on total  $C_{\text{OUT}}$ . See Equation 20 for an approximate expression of the output voltage ripple.

**Table 4. Typical Boost, Filtering and Decoupling Capacitor Requirements**

DESCRIPTION	VALUE	TYPE	PACKAGE	QTY
$V_{\text{CC}}$ Capacitor	1 $\mu$ F/6.3V	X7R/125°C	0402/0603	1
Boost Capacitor	0.47 $\mu$ F/6.3V	X7R/125°C	0402	1
$V_{\text{DDH}}$ HF Capacitor (Note 1)	1 $\mu$ F/16V	X7R/125°C	0603	1
$V_{\text{DDH}}$ HF Capacitor (Note 1)	0.1 $\mu$ F/16V	X7R/125°C	0402	1
$V_{\text{DDH}}$ Bulk Capacitor (Note 2)	10 $\mu$ F/16V	X5R	0805/1206	2

**Note 1:** All  $V_{\text{DDH}}$  high-frequency capacitors must be placed in close proximity to the slave IC and on the same side of the PCB as the slave IC. Refer to Analog Devices' layout guideline for component placement requirements and recommendations.

**Note 2:** For operation below 10.8V, two 22 $\mu$ F bulk capacitors are recommended instead of two 10 $\mu$ F capacitors.

**Equation 20**

$$V_{PP} = ESR(I_{OUTRIP}) + ESL \left( \frac{V_{IN}}{L_{OUT}} \right) + \left( \frac{I_{OUTRIP}}{8 \times f_{SW} \times C_{OUT}} \right)$$

where:

ESR	= Equivalent series resistance at the output
$I_{OUTRIP}$	= Peak-to-peak inductor current ripple
ESL	= High-frequency equivalent series inductance at output
$V_{IN}$	= Input voltage
$L_{OUT}$	= Output inductance
$f_{SW}$	= Switching frequency
$C_{OUT}$	= Output capacitance

Low ESR MLCC capacitors minimize the voltage drop due to fast load transients. Follow Equation 9 and the description in the [Control Loop](#) section to properly size the output capacitor bank.

In addition to output-voltage ripple and transient requirements for determining the output capacitance, ripple-current rating and power dissipation of the output capacitors should also be considered (Equation 21 and Equation 22).

**Equation 21**

$$I_{RMS\_COUT} = \frac{I_{OUTRIP}}{\sqrt{12}}$$

where  $I_{OUTRIP}$  equals peak-to peak ripple current value.

**Equation 22**

$$P_{COUT} = I_{RMS\_COUT}^2 \times ESR$$

where ESR equals the equivalent series resistance of the entire output capacitor bank.

**Input Capacitor Selection**

Input capacitors are designed to filter the pulsed current drawn by the switching regulator when the high-side FET is conducting. Filtering is primarily accomplished by the bulk input capacitors, while the high-frequency capacitors are used to minimize the parasitic inductance between the input supply and the voltage regulator. This arrangement minimizes the voltage transients during the commutations of high-side and low-side MOSFETs. For effective

input decoupling, it is critical that the high-frequency decoupling be placed in close proximity to the MAX16425/MAX16425A  $V_{DDH}$  and GND pins, and on the same side of the PCB board as the MAX16425/MAX16425A. Follow [Table 4](#) for minimum input decoupling recommendations. It is also recommended to keep the input ripple below 3% of the DC voltage. To meet this target, additional capacitance can be required other than the minimum recommendations listed in [Table 4](#). Use Equation 23 to calculate total input capacitance based on desired peak-to-peak input-voltage ripple.

**Equation 23**

$$C_{IN} = \frac{I_{MAX} \times V_{OUT} \times (V_{DDH} - V_{OUT})}{(f_{SW} \times V_{DDH}^2 \times V_{DDH\_P-P})}$$

where:

$C_{IN}$	= Input capacitance (MLCC)
$I_{MAX}$	= Maximum load current
$V_{DDH}$	= Input voltage
$V_{OUT}$	= Output voltage
$f_{SW}$	= Switching frequency (CCM)
$V_{DDH\_P-P}$	= Target peak-to-peak input-voltage ripple

Because of discontinuous current drawn from the input supply, the power-dissipation and ripple-current rating of input capacitors are more important than those of the output capacitors. Use Equation 24 to calculate the RMS current that the input capacitors must withstand. Multiple input caps can be placed in parallel to achieve the required total input RMS current rating.

**Equation 24**

$$I_{RMS\_CIN} = \frac{I_{LOAD} \sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

where  $I_{LOAD}$  equals the output DC load current.

With an equivalent series resistance of the bulk input capacitor bank ( $ESR_{CIN}$ ), the total power dissipation in the input capacitors is given by Equation 25.

**Equation 25**

$$P_{CIN} = I_{RMS\_CIN}^2 \times ESR_{CIN}$$

**Printed Circuit Board Layout**

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. The high current path requires particular attention. If possible, place all the power components on the top side of the board with their ground terminals flushed against one another. Follow these guidelines for good PCB layout:

- 1) Keep the power traces and load connections short. This is essential for high efficiency and stable operation. The use of thick copper PCBs (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Pay close attention to correct routing and PCB trace length reduction even by fraction of inches, where a single mΩ of excess trace resistance causes a measurable efficiency penalty. For maximum efficiency place the regulator, output inductor, and output capacitors as close as possible to the load. If this is not possible, keep the output capacitors close to the load and output inductor close to the regulator.
- 2) Keep the high-current traces (VX, V<sub>DDH</sub>, V<sub>CC</sub> and BST) short and wide to minimize trace resistance and inductance. Traces connecting the input capacitors and V<sub>DDH</sub> (power input node) on the IC require particular attention since they carry currents with the largest RMS values and fastest slew rates.
- 3) The input capacitors should be placed as close to the input supply pins (V<sub>DDH</sub> and GND) as possible. High-frequency filter capacitors (see [Table 4](#)) must be placed within 60 mils of V<sub>DDH</sub>/GND pins. V<sub>CC</sub> and BST decoupling capacitors (see [Table 4](#)) must be placed on the same side of the PCB board as the IC. There should be an uninterrupted ground plane located immediately underneath these high-frequency current paths with the ground plane located no more than 8 mils below the top layer. By keeping the flow of this high frequency AC current localized to a tight loop at the regulator, electromagnetic interference (EMI) can be minimized.

- 4) Keep the sensitive analog signals away from high-speed switching nodes. The ground plane can be used to shield these sensitive signals and protect them from coupling of high-frequency noise. Voltage sense lines should be routed differentially with Kelvin connections to the load points. For remote-sense applications where the load and regulator IC are separated by a significant distance or impedance, it is important to place the majority of the output capacitors directly at the load for system stability. In remote-sense applications, common-mode filtering is necessary to filter high-frequency noise in the sense lines.

The following layout recommendations should be used for optimal performance:

- It is essential to have a low-impedance and uninterrupted ground plane under the IC and extended out underneath the inductor and output capacitor bank.
- Multiple vias are recommended for all paths that carry high currents (i.e., GND, V<sub>DDH</sub>, VX). Vias should be placed close to the IC to create the shortest possible current loops. Via placement must not obstruct the flow of currents or mirror currents in the ground plane.
- A single via in close proximity to the chip should be used to tie the top layer AGND trace to the second layer ground plane. It must not be connected to the top power ground area.
- The feedback divider and compensation network should be close to the IC.

Gerber files with layout information and complete reference designs can be obtained by contacting an Analog Devices account representative.

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## MAX16425/MAX16425A

Integrated, Step-Down Switching Regulator  
with Selectable Applications Configurations

### Ordering Information

PART NUMBER	PIN-PACKAGE	CURRENT LEVEL (A)	SHIPPING METHOD
<b>MAX16425GCJ+</b>	27-bump WLCSP	25	2.5ku Tape & Reel
MAX16425GCJ+T	27-bump WLCSP	25	2.5ku Tape & Reel
<b>MAX16425AGCJ+</b>	27-bump WLCSP	25	2.5ku Tape & Reel
MAX16425AGCJ+T	27-bump WLCSP	25	2.5ku Tape & Reel

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/19	Initial Data Sheet	—



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