LT8210-1

100V V_{IN} and V_{OUT} Synchronous 4-Switch Multiphase Buck-Boost DC/DC Controller

FEATURES

- **Built-In Multiphase Current Sharing**
- **18µA Pass-Thru Mode I_Q with 99.9% Efficiency**
- **Pass-Thru or Fixed Output CCM, DCM Operation**
- **Programmable Non-Switching Pass-Thru Window**
- **V_{IN} Range: 2.8V to 100V (4.5V for Start-Up)**
- **V_{OUT} Range: 1V to 100V**
- **Reverse Input Protection to -40V**
- **±2% Output Voltage Accuracy (–40°C to 125°C)**
- **Programmable Current Limit**
- **10V Quad N-Channel MOSFET Gate Drivers**
- ±20% Cycle-by-Cycle Inductor Current Limit
- No Top MOSFET Refresh Noise in Buck or Boost
- Fixed/Phase-Lockable Frequency: 80kHz to 400kHz
- Spread-Spectrum Frequency Modulation for Low EMI
- Power Good Output Voltage/Overcurrent Monitor
- Available in a 40-Lead (6mm x 6mm) QFN Package

APPLICATIONS

- Industrial, Telecom, Avionics Systems, Automotive Qualification in Progress

GENERAL DESCRIPTION

The **LT®8210-1** is a 4-switch synchronous buck-boost DC/DC controller that can operate in pass-thru mode, forced continuous conduction, or pulse-skipping mode. Pass-Thru is a feature that passes the input directly to the output when the input is within a user programmable window. Pass-Thru mode eliminates switching losses and EMI while maximizing efficiency. For input voltages above or below the pass-thru window, the buck or boost regulation loops maintain the output at the set maximum or minimum values, respectively. The LT8210-1 is pin compatible with the LT8210. The IMON pin on the LT8210-1 has an ISHARE function, which allows for masterless current sharing.

Multiple LT8210-1 can be connected in parallel for higher output current and reduced voltage ripple. A masterless closed loop current sharing loop balances the current per phase and allows phase shedding. Optional reverse input protection down to -40V can be implemented with the addition of a single N-channel MOSFET. The LT8210-1 includes a precision current sense amplifier that can accurately monitor and limit output or input average current.

TYPICAL APPLICATION

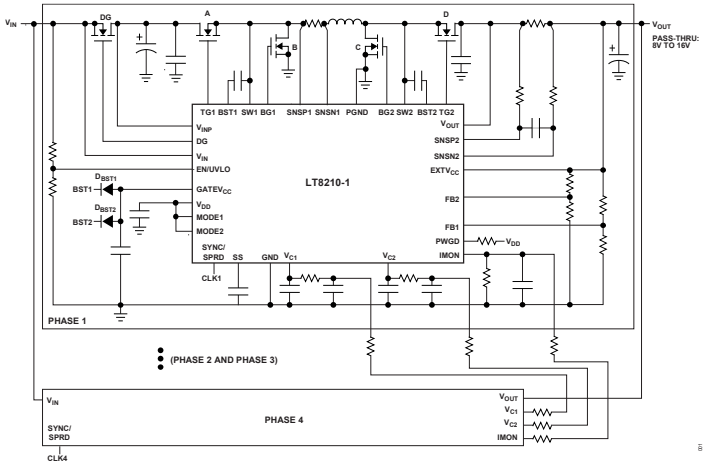

Figure 1. Typical Application Drawing

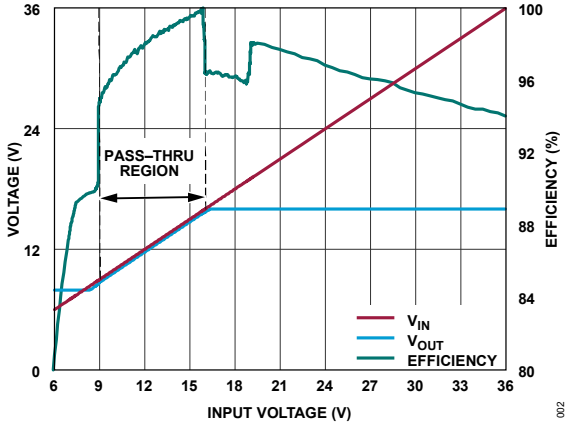

Figure 2. Pass-Thru Transfer Characteristic ($V_{OUT(BOOST)}$ = 8V, $V_{OUT(BUCK)}$ = 16V) 75A LOAD

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REVISION HISTORY

Revision Number	Revision Date	Nature of Change	Page Number
Rev 0	02/2024	Initial Release	—
Rev A	04/2024	Updated Figure 57 and Figure 79	33, 56

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SPECIFICATIONS

Table 1. Electrical Characteristics

(Specifications are at T_A = 25°C. V_{IN} = 12V, V_{INP} = 12V, $V_{EN/UVLO}$ = 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Voltage Supplies and Regulators							
V_{IN}, V_{INP} Input Operating Voltage Range	V_{IN_OPR} V_{INP_OPR}	Minimum Voltage for Start-Up (V_{EXTVCC} = 0V)	-40°C ≤ T_J ≤ 125°C	4.5		100	V
		After Start-Up, V_{EXTVCC} = 12V	-40°C ≤ T_J ≤ 125°C	2.8		100	
V_{IN} Quiescent Current	I_Q	Shutdown ($V_{EN/UVLO}$ = 0V)			1	5	µA
		Not Switching			4	15	
		Internal Charge Pump Enabled (V_{DG} – V_{IN} = 3.5V)			1400	1800	
V_{INP} Quiescent Current	I_{INP_Q}	Shutdown ($V_{EN/UVLO}$ = 0V)			0.1	1.0	µA
		Not Switching			650	1300	
		Internal Charge Pump Enabled (V_{DG} – V_{IN} = 3.5V)			1900	2700	
		Pass-Thru (Non-Switching, V_{INP} = 48V)			18	33	
V_{OUT} Quiescent Current	I_{OUT_Q}	V_{OUT} = 12V			1.5	3	µA
$GATEV_{CC}$ Voltage	V_{GATE_VCC}	$I_{GATEVCC}$ = 25mA	-40°C ≤ T_J ≤ 125°C	9.75	10.5	11.2	V
$GATEV_{CC}$ Current Limit	$I_{GATE\_VCC\_ILIM}$	Regulated from V_{INP}, V_{INP} = 12V, $V_{GATEVCC}$ = 9V	-40°C ≤ T_J ≤ 125°C	65	110		mA
		Regulated from V_{INP}, V_{INP} = 100V, $V_{GATEVCC}$ = 9V	-40°C ≤ T_J ≤ 125°C	16	25		
		Regulated from $EXTV_{CC}$, V_{EXTVCC} = 12V, $V_{GATEVCC}$ = 9V	-40°C ≤ T_J ≤ 125°C	75	115		
		Regulated from $EXTV_{CC}$, V_{EXTVCC} = 40V, $V_{GATEVCC}$ = 9V	-40°C ≤ T_J ≤ 125°C	55	90		

(Specifications are at T_A = 25°C. V_{IN} = 12V, V_{INP} = 12V, $V_{EN/UVLO}$ = 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
$GATEV_{CC}$ Load Regulation		$I_{GATEVCC}$ = 0mA to 50mA	-40°C ≤ T_J ≤ 125°C		1.8	5	%
$GATEV_{CC}$ Regulator Dropout Voltage	$V_{GATE\_VCC\_DO}$	V_{INP} – $V_{GATEVCC}$: $I_{GATEVCC}$ = 50mA	-40°C ≤ T_J ≤ 125°C		750	1600	mV
		V_{EXTVCC} – $V_{GATEVCC}$: $I_{GATEVCC}$ = 50mA	-40°C ≤ T_J ≤ 125°C		600	1400	
$GATEV_{CC}$ Undervoltage Lockout Threshold	V_{UVLO_TH}	Falling	-40°C ≤ T_J ≤ 125°C	3.61	3.75	3.85	V
$GATEV_{CC}$ Undervoltage Lockout Hysteresis	V_{UVLO_HYST}				0.20		V
$GATEV_{CC}$ Backdrive Current	I_{BK_DRV}	To V_{INP} Pin, $V_{GATEVCC}$ = 10V, V_{INP} = 0V			40		µA
		To E_{XTVCC} Pin, $V_{GATEVCC}$ = 10V, V_{EXTVCC} = 0V			3		
$EXTV_{CC}$ Switchover Voltage	$V_{SW\_OV\_EXTVCC}$	Rising	-40°C ≤ T_J ≤ 125°C	7.3	8	8.8	V
$EXTV_{CC}$ Switchover Hysteresis					1.2		V
V_{DD} Voltage	V_{DD}			3.15	3.3	3.4	V
V_{DD} Current Limit	I_{VDD_LIM}	V_{DD} = 3V		9			mA
V_{DD} Undervoltage Lockout Threshold	$V_{UVLO\_TH\_VDD}$	Falling		2.7	2.8	2.9	V
V_{DD} Undervoltage Lockout Hysteresis					140		mV
Enable Comparator							
EN/UVLO Enable Threshold	V_{EN_TH}	Rising	-40°C ≤ T_J ≤ 125°C	1.27	1.45	1.61	V
EN/UVLO Enable Hysteresis	V_{EN_HYST}				100		mV
EN/UVLO Pin Bias Current	I_{EN_BIAS}	$V_{EN/UVLO}$ = 100V	-40°C ≤ T_J ≤ 125°C		0.1	1	µA
Reverse Input Protection							

(Specifications are at T_A = 25°C. V_{IN} = 12V, V_{INP} = 12V, $V_{EN/UVLO}$ = 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
DG Gate Drive Voltage (V_{DG} – V_{IN})	V_{DG_DRIVE}	Non-Switching	-40°C ≤ T_J ≤ 125°C	7.0	8.5		V
Reverse Input Disconnect Threshold (V_{IN})	$V_{REV\_DIS\_TH}$	I_{DG} = 100µA	-40°C ≤ T_J ≤ 125°C	–1.8	–1.2	–0.5	V
DG Pin Pull-Down Current	$I_{DB\_PULL\_DN}$	V_{IN} = –4V, V_{DG} – V_{IN} = 5V	-40°C ≤ T_J ≤ 125°C	50	80	130	mA
DG Pin Pull-Up Current	$I_{DG\_PULL\_UP}$	V_{DG} – V_{IN} = 1.5V	-40°C ≤ T_J ≤ 125°C	100	180		µA
		V_{DG} – V_{IN} = 8.5V	-40°C ≤ T_J ≤ 125°C	4	25		
DG Undervoltage Threshold (V_{DG} – V_{IN})	$V_{DG\_UV\_TH}$	Rising	-40°C ≤ T_J ≤ 125°C	2.3	2.8	3	V
DG Undervoltage Hysteresis (V_{DG} – V_{IN})	$V_{DG\_UV\_HYST}$				700		mV
Voltage Regulation							
FB1 Regulation Voltage	V_{FB1}	Regulation Voltage for CCM, DCM Operation, Pass-Thru Mode Boost Loop	-40°C ≤ T_J ≤ 125°C	0.982	1.00	1.016	V
FB2 Regulation Voltage	V_{FB2}	Regulation Voltage Pass-Thru Mode Buck Loop	-40°C ≤ T_J ≤ 125°C	0.98	1.00	1.02	V
FB1, FB2 Input Bias Current	I_{B_FB1} I_{B_FB2}	-40°C ≤ T_J ≤ 125°C			0.001	0.04	µA
FB1, FB2 Line Regulation		V_{INP} = 3V to 100V	-40°C ≤ T_J ≤ 125°C		0.001	0.008	%/V
FB1, FB2 Error Amplifier Transconductance					450		µA/V

(Specifications are at T_A = 25°C. V_{IN} = 12V, V_{INP} = 12V, $V_{EN/UVLO}$ = 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
V_{C1}, V_{C2} Output Impedance					5		MΩ
V_{C1}, V_{C2} Maximum Sourcing Current	I_{VC1_SOURCE} I_{VC2_SOURCE}	$V_{FB1} = V_{FB2} = 0V$			35		µA
V_{C1}, V_{C2} Maximum Sinking Current	I_{VC1_SINK} I_{VC2_SINK}	$V_{FB1} = V_{FB2} = 2V$			–35		µA
Soft-Start Charging Current	I_{SS}	V_{SS} = 0.5V	-40°C ≤ T_J ≤ 125°C	3.5	5	6	µA
Soft-Start Pull-Down Resistance	R_{SS_PD}				140	250	Ω
Average Current Monitoring / Sharing / Limiting							
SNSP2, SNSN2 Operating Voltage Range	V_{SNSP2_OPR} V_{SNSN2_OPR}	-40°C ≤ T_J ≤ 125°C		0		100	V
SNSP2, SNSN2 Pin Bias Current	I_{B_SNSP2}	$V_{SNSP2} = V_{SNSN2}$ = 100V			1	3	µA
	I_{B_SNSN2}	$V_{SNSP2} = V_{SNSN2}$ = 0V		–3	0		
IMON Output Current	I_{MON}	$V_{SNSP2} – V_{SNSN2}$ = 150mV	-40°C ≤ T_J ≤ 125°C	84	90	95	µA
		$V_{SNSP2} – V_{SNSN2}$ = 50mV	-40°C ≤ T_J ≤ 125°C	27	30	33	
		$V_{SNSP2} – V_{SNSN2}$ = 10mV	-40°C ≤ T_J ≤ 125°C	4	6	8	
Current Sharing Mismatch ($V_{SNSP2} – V_{SNSN2}$)		$V_{SNSP2} – V_{SNSN2}$ = 50mV, R_{IMON} = 11kΩ			5		mV
IMON DC CMRR		$V_{SNSP2} – V_{SNSN2}$ = 150mV, VSNSP2 = 3V to 100V			110		dB
IMON Step Response Time		Step $V_{SNSP2} – V_{SNSN2}$ from 0mV to 150mV			2		ms

(Specifications are at T_A = 25°C. V_{IN} = 12V, V_{INP} = 12V, $V_{EN/UVLO}$ = 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Overcurrent Warning Threshold (V_{IMON})	V_{IMON}	Rising	-40°C ≤ T_J ≤ 125°C	1.15	1.2	1.24	V
Overcurrent Warning Hysteresis	V_{HYST_OC}				45		mV
IMON Disable Threshold (V_{IMON})	V_{IMON_TH}	Rising	-40°C ≤ T_J ≤ 125°C	2.3	2.5	2.8	V
IMON Disable Hysteresis	V_{HYST_IMON}				400		mV
Cycle-by-Cycle Inductor Current Limiting							
Maximum Current Sense Threshold (V_{SNSP1} – V_{SNSN1})	V_{SNS_TH}	Buck Regulation (V_{INP} = 24V, V_{OUT} = 0V)	-40°C ≤ T_J ≤ 125°C	45	53	61	mV
Maximum Current Sense Threshold (V_{SNSP1} – V_{SNSN1})	V_{SNS_TH}	Buck Regulation (V_{INP} = 24V, V_{OUT} = 12V)	-40°C ≤ T_J ≤ 125°C	55	62	70	mV
		Boost Regulation (V_{INP} = 6V, V_{OUT} = 12V)	-40°C ≤ T_J ≤ 125°C	45	51	58	
		Buck Regulation (V_{INP} = 100V, V_{OUT} = 48V)	-40°C ≤ T_J ≤ 125°C	73	85	101	
		Boost Regulation (V_{INP} = 24V, V_{OUT} = 48V)	-40°C ≤ T_J ≤ 125°C	36	45	54	
Maximum Non-Switching Current Sense Threshold in Pass-Thru (V_{SNSP1} – V_{SNSN1})	$V_{SNS\_TH\_PT}$	V_{OUT} = V_{INP}, FB1 = 1.2V, FB2 = 0.8V MODE1 = MODE2 = 3.3V	-40°C ≤ T_J ≤ 125°C	57	63	70	mV
Reverse Current Sense Threshold (V_{SNSP1} – V_{SNSN1})	$V_{SNS\_REV\_TH}$	DCM/Pass-Thru Modes			3		mV
		Pass-Thru Buck-Boost Regions			–6		

(Specifications are at T_A = 25°C. V_{IN} = 12V, V_{INP} = 12V, $V_{EN/UVLO}$ = 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Negative Current Sense Threshold (V_{SNSP1} – V_{SNSN1})	V_{SNS_NEG}	CCM Operating Mode (MODE1 = MODE2 = 0V)		–55		mV
MOSFET Gate Drivers						
TG1, TG2 Gate Driver Pull-Up Resistance	R_{TG_PU}			3		Ω
TG1, TG2 Gate Driver Pull-Down Resistance	R_{TG_PD}			1		Ω
BG1, BG2 Gate Driver Pull-Up Resistance	R_{BG_PU}			2.6		Ω
BG1, BG2 Gate Driver Pull-Down Resistance	R_{BG_PD}			1		Ω
TG1, TG2 Rise Time	T_{TG_RISE}	C_{LOAD} = 3300pF (10% to 90%)		30		ns
TG1, TG2 Fall Time	T_{TG_FALL}	C_{LOAD} = 3300pF (10% to 90%)		20		ns
BG1, BG2 Rise Time	T_{BG_RISE}	C_{LOAD} = 3300pF (10% to 90%)		20		ns
BG1, BG2 Fall Time	T_{BG_FALL}	C_{LOAD} = 3300pF (10% to 90%)		25		ns
TG Off to BG On-Delay	T_{TGBG_DEL}	C_{LOAD} = 3300pF		60		ns
BG Off to TG On-Delay	T_{BGTG_DEL}	C_{LOAD} = 3300pF		60		ns
Minimum TG1 On-Time	T_{TG1_ON}	C_{LOAD} = 3300pF		200		ns
Minimum BG2 On-Time	T_{BG2_ON}	C_{LOAD} = 3300pF		100		ns
BST1, BST2 Bias Current	I_{B_BST1}	Top Gate High, V_{BST} – V_{SW} = 10V		6		µA
	I_{B_BST2}	Top Gate High, V_{BST} – V_{SW} = 10V, PassThru Mode		0.6		
BST1, BST2 Charging Current	I_{Q_BST1}	Non-Switching, V_{BST} – V_{SW} = 8.25V		50		µA
	I_{Q_BST2}	Non-Switching, V_{BST} – V_{SW} = 3V		610		
Oscillator						

(Specifications are at T_A = 25°C. V_{IN} = 12V, V_{INP} = 12V, $V_{EN/UVLO}$ = 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Switching Frequency Range	F_{RNG}	RT Set/Synchronized	-40°C ≤ T_J ≤ 125°C	80		400	kHz
Switching Frequency	F_{SW}	RT = 110k	-40°C ≤ T_J ≤ 125°C	91	100	108	kHz
		RT = 39.2k	-40°C ≤ T_J ≤ 125°C	190	200	210	
		RT = 16.9k	-40°C ≤ T_J ≤ 125°C	380	400	420	
SYNC/SPRD Input Low Level	V_{SYNC_LL}	-40°C ≤ T_J ≤ 125°C				0.8	V
SYNC/SPRD Input High Level	V_{SYNC_HL}	-40°C ≤ T_J ≤ 125°C		1.17			V
Spread-Spectrum Max Frequency (% of f_{SW})		$V_{SYNC/SPRD}$ = 3.3V			112.5		%
Spread-Spectrum Min Frequency (% of f_{SW})		$V_{SYNC/SPRD}$ = 3.3V			100		%
Logic Inputs/Outputs							
MODE1, 2 Input Low Level	V_{LL_MODE1} V_{LL_MODE2}	-40°C ≤ T_J ≤ 125°C				0.8	V
MODE1, 2 Input High Level	V_{HL_MODE1} V_{HL_MODE2}	-40°C ≤ T_J ≤ 125°C		1.17			V
MODE1, 2 Leakage Current	$I_{L\_MODE1,2}$	$V_{MODE1,2}$ = 6 V			0.01	1	µA
PWGD Output Low Voltage	V_{PWGD_LV}	I_{PWGD} = 1mA	-40°C ≤ T_J ≤ 125°C		0.07	0.2	V
PWGD Trip Level		V_{FB1} Falling	-40°C ≤ T_J ≤ 125°C	–13	–10	–8	%
		V_{FB2} Rising	-40°C ≤ T_J ≤ 125°C	7.5	10	12	%
PWGD Anti-Glitch Delay		V_{PWGD} Rising or Falling	-40°C ≤ T_J ≤ 125°C	2	10	20	µs
PWGD Leakage Current	I_{LEAK_PWGD}	V_{PWGD} = 40V			0.01	1	µA

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C ([6]), unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
V_{IN}, EN/UVLO Voltage	–40V to 100V
DG Voltage	–40V to 113V
DG – V_{IN} Voltage	–0.3V to 13V
V_{INP}, V_{OUT}, SNSP2, SNSN2 Voltage	–0.3V to 100V
SNSP1 – SNSN1, SNSP2 – SNSN2 Voltage	–0.5V to 0.5V
BST1, BST2 Voltage	–0.3V to 115V
SW1, SW2, SNSP1, SNSN1 Voltage ([4])	100V
BST1 – SW1, BST2 – SW2 Voltage	–0.3V to 15V
BST1 – SNSP1, BST1 – SNSN1 Voltage	–0.3V to 15V
TG1, TG2, BG1, BG2	([2])
$GATEV_{CC}$ Voltage	–0.3V to 15V
$EXTV_{CC}$, PWGD Voltage	–0.3V to 40V
MODE1, MODE2, SYNC/SPRD Voltage	–0.3V to 6V
FB1, FB2, IMON, RT Voltage	–0.3V to 6V
V_{DD}	–0.3V to 6V
V_{C1}, V_{C2}, SS Voltage ([5])	–0.3V to V_{DD}
Operating Junction Temperature LT8210A-1 ([1], [3])	–40°C to 125°C
Storage Temperature Range	–65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

1 The LT8210A-1 is guaranteed to meet performance specifications from -40°C to 125°C junction temperature.

2 Do not apply a voltage or current source to these pins. They must be connected to capacitive load only, otherwise permanent damage may occur.

3 This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature range may impair the device reliability.

4 Negative voltages on the SW1, SW2, SNSP1, and SNSN1 pins are limited, in an application, by the body diodes of the external NMOS devices, MB and MC, or parallel Schottky diodes when present. These pins are tolerant of these negative voltages in excess of one diode drop below ground, guaranteed by design.

5 Do not force voltage on the VC1, VC2, or SS pin.

[6] Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to PCB design and the operating environment. Close attention to PCB thermal design is required.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

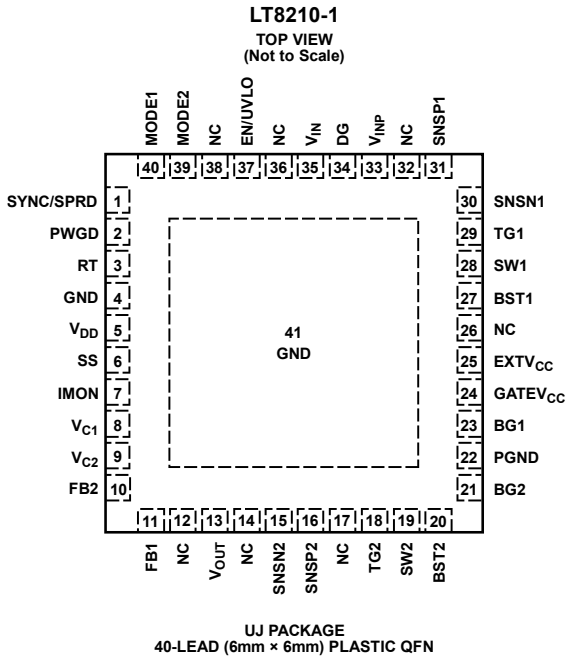


Figure 3. Pin Diagram

Table 3. Pin Descriptions

PIN	NAME	DESCRIPTION
Pin 1	SYNC/SPRD	External Clock Synchronization Input. For external sync, apply a clock signal between 80kHz and 400kHz to this pin. An internal PLL will synchronize the oscillator to the external clock signal. Connect this pin to the V_{DD} pin to enable spread-spectrum operation on the RT set switching frequency; otherwise, connect to ground.
Pin 2	PWGD	Power Good Indicator. Open-drain logic output, which is pulled to ground when the output voltage is outside ±10% of its programmed value or the IMON pin voltage is greater than 1.20V. This pin can be connected to any voltage rail up to 40V through a pull-up resistor. Using either V_{DD} or $GATEV_{CC}$ for the pull-up supply has the advantage that PWGD will be in the correct state when the part is disabled.
Pin 3	RT	Frequency Set Pin. Place a resistor from this pin to GND to set the switching frequency. The range of frequency adjustment is between 80kHz and 400kHz. See *Table 2* in Applications Information section.
Pin 5	V_{DD}	Internally Regulated 3.3V Supply Rail. Bypass this pin to ground with a minimum of a 2.2µF ceramic capacitor. V_{DD} can be used for tying MODE1, MODE2, and SYNC/SPRD pins logic high.
Pin 6	SS	Soft-Start Input. A capacitor to ground at this pin sets the ramp rate of the inductor current at start-up via internal clamping of the V_{C1} and V_{C2} voltages. The SS pin sources 5µA once switching is enabled and is held at ground while switching is disabled.
Pin 7	IMON	Average Current Summing and Sharing Output. Outputs a current proportional to the SNSP2 and SNSN2 differential voltages. Connect this pin to a 11kΩ resistor to ground and to the IMON pins of multiple LT8210-1 for current sharing. An RC filter between IMON pins can resolve noise issues due to local ground voltage variation.
Pin 8	V_{C1}	Error Amplifier Output and Switching Regulator Compensation Point for CCM and DCM Operations. In pass-thru mode, this pin is the compensation point for the boost regulator loop. The current mode comparator trip point increases with this control voltage.
Pin 9	V_{C2}	Error Amplifier Output and Switching Regulator Compensation Point for Buck Loop When in pass-thru mode. The current mode comparator trip point increases with this control voltage. If pass-thru mode is not used, leave V_{C2} floating.
Pin 10	FB2	Error Amplifier Feedback Input for Buck Regulation Loop When in pass-thru mode. Receives the feedback voltage for the buck controller from an external resistive divider across the output. If pass-thru mode is not used, leave this pin floating.
Pin 11	FB1	Error Amplifier Feedback Input for CCM and DCM Operation Modes. Feedback input for the boost regulation loop in pass-thru mode. Receives the feedback voltage from an external resistive divider across the output.

PIN	NAME	DESCRIPTION
Pin 13	V_{OUT}	Output Voltage Sense. This pin must have a Kelvin connection to the drain of switch D. Use a small RC low-pass filter (e.g., 50Ω and 22nF) for improved jitter performance when V_{OUT} ripple is large.
Pins 15, 16	SNSN2, SNSP2	Positive (+) and Negative (–) Inputs for the Average Current Sense Monitor. SNSP2, SNSN2 should connect to the positive and negative terminals of a sense resistor placed in series with the input, output or load. A filter network with a time constant of roughly 1µs should be placed between the sense resistor and the part to filter switching noise.
Pin 18	TG2	Top Gate Drive for Boost Regulator. Drives the top N-channel MOSFET with a voltage swing equal to $GATEV_{CC}$ superimposed onto the SW2 node voltage. When operating in the buck region or within the pass-thru window, TG2 is held roughly at V_{OUT} + $GATEV_{CC}$.
Pin 19	SW2	Boost Regulator Switch Node. The (–) terminal of the bootstrap capacitor connects here.
Pin 20	BST2	Boosted Floating Driver Supply for Boost Regulator. The (+) terminal of the bootstrap capacitor connects here. The BST2 pin swings from roughly $GATEV_{CC}$ to V_{OUT} + $GATEV_{CC}$ when the boost regulation loop is switching. When operating in the buck region or within the pass-thru window, this pin is held roughly at V_{OUT} + $GATEV_{CC}$.
Pin 21	BG2	Bottom Gate Drive for Boost Regulator. Drives bottom N-channel MOSFET with a voltage swing between $GATEV_{CC}$ and PGND.
Pin 22	PGND	Driver Power Ground. Connect to C_{IN}, C_{OUT}, and sources of MOSFETs, M_C, and M_D.
Pin 23	BG1	Bottom Gate Drive for Buck Regulator. Drives bottom N-channel MOSFET with a voltage swing between $GATEV_{CC}$ and PGND.
Pin 24	$GATEV_{CC}$	Power Supply for Gate Drivers. Internally regulated to 10.6V. Bypass this pin to ground with a minimum 4.7µF ceramic capacitor.
Pin 25	$EXTV_{CC}$	External Power Supply Input for the $GATEV_{CC}$ Regulator. $GATEV_{CC}$ will be linearly regulated from $EXTV_{CC}$ if its voltage is higher than 8V and is simultaneously lower than V_{INP}. May be driven with voltages up to 40V. If this feature is not used, connect this pin to ground through a 100k resistor.
Pin 27	BST1	Boosted Floating Driver Supply for Buck Regulator. The (+) terminal of the bootstrap capacitor connects here. The BST1 pin swings from roughly $GATEV_{CC}$ to V_{IN} + $GATEV_{CC}$ when the buck regulation loop is switching. When operating in the boost region or within the pass-thru window, this pin is held roughly at V_{IN} + $GATEV_{CC}$.
Pin 28	SW1	Buck Regulator Switch Node. The (–) terminal of the bootstrap capacitor connects here.
Pin 29	TG1	Top Gate Drive for Buck Regulator. Drives the top N-channel MOSFET with a voltage swing equal to $GATEV_{CC}$ superimposed onto the SW1 node voltage.

PIN	NAME	DESCRIPTION
		When operating in the boost region or within the pass-thru window, TG1 pin is held roughly at V_{IN} + $GATEV_{CC}$ continuously.
Pin 30, 31	SNSN1, SNSP1	Positive (+) and Negative (–) Inputs for the Inductor Current Sense Amplifier. Place an appropriately valued shunt resistor in series with the inductor on the SW1 side and connect to SNSP1 and SNSN1. The SNSP1 – SNSN1 voltage is used for current mode control and reverse current detection.
Pin 33	V_{INP}	Protected Main Input Supply. This pin must connect to the drain terminal of switch A. Use a small RC low-pass filter (e.g., 1Ω and 1µF) for improved jitter performance. When reverse input protection is implemented, connect this pin to the drain of the DG MOSFET; otherwise, connect to V_{IN}.
Pin 34	DG	Reverse Input Protection Gate Drive Output. When V_{IN} is pulled below –1.2V, this pin is clamped internally to V_{IN} with a low resistance switch, forcing an external MOSFET between the V_{IN} and V_{INP} pins into cutoff. In normal operation, this pin is charged to roughly V_{IN} + $GATEV_{CC}$ with an internal charge pump to fully enhance the external MOSFET. DG can tolerate negative voltages down to –40V.
Pin 35	V_{IN}	Input Voltage Pin. This pin is used for powering the start-up circuitry and the internal charge pump. V_{IN} can withstand negative voltages down to –40V without damaging the regulator or drawing large currents.
Pin 37	EN/UVLO	Precision Enable Input. The part is enabled when this pin is pulled above 1.45V. A voltage below 1.35V causes the LT8210-1 to reside in a low-power shutdown mode. Tie to V_{IN} for always-on operation. Connect to a resistor divider between V_{IN} and ground to set an undervoltage lockout threshold. EN/UVLO can tolerate negative voltages up to 40V.
Pin 39	MODE2	Operating Mode Selection Input #2. Used in conjunction with the MODE1 pin to select between continuous conduction switching (CCM), discontinuous switching (DCM), and pass-thru operating modes. See *Table 1* in the Operation section for mode pin settings.
Pin 40	MODE1	Operating Mode Selection Input #1. Used in conjunction with MODE2 pin to select between continuous conduction switching (CCM), discontinuous switching (DCM), and pass-thru operating modes. See *Table 1* in the Operation section for mode pin settings.
Pin 41/Exposed Pad	GND	Signal Ground. All small-signal components and compensation components should connect to this ground, which in turn connects to the PCB ground at one location away from high currents and switching noise. The exposed pad must be soldered to the PCB and connected to the GND pin using top layer metal.

BLOCK DIAGRAM

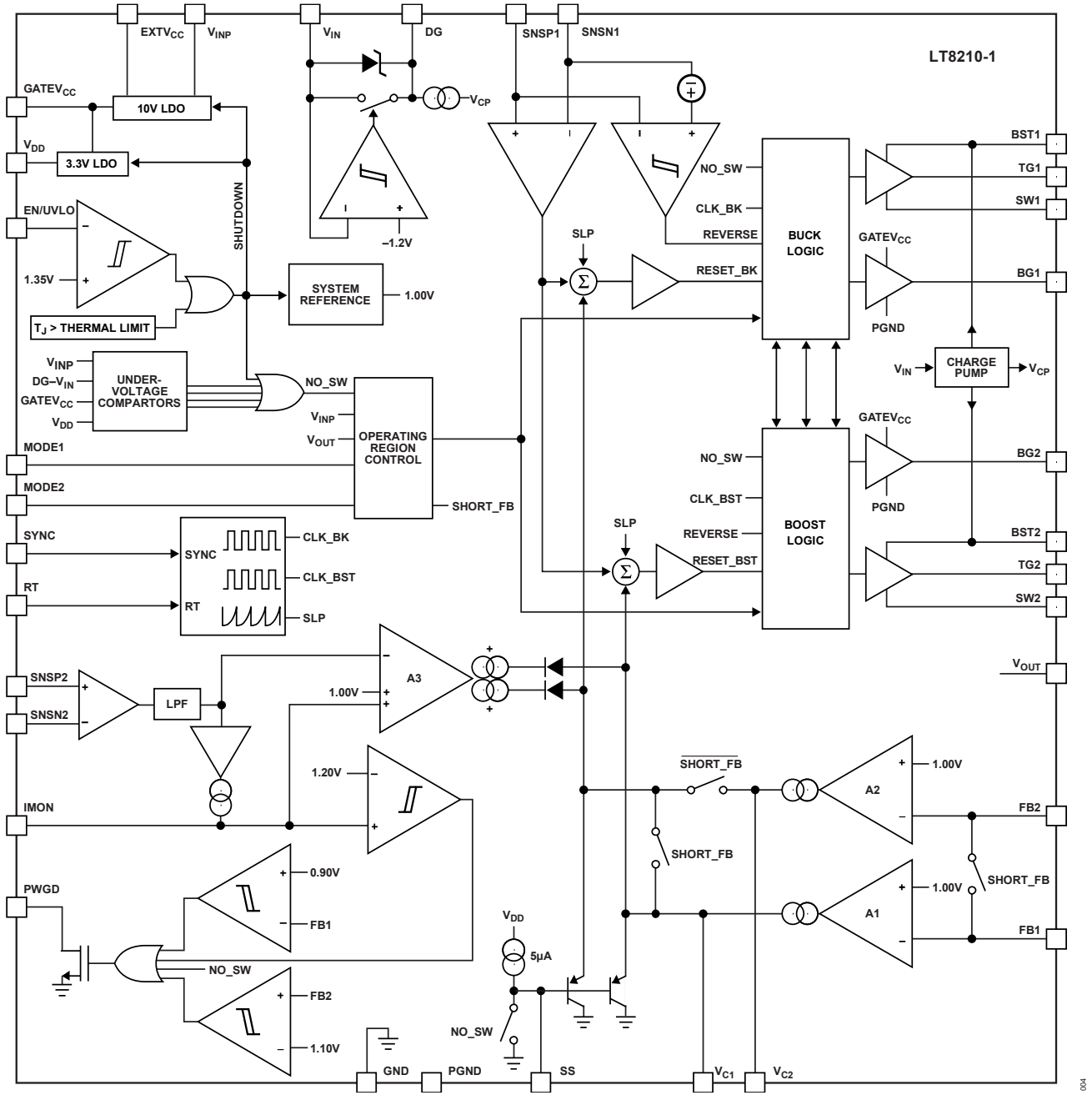


Figure 4. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

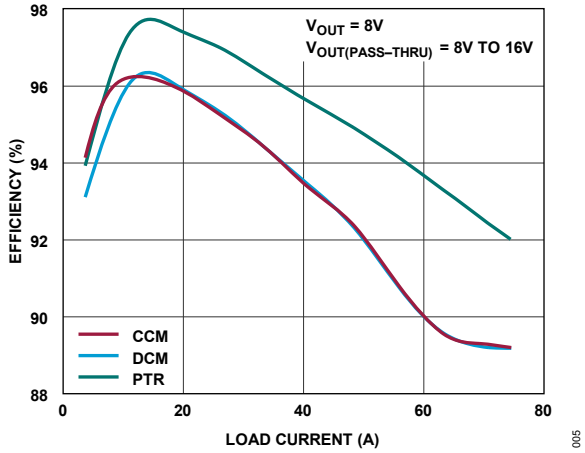


Figure 5. Efficiency vs. Load Current (V_{IN} = 6V – Figure 79)

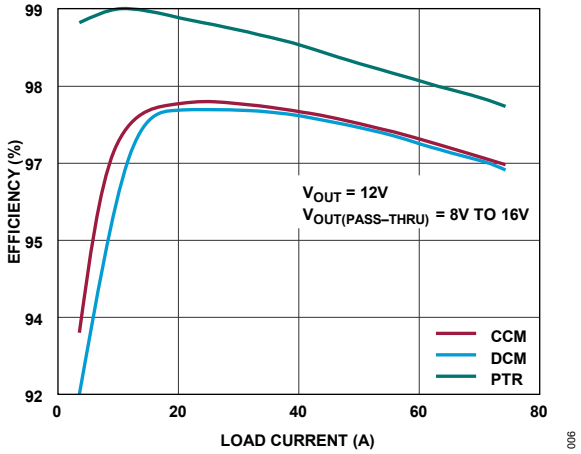


Figure 6. Efficiency vs. Load Current (V_{IN} = 12V – Figure 79)

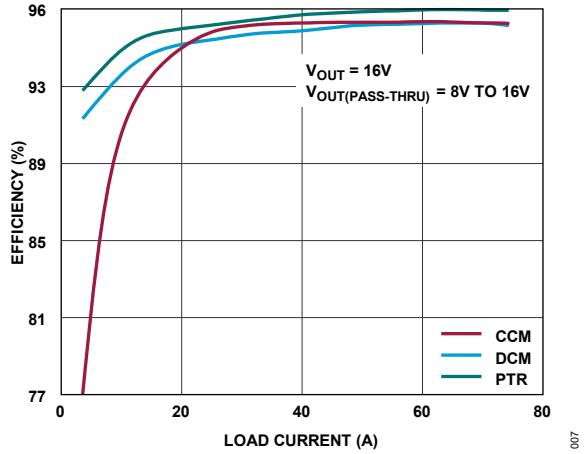


Figure 7. Efficiency vs. Load Current (V_{IN} = 36V – Figure 79)

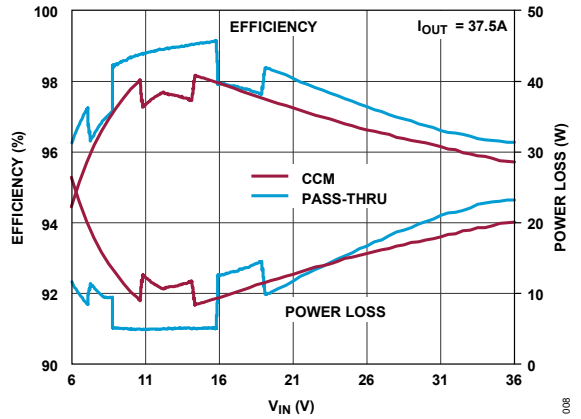


Figure 8. Efficiency and Power Loss vs. Input Voltage (Figure 79)

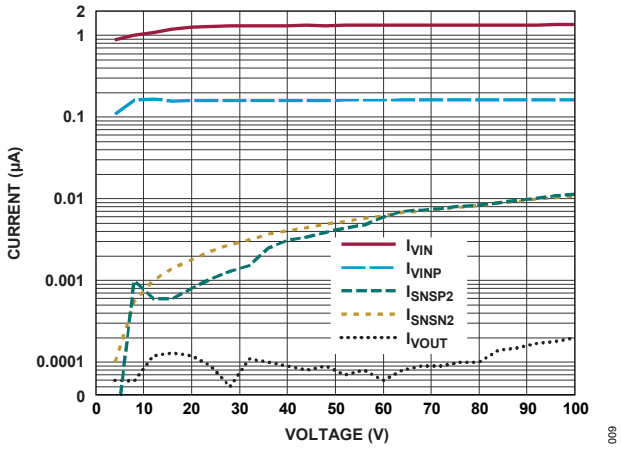


Figure 9. Shutdown Currents vs. Voltage

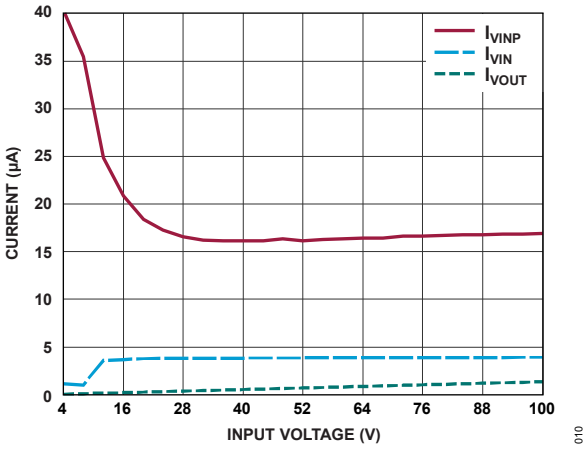


Figure 10. Pass-Thru Non-Switching Currents vs. Input Voltage

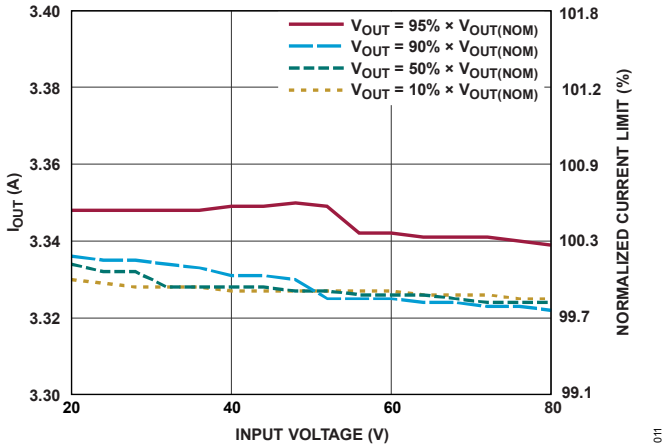


Figure 11. IMON Current Limit vs. Input Voltage (Figure 79)

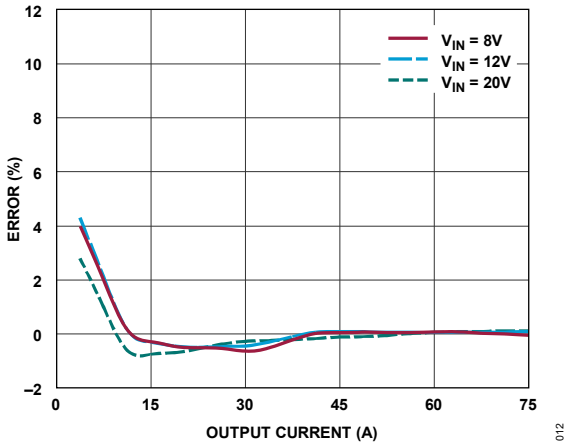


Figure 12. IMON Measurement Accuracy (Figure 79): V_{IN} = 8V, DCM

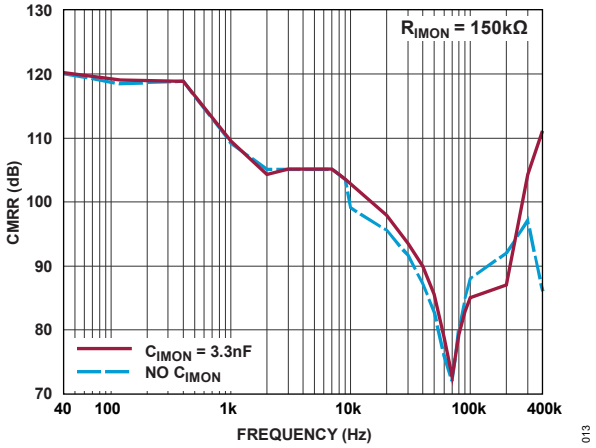


Figure 13. IMON CMRR vs. Frequency

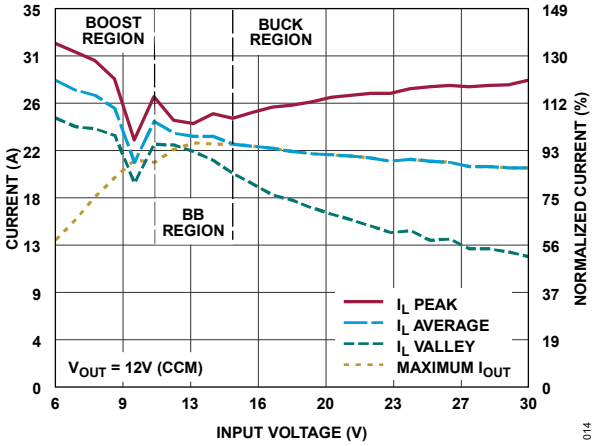


Figure 14. Maximum Inductor Current: $f_{SW} = f_{SW}$ (Optimal) (Figure 79)

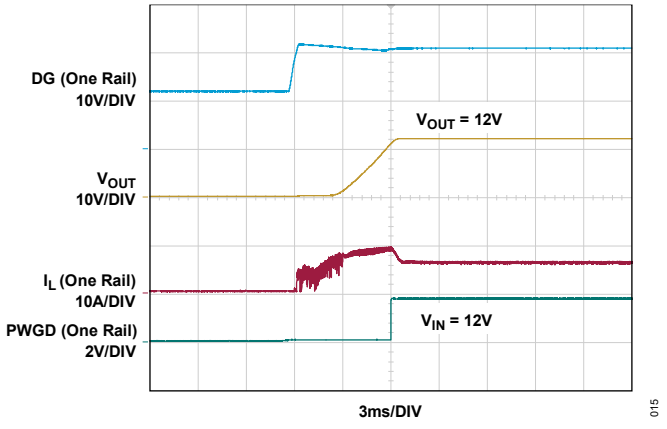


Figure 15. Start-Up (CCM Mode – Figure 79), 22.5A Load

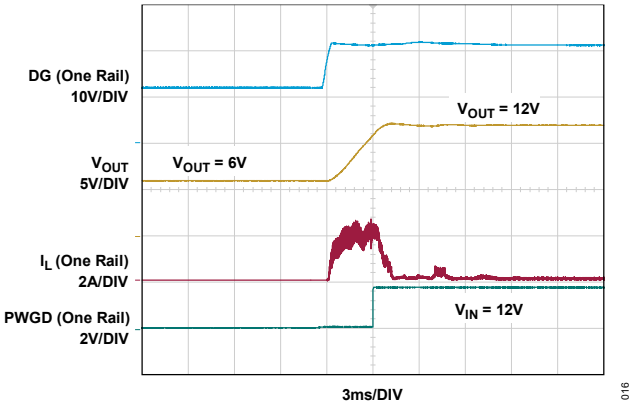


Figure 16. Pre-Biased Output Start-Up (CCM Mode – Figure 79)

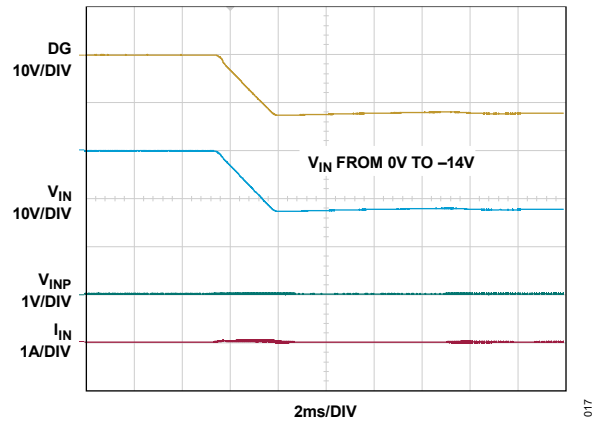


Figure 17. Static Reverse Input Protection (Figure 79)

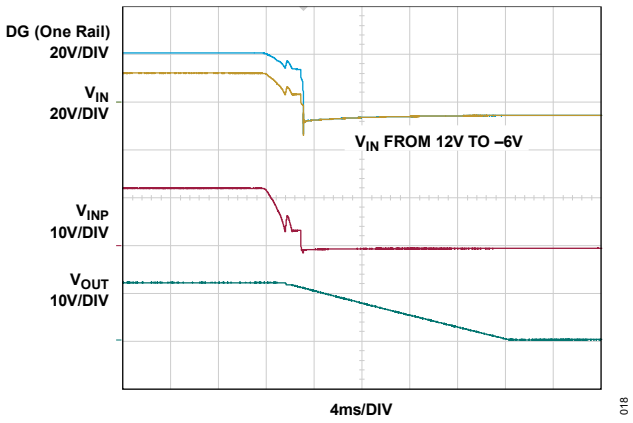


Figure 18. Dynamic Reverse Input Protection (Figure 79)

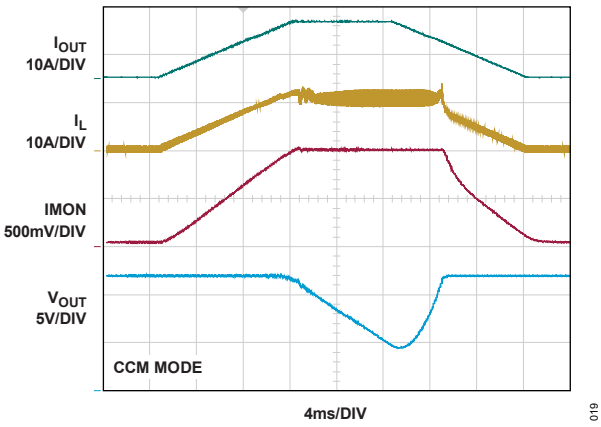


Figure 19. Transition to Current Regulation (Figure 79)

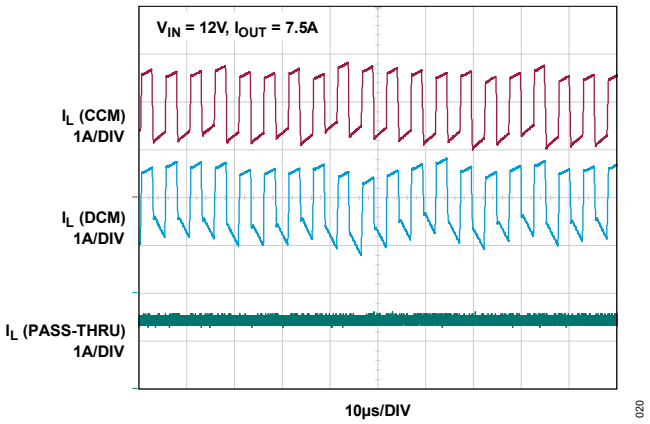


Figure 20. Inductor Current at Light Load (Figure 79)

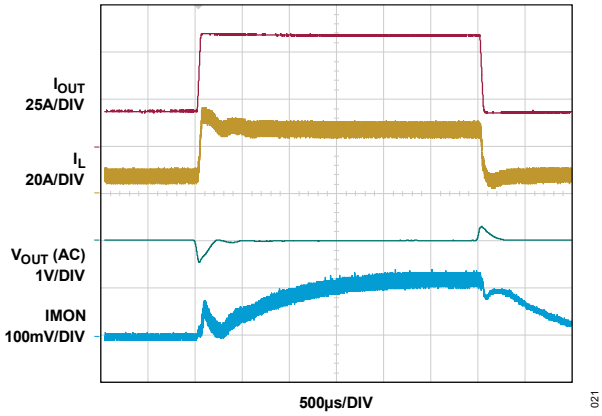


Figure 21. Load Step (Boost Region – Figure 79), 18.75A to 60A, V_{IN} = 7V, V_{OUT} = 12V, CCM

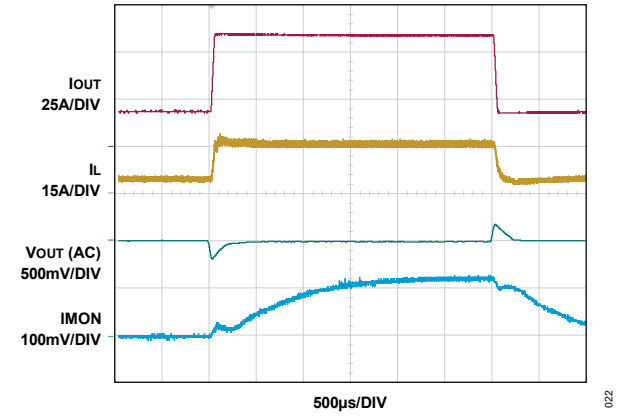


Figure 22. Load Step (Buck-Boost Region – Figure 79), 18.75A to 60A, V_{IN} = 12V, V_{OUT} = 12V, CCM

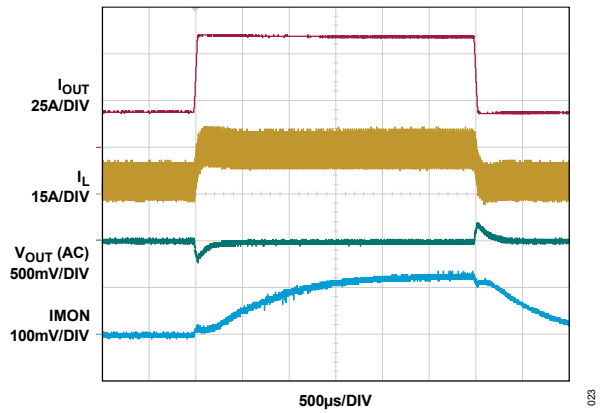


Figure 23. Load Step (Buck Region – Figure 79), 18.75A to 60A, V_{IN} = 24V, V_{OUT} = 12V, CCM

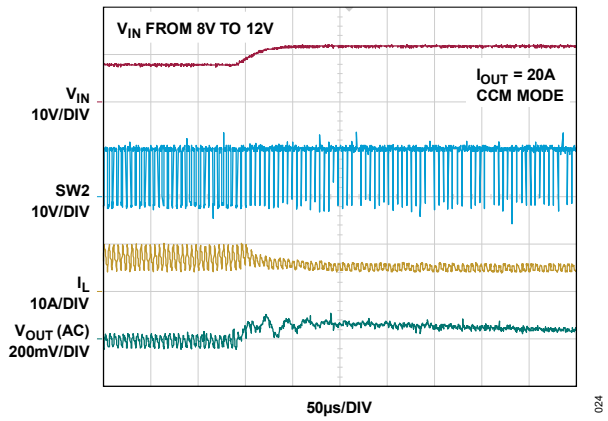


Figure 24. Line Step (Boost Region – Figure 79)

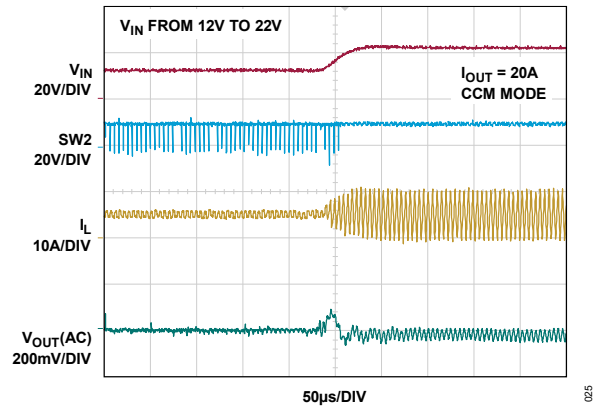


Figure 25. Line Step (Buck-Boost Region – Figure 79)

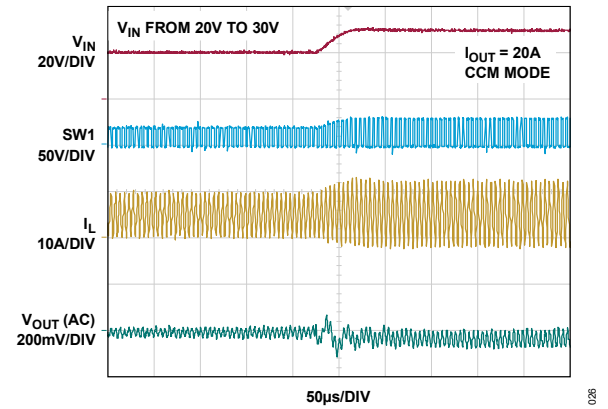


Figure 26. Line Step (Buck Region – Figure 79)

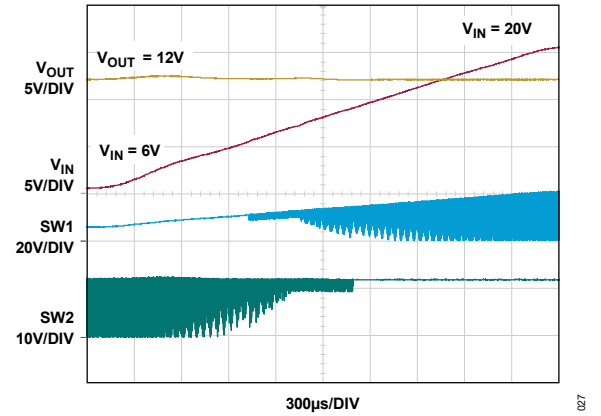


Figure 27. Input Voltage Sweep (CCM Mode – Figure 79), 37.5A Load

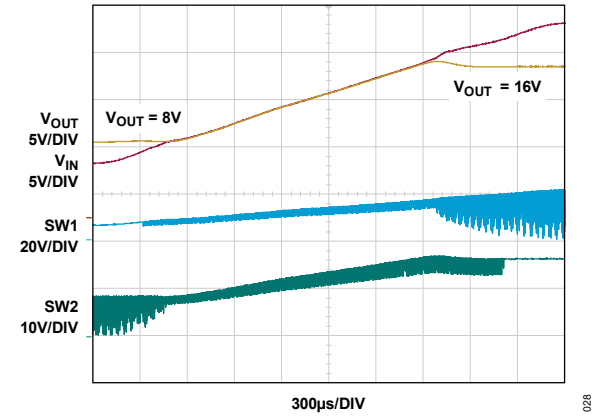


Figure 28. Input Voltage Sweep (Pass-Thru – Figure 79), 37.5A Load

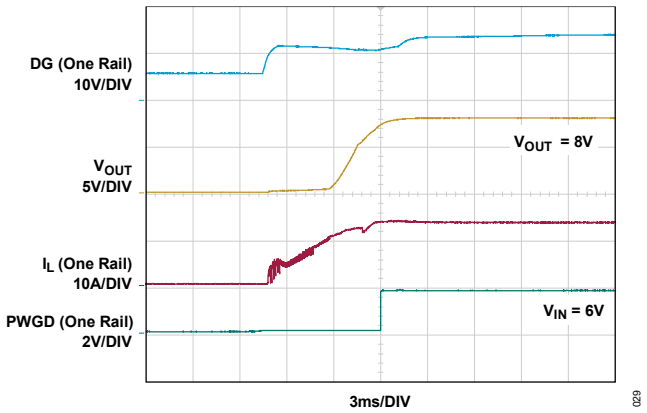


Figure 29. Pass-Thru Start-Up: V_{IN} Below Pass-Thru Window (Figure 79)

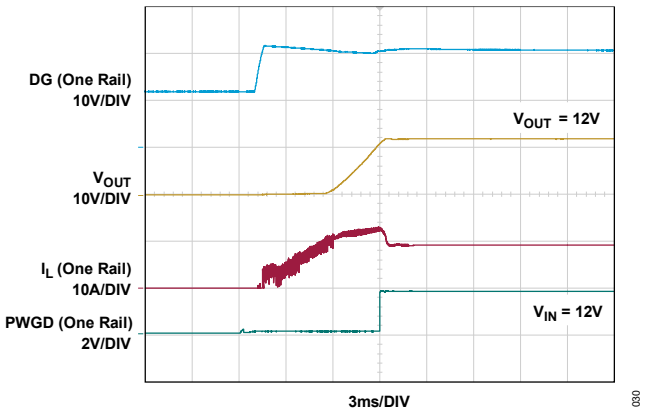


Figure 30. Pass-Thru Start-Up: V_{IN} in Pass-Thru Window (Figure 79)

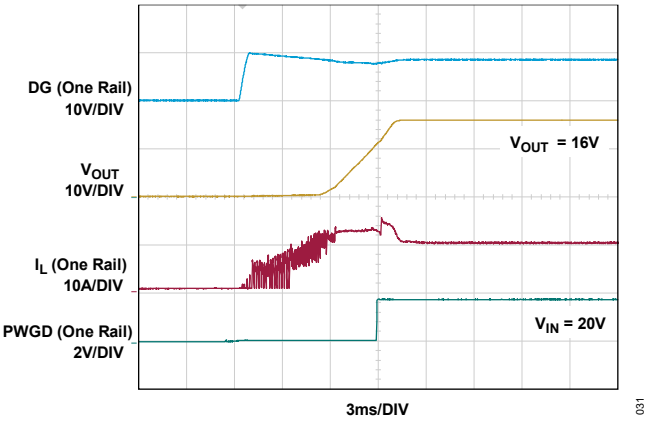


Figure 31. Pass-Thru Start-Up: V_{IN} above Pass-Thru Window (Figure 79)

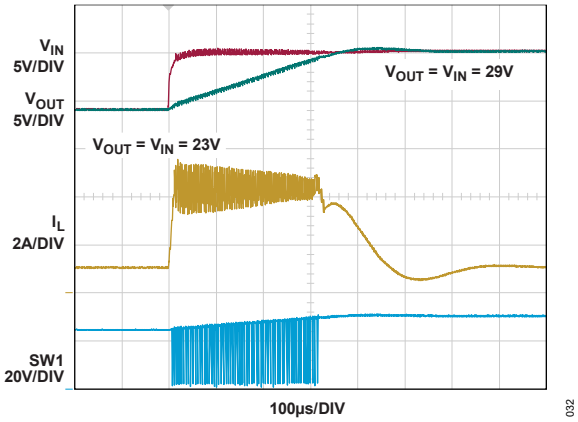


Figure 32. Pass-Thru Line Step (Figure 79)

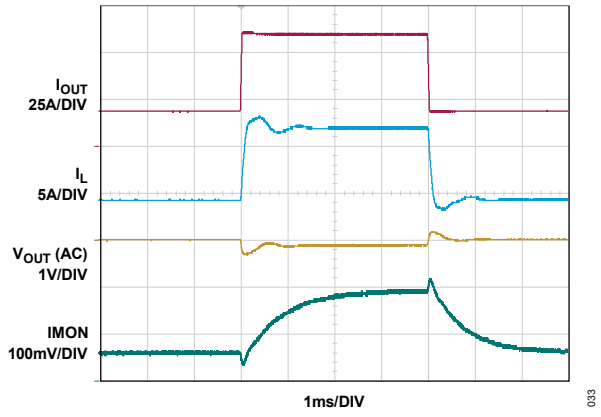


Figure 33. Pass-Thru Load Step (Figure 79)

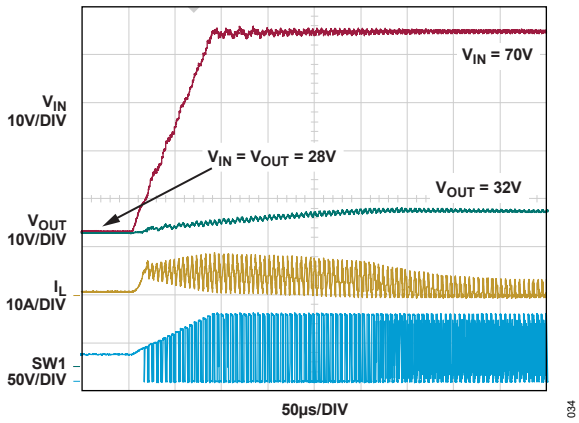


Figure 34. Pass-Thru Positive Surge (Figure 79)

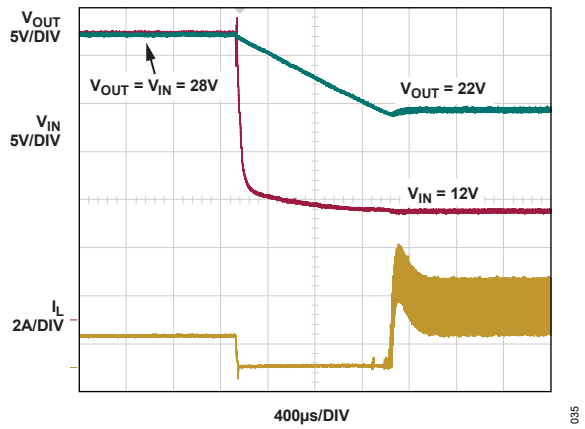


Figure 35. Pass-Thru Negative Surge (Figure 79)

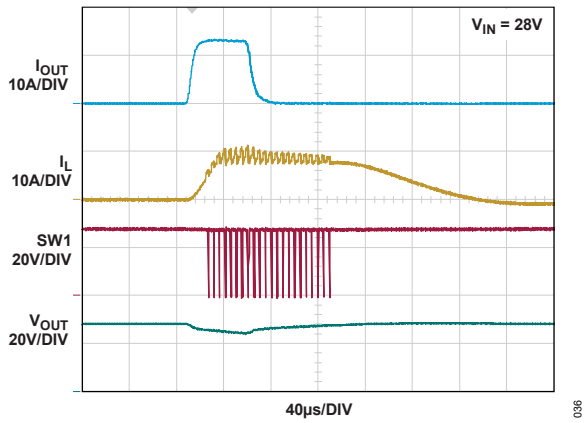


Figure 36. Pass-Thru Current Limit (Figure 79)

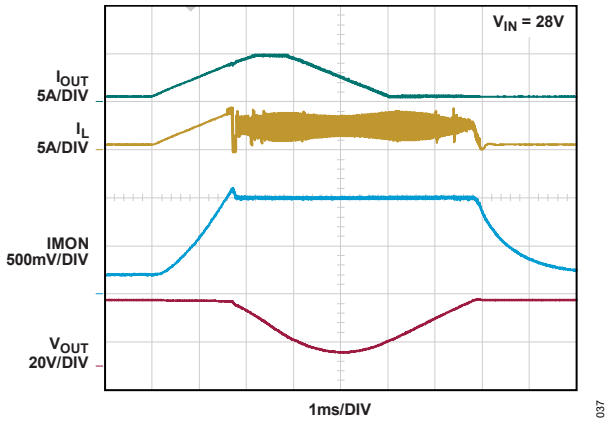


Figure 37. Pass-Thru IMON Limit (Figure 79)

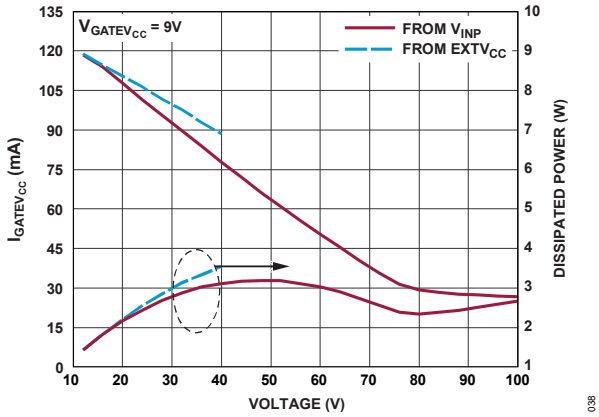


Figure 38. GATEV$_{CC}$ Max Current vs. Voltage

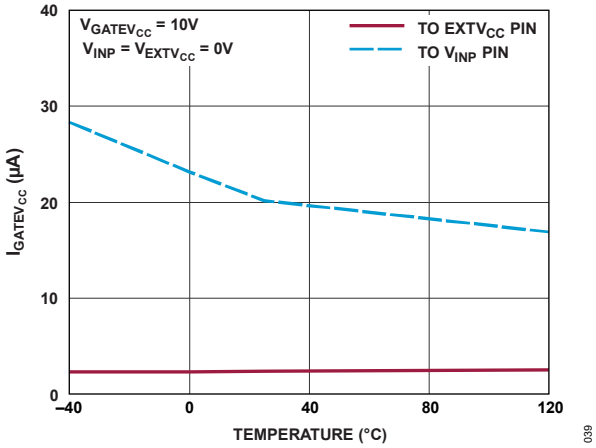


Figure 39. GATEV$_{CC}$ Backdrive Current

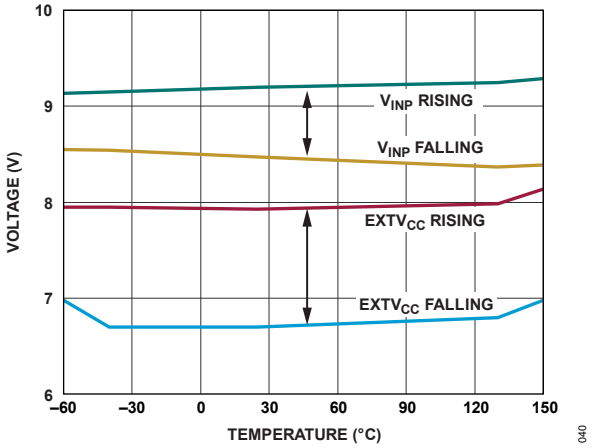


Figure 40. EXTV$_{CC}$, V$_{INP}$, Switchover Thresholds for GATEV$_{CC}$ Regulation

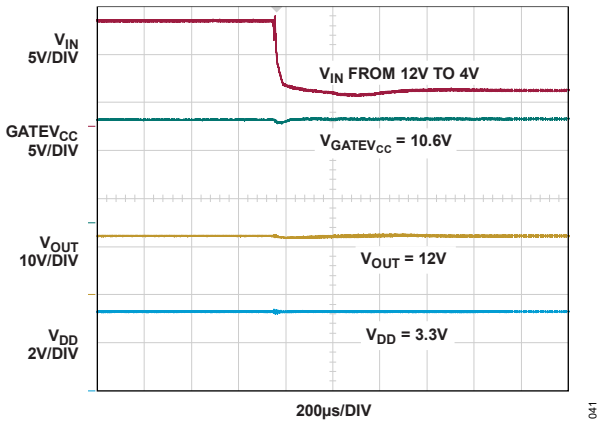


Figure 41. $GATEV_{CC}$ Response to Input Brownout ($EXTV_{CC}$ = 12V)

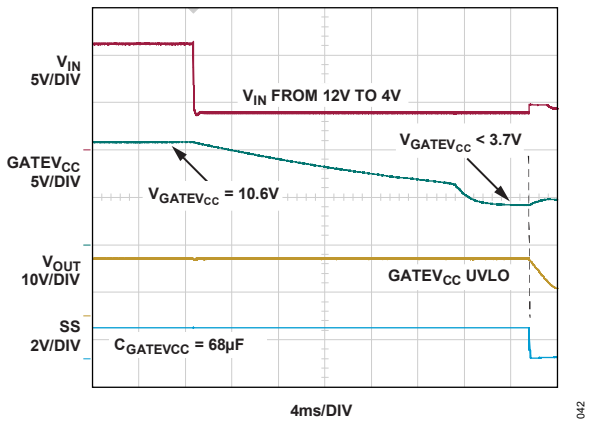


Figure 42. $GATEV_{CC}$ Response to Input Brownout ($EXTV_{CC}$ = 0V)

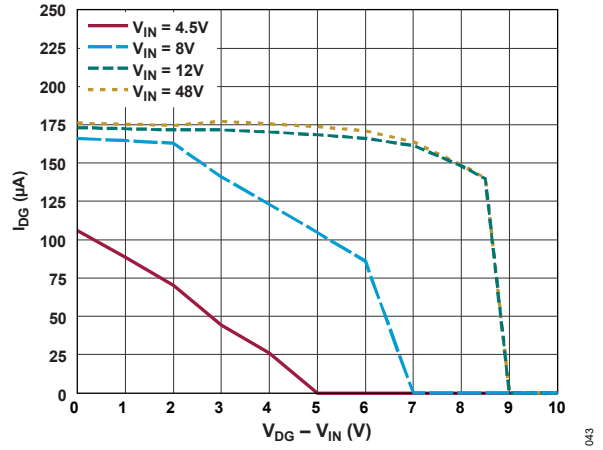


Figure 43. DG Pin Charging Current vs. Voltage

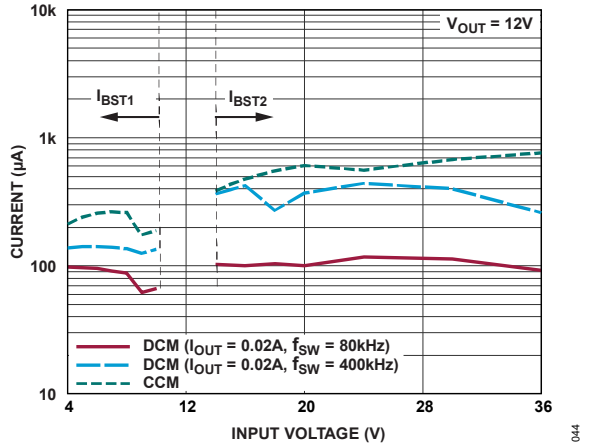


Figure 44. BST1, BST2 Average Charging Current for Non-Switching Channel

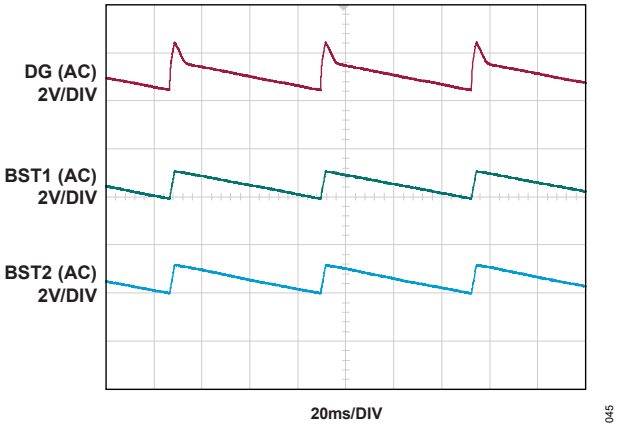


Figure 45. DG, BST1, BST2 Charging in Pass-Thru (Figure 79)

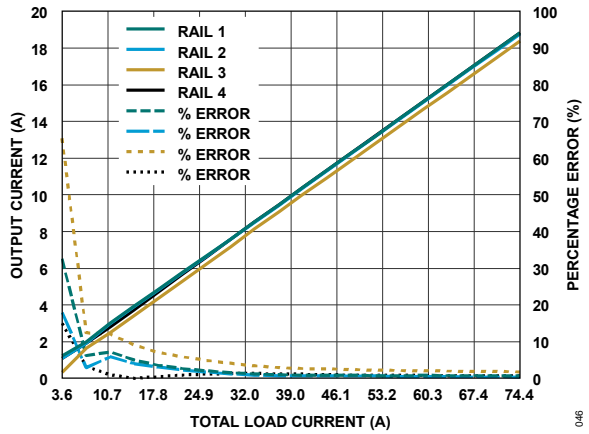


Figure 46. Current Sharing, $12V_{IN}$, CCM

THEORY OF OPERATION

See *Figure 4* when reading the following sections about the operation of the LT8210-1.

Overview

The LT8210-1 has three operating modes that can be selected by setting the MODE1 and MODE2 pins either high (> 1.17V) or low (< 0.80V). The threshold voltages of the MODE1 and MODE2 pins allow them to be driven with 1.8V, 2.5V, 3.3V or 5V logic levels for dynamic control. If the operating mode is fixed, tie the MODE1 and MODE 2 pins to V_{DD} to set high or to ground to set low.

Table 4 shows the operating mode corresponding to the various MODE1 and MODE2 pin combinations. In continuous conduction mode (CCM) and discontinuous conduction mode (DCM) operation, the LT8210-1 operates as a conventional buck-boost controller with the output regulated to a voltage set by the resistive divider between V_{OUT}, FB1, and GND. In pass-thru mode, the output voltage is regulated to a window defined by a minimum and maximum value programmed using the FB1 and FB2 resistor dividers, respectively.

Table 4. LT8210-1 Operating Modes

MODE2	MODE1	OPERATING MODE
LOW	LOW	Continuous Conduction Mode (CCM)
LOW	HIGH	Discontinuous Conduction Mode (DCM)
HIGH	LOW	Do Not Use
HIGH	HIGH	Pass-Thru Mode

Continuous Conduction Mode (CCM)

Continuous conduction mode allows the inductor current to reverse directions once the voltage at the SS pin has exceeded 2.5V (typical). This precaution is intended to prevent large negative inductor currents during start-up when the output is pre-biased to a non-zero voltage. Once CCM mode is enabled, a negative current sense limit with a magnitude roughly equal to the positive current sense limit sets the lower bound on the inductor current. This ensures that the inductor current is limited on a cycle-by-cycle basis, whether the direction of current flow is forward or reverse. The maximum recommended switching frequency for CCM operation is 350kHz.

Discontinuous Conduction Mode (DCM)

Discontinuous conduction mode prevents the inductor current from reversing direction at low output currents. DCM operation improves light load efficiency and also blocks significant current draw from the output back into the input. Reverse current is detected when the SNSP1 – SNSN1 voltage drops below its reverse current threshold while either switch B or D is conducted. When operating in either the buck or buck-boost regions, the on-time of switch B ends upon reverse current detection. Similarly, in the boost and buck-boost regions, the on-time of switch D ends when reverse inductor current is detected. At very light loads, the LT8210-1 may be forced to skip multiple switching pulses to maintain output voltage regulation in DCM. This situation arises when the average inductor current exceeds the load current even while switching at duty cycle limits. If pulse-skipping behavior is undesired, it may be possible to resolve it by increasing the size of the inductor or reducing the switching frequency. Otherwise, the LT8210-1 can be operated in CCM for full switching frequency operation.

Pass-Thru Mode

In pass-thru mode, the respective output voltages for the buck and boost loops, $V_{OUT(BUCK)}$ and $V_{OUT(BOOST)}$, are programmed independently. The output voltage is regulated to a window defined by a minimum at $V_{OUT(BOOST)}$ and a maximum at $V_{OUT(BUCK)}$. $V_{OUT(BUCK)}$ is set with a resistive divider between V_{OUT}, FB2, and GND. The FB2 voltage is compared with the 1.00V system reference, and the resulting output of amplifier A2, V_{C2}, controls the inductor current when the buck loop is active. Similarly, $V_{OUT(BOOST)}$ is set with a resistive divider between V_{OUT}, FB1, and GND. The voltage on FB1 is compared with the 1.00V system reference using amplifier A1, and the resulting output on the V_{C1} pin controls the inductor current when the boost loop is active. The boost loop will control the inductor current and regulate the output to $V_{OUT(BOOST)}$ when V_{INP} is less than or equal to $V_{OUT(BOOST)}$. Likewise, when the input voltage is greater than or equal to $V_{OUT(BUCK)}$, the buck loop will control the inductor current and regulate the output to $V_{OUT(BUCK)}$. Near the boundaries of the pass-thru window, interleaved buck-boost switching is used to avoid pulse-skipping.

When the input is between $V_{OUT(BOOST)}$ and $V_{OUT(BUCK)}$, both top switches will turn on continuously once V_{OUT} has settled close in value to V_{INP}. In this state, V_{OUT} follows V_{INP}, and the LT8210-1 enters a power saving mode with typical quiescent currents on the V_{IN} and V_{INP} pins of 4µA and 18µA, respectively. Switching will recommence if the SNSP1 – SNSN1 voltage exceeds 63mV (typical) to limit the maximum inductor current. Similarly, if a current regulation loop is implemented, switching will resume when the IMON pin voltage approaches 1.01V. With no switching losses and an extremely low quiescent current, it is possible to achieve efficiencies greater than 99.9% in the pass-thru region.

Power Switch Control (CCM, DCM Operation)

The LT8210-1 is a current mode buck-boost controller that regulates the output voltage above, equal to, or below the input voltage. The LTC® proprietary topology and control architecture employs a current-sensing resistor in series with the inductor that is used for current mode control and provides clean transitions between buck, buck-boost, and boost switching regions. When the LT8210-1 is configured for CCM or DCM operation, the inductor current is controlled by the voltage on the V_{C1} pin. If a current regulation loop is implemented, then the V_{C1} voltage will be controlled by either the sensed feedback voltage (FB1) or the sensed current when the IMON pin voltage approaches 1.01V. *Figure 47* shows a simplified diagram of how the power switches A, B, C, and D are connected to the inductor L, the current sense resistor R_{SENSE}, the power input V_{INP}, the power output V_{OUT}, and ground. Switches A and B form the synchronous buck power stage, while switches C and D form the synchronous boost power stage. The current sense resistor R_{SENSE} is connected to the SNSP1 and SNSN1 pins and provides the inductor current information for both current mode control and reverse current detection. *Figure 48* shows the switching region as a function of the V_{INP}/V_{OUT} ratio. The power switches are controlled to smoothly transition between switching regions, with hysteresis added to prevent chattering between modes.

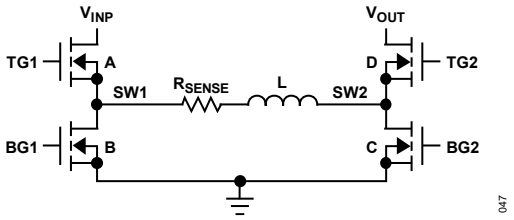


Figure 47. Simplified Diagram of the Power Switches

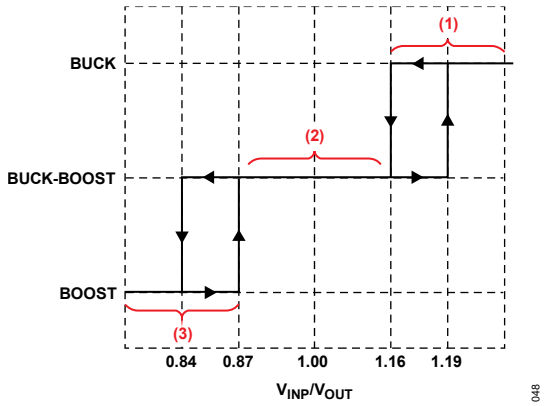


Figure 48. Switching Region vs. V_{INP}/V_{OUT} Ratio

Power Switch Control: Buck Region (V_{INP} > 1.19 • V_{OUT})

When V_{INP} is greater than V_{OUT} by 19% (typical) or more, the part will run in the buck region. In the buck region, switch D is always on while switch C is always off. Switches A and B will toggle on and off, acting as a synchronous buck regulator. If the inductor current drops below the reverse current sense threshold in DCM or the negative current sense threshold in CCM, switch B will be turned off for the remainder of the switching cycle, preventing the inductor current from falling any further. See *Figure 49*.

Power Switch Control: Boost Region (V_{INP} < 0.84 • V_{OUT})

When V_{INP} is less than V_{OUT} by more than 16%, the part will run in the boost region. In this region, switch A is always on while switch B is always off. Switches C and D will toggle on and off, acting as a synchronous boost regulator. The on-time of switch D will be terminated if the inductor current drops below the reverse current sense threshold in DCM or the negative current sense threshold in CCM. See *Figure 50*.

Power Switch Control: Buck-Boost Region (0.84 • V_{OUT} < V_{INP} < 1.19 • V_{OUT})

When V_{INP} is within –16% to +19% of V_{OUT}, the part operates in the buck-boost region, where all four power switches (A, B, C, and D) are active. The buck-boost region can be thought of as an over-lapping of the buck and boost control regions where the buck and boost regulation loops both control the inductor current. The sharing of inductor current control between the buck and boost loops avoids abrupt handoffs within the buck-boost region that can perturb the inductor current and output voltage. The on-time of switches B and D will be terminated if the inductor current drops below the reverse current sense threshold in DCM or the negative current sense threshold in CCM. See *Figure 51*.

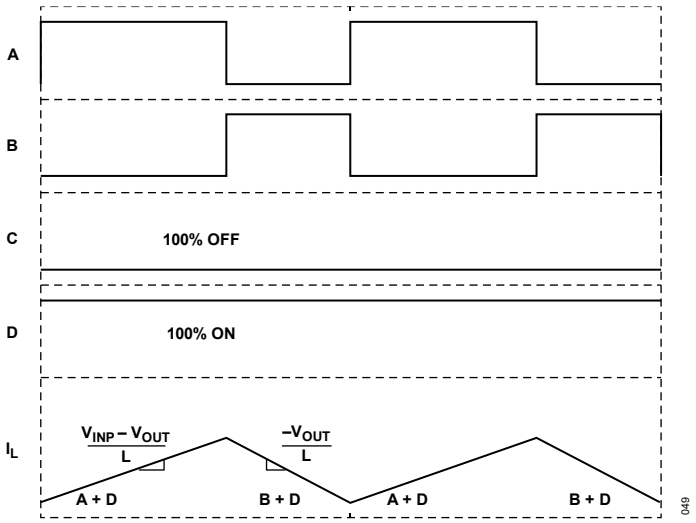


Figure 49. Buck Region Switching Waveforms

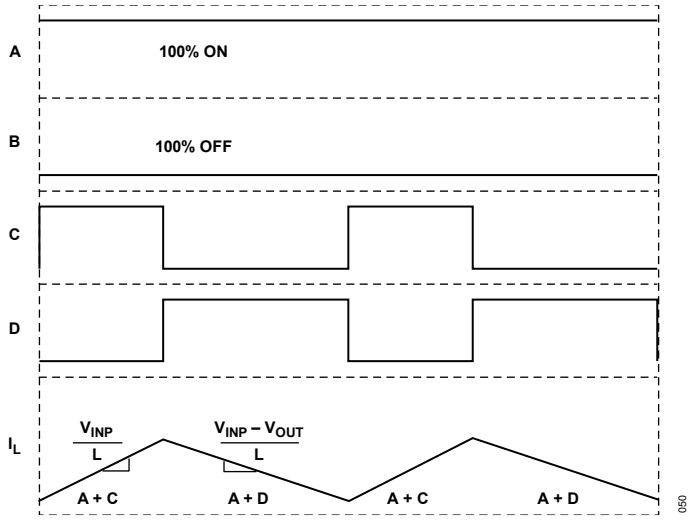


Figure 50. Boost Region Switching Waveforms

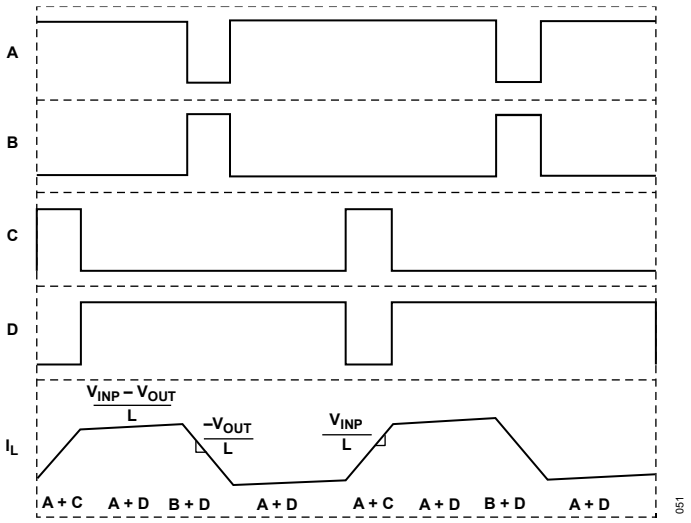


Figure 51. Buck-Boost Region Switching Waveforms

Power Switch Control (Pass-Thru Mode)

In pass-thru mode, the buck and boost regulation loops function independently after start-up. Separate error amps are used to create a pass-thru window by setting the output voltage for the buck regulation, $V_{OUT(BUCK)}$, higher than the programmed output voltage for boost regulation, $V_{OUT(BOOST)}$. *Figure 52* shows the switching regions in pass-thru mode versus input voltage.

When V_{INP} >> $V_{OUT(BUCK)}$, the LT8210-1 operates in the buck region. In this region, switch D is always on while switch C is always off, switches A and B will toggle on and off, acting as a synchronous buck regulator with the output at $V_{OUT(BUCK)}$. When V_{IN} is between 93% to 119% of $V_{OUT(BUCK)}$, switch D will also begin switching to avoid the need for pulse skipping. Switch C will alternate with D in this region. When V_{INP} << $V_{OUT(BOOST)}$ switch A is always on while switch B is always off, switches C and D toggle on and off, acting as a synchronous boost regulator to maintain the output at $V_{OUT(BOOST)}$. When V_{IN} is between 84% to 107% of $V_{OUT(BOOST)}$, switch A will also begin switching, alternating with switch B. When V_{INP} is between $V_{OUT(BOOST)}$ and $V_{OUT(BUCK)}$, the output voltage will track the input. Once V_{OUT} has settled close to V_{INP}, the LT8210-1 will enter a low power state where switches A and D are turned on continuously and switches B and C are off. In pass-thru mode, reverse current is handled in a similar manner to DCM while switching. In the non-switching state, reverse-current is detected through direct comparison of the V_{INP} and V_{OUT} voltages. If the voltage on V_{OUT} exceeds that on V_{INP} by a set percentage, switches A, C, and D are turned off and the output is only reconnected after it has discharged to be nearly equal to V_{INP}. If a positive line transient occurs while in the non-switching pass-thru window causing V_{INP} to exceed V_{OUT} by a set percentage, switching will recommence to prevent large amplitude ringing in the inductor current. The output will be driven to the input voltage in a manner similar to soft-start and switches A and D will turn on continuously again after V_{OUT} settles close to V_{INP}.

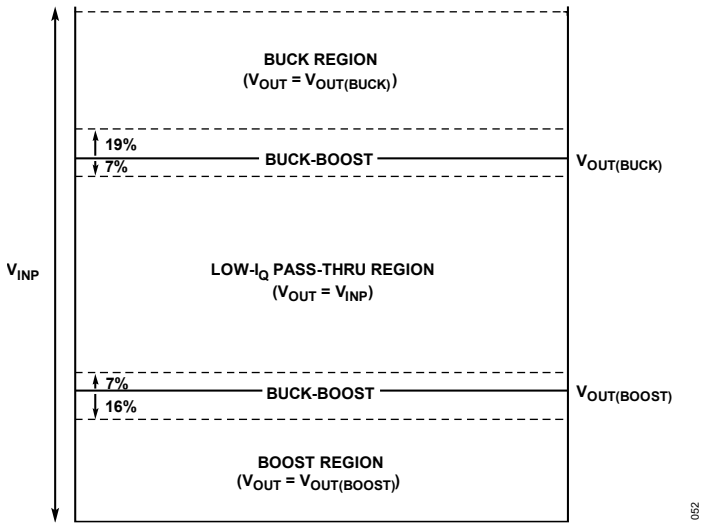


Figure 52. Pass-Thru Regions vs. V_{INP}

Transitioning Between Operating Modes

It is possible to dynamically transition between pass-thru mode and CCM or DCM operation by toggling the MODE1 and/or MODE2 pins. While in CCM or DCM operation, the FB1 and FB2 pins are internally connected with a low resistance switch. In pass-thru mode, this switch is disabled after start-up, allowing the feedback pins to move independently. When exiting pass-thru mode, the FB1 and FB2 pins will once again be connected. By scaling the relative magnitudes of R_{2B}, R_{2A}, R_{1B}, and R_{1A} resistors, the fixed output voltage in CCM or DCM operation can be placed at any desired voltage between the $V_{OUT(BUCK)}$ and $V_{OUT(BOOST)}$ voltages that define the top and bottom of the pass-thru window (*Figure 53*). Cycling into and out of pass-thru mode allows the user to exchange a wider output voltage tolerance for no switching losses or noise as the conditions in the application change.

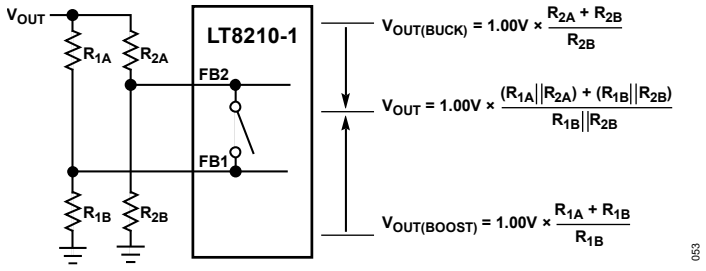


Figure 53. Output Voltage when Exiting Pass-Thru Mode

Enable and Start-Up

The LT8210-1 start-up sequence is shown in *Figure 54*.

When the voltage on the EN/UVLO pin is less than the turn-on threshold (typically 1.45V), the LT8210-1 is in a low power shutdown mode where the internal $GATEV_{CC}$ and V_{DD} regulators are disabled, and the quiescent current of the V_{IN} and V_{INP} pins drops to approximately 1µA. When the EN/UVLO voltage is pulled above 1.45V, the $GATEV_{CC}$ and V_{DD} regulators are activated. After both the $GATEV_{CC}$ and V_{DD} voltages have risen beyond their undervoltage lockout thresholds (typical values of 3.95V and 2.94V, respectively), the internal charge pump will begin sourcing current from

the DG pin. When the DG to V_{IN} voltage is charged to greater than 2.8V (typical), the switching control logic is initialized. A brief delay allows analog circuitry to settle prior to start-up, after which a 5µA current is sourced from the SS pin, initiating the soft-start ramp. The LT8210-1 begins switching. Connect EN/UVLO to V_{IN} for always-on operation or to a resistive divider between V_{IN} and ground to program an undervoltage lockout (UVLO) threshold.

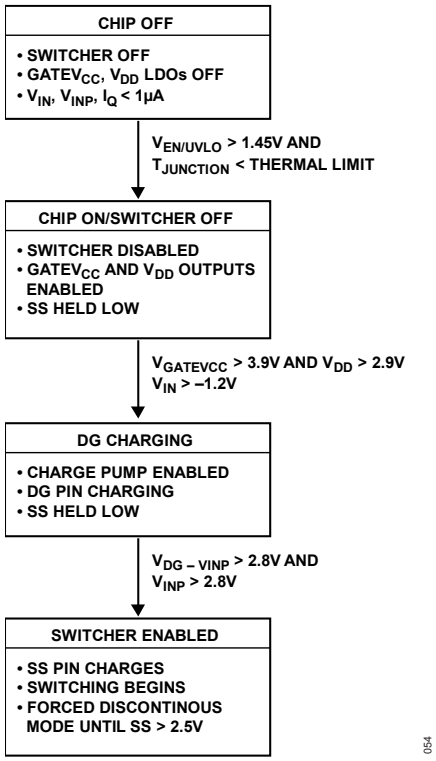


Figure 54. Start-Up Sequence

EXTV$_{CC}$/GATEV$_{CC}$/V$_{DD}$ Power Supplies

Power for the TG1, BG1, TG2, and BG2 MOSFET drivers and the internal V_{DD} regulator are derived from $GATEV_{CC}$. The $GATEV_{CC}$ supply is linearly regulated to 10.6V (typical) from PMOS low dropout regulators powered by either the V_{INP} or $EXTV_{CC}$ pins. When the voltage on $EXTV_{CC}$ exceeds 8V (typical) and is simultaneously lower than V_{INP}, $GATEV_{CC}$ will be regulated from $EXTV_{CC}$. The internal comparison between $EXTV_{CC}$ and V_{INP} causes the LT8210-1 to regulate $GATEV_{CC}$ from the lower of these two voltages, minimizing power dissipation. This allows the $EXTV_{CC}$ pin to maintain $GATEV_{CC}$ above 10V during an input brownout condition. If $EXTV_{CC}$ is not used, connect to ground through a 100k resistor. The $GATEV_{CC}$ regulator has built-in backdrive protection should the input momentarily drop below the $GATEV_{CC}$ voltage to avoid discharging the bypass capacitor and resetting the part. The LT8210-1 operates normally while both the V_{INP} and $GATEV_{CC}$ voltages remain above their undervoltage lockout (UVLO) thresholds, typically 2.7V and 3.7V, respectively. The $GATEV_{CC}$ regulator is current limited in order to prevent excessive power dissipation and possible damage. This current limit decreases linearly at higher voltages, effectively clamping the internal power dissipation at 3W (typical). *Figure 55* shows the typical $GATEV_{CC}$ current limit as a function of voltage on the V_{INP} and $EXTV_{CC}$ pins. The lower current limit at higher voltages restricts the amount of gate drive current that the LT8210-1 can provide and should be considered when selecting the power MOSFETs and the switching frequency. The V_{DD} voltage is linearly regulated to 3.3V from $GATEV_{CC}$ and powers the low voltage circuitry within the LT8210-1. It should be bypassed with a minimum of a 2.2µF capacitor to the ground and placed close to the pin. V_{DD} is a good choice for tying logic pins

high (e.g., MODE1, MODE2, and SYNC/SPRD) and as the pull-up supply for the PWGD pin. The V_{DD} regulator has a 9mA current limit. For powering external loads other than those described from the V_{DD} rail, contact the factory for support.

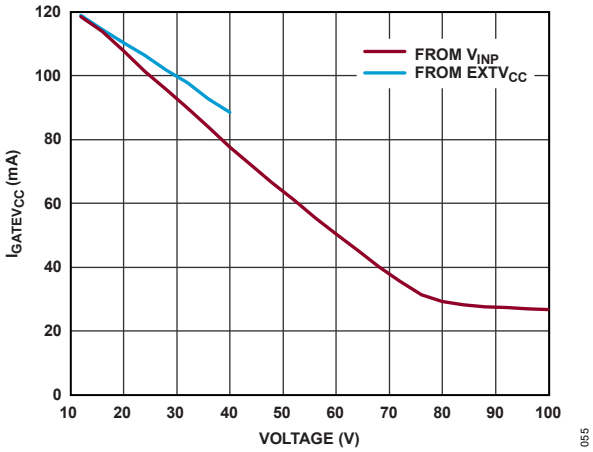


Figure 55. $GATEV_{CC}$ Current Limit vs. V_{INP}, $EXTV_{CC}$

Reverse Input Protection

The LT8210-1 includes optional reverse input protection down to –40V. To implement a power N-channel MOSFET, it should be placed with its source connected to V_{IN}, its drain connected to V_{INP}, and its gate connected to the DG pin. When the voltage at the V_{IN} drops below –1.2V (typical), the DG pin is clamped to the V_{IN} pin through an internal 30Ω (typical) switch. With its gate and source shorted, the external MOSFET is forced into cutoff, disconnecting V_{INP} and downstream circuitry from the input and preventing damage. The V_{IN}, DG, and EN/UVLO pins are all able to withstand voltages down to –40V without damage or excessive current flow. If polarized capacitors are used for input filtering, they should be placed on the V_{INP} side of the DG MOSFET. During normal operation, the DG – V_{IN} voltage is charged to approximately 8.5V via the internal charge pump in order to fully enhance the MOSFET. Switching will be disabled if the DG – V_{IN} voltage drops below 2.1V (typical) and re-enabled when it exceeds 2.8V (typical). The DG undervoltage lockout is intended to prevent excessive power dissipation in the DG MOSFET when it is not enhanced and current conducts through its body diode. The internal charge pump is able to source up to 180µA from the DG pin for fast charging and minimal delay at start-up. If reverse input protection is not needed, V_{INP} should be connected to V_{IN} directly or through a small RC filter (e.g., 1Ω, 1µF), and a 1nF, 25V ceramic capacitor should be placed between the DG and V_{IN} pins.

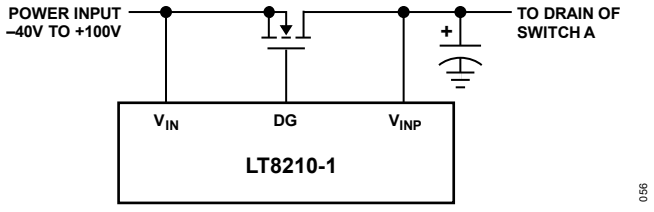


Figure 56. Implementing Reverse Input Protection

Multiphase Current Sharing

The LT8210-1 uses a closed loop approach to balance the currents of multiple phases. The IMON pins of all LT8210-1 should be connected together, creating an average current measurement. Each individual phase will adjust its switch duty cycle to match this average. The IMON pin for each LT8210-1 sources a current proportional to the differential voltage across its SNSP2 and SNSN2 inputs. These pins should connect to a sense resistor in the path of the current for that phase. An 11kΩ resistor must be connected from IMON to ground for each LT8210-1. In order to avoid issues due to local ground noise, it is recommended to isolate each 11kΩ resistor with a small RC filter (e.g., 499Ω and 10nF). Each LT8210-1 should be compensated with its own type II compensation network, as described in the *Loop Compensation* section of this data sheet. The V_{C1} (and V_{C2} if operated in pass-thru) should be coupled together with resistors 10kΩ or bigger.

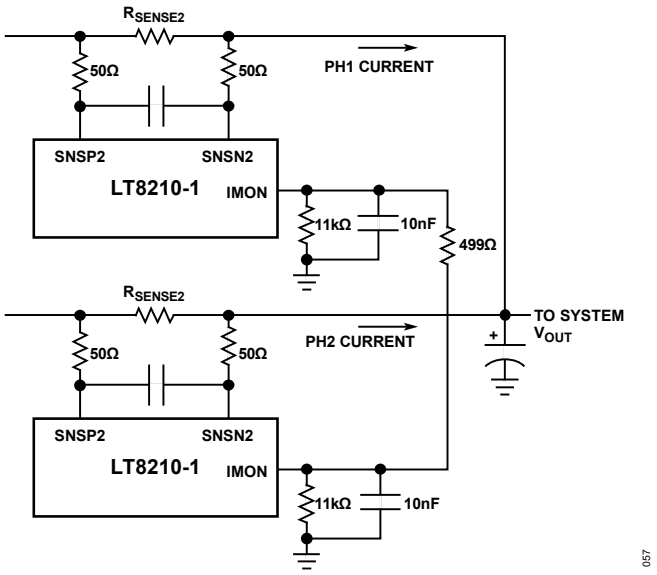


Figure 57. 2-Phase Current Sharing

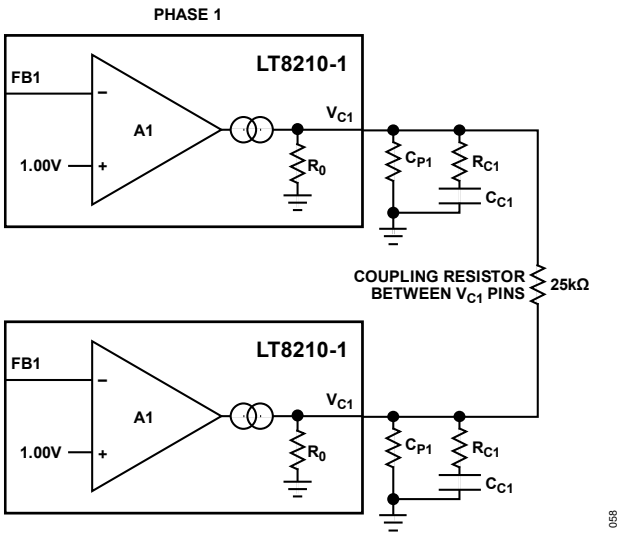


Figure 58. Loop Compensation for Multiple LT8210-1

Multiple LT8210-1 can share common resistor dividers for the FB1 and FB2 inputs, although routing these noise sensitive signals between phases can affect stability. Alternatively, each phase can use its own FB1 and FB2 dividers at the expense of less accurate current sharing. This can be mitigated by using 0.1% tolerance resistors for the feedback dividers.

Buck Foldback

The LT8210-1 actively prevents inductor current runaway while the buck loop is switching. The inductor current can run away when its rising slope exceeds the falling slope to such a degree that the current continues to increase each period even while switching at the minimum SW1 duty cycle. A buck regulator is most susceptible to runaway when the output voltage is near ground, causing the inductor current falling slope to be flat. This situation is exacerbated by a high input voltage and a high switching frequency. To prevent runaway, the LT8210-1 may skip switch A pulses while V_{OUT} is less than 10% of V_{INP} and the FB1 voltage is lower than 900mV. At the start of the switch A on-time, the sensed inductor current must be below an internally set pulse-skipping threshold; otherwise, the next pulse on switch A will be skipped. If the inductor current exceeds the pulse-skipping threshold on the next switch A turn-on, the following three pulses will be skipped, and so on. The foldback circuit increases the number of skipped pulses with each successive switch A pulse where this threshold is exceeded; otherwise, the skip count is reset. In addition to preventing inductor runaway, the LT8210-1 foldback scheme significantly reduces switch A power dissipation in a short circuit condition. When the output is shorted to ground, the power dissipation in switch A is dominated by transitional losses as it turns on and off. Reducing the number of switch A pulses over a given period reduces the dissipated power proportionally. The boost loop is naturally protected from inductor current runaway in the LT8210-1 as it can only occur when $V_{INP} \sim V_{OUT}$, which is within the buck-boost region. While the buck loop is simultaneously controlling the inductor current each cycle, it is not possible for the boost channel to run away.

PWGD Pin

The PWGD pin is an open drain logic output that goes high when the output voltage and IMON pin voltage are within preset limits after switching is enabled. The internal PWGD pull-down is released when V_{OUT} is within ±10% of its programmed value. In CCM and DCM operations, this occurs when the FB1 voltage is within ±10% of the 1.00V reference. In pass-thru mode, PWGD will go high when $V_{FB1} > 0.90V$ and $V_{FB2} < 1.10V$, indicating that the output voltage is within ±10% of the programmed output pass-thru window. PWGD will be pulled low if the voltage on the IMON pin exceeds 1.20V, indicating that the average current exceeds its programmed limit by 20% or more. The LT8210-1 includes a built-in self-test to confirm the system reference circuitry is functioning properly. This reference voltage is used for voltage regulation, current regulation, clock generation, and fault detection. If the system reference is outside of preset tolerances, switching is disabled, and the PWGD pin is pulled low. Switching will also be disabled, and the PWGD pin will be pulled low if the V_{INP}, $GATEV_{CC}$, V_{DD}, or DG pin voltages fall below their respective undervoltage lockout thresholds. The PWGD pin pull-up resistor can be connected to any external rail up to 40V. Using either V_{DD} or $GATEV_{CC}$ as the pull-up supply has the added advantage that PWGD will be in the correct state when the LT8210-1 is disabled. *Figure 59* shows the conditions that determine the state of the PWGD pin.

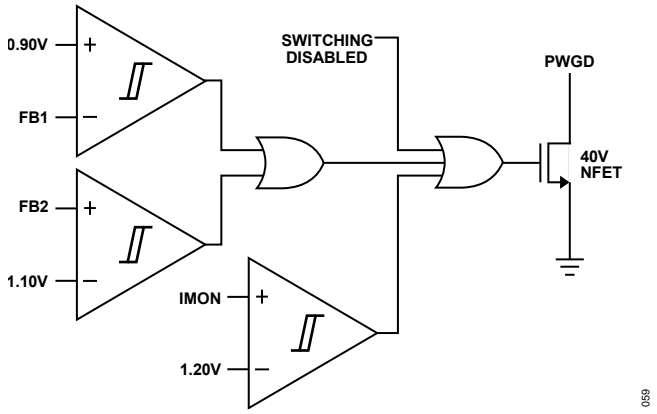


Figure 59. PWGD Logic

APPLICATIONS INFORMATION

The applications information section serves as a guideline for selecting external components based on the details of the application. For this section, refer to the basic LT8210-1 application circuit shown in *Figure 60*. Component selection typically follows the approach described below:

- R_{SENSE} is selected based on the required output current and the input voltage range .
- Inductor value (L) and switching frequency (f_{SW}) are chosen based on ripple, stability, and efficiency requirements.
- Power MOSFETs (A, B, C, and D) are selected to maximize efficiency while satisfying the voltage and current ranges of the application.
- C_{IN} and C_{OUT} capacitors are selected to filter input and output RMS currents and achieve the desired voltage ripple.
- C_{BST1}, C_{BST2}, and $C_{GATEVCC}$ capacitors are selected to store adequate charge to power the gate drivers.
- Type II compensation network is designed for V_{C1} (and V_{C2} if pass-thru mode is used).
- C_{SS} selected to set soft-start behavior.
- (Optional) – Reverse input protection (DG) MOSFET selected to stand-off the worst-case V_{INP} to V_{IN} voltage and minimize conduction loss during regulation.
- (Optional) – Current regulation and/or monitoring implemented with R_{SENSE2}, R_{IMON}, and C_{IMON}.

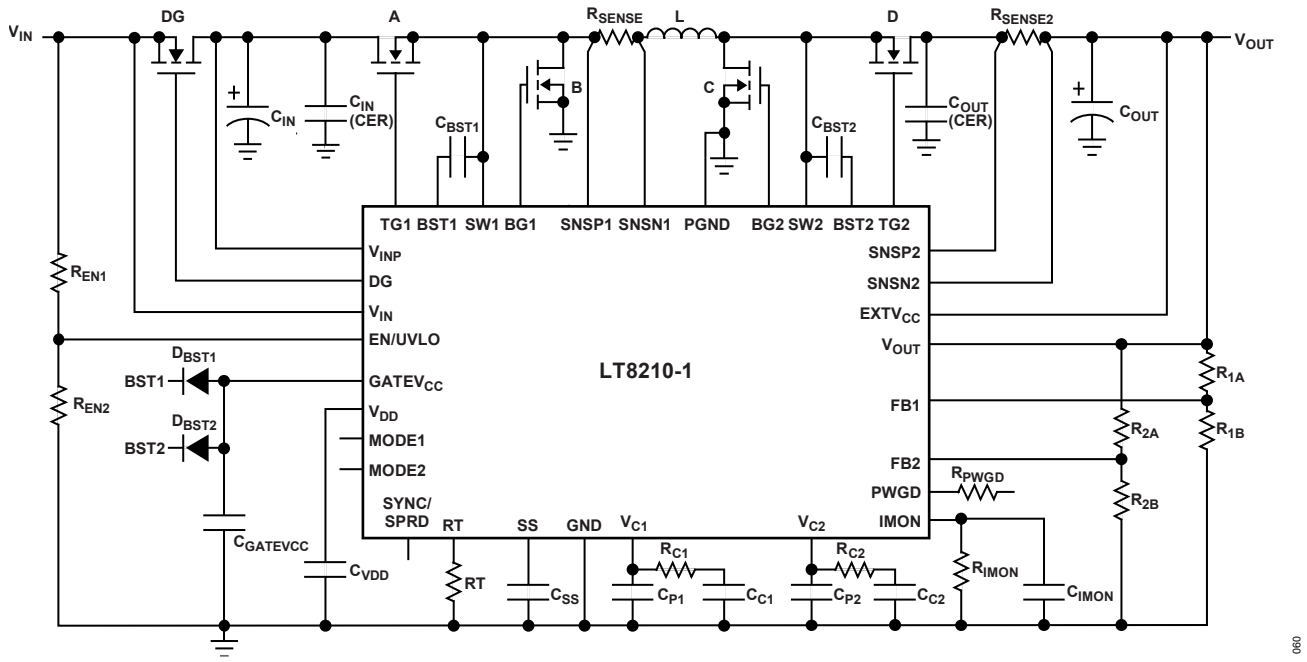


Figure 60. Basic LT8210-1 Applications Circuit

The examples and equations in this section assume continuous conduction mode unless otherwise noted. For pass-thru mode, use $V_{OUT(BUCK)}$ and $V_{OUT(BOOST)}$ in place of V_{OUT} for buck and boost calculations, respectively. All electric characteristics referred to in this section represent typical values unless otherwise specified.

Maximum Output Current and R_{SENSE} Selection

R_{SENSE} is chosen based on the required output current. With a properly selected inductor value, the maximum average inductor current is relatively independent of the inductor current ripple, duty cycle, and switching region. This simplifies the selection of R_{SENSE}, which can often be an iterative process. The R_{SENSE} value in the buck region for a given maximum output current, $I_{OUT(MAX)}$, can be calculated using Equation 1.

$$R_{SENSE(BUCK)} = \frac{50mV}{I_{OUT}(MAX)} \quad (1)$$

While operating in the boost region, the output current is equal to the inductor current multiplied by

$D'_{BST} \cong (1\text{-}D_{BST}) = V_{INP}/V_{OUT}$. Using $V_{INP(MIN)}$ the R_{SENSE} for a desired $I_{OUT(MAX)}$ can be calculated using Equation 2.

$$R_{SENSE(BOOST)} = \frac{40mV}{I_{OUT(MAX)}} \cdot \frac{V_{INP(MIN)}}{V_{OUT}} \quad (2)$$

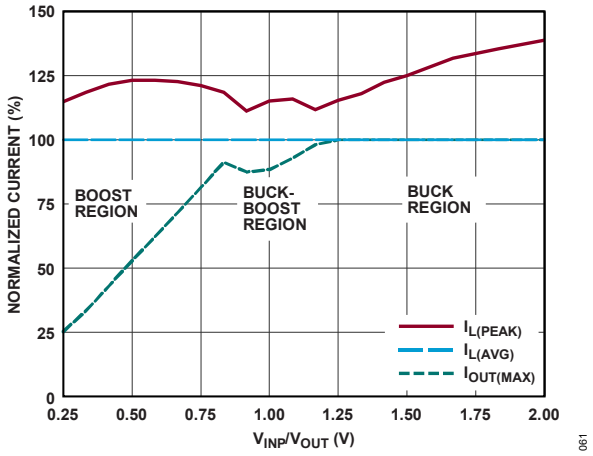


Figure 61. Example of Maximum Average Inductor Current and Output Current vs. V_{INP}/V_{OUT}

A margin of 20% to 30% on the lower of the two calculated R_{SENSE} values is usually recommended. The R_{SENSE} resistor should be a low inductance type so as not to degrade stability. A small low-pass filter between R_{SENSE} and the SNSP1 and SNSN1 pins, like that shown in *Figure 62*, is not required but may improve switching edge jitter in some applications. These filter components should be placed near the pins.

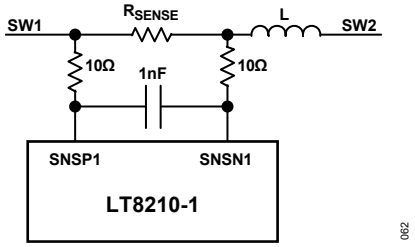


Figure 62. Optional SNSP1, SNSN1 Filter for Improved Jitter

Inductor Selection

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. The inductor value is inversely related to the ripple current. Typically, the inductor ripple current, ΔI_L, is set to 20% to 40% of the maximum inductor current. The minimum inductor value necessary to maintain a desired ripple can be calculated using Equation 3 for both buck and boost regions.

$$L_{(BUCK)} > \frac{V_{OUT} \cdot (V_{IN(MAX)} - V_{OUT})}{f_{SW} \cdot I_{OUT(MAX)} \cdot \Delta I_L\% \cdot V_{IN(MAX)}} \quad (3)$$

$$L_{(BOOST)} > \frac{V_{in(min)}^2 \cdot (V_{OUT} - V_{IN(MIN)})}{f_{SW} \cdot I_{OUT(MAX)} \cdot \Delta I_L\% \cdot V_{OUT}^2}$$

In addition to ripple considerations, the inductance should be large enough to prevent subharmonic oscillations. In a current mode-controlled regulator, the current sense loop creates a double pole at half the switching frequency, which can degrade system stability when its quality factor (Q_{CS}) is much greater than 1.0. The current sense loop damping is a function of the inductor current slope and the internal slope compensating ramp. The LT8210-1 slope

compensation scheme is designed to provide optimal damping of the current sense loop for any input voltage when the inductor value is set to the value given by Equation 4.

$$L_{OPTIMAL} = \left(260 + (5.5 \cdot V_{OUT})\right) \cdot R_{SENSE} \cdot \frac{1}{f_{SW}} \quad (4)$$

For example:

$$L_{OPTIMAL(VOUT=12V)} = 325 \cdot R_{SENSE} \cdot \frac{1}{f_{SW}}$$

$$L_{OPTIMAL(VOUT=48)} = 525 \cdot R_{SENSE} \cdot \frac{1}{f_{SW}}$$

This simplifies loop compensation as the current sense loop damping becomes independent of the duty cycle and switching region. Selecting $L_{OPTIMAL}$ also optimizes line regulation and line step response. A lower inductance value will increase Q_{CS}, and a sufficiently undersized inductor can result in subharmonic oscillation for buck duty cycles above 50% and boost duty cycles below 50%. Choose an inductor at least 70% of the calculated optimal value to avoid subharmonic instability. Inductor parasitics can significantly impact converter efficiency. For high efficiency, choose an inductor with low core loss, such as ferrite. The inductor should also have low DC resistance (DCR) to reduce the I^2R losses. Selecting an inductor with a DCR comparable to the $R_{DS(ON)}$ of the power MOSFETs is a reasonable starting point. If radiated noise is a concern, a shielded inductor should be used. Ferrite cores saturate abruptly, leading to a significant increase in ripple when the saturation current rating, I_{SAT}, is exceeded. I_{SAT} should be greater than the worst-case peak inductor current with an added margin. The maximum peak inductor current can be approximated by Equation 5.

$$I_{L(MAX)} \approx \frac{60mV}{R_{SENSE}} + \Delta I_{L(MAX)}A \quad (5)$$

Assuming an inductor ripple current, $\Delta L_{L(MAX)}$, of 40%, the peak inductor current could be 145% of the maximum output current. Adding an additional margin of 25% beyond the worst-case yields a conservative minimum inductor I_{SAT} rating of $90mV/R_{SENSE}$, for example.

Switching Frequency Selection

The RT frequency adjust pin allows the user to program the switching frequency from 80kHz to 400kHz. The selection of the switching frequency is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses, but requires larger inductor and capacitor values. For high power applications, consider operating at lower frequencies to minimize MOSFET heating from switching losses. For low power applications, consider operating at higher switching frequencies to minimize the total solution size. The selection of R_{SENSE}, the inductor value, and the switching frequency are interrelated. To maintain the ripple current amplitude and subharmonic stability, the inductor value will track the product of R_{SENSE} and the switching period, T. The R_{SENSE} value is set by load requirements. The inductor value is determined by ripple current and subharmonic stability criteria. A practical approach is to adjust the switching frequency to optimize system performance once the R_{SENSE} and L values have already been chosen. The component selection flow would be as follows:

1. Select R_{SENSE} based on the required output current.

2. Select inductor value based on the desired ripple for a range of f_{SW} (e.g., 80kHz to 120kHz).

3. Adjust the switching frequency to satisfy Equation 6.

$$f_{SW(OPTIMAL)} = \frac{(260+(5.5 \cdot V_{OUT})) \cdot R_{SENSE}}{L} \quad (6)$$

Setting the switching frequency to $f_{SW(OPTIMAL)}$ has a host of benefits, including optimized loop stability, optimized line rejection, and a flat average maximum inductor current across the duty cycle and switching region.

RT Set Switching Frequency

The switching frequency of the LT8210-1 is set with a resistor from the RT pin to the ground. *Table 5* shows switching frequency versus RT for 1% resistor values. The minimum and maximum switching frequencies are internally limited should the RT resistor be shorted (typically f_{SW} = 700kHz) or opened (typically f_{SW} = 45kHz). It is strongly recommended to use an RT resistor even when LT8210-1 is synchronized to an external clock using the SYNC/SPRD pin. If the synchronization signal is lost, the LT8210-1 will revert to the RT set value within approximately 20µs.

Table 5. Switching Frequency vs. RT Value (1% Resistor)

RT (kΩ)	f_{SW} (kHz)	RT (kΩ)	f_{SW} (kHz)
16.2	411	41.2	190
16.9	397	13.2	184
17.8	379	45.2	177
18.7	364	47.5	171
20.0	343	49.9	165
21.0	329	52.3	160
22.1	315	54.9	155
23.2	300	59.0	147
24.3	289	64.9	138
25.5	277	71.5	130
26.7	267	78.7	122
28.0	257	86.6	115
29.4	247	95.3	109
30.9	237	100	105
32.4	229	110	100
34.0	220	121	95
35.7	212	133	90
37.4	205	150	85
39.2	200	174	80

Frequency Synchronization

The LT8210-1 switching frequency can be synchronized to an external clock using the SYNC/SPRD pin. The threshold of the SYNC/SPRD receiver makes it compatible with standard 1.8V to 5.0V logic levels. Because an internal phase-locked loop (PLL) is used, there is no restriction between the synchronization frequency and the RT set oscillator frequency. The LT8210-1 is designed to transition seamlessly between the RT set switching frequency and the external synchronization clock. If the SYNC/SPRD signal drops below 50kHz or stops altogether, the LT8210-1 will revert to the RT set frequency within 20µs (typical). Setting the RT programmed frequency near the synchronization frequency is recommended to maintain normal switching should the external clock signal be lost. When a synchronization clock is first applied, the internal PLL may take 50µs or more to settle within 5% of the external clock frequency. When the clock synchronization feature is not used, connect SYNC/SPRD to V_{DD} to enable spread-spectrum modulation; otherwise, connect to GND.

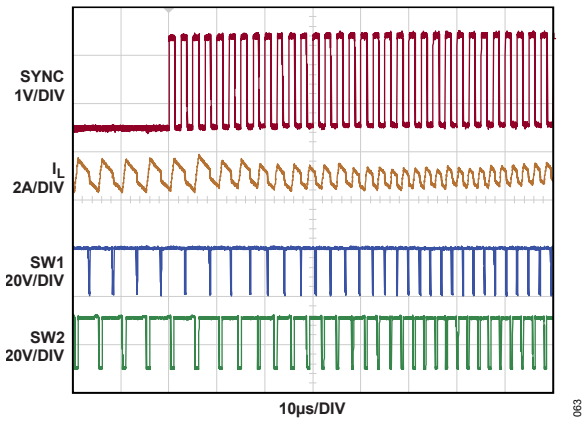


Figure 63. Transition from RT Set Frequency to Synchronization

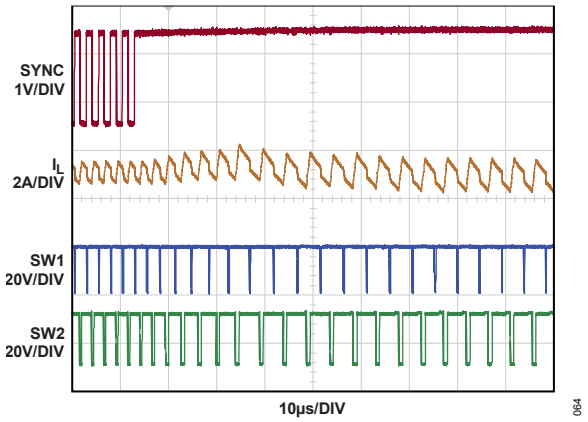


Figure 64. Transition from Synchronization to RT Set Frequency

Spread-Spectrum Frequency Modulation

Switching regulators can be particularly troublesome for applications where electromagnetic interference (EMI) is a concern. To improve EMI performance, the LT8210-1 includes a user-selectable triangular frequency modulation scheme. When the SYNC/SPRD pin is tied to the V_{DD} spread spectrum, functionality is enabled. The LT8210-1 will slowly spread f_{SW} between the nominal RT set frequency to 112.5% of that value. *Figure 65* and *Figure 66* demonstrate the difference in the noise spectrum and switching waveforms with the spread spectrum feature enabled.

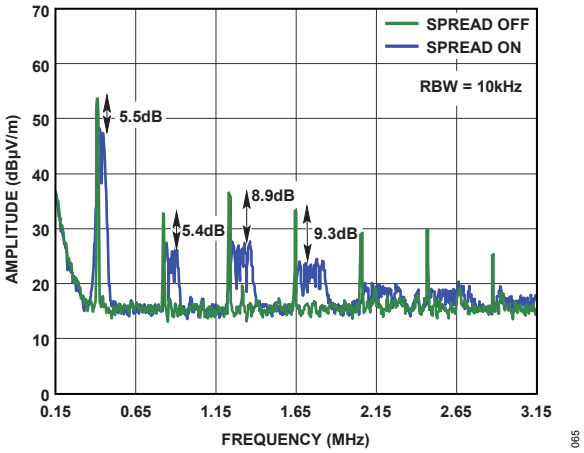


Figure 65. Conducted Average EMI Comparison (AM Band) Example

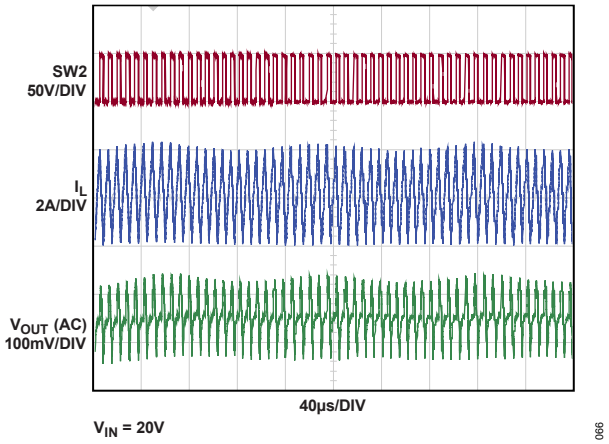


Figure 66. Switching Waveforms with Spread-Spectrum Enabled

Power MOSFET Selection

The LT8210-1 requires four external N-channel power MOSFETs (switches A, B, C, and D in *Figure 60*). The gate drive voltage of the LT8210-1 is typically greater than 10V allowing the use of both logic-level and standard-level threshold devices. The MOSFET maximum $V_{BR(DSS)}$ and drain current (I_D) ratings should exceed the worst-case voltage and current conditions of the application, with an added margin for safety. The maximum continuous drain current of a power MOSFET is de-rated as a function of temperature, with that information commonly available in the data sheet. It is important to consider power dissipation when selecting power MOSFETs. The most efficient circuit will use MOSFETs that dissipate the least amount of power. Dissipated power and the resulting temperature rise in external components will set the upper bound on the power that can be delivered by the LT8210-1. MOSFET power dissipation comes from two primary components: (1) I^2R conduction losses when the switch is fully turned on and drain current is flowing, and (2) power dissipated while the switch is turning on or off. Conduction losses are independent of frequency. Switching losses, on the other hand, scale with frequency and voltage. Generally speaking, conduction losses are dominant at higher currents and lower voltages, whereas switching losses tend to dominate at lower currents and higher voltages. Accurately predicting MOSFET power dissipation is a complex problem that is best suited to efficiency calculators such as those included in LTpowerCAD® II. That being said, efficiency calculators are no substitute for real-world measurements. The following section provides approximations of the main source(s) of

power dissipation for switches A, B, C, and D as a function of the input and output voltages and switching region. The purpose is to guide MOSFET selection by determining where the majority of power is being dissipated. In the following equations, ρ_τ is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically 0.4%/°C, as shown in *Figure 67*. For a maximum junction temperature of 125°C, using a value of $\rho_\tau = 1.5$ is reasonable. Q_{SW} is the switching charge and can be approximated as $Q_{SW} = Q_{GD} + Q_{GS}/2$ if not explicitly stated in the MOSFET data sheet.

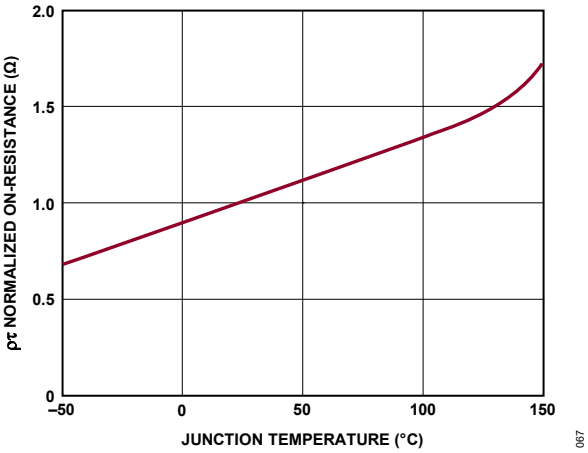


Figure 67. Normalized $R_{DS(ON)}$ vs. Temperature

The constant k is empirically derived to equal 1.3 and is a function of driver resistance, MOSFET threshold, and gate resistance.

Switch A:

The power dissipation in switch A is due to both conduction and switching losses and typically reaches a maximum at either $V_{IN(MIN)}$ in the boost region or $V_{IN(MAX)}$ in the buck region.

Table 6. Switch A Power Dissipation

REGION	POWER DISSIPATION
Buck	$I_{OUT}^2 \cdot (V_{OUT}/V_{IN}) \cdot \rho_\tau \cdot R_{DS(ON)} + k \cdot I_{OUT} \cdot V_{IN} \cdot f_{SW} \cdot Q_{SW}$
Buck-Boost	$I_{OUT}^2 \cdot (V_{OUT}/V_{IN}) \cdot \rho_\tau \cdot R_{DS(ON)} + k \cdot I_{OUT} \cdot V_{IN} \cdot f_{SW} \cdot Q_{SW}$
Boost	$I_{OUT}^2 \cdot (V_{OUT}/V_{IN})^2 \cdot \rho_\tau \cdot R_{DS(ON)}$
Pass-Thru (Non-Switching)	$I_{OUT}^2 \cdot \rho_\tau \cdot R_{DS(ON)}$

Switch B:

Switch B power dissipation is due mainly to conduction losses and reaches a maximum in the buck region at $V_{IN(MAX)}$.

Table 7. Switch B Power Dissipation

REGION	POWER DISSIPATION
Buck	$I_{OUT}^2 \cdot (1 - V_{OUT}/V_{IN}) \cdot \rho_\tau \cdot R_{DS(ON)}$
Buck-Boost	$I_{OUT}^2 \cdot (1 - V_{OUT}/V_{IN}) \cdot \rho_\tau \cdot R_{DS(ON)}$
Boost	0
Pass-Thru (Non-Switching)	0

Switch C:

Switch C power dissipation is due to both conduction and switching losses and reaches a maximum at $V_{IN(MIN)}$.

Table 8. Switch C Power Dissipation

REGION	POWER DISSIPATION
Buck	0
Buck-Boost	$I_{OUT}^2 \bullet V_{OUT} \bullet (V_{OUT} - V_{IN}) \bullet \rho_\tau \bullet R_{DS(ON)}/V_{IN}^2 + k \bullet I_{OUT} \bullet V_{OUT}^2 \bullet f_{SW} \bullet Q_{SW}/V_{IN}$
Boost	$I_{OUT}^2 \bullet V_{OUT} \bullet (V_{OUT} - V_{IN}) \bullet \rho_\tau \bullet R_{DS(ON)}/V_{in}^2 + k \bullet I_{OUT} \bullet V_{OUT}^2 \bullet f_{SW} \bullet Q_{SW}/V_{IN}$
Pass-Thru (Non-Switching)	0

Switch D:

Switch D power dissipation is due mainly to conduction losses and reaches a maximum in the boost region at $V_{IN(MIN)}$.

Table 9. Switch D Power Dissipation

REGION	POWER DISSIPATION
Buck	$I_{OUT}^2 \bullet \rho_\tau \bullet R_{DS(ON)}$
Buck-Boost	$I_{OUT}^2 \bullet (V_{OUT}/V_{IN}) \bullet \rho_\tau \bullet R_{DS(ON)}$
Boost	$I_{OUT}^2 \bullet (V_{OUT}/V_{IN}) \bullet \rho_\tau \bullet R_{DS(ON)}$
Pass-Thru (Non-Switching)	$I_{OUT}^2 \bullet \rho_\tau \bullet R_{DS(ON)}$

In most applications, the losses reach a maximum when the LT8210-1 is delivering $I_{OUT(MAX)}$ at $V_{IN(MIN)}$. Switches A and C will typically dissipate the majority of the power in these situations. To achieve a higher output current, it may be beneficial to use two MOSFETs in parallel for switches A and C to minimize conduction losses. While the power dissipated in switches B and D is comparatively low during normal operation, it may become significant if the output is shorted to ground. A representative example of switch power dissipation as a function of input voltage is shown in *Figure 68*. Other power loss sources include the gate drive current ($f_{SW} \bullet \sum$ switching MOSFET Q_G) multiplied by the supply voltage of the GATEV_{CC} regulator (either V_{INP} or V_{EXTVCC}), as well as the energy required to charge MOSFET Q_{OSS} and Q_{RR} each switching cycle depending on the switching region. Power MOSFETs of a particular technology trade on-resistance, $R_{DS(ON)}$, and gate charge Q_G (along with Q_{SW}, Q_{OSS}, and Q_{RR}), and maximizing efficiency often comes down to finding a MOSFET that strikes the right balance between these factors. Higher switching frequency and higher voltage operations drive up switching losses, making the value of Q_G (Q_{SW}, Q_{OSS}, and Q_{RR}) increasingly significant. In the non-switching pass-thru state, efficiency depends primarily on conduction losses in power switches A, D, and DG (if used) along with the inductor DCR. In these situations, prioritize low $R_{DS(ON)}$ over Q_G to maximize efficiency.

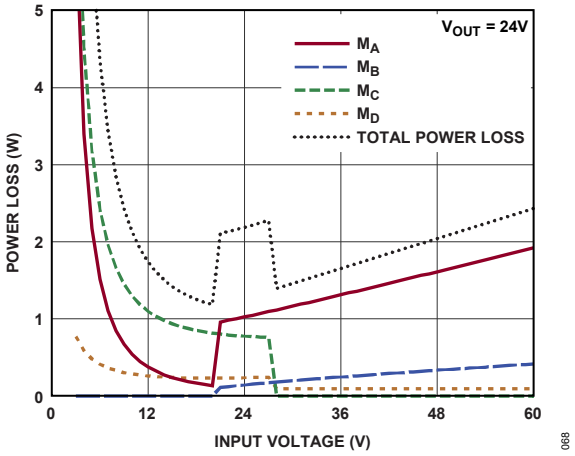


Figure 68. Example of Switch Power Dissipation vs. V_{INP}

C_{IN} and C_{OUT} Selection

Input and output capacitors are necessary to suppress the voltage ripple caused by discontinuous current moving in and out of the regulator. In the buck region, the input current is discontinuous, while in the boost region, the output current is discontinuous. Selecting the proper input and output capacitors boils down to three considerations.

1. Voltage ripple is inversely proportional to capacitance.

2. ESR must be low to minimize its contribution to voltage ripple.

3. RMS current rating of the capacitor(s) should exceed the worst-case application conditions with a margin.

For buck operation, the value of C_{IN} to achieve the desired input ripple voltage (ΔV_{IN}) can be calculated by Equation 7.

$$C_{IN} \cong \frac{I_{OUT(MAX)}}{\Delta V_{IN} * f_{SW}} \bullet \left(\frac{V_{OUT}}{V_{IN}}\right) \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

ΔV_{IN} is typically chosen at a level acceptable to the user. 100mV to 200mV is a good starting point. The ESR of the input capacitance should be less than Equation 8.

$$ESR_{(IN,MAX)} < \frac{\Delta V_{IN}}{I_{OUT(MAX)}} \quad (8)$$

The input R_{MS} current can be approximated by Equation 9.

$$I_{IN(RMS)} \cong I_{OUT(MAX)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \sqrt{\frac{V_{IN}}{V_{OUT}} - 1} \quad (9)$$

E9 has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. The capacitance necessary to achieve a desired output ripple, ΔV_{OUT}, can be calculated with Equation 10 for the buck and boost switching regions.

$$C_{OUT(BOOST)} = \frac{I_{OUT(MAX)} \bullet (V_{OUT} - V_{IN(MIN)})}{\Delta V_{OUT} \bullet f_{SW} \bullet V_{OUT}} \quad (10)$$

$$C_{OUT(BUCK)} = \frac{V_{OUT} \bullet (V_{IN(MAX)} - V_{OUT})}{\Delta V_{OUT} \bullet f_{SW}^2 \bullet V_{IN(MAX)} \bullet 8 \bullet L}$$

The ESR of the output capacitor should be low enough to not significantly increase the ripple voltage (Equation 11).

$$ESR_{(BOOST)} < \frac{\Delta V_{OUT} \bullet V_{IN(MIN)}}{I_{OUT(MAX)} \bullet V_{OUT}} \quad (11)$$

$$ESR_{(BUCK)} < \frac{\Delta V_{OUT} \bullet L \bullet f_{SW}}{V_{OUT} \bullet (1 - \frac{V_{OUT}}{V_{IN(MAX)}})}$$

C_{OUT} should also tolerate the maximum RMS output current when operating in the boost region (Equation 12).

$$I_{OUT(RMS)} \cong I_{OUT(MAX)} \bullet \sqrt{\frac{V_{OUT}}{V_{IN(MIN)}} - 1} \quad (12)$$

For both the C_{IN} and C_{OUT} capacitors, a good approach for larger values is to use a parallel combination of aluminum electrolytics for bulk capacitance and ceramics for low ESR and to handle the RMS currents. When used together, the percentage of RMS current that will flow through the aluminum electrolytic capacitor can be approximated by Equation 13.

$$\%I_{RMS,ALUM} \approx \frac{100\%}{\sqrt{1+(2\pi \bullet f_{SW} \bullet C_{(CER)} \bullet R_{ESR(ALUM)})^2}} \quad (13)$$

Where $R_{ESR(ALUM)}$ is the ESR of the aluminum capacitor and $C_{(CER)}$ is the total value of the ceramic capacitor(s). Ceramic capacitors should be placed near the regulator input and output to suppress high frequency switching spikes. Specifically, the ceramic capacitors on the input should be placed in close proximity to switches A and B, and the output ceramics should be placed close to switches C and D. Due to their excellent low ESR characteristics, ceramic capacitors can significantly reduce ripple voltage and help reduce power loss in higher ESR bulk capacitors. X5R and X7R are preferred, as these materials retain their capacitance over wide voltage and temperature ranges. At higher input and output voltages, multiple ceramic capacitors in parallel may be needed due to the limited availability of high voltage, large value ceramic capacitors in standard footprints. In situations with high input and/or output voltage ripple, an RC low-pass filter with a time constant of 1µs or greater is recommended for V_{INP} and V_{OUT} inputs to maintain low jitter on switching edges.

Bootstrap Capacitors (C_{BST1} and C_{BST2})

The top MOSFET gate drive signals, TG1 and TG2, are driven between their respective BST and SW pin voltages. The BST1 and BST2 voltages are biased from floating bootstrap capacitors C_{BST1} and C_{BST2}, which are normally recharged from $GATEV_{CC}$ through diodes D_{BST1} and D_{BST2} when their respective top MOSFETs are off. The bootstrap capacitors C_{BST1} and C_{BST2} need to store roughly 100 times the gate charge (Q_G) required by top switches A and D. In most situations, a 0.1µF to 0.47µF, X5R or X7R, 25V capacitor is adequate. The bypass capacitance from $GATEV_{CC}$ to ground should be at least ten times the value of the C_{BST1} and C_{BST2} capacitors. The rise times of the SW1 and SW2 pins can be slowed down through the addition of series resistors between the respective bootstrap capacitors and the BST1 or BST2 pins. The slowing down of the switch edges can improve overshoot but may also degrade efficiency due to increased transitional losses.

Bootstrap Diodes (D_{BST1} and D_{BST2})

Silicon diodes rated for 1A with a very fast reverse recovery time (< 50ns) are recommended for the bootstrap diodes, D_{BST1} and D_{BST2}. Although schottky diodes have the benefit of low forward drops, they can exhibit high reverse current leakage and have the potential for thermal runaway under high voltage and temperature conditions. Make sure that D_{BST1} and D_{BST2} have reverse breakdown voltage ratings higher than $V_{INP(MAX)}$ and $V_{OUT(MAX)}$, respectively, and have less than 50µA of reverse leakage at the maximum operating temperature. In pass-thru mode, low reverse leakage is critical. The bootstrap diode leakage current will have a disproportionate effect on the quiescent current due to the limited efficiency of the internal charge pump. For pass-thru, use diodes with reverse leakage currents 10µA or less at the maximum operating temperature. In some cases, it can be beneficial to add a small resistor (< 5Ω) in series with D_{BST1} and D_{BST2}. The resistors reduce surge currents in the diodes and can reduce ringing at the SW and BST pins of the IC. Since SW pin ringing is highly dependent on PCB layout, SW pin edge rates, and the types of diodes used, careful measurements directly at the SW pins of the IC are recommended. If required, a single resistor can be placed between $GATEV_{CC}$ and the anodes of both D_{BST1} and D_{BST2}, or by placing separate resistors between the cathodes of each diode and the respective BST pins. Excessive resistance in series with D_{BST1} and D_{BST2} can reduce the bootstrap capacitor voltage when the switch B and C on-times are very short and should be avoided.

$EXTV_{CC}$, $GATEV_{CC}$, and V_{DD}

$GATEV_{CC}$ is the power supply for the gate drivers and should be bypassed with a minimum 4.7µF, 25V, ceramic capacitor to the ground placed close to the pin. A good local bypass is necessary to supply the high transient current required by the MOSFET gate drivers. The $GATEV_{CC}$ voltage is regulated to 10.6V from PMOS low-dropout regulators powered from the V_{INP} or $EXTV_{CC}$ pins. V_{INP} is the default power supply, but if the voltage on $EXTV_{CC}$ exceeds 8V (typical) and is simultaneously lower than the V_{INP} voltage, $GATEV_{CC}$ will be regulated from $EXTV_{CC}$. The LT8210-1 selects the lower of the two supplies to minimize power dissipation. $EXTV_{CC}$ can be connected to V_{OUT} or any supply up to 40V for improved system efficiency. If not used, $EXTV_{CC}$ should be tied to ground through a 100k resistor. The maximum current the $GATEV_{CC}$ regulator can supply is typically 110mA at V_{IN} = 12V and drops linearly at higher voltages. This limits the power dissipation of the LT8210-1 to roughly 3W. The current limit should be considered when selecting power MOSFETs and setting the switching frequency. $I_{GATEVCC}$ is dominated by gate charge current, which reaches a maximum in the buck-boost region when all four power MOSFETs are switching. The peak gate drive current is equal to the product of f_{SW} and the sum of the MOSFET gate charges ($Q_{G(TOT)} = Q_{G(A)} + Q_{G(B)} + Q_{G(C)} + Q_{G(D)}$). The $GATEV_{CC}$ pin is backdrive-protected should the voltage on either the V_{INP} or $EXTV_{CC}$ drop below $GATEV_{CC}$. This is a useful feature, allowing the LT8210-1 to operate during input brownout conditions even when $EXTV_{CC}$ is not used. The length of time $GATEV_{CC}$ is able to ride through an input transient will depend on $I_{GATEVCC}$ and the size of its bypass capacitor. The $GATEV_{CC}$ regulator is stable with capacitors up to 220µF for flexibility in designing for many millisecond ride-through conditions. The V_{DD} pin is regulated to 3.3V from $GATEV_{CC}$ with a low-dropout PMOS regulator. The V_{DD} pin powers internal low voltage circuitry within the LT8210-1 and can source a maximum of 10mA. It must have a minimum 2.2µF X5R/ X7R capacitor to ground placed close to the pin. The V_{DD} supply is a convenient pull-up rail for the MODE1, MODE2, SYNC, and PWGD pins when tying those input logic high. For powering loads other than those specified, contact the factory for support.

Programming Output Voltage

The LT8210-1 has a voltage feedback pin FB1 that is used to program a constant output voltage when the LT8210-1 is configured for CCM or DCM operation. The output voltage can be set by selecting the values of R_{1A} and R_{1B} (*Figure 69*) according to Equation 14.

$$V_{OUT} = 1.00V \bullet \frac{R_{1A}+R_{1B}}{R_{1B}} \quad (14)$$

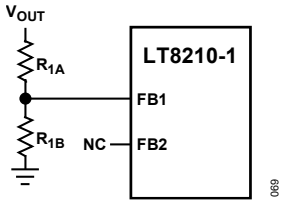


Figure 69. Setting the Output Voltage for CCM and DCM Operation Switching Modes

In pass-thru mode, the output voltages for the buck and boost channels are programmed independently according to Equation 15. See *Figure 70* .

$$V_{OUT(BOOST)} = 1.00V \bullet \frac{R_{1A}+R_{1B}}{R_{1B}} \quad (15)$$

$$V_{OUT(BUCK)} = 1.00V \bullet \frac{R_{2A}+R_{2B}}{R_{2B}}$$

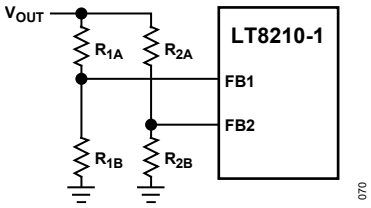


Figure 70. Setting the Output Voltage Window for Pass-Thru Mode

The FB1 and FB2 dividers can also be set with a single string of three resistors, as shown in *Figure 71*, to reduce system quiescent current and Equation 16.

$$V_{OUT(BOOST)} = 1.00V \bullet \frac{R_{1A}+R_{1B}+R_{1C}}{R_{1B}+R_{1C}} \quad (16)$$

$$V_{OUT(BUCK)} = 1.00V \bullet \frac{R_{1A}+R_{1B}+R_{1C}}{R_{1C}}$$

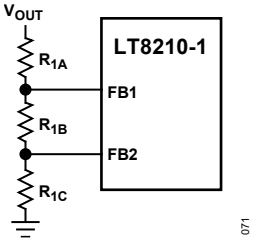


Figure 71. Power Saving Feedback Resistor Connection in Pass-Thru Mode

If pass-thru mode is exited during operation, the FB1 and FB2 pins will be shorted with an internal switch, creating a composite value for V_{OUT} between $V_{OUT(BOOST)}$ and $V_{OUT(BUCK)}$. The relative magnitude of the FB1 and FB2 resistive dividers can be used to place V_{OUT} at a desired value between $V_{OUT(BOOST)}$ and $V_{OUT(BUCK)}$ (Equation 17).

$$V_{out} = 1.00V \bullet \frac{R_{1A}||R_{2A}+R_{1B}||R_{2B}}{R_{1B}||R_{2B}} \quad (17)$$

If the resistor configuration shown in *Figure 70* is used for defining the pass-thru window top and bottom, V_{OUT} will equal $V_{OUT(BUCK)}$ when exiting the pass-thru.

Programming Current Limit

In boost and buck-boost operating modes, when $V_{OUT} > V_{INP}$, the current limit set by R_{SENSE} will vary with the duty ratio (Equation 2). If less variation is desired at the expense of higher power loss, R_{SENSE2} can be used to program an average current limit. The recommended choice is to set $R_{SENSE2} \approx 1.5^{*} R_{SENSE}$. This value optimizes the tradeoff between power loss and current limit variation, i.e., minimizes power loss while still reducing somewhat the variation of the current limit when input voltage drops below output voltage.

To program current limit variation that is independent of V_{INP} (but with higher power loss), an alternate choice for R_{SENSE2} is:

$$R_{SENSE2} = \frac{0.15}{I_{OUT(MAX)}} - \frac{V_{OUT}}{V_{INP(MIN)}} \cdot R_{SENSE} \cdot \left(1 + \frac{\Delta I_L\%}{2}\right) \quad (18)$$

A margin of 20% to 30% below the calculated value is recommended.

Where:

$I_{OUT(MAX)}$ is the maximum average current out.

$V_{INP(MIN)}$ is the minimum input at the V_{INP} pin.

ΔI_L % is the inductor ripple current divided by the output current. 30% to 40% is typically optimal.

Multiphase Current Component Selection

An RC network from the R_{SENSE2} terminals to SNSP2 and SNSN2 inputs is required to average out ripple current that may degrade current matching between phases at light loads. The time constant of this low-pass filter should be greater than 5µs (e.g., 49.9Ω and 100nF), but it can be increased for better current matching. Each LT8210-1 phase should have its own 11k resistor from its IMON pin to that IC's signal ground. The IMON pins of all phases should connect to a common node through resistors of several hundred Ohms or greater. Each IMON pin should have a local bypass capacitor (for example, 10nF) to prevent noise due to local ground voltage variation. The V_{C1} (and V_{C2} if pass-thru mode is used) pins for each phase must have their own Type II compensation networks and these pins should be connected to a common node through a resistor between 1k and 10k. The coupling of the V_{C1} (and V_{C2} in pass-thru) pins dramatically reduces current matching error from reference voltage variation and feedback resistor divider mismatch. The resistors connecting the V_{C1} pins isolate the compensation networks from switching noise picked up in the PCB traces connecting them. It is recommended to use separate FB1 (and FB2 in pass-thru) resistor dividers for each phase. While this increases the current matching error, it can be greatly reduced by using 0.1% tolerance resistors. The risks of routing high-impedance feedback signals long distances between phases are not worth a slight increase in current mismatch.

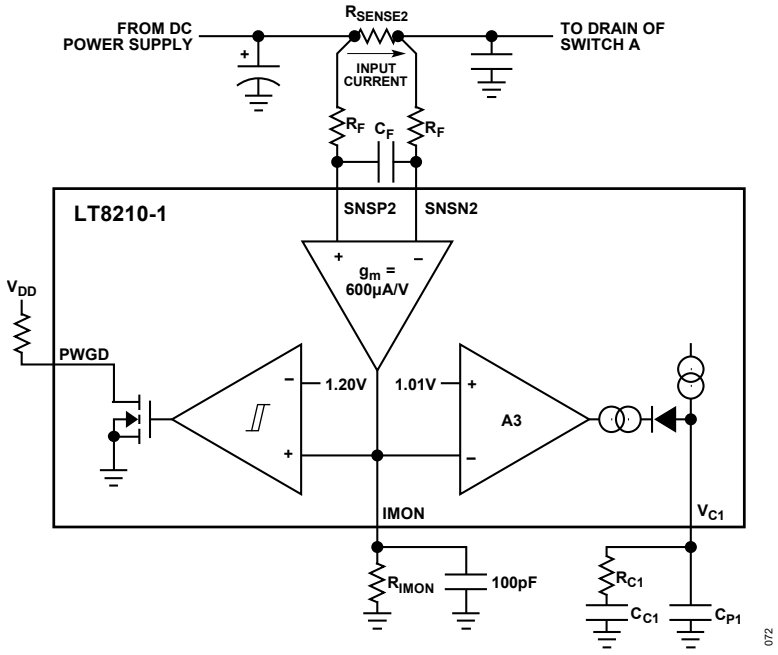


Figure 72. 2-Phase Current Sharing Application

Programming V_{IN} UVLO

A resistor divider from V_{IN} to the EN/UVLO pin implements V_{IN} undervoltage lockout (UVLO). The EN/UVLO falling threshold is set at 1.35V with 100mV of hysteresis. The programmable UVLO threshold can be calculated using Equation 19.

$$V_{UVLO-} = 1.35 \bullet \frac{R_1+R_2}{R_2} \quad (19)$$

Figure 73 shows the implementation of external shutdown control while still using the UVLO function. The NMOS grounds the EN/UVLO pin when turned on and puts the LT8210-1 into shutdown with a quiescent current around 1µA. If the functionality of the EN/UVLO pin is not needed, connect to the V_{IN} pin for always-on operation.

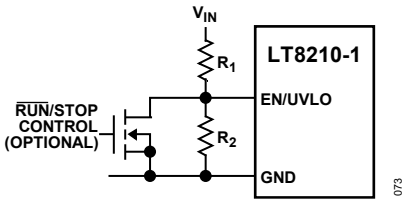


Figure 73. V_{IN} UVLO Implementation Using the EN/UVLO Pin

Soft-Start

Soft-start reduces the input power sources surge current by gradually increasing the controller's current limit. Both the V_{C1} and V_{C2} pins are internally clamped to a diode voltage above the SS pin voltage. As the SS capacitor is charged, V_{C1} and V_{C2} ramp along with SS and the commanded inductor current ramps in a similar fashion. The soft-start interval will be a function of C_{SS}, C_{OUT}, V_{OUT}, and R_{SENSE} and can be approximated using Equation 20.

$$t_{SS} \cong 2000 \bullet \sqrt{C_{SS} \bullet C_{OUT} \bullet V_{OUT} \bullet R_{SENSE}} \quad (20)$$

This assumes buck region operation and that the inductor current does not reach its cycle-by-cycle maximum during start-up. If starting up into the boost switching region or if the inductor current reaches its limit, the soft-start time will be extended. If no C_{SS} is used, the inductor current will quickly ramp to its maximum value, and the output voltage ramp time can be approximated using Equation 21.

$$t_{SS} \approx 20 \bullet C_{OUT} \bullet V_{OUT} \bullet R_{SENSE} \quad (21)$$

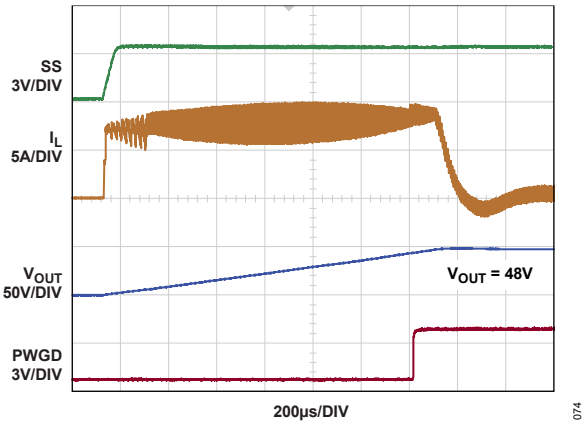


Figure 74.Typical Start-Up with No C_{SS}

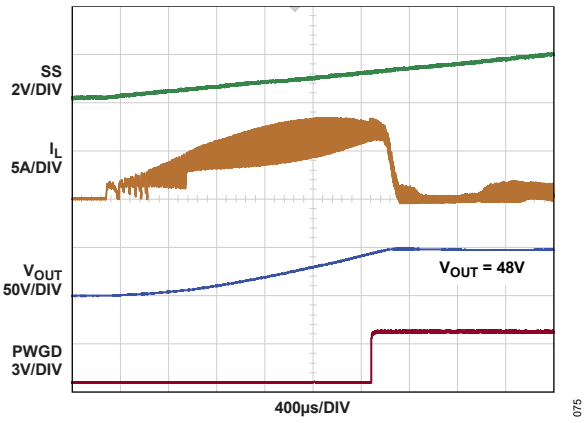


Figure 75. Typical Start-Up with C_{SS} = 10nF

Determining the value of C_{SS} empirically with a capacitance-decade box is often the most straightforward approach. In pass-thru mode, use $C_{SS} \leq 10nF$.

Loop Compensation

The loop stability is affected by a number of factors, including the inductor value, output capacitance, load current, switching frequency, and the range of input and output voltages. The LT8210-1 uses internal transconductance amplifiers with outputs at V_{C1} and V_{C2} to compensate the control loop(s). The Type II compensation network used to compensate the LT8210-1 is shown in *Figure 76* and *Figure 77*.

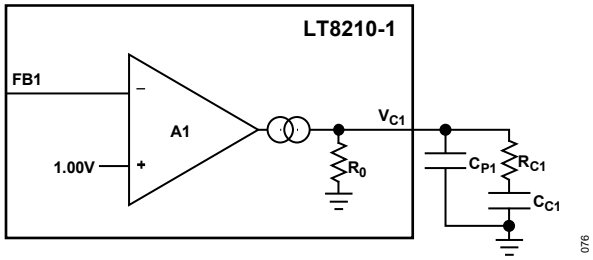


Figure 76. Loop Compensation on V_{C1}

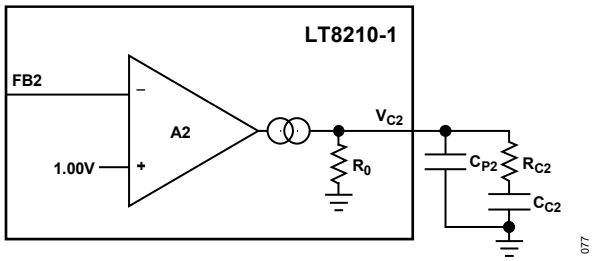


Figure 77. Loop Compensation on V_{C2}

For most applications, a C_{C1} of 2.2nF is a good starting point. Smaller values of C_{C1} can improve settling time after a load transient. C_{P1} is used to filter switching noise and reduce jitter and is typically set at one tenth the value of C_{C1} or less. Increasing the value of C_{P1} may improve the jitter performance between switching bursts in pulse-skipping operation. If the C_{P1} value is set too high, it may degrade loop bandwidth and phase margin. The R_{C1} value can range from less than 5k to more than 100k. Higher R_{C1} values will improve loop bandwidth, possibly at the expense of phase margin. The compensation of a buck-boost regulator depends strongly on the details of the boost region operation due to the presence of the right-half plane zero in the control-to-output transfer function. Higher output currents and lower minimum D'_{BST} ($V_{INP(MIN)}/V_{OUT}$) will require more conservative compensation, translating to a lower value for R_{C1}. The V_{C2} pin is used for compensating the buck regulation loop when the LT8210-1 is operated in pass-thru mode. The buck current mode control transfer function does not contain a right-half plane zero, allowing it to be compensated more aggressively for improved transient response. For most applications, a C_{C2} of 1.5nF is a good starting point. A C_{P2} of 100pF to 220pF is typically sufficient for filtering switching noise. Choose an R_{C2} value between 20k and 150k to start your design. For a more detailed description of Type II compensation for current mode control, refer to ADI *Application Note 149*.

Optional DG MOSFET Selection

To implement reverse protection, an N-channel MOSFET must be placed with its source at the V_{IN} pin, drain at the V_{INP} pin, and its gate tied to DG. The important considerations for the DG MOSFET selection include breakdown voltage $V_{BR(DSS)}$, continuous drain current (ID), and on resistance ($R_{DS(ON)}$), as this degrades converter efficiency through conduction loss. The breakdown voltage of the DG MOSFET should be greater than the worst-case voltage difference between V_{INP} and V_{IN}. The continuous drain current of the DG MOSFET should exceed the maximum input current (50mV/R_{SENSE}) at the maximum temperature. While the gate charge (QG) of the DG MOSFET does not degrade system efficiency, a larger QG will increase both start-up time and reverse input protection response time. In most cases, it is beneficial to choose a lower $R_{DS(ON)}$ MOSFET at the expense of a higher QG to minimize power dissipation. When the V_{IN} voltage drops below –1.2V (typical), the DG pin is internally clamped to the V_{IN} with a low resistance switch capable of sinking 80mA. For a power MOSFET with a gate charge of 50nC, the DG will be shorted to V_{IN} within 1µs after a negative input voltage is detected. Switching is halted in this state and only resumes when the input is no longer reversed and the DG – V_{IN} voltage is charged above its undervoltage threshold of 2.8V (typical). The V_{IN}, EN/UVLO, and DG pins tolerate negative voltages down to –40V. If reverse protection is not needed, V_{IN} and V_{INP} should be connected and a 1nF, 25V capacitor placed between V_{IN} and DG.

Component Optimization for Pass-Thru Operation

Special consideration must be given to component selection to optimize performance when operating in the pass-thru region. When the LT8210-1 enters the non-switching pass-thru state, switches A and D turn on continuously, forming an RLC tank circuit between V_{INP} and V_{OUT}. In this non-switching pass-thru state, efficiency is determined by conduction losses in the total series resistance between input and output (Equation 22).

$$\eta = 100\% \cdot \left(1 - \frac{I_{OUT} \cdot R_{SERIES}}{V_{IN}}\right) \quad (22)$$

$$R_{SERIES} = R_{DSON(A)} + R_{SENSE} + R_{DCR} + R_{DSON(D)} + R_{SENSE2}$$

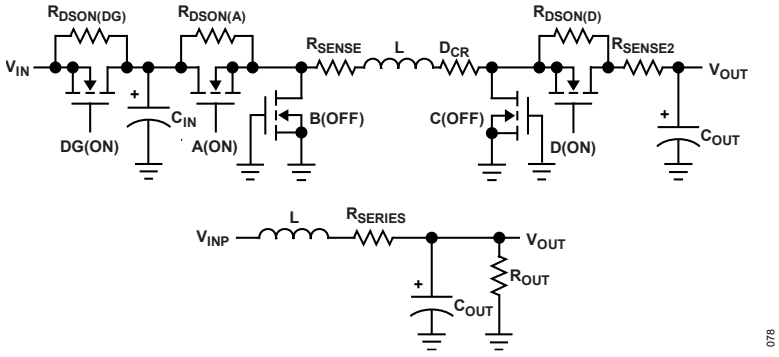


Figure 78. Non-Switching Pass-Thru Equivalent Circuit

R_{SERIES} should be minimized to maintain efficiency at higher output currents. If reverse input protection is implemented, the $R_{DS(ON)}$ of the DG MOSFET must also be accounted for in efficiency calculations. The quality factor of the RLC network between V_{INP} and V_{OUT} strongly effects the inductor current and output voltage response due to line and load transients and should be minimized wherever possible. This quality factor, Q, can be approximated by Equation 23.

$$Q \cong \sqrt{\frac{L}{C_{OUT}}} \cdot \frac{1}{R_{SERIES}} \quad (23)$$

While beneficial for efficiency, low series resistance leads to high Q and an underdamped transient response. Without increasing R_{SERIES}, the quality factor can be reduced either by decreasing the inductor value or increasing the output capacitance. A lower inductor value requires operating at a higher switching frequency to maintain ripple performance and sub-harmonic stability while switching. Depending on the details of the application, this can be a good approach if the input voltage is expected to be within the pass-thru window the majority of the time, and lower efficiency due to increased switching losses is not a major concern. Otherwise, increasing the output capacitance is a more or less benign approach for lowering Q other than possibly requiring adjustment to the loop compensation. The resonant frequency of the RLC network can be calculated using Equation 24.

$$f_0 = \frac{1}{2\pi} \cdot \sqrt{\frac{1}{L \cdot C_{OUT}}} \quad (24)$$

Generally speaking, the output closely tracks the input for frequencies below resonance. Above the resonant frequency, the majority of the AC voltage from the input shows up as voltage across the inductor. The LT8210-1 monitors the inductor's voltage and current in the non-switching state, and switching will resume if the inductor current exceeds the pass-thru DC current limit (typically, $V_{SNSP1} - V_{SNSN1} > 63mV$) or if the difference in voltage between V_{INP} and V_{OUT} exceeds 4% of the input voltage. This means that the total series resistance between V_{INP} and V_{OUT} should be sized less than Equation 25.

$$R_{DSON(A)} + R_{SENSE} + R_{DCR} + R_{DSON(D)} \ll \frac{0.04 \cdot V_{OUT(BOOST)}}{I_{OUT(MAX)}} \quad (25)$$

If the input supply noise has an amplitude greater than 4% of the nominal value at frequencies above resonance, consider adding an input filter to reduce high frequency content and minimize/prevent switching in the pass-thru region. The load transient response in the pass-thru region is determined primarily by the ESR of the output capacitor, which should be kept low through the use of parallel ceramic capacitors. The ESR of the bulk output capacitor should also be kept relatively low, as this determines the output impedance near resonance. The soft-start capacitor, C_{SS}, controls the ramping of the inductor current whenever the LT8210-1 exits the non-switching pass-thru state due to a line or load transient or mode change. A C_{SS} value greater than 10nF may slow the output response at this non-switching to switching transition and should be verified in the application under the worst-case transient conditions. Efficiency at light loads ($I_{OUT} < 10mA$) and system quiescent current draw are optimized through the use of large value resistors for the FB1, FB2, and EN/UVLO (if an input UVLO is implemented) dividers. If possible, use a single 3-resistor divider between the output and ground to program $V_{OUT(BOOST)}$ and $V_{OUT(BUCK)}$.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting efficiency and which change would produce the most improvement. Although all dissipative elements in the circuit produce losses, these are the main sources of losses in LT8210-1 circuits:

1. Switching Losses. These losses arise from the brief amount of time switch A or switch C spends in the saturated region during SW1 and SW2 node transitions, respectively. Power loss depends on the input voltage, output voltage, load current, driver strength, and MOSFET capacitance, among other factors. See the *Power MOSFET Selection* section for more details.

2. DC I^2R Losses. These arise from the resistances of the MOSFETs, sensing resistors, inductors, and PC board traces and cause the efficiency to drop at high output currents.

3. $GATEV_{CC}$ Current. The sum of the MOSFET driver current, V_{DD} pin current, and control currents. The $GATEV_{CC}$ regulator's power supply voltage times the current represents lost power. This loss can be reduced by supplying $GATEV_{CC}$ current through the $EXTV_{CC}$ pin from a high efficiency source, such as the output or an alternate supply if available. Lower Q_G MOSFETs can reduce $GATEV_{CC}$ current and power loss, as well as lowering the switching frequency.

4. C_{IN} and C_{OUT} Loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator in buck mode. The output capacitor has the difficult job of filtering the large RMS output current in boost mode. Both C_{IN} and C_{OUT} are required to have low ESR to minimize the AC I^2R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.

5. Other Losses. Inductor core loss occurs predominately at light loads. When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If one makes a change and the input current decreases, then the efficiency has increased. If there is no change in input current, then there is no change in efficiency.

PC Board Layout Checklist

The basic circuit board layout requires a dedicated ground plane layer. Also, for high current, a multilayer board provides heat sinking for power components.

• The ground plane layer should not have any traces and should be as close as possible to the layer with the power MOSFETs.

• Separate the power ground from the signal ground. The power ground should connect to the (–) terminals of C_{IN}, C_{OUT}, $C_{GATEVCC}$, and the sources of switches B and C. All small-signal components and compensation components should connect to a separate signal ground, which in turn connects to the PCB ground at one location away from high currents and switching noise. The GND pin and back tab must connect to this signal ground.

• Place switch A, switch B, and the input capacitor(s) in one compact area with short PC trace lengths.

• Place switch C, switch D, and the output capacitor(s) in one compact area with short PC trace lengths.

• Minimize the routing resistance from the TG1 and BG2 pins to power switches A and C, respectively.

• Use planes for V_{IN}, V_{INP}, and V_{OUT} to maintain good voltage filtering and to keep power losses low.

• The SW1 and SW2 planes should be wide enough to provide low resistance connections between the power switches, inductor, and sense resistor, but otherwise as compact as possible to minimize parasitic capacitance.

• Route the inductor current sense traces (SNSP1/N1) together with minimum PC trace spacing. The optional filter network capacitor between positive and negative sense traces should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the R_{SENSE} resistor.

• Route the average current sense traces (SNSP2/N2) together with the minimum PC trace spacing. Avoid crossing or running parallel to high dV/dT signals. The optional filter network capacitor between positive and negative sense traces should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the R_{SENSE2} resistor.

• Keep the high dV/dT nodes SW1, SW2, BST1, BST2, TG1, TG2, SNSP1, and SNSN1 away from sensitive small-signal nodes.

• Avoid running signal traces parallel to the traces that carry high di/dt current because they can receive inductively coupled voltage noise. This includes the SW1, SW2, TG1, TG2, BG1, and BG2 traces to the controller.

• Connect the top driver bootstrap capacitor, C_{BST1}, closely to the BST1 and SW1 pins. Connect the top driver bootstrap capacitor, C_{BST2}, closely to the BST2 and SW2 pins.

• Connect the FB1 and FB2 pin resistor dividers between the (+) terminal of COUT and signal ground. The resistor connections should not be along high current or noise paths.

• If $EXTV_{CC}$ is connected to V_{OUT}, it should have a Kelvin connection to the (+) terminal of C_{OUT}, and a ceramic bypass capacitor should be placed close to the $EXTV_{CC}$ pin.

• Connect the V_{C1}/V_{C2} pin compensation networks closely to the IC, between V_{C1}/V_{C2} and the signal ground pins. The capacitor helps to filter the effects of PCB noise and output ripple voltage from the compensation loop.

• Connect the $GATEV_{CC}$ and V_{DD} bypass capacitors close to the IC. The capacitors carry the MOSFET drivers' current peaks. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to a DC net (e.g., quiet GND).

TYPICAL APPLICATIONS

4-Phase; 12V CCM and DCM Operation; 8V to 16V Pass-Thru

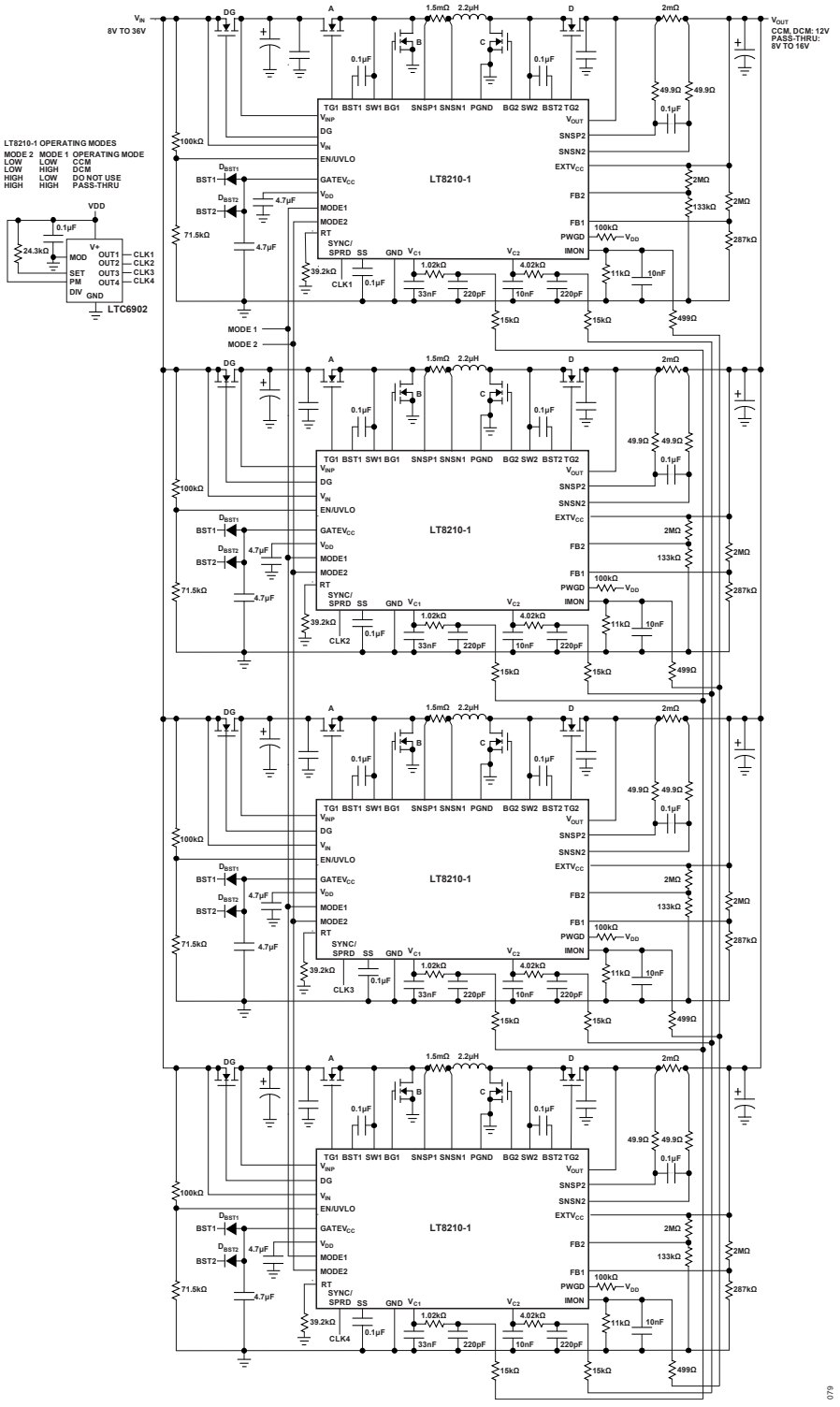
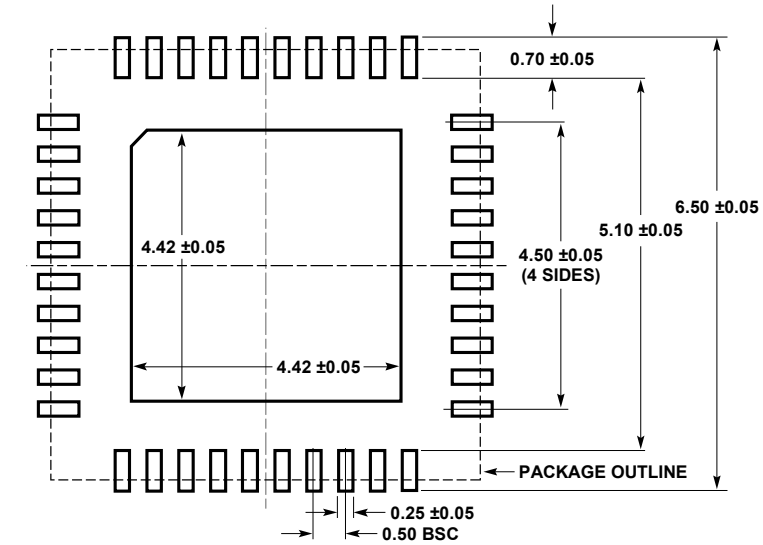


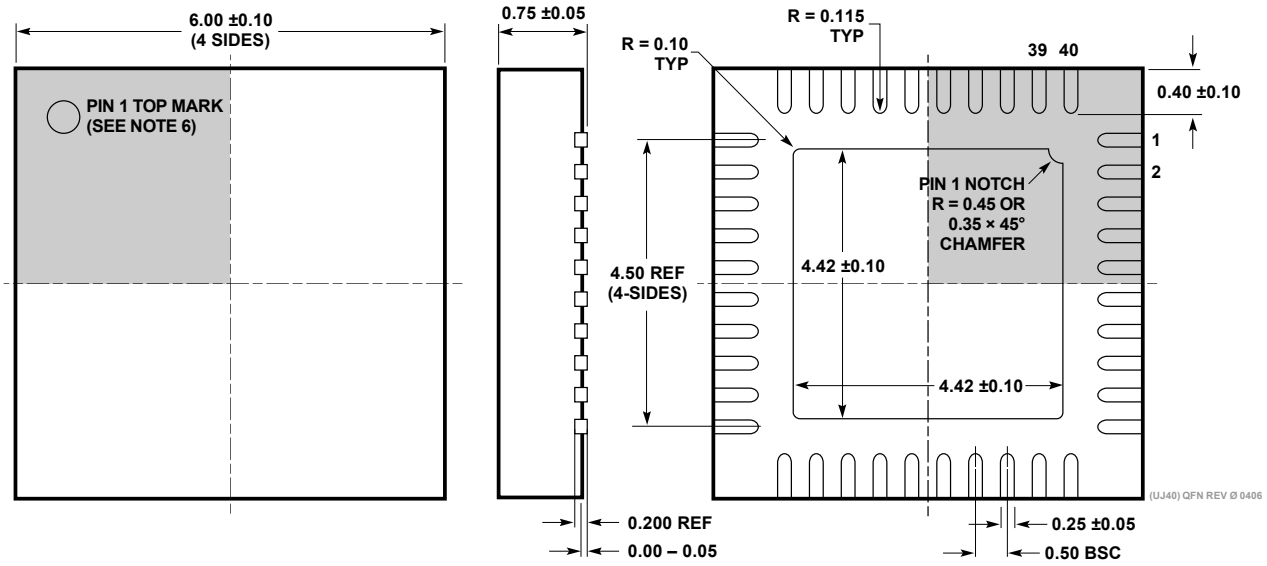
Figure 79. Typical Application, 4-Phase Schematic

OUTLINE DIMENSIONS

UJ Package
40-Lead Plastic QFN (6mm × 6mm)
(Reference LTC DWG # 05-08-1728 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS A JEDEC PACKAGE OUTLINE VARIATION OF (WJJD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Figure 80. Package Drawing

ORDERING GUIDE

Table 10.Ordering Guide

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8210AUJ-1#PBF	LT8210AUJ-1#TRPBF	LT8210UJ-1	40-Lead (6mm x 6mm) Plastic QFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3779	150V V_{IN} and V_{OUT} Synchronous 4-Switch Buck-Boost Controller	4.5V ≤ V_{IN} ≤ 150V, 1.2V ≤ V_{OUT} ≤ 150V, Up to 99% Efficiency Drives Logic Level or STD Threshold MOSFETs, TSSOP-38
LTC3777	150V V_{IN} and V_{OUT} Synchronous 4-Switch Buck-Boost Controller + Switching Bias Supply	4.5V ≤ V_{IN} ≤ 150V, 1.2V ≤ V_{OUT} ≤ 150V, Up to 99% Efficiency Drives Logic Level or STD Threshold MOSFETs, TSSOP-38
LT8705A	80V V_{IN} and V_{OUT} Synchronous 4-Switch Buck-Boost DC/DC Controller	2.8V ≤ V_{IN} ≤ 80V, Input and Output Current Monitor, 5mm × 7mm QFN-28/TSSOP-38
LTC7813	60V Low IQ Synchronous Boost + Buck Controller Low EMI and Low Input/Output Ripple	4.5V (Down to 2.2V after Start-Up) ≤ V_{IN} ≤ 60V, Boost V_{OUT} Up to 60V, 0.8V < Buck V_{OUT} < 60V, IQ = 29µA, 5mm × 5mm QFN-32
LT8390A	High Efficiency Synchronous 4-Switch Buck-Boost Controller	4V ≤ V_{IN} ≤ 60V, V_{OUT} Range: 1V to 60V, ±1.5% Output Voltage Accuracy 4mm × 5mm QFN-2/TSSOP-28 Packages
LTM8056	58V Buck-Boost DC/DC µModule® Regulator, Adjustable Input and Output Current Limiting	5V ≤ V_{IN} ≤ 58V, 1.2V ≤ V_{OUT} ≤ 48V 15mm × 15mm × 4.92mm BGA Package
LTC3895/LTC7801	150V Low IQ, Synchronous Step-Down DC/DC Controller with 100% Duty Cycle	4V ≤ V_{IN} ≤ 140V, 150V Abs Max, PLL Fixed Frequency 50kHz to 900kHz, 0.8V ≤ V_{OUT} ≤ 60V, Adjustable 5V to 10V Gate Drive, IQ = 40µA 4mm × 5mm QFN-24/TSSOP-24/TSSOP-38(31)
LTC7103	105V, 2.3A Low EMI Synchronous Step-Down Regulator	4.4V ≤ V_{IN} ≤ 105V, 1V ≤ V_{OUT} ≤ V_{IN}, IQ = 2µA Fixed Frequency 200kHz to 2MHz, 5mm × 6mm QFN
LT8210	100V V_{IN} and V_{OUT} Synchronus 4-Switch Buck-Boost DC/DC Controller with Pass-Thru	2.8V ≤ V_{IN} ≤ 100V, 1V ≤ V_{OUT} ≤ 100V, Pass-Thru Mode, 6mm × 6mm QFN
LTC7878	70V Parallelable 4-Switch Buck-Boost Controller with Inductor DCR Current Sensing	5V to 70V input and output range, seamless low-noise transitions between operating regions, 5mm × 5mm QFN

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LT8210AUJ-1#TRPBF LT8210AUJ-1#PBF