

## Evaluating the **LTC2065** 2 $\mu$ A Supply Current, Low $I_B$ , Zero-Drift, Op Amp

### FEATURES

- Fully featured evaluation board for the **LTC2065**
- Enables efficient prototyping
- User defined circuit configuration
- Simplified connection to test equipment and other circuits

### EVALUATION KIT CONTENTS

EVAL-LTC2065-TQFN

### EQUIPMENT NEEDED

- Dual-output dc power supply
- Dual-channel signal generator
- Oscilloscope
- Banana jack to grabber cables

### DOCUMENTS NEEDED

[LTC2065 data sheet](#)

### GENERAL DESCRIPTION

The EVAL-LTC2065-TQFN evaluates the **LTC2065** 16-lead, quad-channel, lead frame chip scale package (LFCSP)/quad flat no-lead (QFN) operational amplifier (op amp). The EVAL-LTC2065-TQFN is a prepopulated board using a gain of 2 configuration with a low-pass filter at the noninverting input that has a cutoff frequency of 480 Hz. This pass band is sufficient for most input signals because of the slew rate limitation of the device. To minimize the effect of chopper clock feedthrough, limit signal bandwidths to at least a decade below the internal chopping frequency, which is 5 kHz for the **LTC2065**.

The EVAL-LTC2065-TQFN design allows simplified and efficient use. Bulk test points are used for the inputs and outputs. The optimized EVAL-LTC2065-TQFN ground plane, component placement, and power supply allow maximum circuit flexibility and performance. The exposed pad, or EPAD, is shorted to the  $V^-$  pin (also connected to the  $VS^-$  turret), which is required for device operation. The EVAL-LTC2065-TQFN combines surface-mount technology (SMT) with almost all components being 0805 in size to provide simplified installation and the option to replace and solder when needed, except for the bypass capacitors (C1 to C4) that are fixed in 0603 sizes. The EVAL-LTC2065-TQFN also has unpopulated resistor and capacitor pads, which provide the user with the options and flexibility to implement different application circuits and configurations, such as active loop filters, transimpedance amplifiers (TIAs), and sense amplifiers.

### EVALUATION BOARD PHOTOGRAPHS

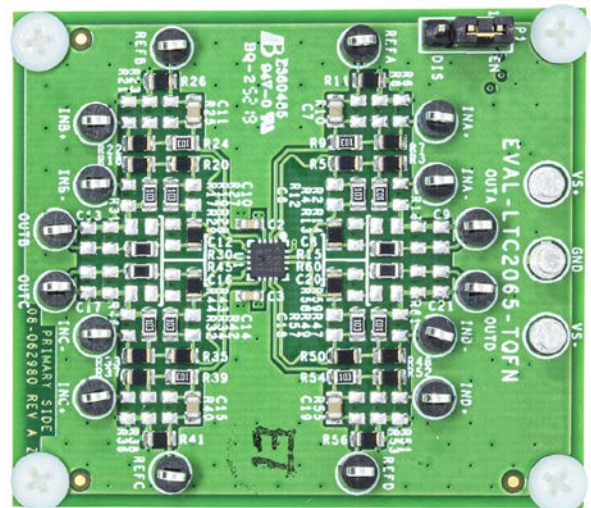


Figure 1. EVAL-LTC2065-TQFN, Primary Side

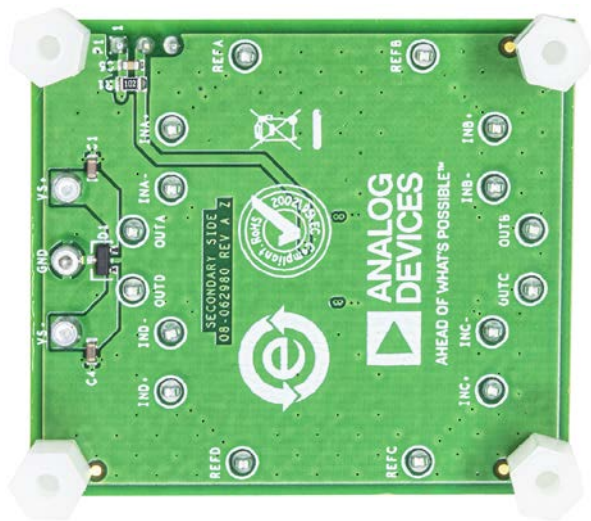


Figure 2. EVAL-LTC2065-TQFN, Secondary Side

For full specifications on the **LTC2065**, see the [LTC2065 data sheet](#), which must be consulted in conjunction with this user guide when using the EVAL-LTC2065-TQFN.

## TABLE OF CONTENTS

Features .....	1	Power Supply Consideration .....	3
Evaluation Kit Contents .....	1	Initial Board Configuration .....	3
Equipment Needed.....	1	Using the Evaluation Board for Testing .....	3
Documents Needed.....	1	Evaluation Board Schematics and Artwork.....	4
General Description .....	1	Ordering Information.....	7
Evaluation Board Photographs.....	1	Bill of Materials .....	7
Revision History .....	2		
Evaluation Board Quick Start Procedures .....	3		

## REVISION HISTORY

3/2020—Revision 0: Initial Version

## EVALUATION BOARD QUICK START PROCEDURES

The following sections outline the basic, prepopulated EVAL-LTC2065-TQFN configuration required to test the basic functionality of the device. All LTC2065 channels are set up with the same configuration. Channel A is used as an example in the following sections.

### POWER SUPPLY CONSIDERATION

Use the turret pins (VS+, VS-, and GND) to power up the EVAL-LTC2065-TQFN. Ensure that the correct polarity and voltage level is used to avoid reverse polarity and overvoltage, which can permanently damage the EVAL-LTC2065-TQFN. The operating supply voltage range is from 1.7 V to 5.25 V. Higher voltages can damage the amplifier. Decoupling capacitors of 10  $\mu$ F and 0.1  $\mu$ F are preinstalled on the EVAL-LTC2065-TQFN for ready operation.

### INITIAL BOARD CONFIGURATION

To set up the initial EVAL-LTC2065-TQFN configuration, take the following steps:

1. Ensure that all equipment is powered down, including the power supply and the signal generator. Use the banana jack to grabber cables to connect the positive supply, ground, and negative supply to the VS+, VS-, and GND turret pins, respectively.
2. Verify that the P1 jumper for  $\overline{\text{SHDN}}$  is in Position 1 (labeled EN) so that the device is enabled.
3. Connect a signal generator at the INA+ bulk test point and GND turret to evaluate Channel A.
4. Connect the oscilloscope 10 $\times$  probe to the OUTA bulk test point and clip the oscilloscope 10 $\times$  probe GND to the GND turret.

### USING THE EVALUATION BOARD FOR TESTING

When the procedure in the Initial Board Configuration section is complete, implement the following settings and verify the expected output:

1. Set the power supply to 2.5 V for the positive supply and -2.5 V for the negative supply, and then turn on the power supply.
2. Configure the signal generator to output a 100 Hz sine wave with 0 V offset and 0.5 V p-p and enable the generator.
3. Set the oscilloscope scaling to 100 mV/2 ms per division. A 100 Hz, 1 V p-p sine wave centered at 0 V appears on the oscilloscope.
4. To evaluate the device shutdown performance, move the P1 jumper into Position 3 (labeled DIS) to tie  $\overline{\text{SHDN}}$  to VS-. There is no output at the OUTA bulk test point. To reenable the device, move the P1 jumper back into Position 1 (labeled EN).

Move to the next channel and repeat Step 2 and Step 3 to test the device functionality of that channel.

EVALUATION BOARD SCHEMATICS AND ARTWORK

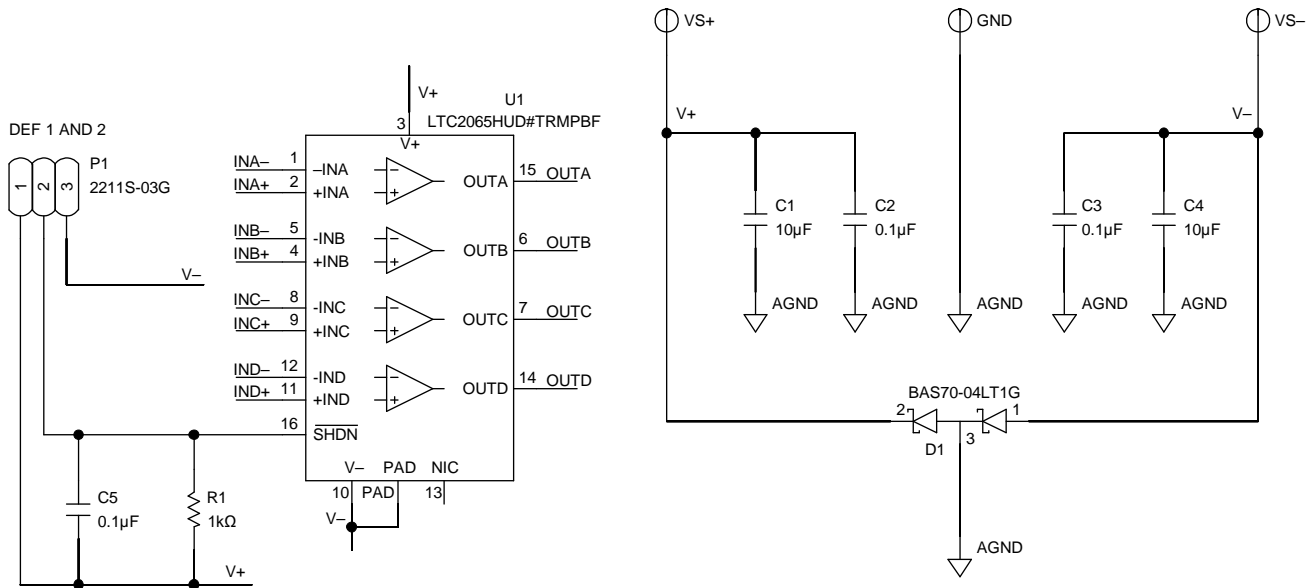


Figure 3. EVAL-LTC2065-TQFN Schematic, Page 1

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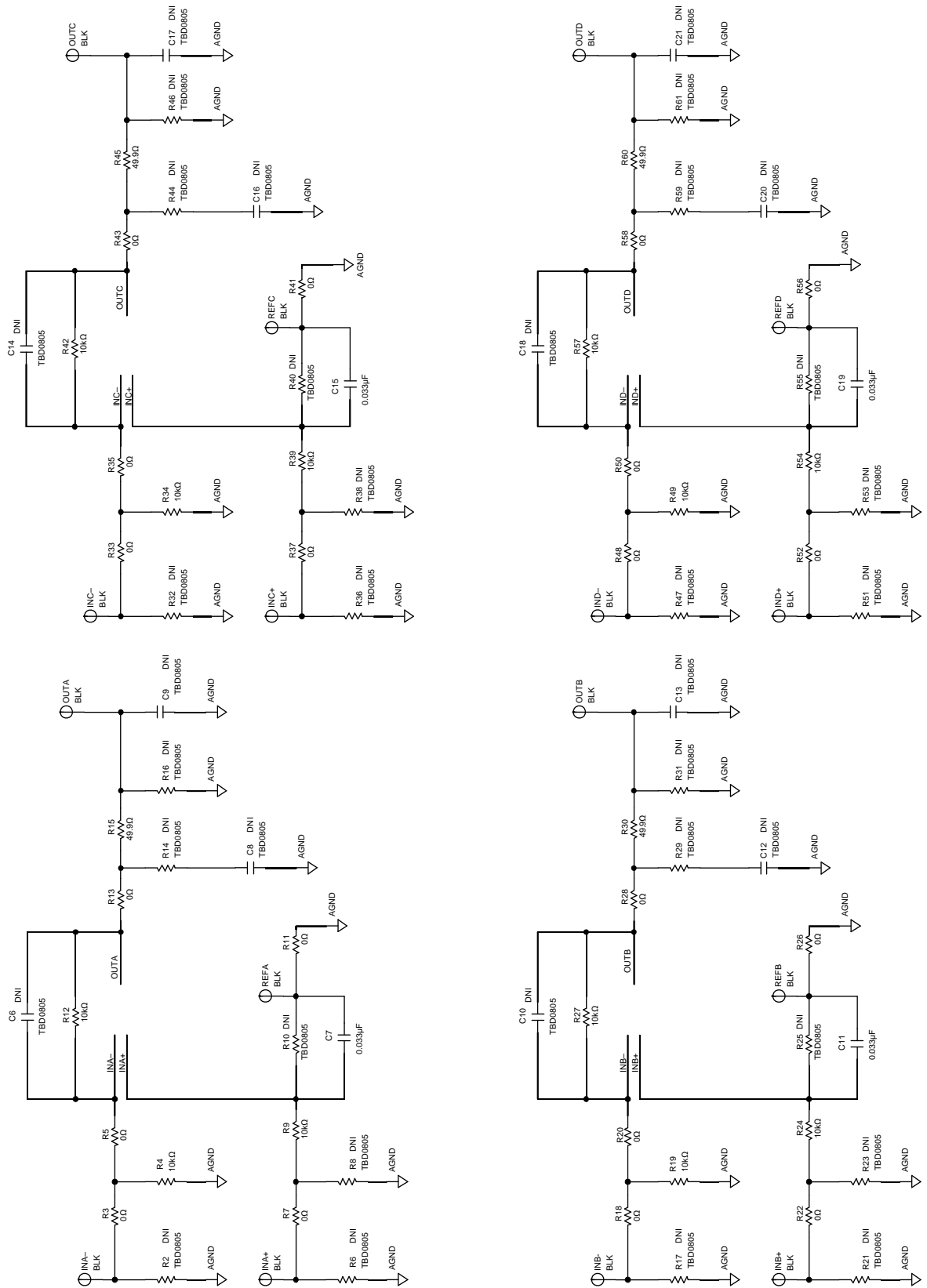
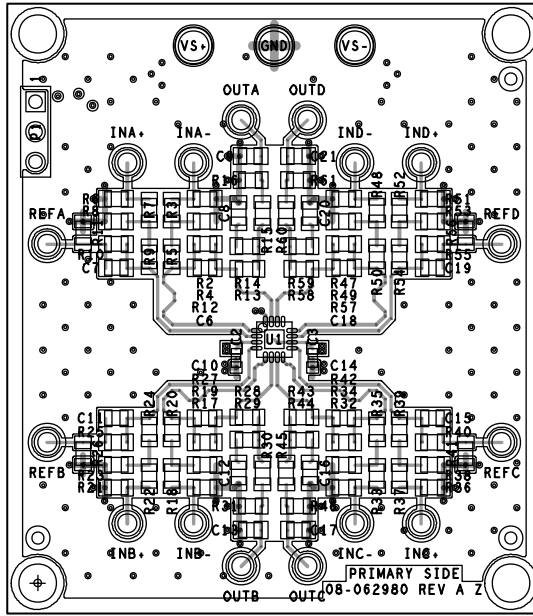
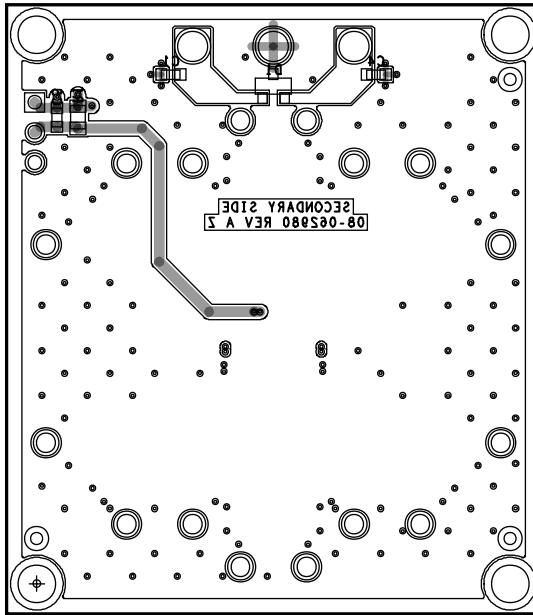


Figure 4. EVAL-LTC2065-TQFN Schematic, Page 2



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Figure 5. EVAL-LTC2065-TQFN Layout Pattern, Primary Side



23178-006

Figure 6. EVAL-LTC2065-TQFN Layout Pattern, Secondary Side

# ORDERING INFORMATION

## BILL OF MATERIALS

Table 1.

Qty	Reference Designator	Description	Part Number
2	C1, C4	Ceramic capacitors, X5R, 0603, 10 $\mu$ F	GRM188R61E106KA73D
3	C2, C3, C5	Ceramic capacitors, X7R, 0603, 0.1 $\mu$ F	C0603C104K3RACTU
12	C6, C8 to C10, C12 to C14, C16 to C18, C20, C21	Capacitors, 0805, user defined	Not applicable
4	C7, C11, C15, C19	Ceramic capacitors, X7R, 0805, 0.033 $\mu$ F	2238 580 15643
1	D1	Diode Schottky barrier	BAS70-04LT1G
3	GND, VS+, VS-	PCB connector, terminal turrets	2501-2-00-80-00-00-07-0
16	INA+, INA-, INB+, INB-, INC+, INC-, IND+, IND-, OUTA, OUTB, OUTC, OUTD, REFA, REFB, REFC, REFD	PCB connector, bulk test points	5006
1	P1	Printed circuit board (PCB) connector, 3-position, male header	2211S-03G
12	R4, R9, R12, R19, R24, R27, R34, R39, R42, R49, R54, R57	Resistors, 10 k $\Omega$	ERA-6AEB103V
1	R1	Resistor, 1 k $\Omega$	ERA-6AEB102V
4	R15, R30, R45, R60	Resistors, 49.9 $\Omega$	ERA-6AEB49R9V
24	R2, R6, R8, R10, R14, R16, R17, R21, R23, R25, R29, R31, R32, R36, R38, R40, R44, R46, R47, R51, R53, R55, R59, R61	Resistors, 0805, user defined	Not applicable
20	R3, R5, R7, R11, R13, R18, R20, R22, R26, R28, R33, R35, R37, R41, R43, R48, R50, R52, R56, R58	Resistors, 0 $\Omega$	CRCW08050000Z0EA
1	U1	2 $\mu$ A supply current, low I <sub>B</sub> , zero-drift, op amp	LTC2065HUD#TRMPBF



**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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