DESCRIPTION

Demonstration circuit 887 features the LTC1408 6-channel, 14-Bit, simultaneous sampling ADC. Total throughput is 600KSPS; 100KSPS per channel, with a typical channel-to-channel aperture skew of 200ps. The board is designed to be used with the DC890B Fast DAACS data collection board to show the AC performance of the LTC1408. Alternatively, the board can be directly connected to an application to evaluate the ADC's performance.

Design files for this circuit board are available. Call the LTC factory.

QUICK START PROCEDURE

BASIC CONNECTIONS

Connect DC887 to a DC890B USB High Speed Data Collection Board using connector J2. Connect DC890B to a host PC with a standard USB A/B cable. Apply 5-7V DC to the VIN and GND terminals. Apply a 10MHz 3.3Vp-p sine wave or square wave to connector J3. Note that J3 has a 50 Ohms termination resistor to ground. CH0-CH5 are provided through connector J1 (See schematic for details.). Run the QuickEval II (Pscope.exe) evaluation software supplied with DC890 or download it from www.linear.com/software.

Figure 1. CONNECTION DIAGRAM

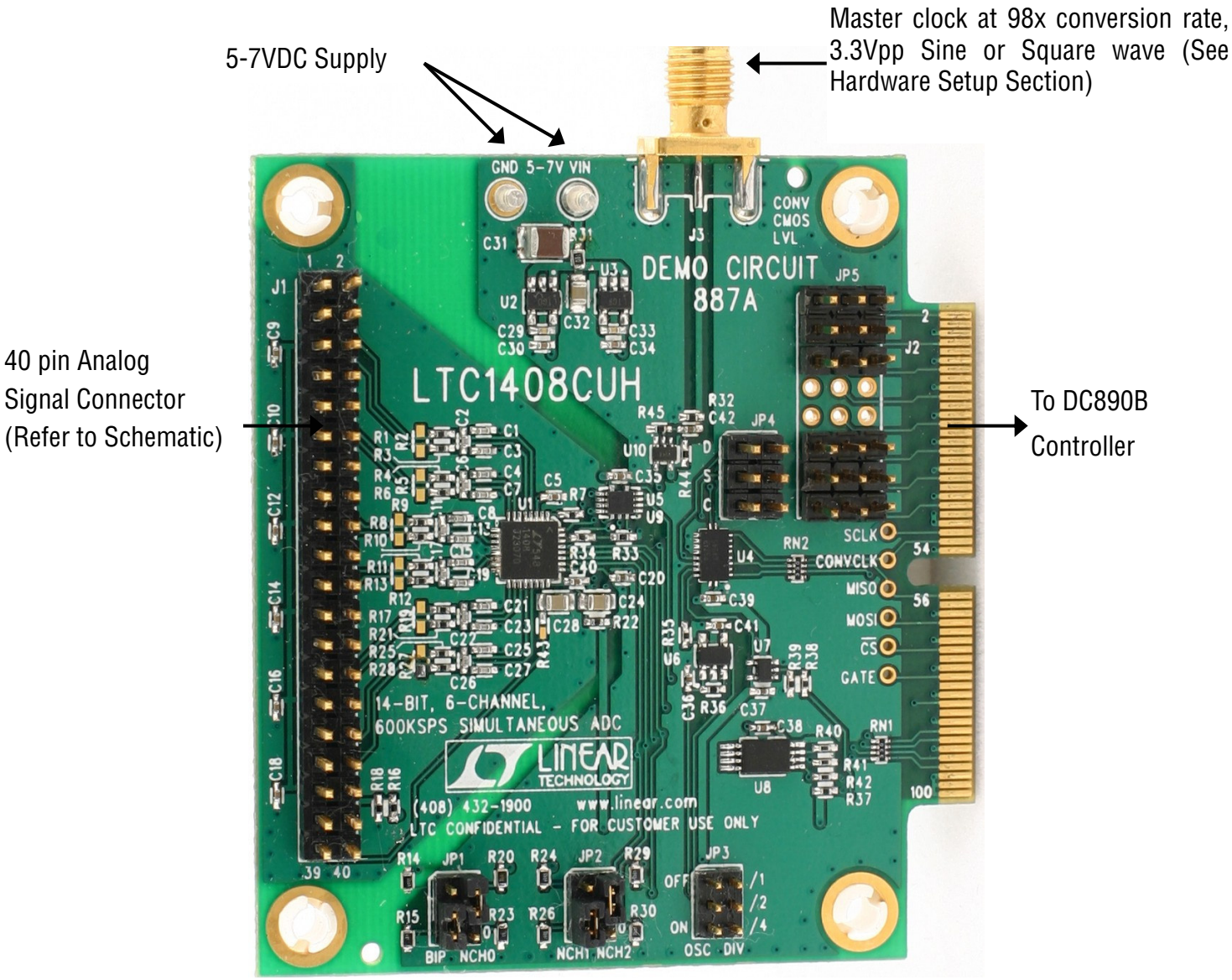


Figure 2. SOFTWARE SCREENSHOT

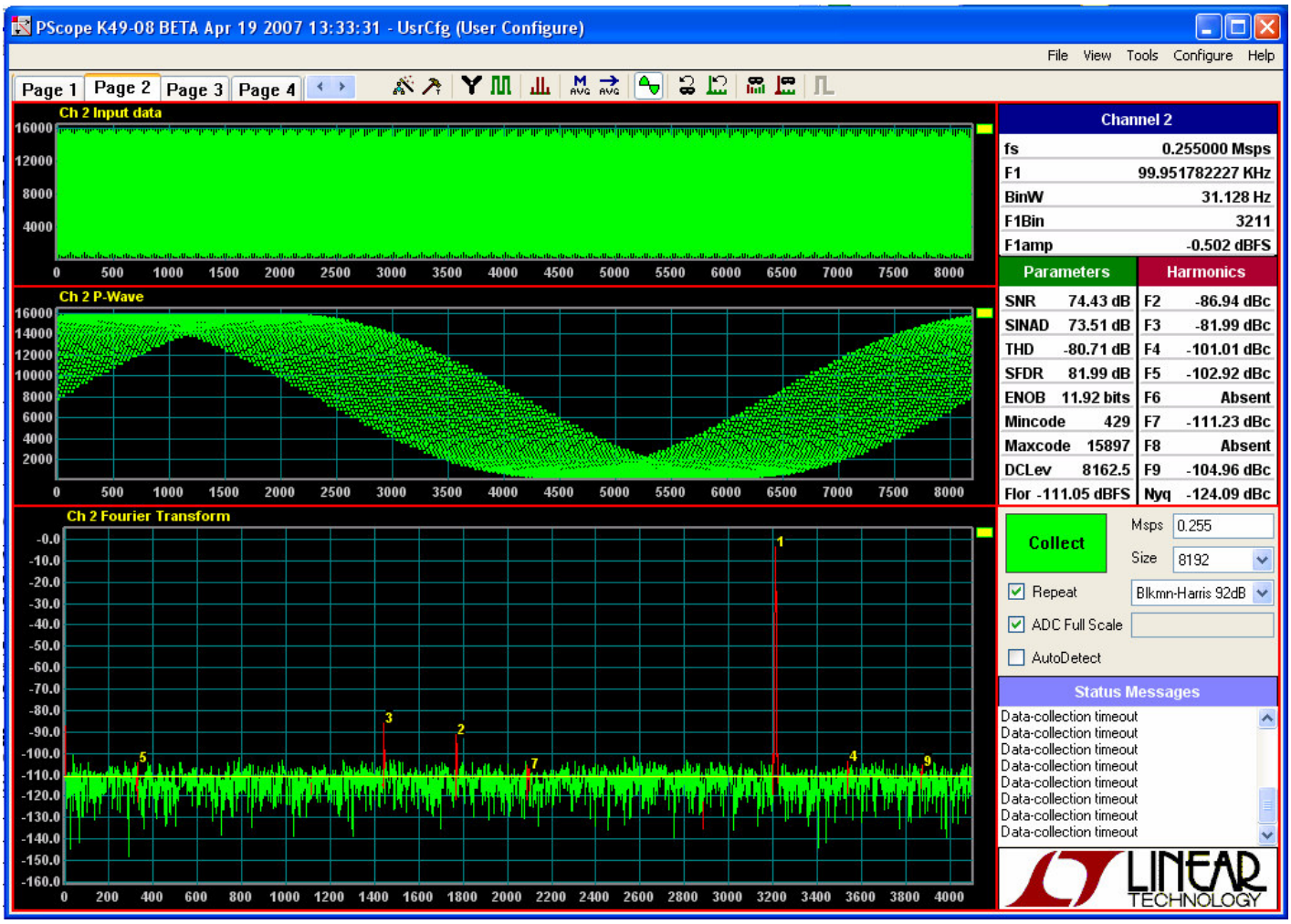
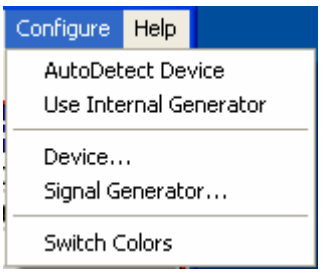
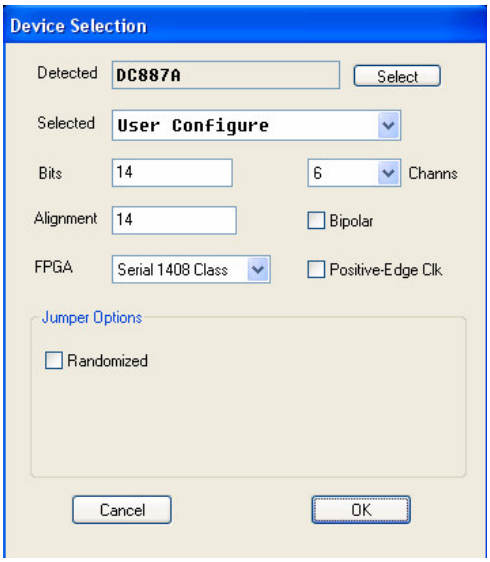


Figure 3. CONFIGURE MENUS





SOFTWARE CONFIGURATION

CONFIGURE DEVICE

The Pscope software should automatically configure itself after detecting the demo board. To change from Bipolar to Unipolar mode it will be necessary to manually configure the software. In the CONFIGURE menu (See Figure 3) select Device, which will bring up another window. In this window, select User Configure and adjust the other settings as follows:

Bits: 14

Alignment: 14

Bipolar: Checked if BIP jumper is set high, Un-Checked if BIP jumper is set to low. (Default is checked)

Channels: 6

Positive Edge Clk: UN-Checked

FPGA: Serial 1408 Class.

CONFIGURE SOFTWARE SCREEN

The software interface is highly configurable and displays any combination of time domain data, frequency domain data, primitive wave and performance parameters (SNR, THD, SINAD, etc.). The screen can be broken into multiple panes as shown in Figure 2. Complete documentation on configuring PSCOPE can be found in the help file.

Click the COLLECT button to begin acquiring data.

Complete software documentation is available from the Help menu item, as features may be added periodically.

HARDWARE SET-UP

JUMPERS

JP1, JP2 - Select number of channels to convert and Unipolar / Bipolar selection. NCH2, NCH1, NCH0 are set to 111 which selects all six channels. These switches should be left in this position when running Pscope software. UNI/BIP selection applies to all channels. Refer to Figure 4.

JP3 – Enable Oscillator and Oscillator Division. Presently not used. This may be used in the future as serial clock, to allow a convert signal at 1X the conversion rate.

JP4 – Digital Interface Header. Provides direct connection to the LTC1408 CONV, SDO, and SCK pins. This can be used to either monitor signals with a logic analyzer or to drive the LTC1408 directly from the customer's test equipment or prototype circuitry. DC890B should be disconnected before driving the LTC1408 externally with JP4. Note that R34 should be removed if the CONV signal is being driven externally.

JP5 – Currently not used

SIGNAL CONNECTIONS

J1 – 40 pin connector with CH0-CH5 differential inputs, multiple grounds, a mid-supply bias voltage and Vref. Refer to schematic for pin out. The mid-supply bias voltage can be used to bias the minus ADC inputs for bipolar conversions.

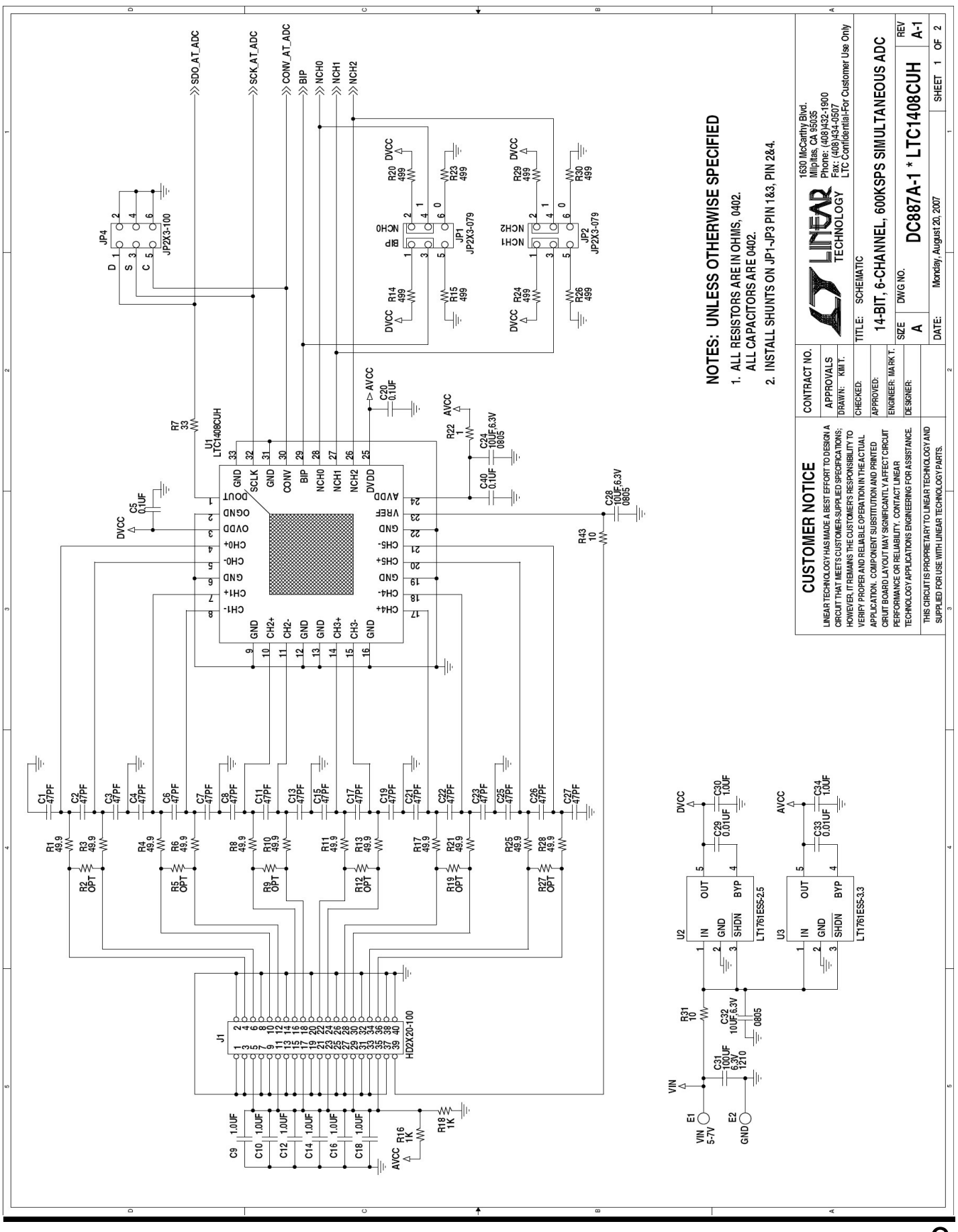
J2 – Data connections to DC890B collection board.

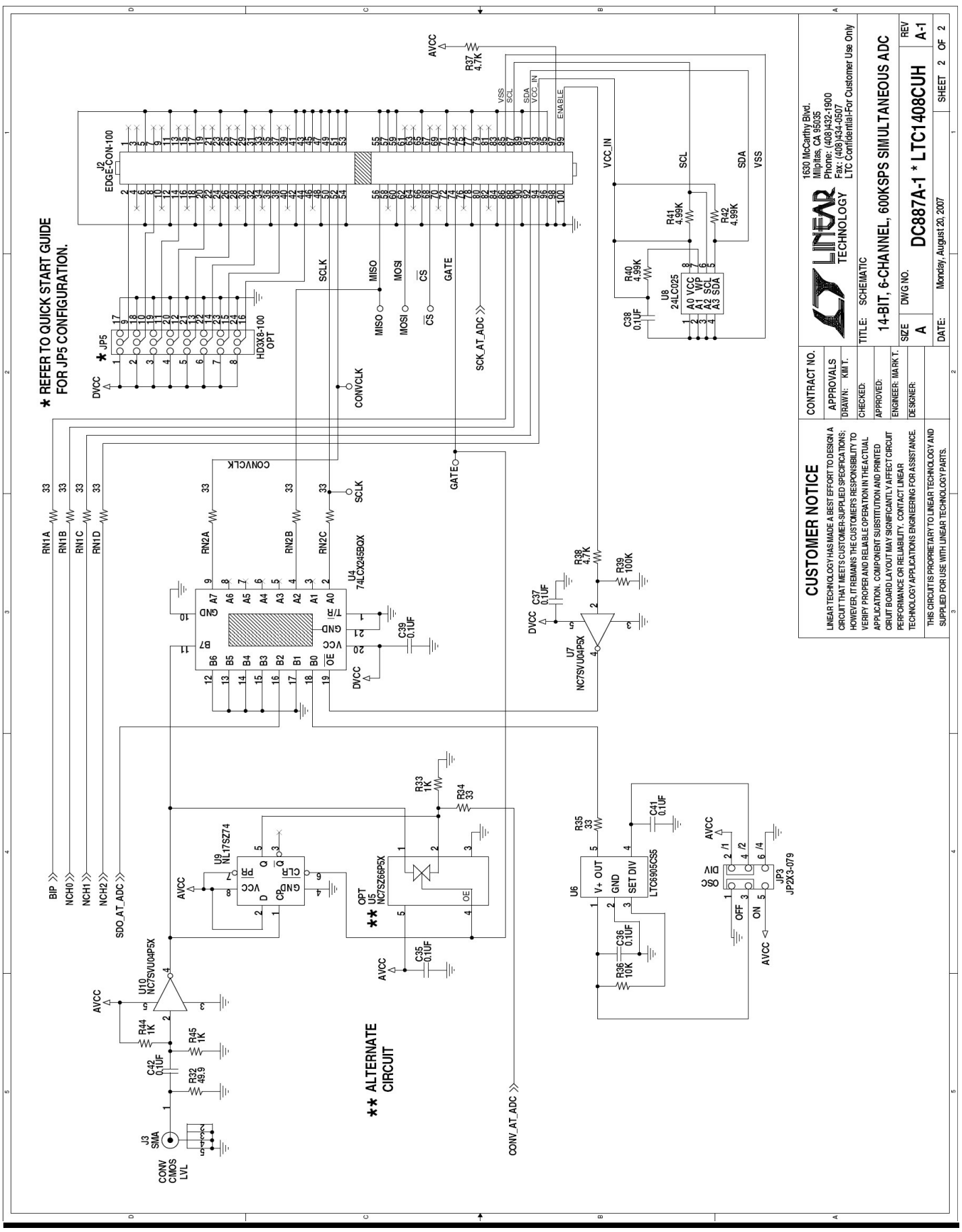
J3 – Conversion Clock Input. This input has a 50 ohm termination resistor, and is intended to be driven by a 3.3Vpp sine or square wave. This clock is divided by 98 in the DC890B collection board to control the serial interface and convert pulse. To run the LTC1408 at maximum conversion rate, apply a 10MHz signal to this input.

GROUNDING AND POWER CONNECTION

Connect a 5V to 7V power supply to the Vin and GND turret posts. For optimum performance, this supply should be floating with respect to any signal generators connected to the analog inputs.

Figure 4 – JP1, JP2 CONFIGURATION


NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 0402.
ALL CAPACITORS ARE 0402.
2. INSTALL SHUNTS ON JP1-JP3 PIN 1&3, PIN 2&4.
CUSTOMER NOTICE
LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER-SUPPLIED SPECIFICATIONS; HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY PROPER AND RELIABLE OPERATION IN THE ACTUAL APPLICATION. COMPONENT SUBSTITUTION AND PRINTED CIRUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT LINEAR TECHNOLOGY APPLICATIONS ENGINEERING FOR ASSISTANCE.
THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.
CONTRACT NO.
APPROVALS
DRAWN: KIM T.
CHECKED:
APPROVED:
ENGINEER: MARK T.
DESIGNER:
LINEAR TECHNOLOGY
1630 McCarthy Blvd.
Milpitas, CA 95035
Phone: (408)432-1900
Fax: (408)434-0507
LTC Confidential-For Customer Use Only
TITLE: SCHEMATIC
14-BIT, 6-CHANNEL, 600KSPS SIMULTANEOUS ADC
SIZE A
DWG NO. DC887A-1 * LTC1408CUH
REV A-1
DATE: Monday, August 20, 2007
SHEET 1 OF 2


* REFER TO QUICK START GUIDE FOR JP5 CONFIGURATION.
** ALTERNATE CIRCUIT
CUSTOMER NOTICE
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SIZE A
DWG NO. DC887A-1 * LTC1408CUH
REV A-1
DATE: Monday, August 20, 2007
SHEET 2 OF 2

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