

LTC4121EUD/LTC4121EUD-4.2 400mA Synchronous Buck Battery Charger

DESCRIPTION

DC1977A-A	LTC4120EUD-4.2 (Fixed Output)
DC1977A-B	LTC4121EUD (Adjustable Output)

Demonstration Board DC1977A showcases the [LTC4121-4.2](#) and [LTC4121](#) 40V, 400mA synchronous-buck battery charger integrated circuit. The DC1977A supports the maximum-power-point tracking (MPPT) feature of the LTC4121EUD to optimize power delivery from photovoltaic cells or highly resistive sources.

The LTC4121 and LTC4121-4.2 feature constant-current-constant-voltage charging capability suitable for lithium-ion or lead-acid cells. The LTC4121-4.2 supports charging a single lithium-ion cell with a cell voltage of 4.2V. The LTC4121 may be programmed to charge battery voltages up to 18V with a resistive divider.

Design files for this circuit board are available at <http://www.linear.com/demo/DC1977>

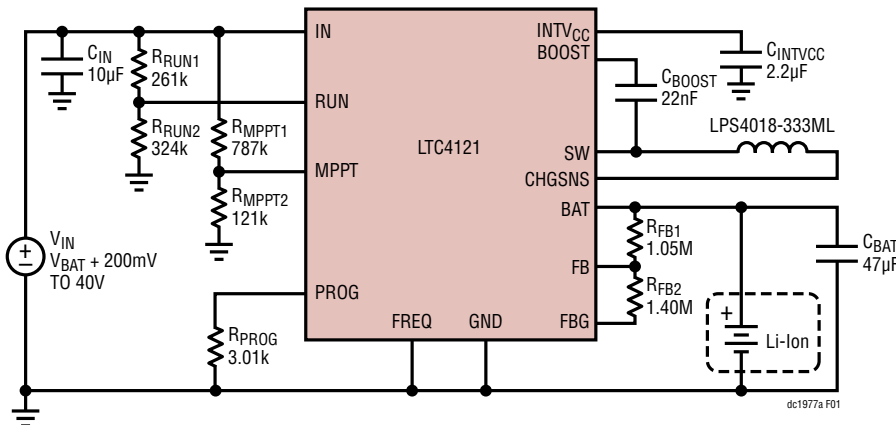
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PERFORMANCE SUMMARY Specifications are at T_A = 25°C

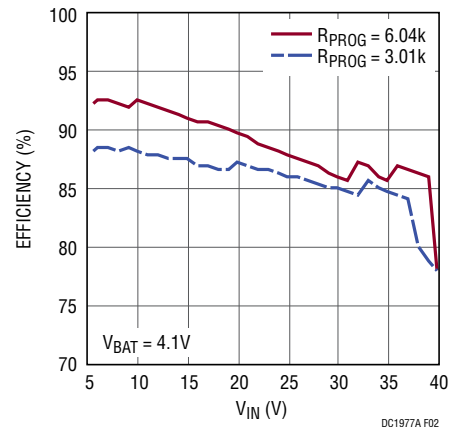
SYMBOL	PARAMETER	CONDITIONS <small>Note: Reference designators refer to Schematic on p. 7.</small>	MIN	TYP	MAX	UNITS
IN	DC1977A Input Voltage	I(IN) < 800mA	4.4		40	V
PV _{IN}	DC1977A PV Cell Input	I(IN) < 800mA	5		40.5	V
V(BAT)	DC1977A BAT Pin Voltage	R11 = 1.40MΩ, R12 = 1.05MΩ	2.5		4.25	V
I(BAT)	DC1977A BAT Pin Current	V(BAT) = 3.7V; DC1977A; (R7) = 3.01kΩ; JP1 ("MPPT") = 'OFF'	383	402	421	mA

DEMO BOARD APPLICATION

High Efficiency, Wide Input Voltage Range Charging with LTC4121



LTC4121 Efficiency vs V_{IN}



DEMO MANUAL

DC1977A-A/DC1977A-B

ASSEMBLY TEST PROCEDURE

Refer to Figure 1 for the proper measurement equipment setup and jumper settings and follow the procedure below.

1. Set JP1 ("MPPT") to 'ON', set PS1 to 3.6V and turn on.
2. Connect PS2 to point A, set to 15V and turn on.
3. Verify that VM1 indicates 3.3V to 3.9V, and then verify that AM1 indicates 387mA to 417mA. Verify that VM2 shows 14.5V to 15.1V. There is only a series diode between PV+ and the V_{IN} pin of the LTC4121. The purpose of this diode is prevent backfeeding a PV cell, if connected. A single diode V_f is insufficient to activate the MPPT feature, and the LTC4121 delivers full charge current to the battery.
4. Turn PS2 off, move connection to point B, and turn PS2 on.
5. Verify that VM1 indicates 3.3V to 3.9V, and then verify that AM1 indicates 387mA to 417mA. Verify that VM2 shows 12.6V to 13.2. The source impedance of the power supply is now $\approx 16\Omega$. But this impedance still allows delivering full charge current without engaging the MPPT feature.
6. Turn PS2 off, move connection to Point C, and turn PS2 on.
7. Verify that VM1 indicates 3.3V to 3.9V, and then Verify that AM1 indicates 105mA to 115mA. Verify that VM2 shows 10.6V to 11.3V. The source impedance of the power supply is now 98Ω . The MPPT feature has engaged and the charge delivered to the battery has been reduced to allow V_{IN} to stay at the programmed MPPT point.
8. Set JP1 ("MPPT") to 'OFF', test is finished.

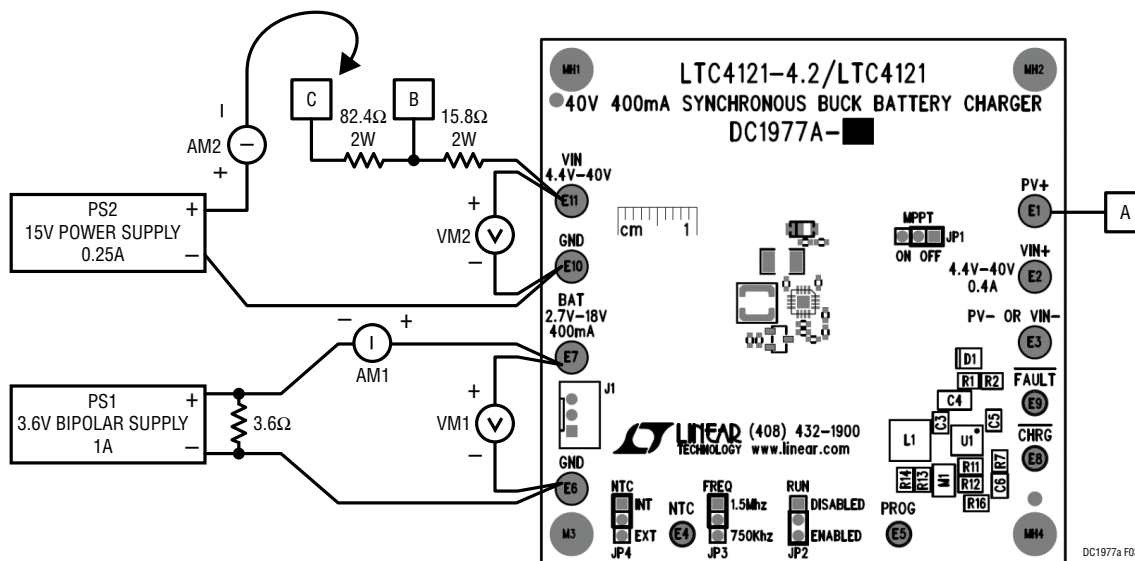


Figure 1. DC1977A Equipment Setup

Note: All connections from equipment should be kelvin-connected directly to the board pins which they are connected on this diagram. All input or output leads should be twisted pair.

THEORY OF OPERATION

The LTC4121EUD-4.2/LTC4121EUD is a 4.4V ~ 40V input buck topology battery charger with maximum power point tracking (MPPT) for use with PV cells or highly resistive power supplies. The buck-topology charger uses current mode control for stable operation.

LTC4121EUD ENABLE

The LTC4121 can be enabled or disabled via the RUN pin, and this functionality can be accessed via JP2, the RUN jumper. When JP2 is in the “ENABLE” position, R3 and R4 ensure that the LTC4121 is not enabled until V_{in} is greater than 4.4V.

Note: Do not float the LTC4121 RUN pin. Operate the demo board with JP2 in either the DISABLED or ENABLED position.

Buck Charger

The heart of the LTC4121EUD is the buck-topology battery charger. The buck-topology charger is a synchronous, current-mode-control regulator with N-channel FETs. The use of N-channel FETs minimizes conduction losses, and requires only a single external 0.022 μ F capacitor to generate the high-side gate drive.

The LTC4121EUD can charge up to four Li-Ion cells in series, and supports a maximum battery voltage of 18V. The LTC4121EUD-4.2 is optimized for charging a single Li-Ion cell to a fixed cell voltage of 4.2V.

The current in the buck inductor passes through a small on-die resistor for current measurement, and then goes back out to the BAT pin. The battery is connected to the BAT pin; this allows the LTC4121EUD to measure not only the cycle-by-cycle current, but also the average current. The cycle-by-cycle current is used by the current-mode buck regulator, and the average current is the battery charge current as programmed by R_{PROG} . On DC1977A, $R_{PROG} = 3.01k\Omega$, so $I(BAT) = 402mA$ provided that the MPPT function does not reduce the current.

The buck regulator acts as a current source when the battery is in the constant-current charging region and as a classic voltage output buck regulator when the battery is in the constant-voltage charging region.

The battery charge current is programmed by $R_{PROG} = 3.01k\Omega$. The equation for R_{PROG} is:

$$R_{PROG} = h_{PROG} \cdot \frac{V_{PROG}}{I_{CHG}} = 986 \cdot \frac{1.227V}{0.4} = 3.01k\Omega$$

The LTC4121EUD provides a switching frequency select pin, FREQ, to select between 750kHz and 1.5MHz; this function is accessed by JP4, the “FREQ” jumper.

Note: Do not float the LTC4121 FREQ pin. Operate the demo board with JP3 in either the 750kHz or 1.5MHz position.

Figure 2 shows various nodes of interest with $V_{IN} = 5V$, and the switching frequency at 750kHz ($T = 1.333\mu s$). The duty cycle is 86% for $V(BAT) = 3.6V$, not the 72% duty expected from a buck regulator. When the battery voltage is 3.6V, the charger is in constant-current mode, so the control loop is forcing the output of the buck regulator to the voltage necessary to push 400mA into the battery. This “effective” voltage, $5 \cdot 0.86 = 4.3V$, is the voltage necessary to ensure that a 400mA average current is flowing through the on-die sense resistor.

Figure 3 shows the same nodes as Figure 2, but with $V_{IN} = 40V$. The switching frequency is still 750kHz. The duty cycle is $\approx 200ns/1.333\mu s$, or 15%, but the period is 2.7 μs . This is because the LTC4121 minimum on time was greater than that needed to achieve 4.3V, and the LTC4121 starts to pulse skip to get the necessary average duty cycle. The average duty cycle is $300ns/2.667\mu s = 11\%$. This produces an output voltage of 4.3V, so the battery still charges at 400mA.

Maximum Power Point Tracking (MPPT)

The LTC4121EUD provides a maximum-power-point tracking (MPPT) function for use with PV cells or highly

THEORY OF OPERATION

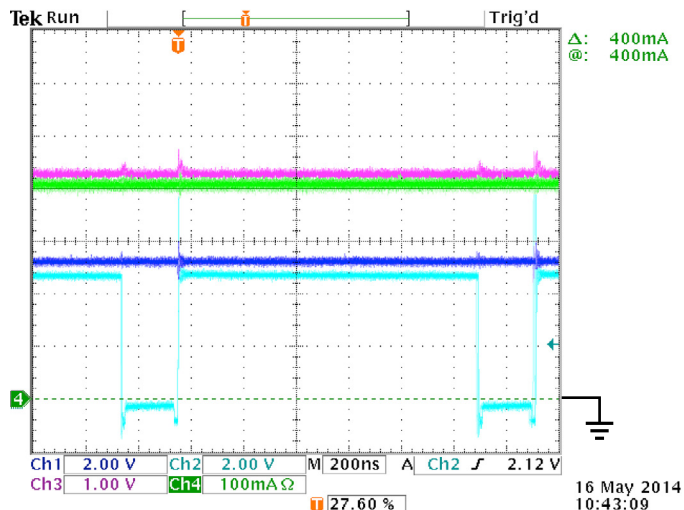


Figure 2. Normal Operation, Zoom, $V_{IN} = 5.1V$, DK. Blue = V_{IN} , Grn = I_{CHARGE} , LT. Blue = V_{SW} , Pk. = $INTV_{CC}$, 750kHz

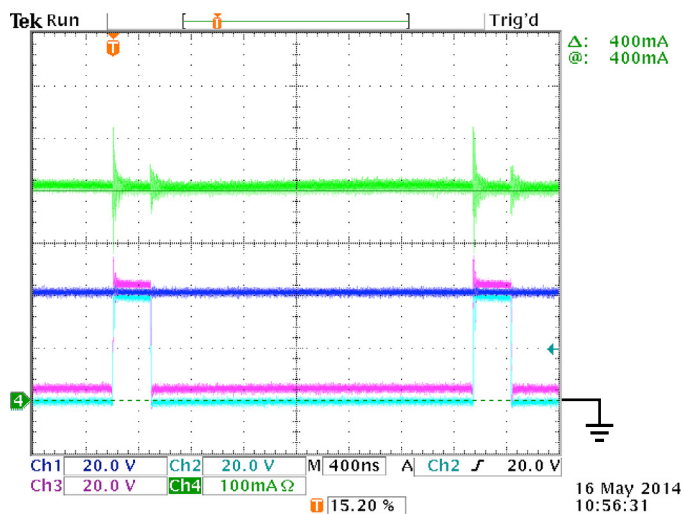


Figure 3. Normal Operation, Zoom, $V_{IN} = 40V$, DK. Blue = V_{IN} , Grn = I_{CHARGE} , LT. Blue = V_{SW} , Pk. = V_{BOOST} , 750kHz

resistive power supplies. The MPPT pin allows programming of the MPPT point as a percentage of the open-circuit V_{IN} (V_{OC}). To access this functionality the demo board provides JP1, the “MPPT” jumper, and R1 and R2.

It is important to note that the disabled position for MPPT is the MPPT pin at V_{IN} . To enable MPPT, set the MPPT point as a fraction of V_{OC} . See the discussion in Maximum Power Point Tracking section of the LTC4121 data sheet.

When MPPT is enabled (not equal to V_{IN}), the LTC4121EUD periodically disconnects the load from the power source, and measures V_{IN} with no load = V_{OC} . It then increases the load on V_{IN} to meet charger demand until the V_{MPPT} threshold is reached, after which it no longer increases the load. This allows the MPPT voltage divider to set the desired MPPT point as a percentage of V_{IN} with no load.

Figure 4 shows the LTC4121EUD operating from a source impedance of 98Ω . The MPPT pin of the LTC4121EUD sets the MPPT point to 0.75 of the open-circuit voltage. First, V_{OC} is determined by removing all load and letting V_{IN} rise to V_{OC} . The power drawn from V_{IN} is increased until the voltage at V_{IN} falls to the MPPT point, $0.75 \cdot V_{OC} = 0.75 \cdot 15V = 11.25V$. The resolution of the MPPT DAC is 330mV, thus this example has the MPPT point at 11V. The LTC4121 stops drawing power at this point, and the charge current (green) never exceeds 200mA, even though the Rprog value was chosen for 400mA.

Figure 5 shows the same system, but the source impedance was lowered to 16Ω . Consequently, the full power needed to meet the requirements of the programmed charge current is available before V_{IN} falls to the MPPT voltage.

THEORY OF OPERATION

Battery capacitors C1 and C2

The maximum battery voltage for the LTC4121EUD is 18V, and for the LTC4121EUD-4.2, it is 4.2V. Analog Devices recommends 47 μ F of capacitance on the BAT pin, if the battery is not present. For the LTC4121EUD the voltage rating of the capacitor will need to be 25V, so two 22 μ F, 25V, MLCC capacitors are used. In the case of the LTC4121EUD-4.2, a 6.3V capacitor will suffice, and a single 47 μ F, 6.3V, MLCC capacitor is used for C1, with C2 not placed.

Reverse-Blocking Circuit

Components Q1, R16 and C6 comprise a reverse-blocking circuit. The circuit performs two functions. First, the circuit prevents the battery from back-charging the power source when the power source is dormant (e.g., a solar cell in the absence of illumination). Note that this functionality can also be provided through D1. Second, when a charged battery is connected to the circuit in the absence of input voltage, current will flow from the battery into the BAT pin and out the IN pin, charging C4. With battery voltages in excess of ~10V, this current surge can destroy the device. Note that this is not a problem when only one or two series Li-Ion cells are employed. Thus, this reverse-blocking circuit may not be necessary depending on the application. If reverse-blocking is not required, C6 and R16 also become unnecessary. These two components provide a path to the BAT pin from which the LTC4121 derives bias for internal circuits which would be provided by the battery directly in the absence of Q1. See, for example, the application on the first page of this manual.

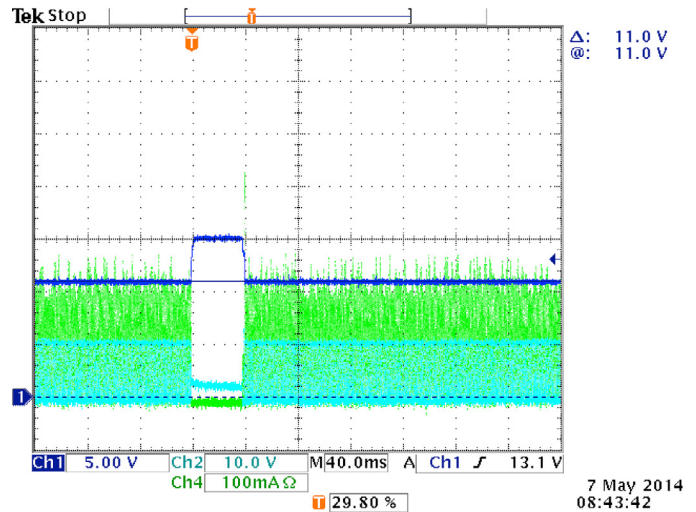


Figure 4. MPPT Test, DK. Blue = V_{IN} (Through 98 Ω), Green = I_L , LT. Blue = $V(SW)$, $k = 0.15$, $V_{MPPT}/V_{OC} = 0.75$

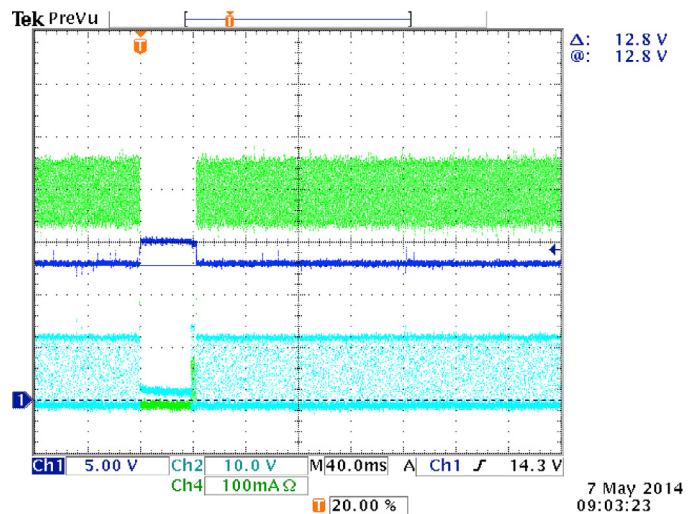


Figure 5. MPPT Test, DK. Blue = V_{IN} (Through 16 Ω), Green = I_L , LT. Blue = $V(SW)$, $k = 0.15$, $V_{MPPT}/V_{OC} = 0.75$

DEMO MANUAL

DC1977A-A/DC1977A-B

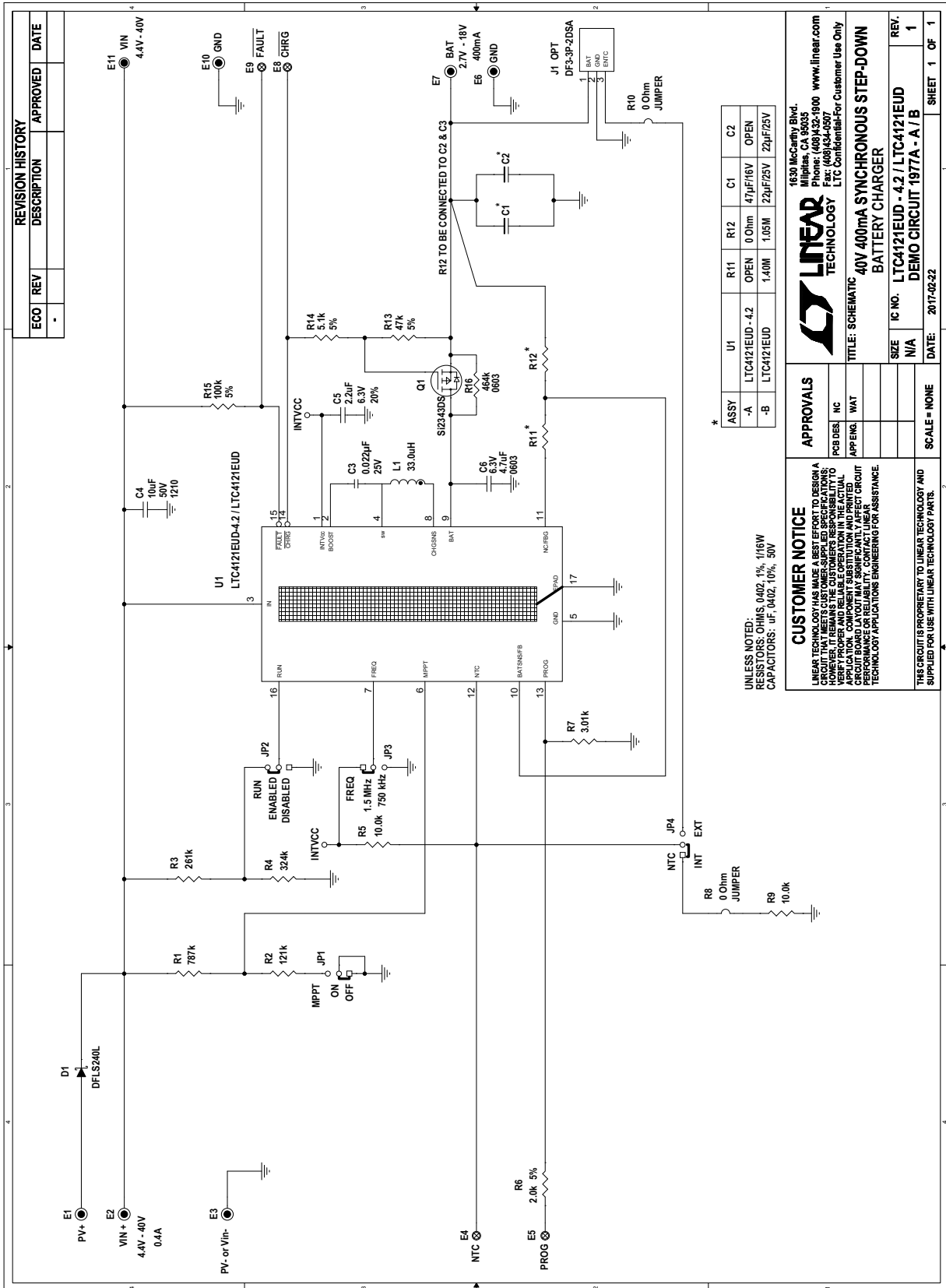
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
DC1977A General Bill of Materials				
Required Circuit Components				
1	1	C3	CAP, CHIP, X7R, 0.022 μ F, \pm 10%, 50V, 0402	TDK, C1005X7R1E223K
2	1	C4	CAP, CHIP, X5R, 10 μ F, \pm 10%, 50V, 1210	TAIYO-YUDEN, UMK325BJ106KM-T
3	1	C5	CAP, CHIP, X5R, 2.2 μ F, \pm 20%, 6.3V, 0402	MURATA, GRM155R60J225ME15D
4	1	L1	IND, SMT, 33 μ H, 420m Ω , \pm 20%, 0.80A, 4mm \times 4mm	COILCRAFT, LPS4018-333ML
5	1	R1	RES, CHIP, 787k Ω , \pm 1%, 1/16W, 0402	VISHAY, CRCW0402787KFKED
6	1	R2	RES, CHIP, 121k Ω , \pm 1%, 1/16W, 0402	VISHAY, CRCW0402121KFKED
7	1	R3	RES, CHIP, 261k Ω , \pm 1%, 1/16W, 0402	VISHAY, CRCW0402261KFKED
8	1	R4	RES, CHIP, 324k Ω , \pm 1%, 1/16W, 0402	VISHAY, CRCW0402324KFKED
9	1	R7	RES, CHIP, 3.01k Ω , \pm 1, 1/16W, 0402	VISHAY, CRCW04023K01FKED
Additional Demo Board Circuit Components				
1	1	C6	CAP, CHIP, X5R, 4.7 μ F, \pm 20%, 6.3V, 0603	MURATA, GRM188R60J475KE19D
2	1	D1	DIODE, SCHOTTKY, 40V, 2A, PowerDI123	DIODES, DFLS240L
3	1	M1	MOSFET, P-Channel, -30V, -5.9A, 45m Ω , SOT-23	VISHAY, Si2343CDS
4	2	R5, R9	RES, CHIP, 10k Ω , \pm 1%, 1/16W, 0402	VISHAY, CRCW040210K0FKED
5	1	R6	RES, CHIP, 2k Ω , \pm 5%, 1/16W, 0402	VISHAY, CRCW04022K00JNED
6	2	R8, R10	RES, CHIP, 0 Ω jumper, 1/16W, 0402	VISHAY, CRCW04020000Z0ED
7	1	R13	RES, CHIP, 47k Ω , \pm 5%, 1/16W, 0402	VISHAY, CRCW040247K0JNED
8	1	R14	RES, CHIP, 5.1k Ω , \pm 1%, 1/16W, 0402	VISHAY, CRCW04025K10JNED
9	1	R15	RES, CHIP, 100k Ω , \pm 5%, 1/16W, 0402	VISHAY, CRCW0402100KJNED
10	1	R16	RES, CHIP, 464k Ω , \pm 1%, 1/10W, 0603	YAGEO, RC0603FR-07464KL
Hardware: For Demo Board Only				
1	7	E1, E2, E3, E6, E7, E10, E11	TURRET, 0.09 DIA	MILL-MAX, 2501-2-00-80-00-00-07-0
2	4	E4, E5, E8, E9	TURRET, 0.061"	MILL-MAX, 2308-2-00-80-00-00-07-0
3	0	J1-OPT	CONN, 3 Pin Polarized	HIROSE, DF3-3P-2DSA
4	4	JP1-JP4	HEADER, 3 Pin, SMT, 2mm	SULLIN, NRPNO31PAEN-RC
5	4	JP1-JP4	SHUNT, 2mm	SAMTEC, 2SN-BK-G

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
DC1977A-A Bill of Materials				
Required Circuit Components				
1	0	R11	DO NOT INSTALL	
2	1	R12	RES, CHIP, 0 Ω jumper, 1/16W, 0402	VISHAY, CRCW04020000Z0E
3	1	U1	40V 400mA SYNCHRONOUS STEP-DOWN BATTERY CHARGER, 3mm \times 3mmQFN16	LINEAR TECH., LTC4121EUD-4.2#PBF
1	1	C1	CAP, CHIP, X5R, 47 μ F, \pm 10%, 16V, 1210	MURATA, GRM32ER61C476KE15L
2	0	C2	CAP, CHIP, X5R, 47 μ F, \pm 10%, 16V, 1210	MURATA, GRM32ER61C476KE15L

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
DC1977A-B Bill of Materials				
Required Circuit Components				
1	1	R11	RES, CHIP, 1.40M Ω , \pm 1%, 1/16W, 0402	VISHAY, CRCW04021M40FKE
2	1	R12	RES, CHIP, 1.05M Ω , \pm 1%, 1/16W, 0402	VISHAY, CRCW04021M05FKED
3	1	U1	40V, 400mA SYNCHRONOUS STEP-DOWN BATTERY CHARGER, 3mm \times 3mmQFN16	LINEAR TECH., LTC4121EUD#PB
1	2	C1, C2	CAP, CHIP, X5R, 47 μ F, \pm 10%, 16V, 1210	MURATA, GRM32ER61C476KE15L

SCHEMATIC DIAGRAM



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DEMO MANUAL

DC1977A-A/DC1977A-B

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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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