

LT6411 High-Speed
 ADC Driver Combo
 Board

DESCRIPTION

Demonstration circuit 1057 is a reference design featuring Linear Technology Corporation's LT6411 High Speed Amplifier/ADC Driver with an on-board LTC2249 14-bit, 80MSPS ADC. DC1057 demonstrates good circuit layout techniques and recommended component selection for optimal system performance. The ADC driver input and output networks are flexible, allowing for AC or DC coupling, gains of 0dB or 6dB, single-ended or differential configurations, and signal low-pass or band-pass filtering before the ADC.

DC1057 also allows the flexibility of selecting the CMOS output supply voltage. DC1057 includes an on-board 40-pin edge connector for use with the DC718 Data Acquisition demo board and Linear Technology's QuickEval-II data processing software, available on our website at <http://www.linear.com>.

Design files for this circuit board are available. Call the LTC factory.

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QUICK START PROCEDURE

Validating the performance of the LT6411 ADC Driver-ADC combination is simple with DC1057, and requires only two signal generators and some basic lab equipment. Table 1 shows the function of each I/O connector and selectable jumper on the board. Refer to Figure 1 for proper board evaluation equipment setup and follow the procedure below:

1. Connect the power supplies as shown. The power supply connector labeled VCC powers the ADC driver. VDD powers the ADC, and OVDD provides power to both the ADC output stage and the two CMOS output buffers. The entire board and all components share common ground planes. Check the supply voltages before applying power, to avoid damage from over-voltage conditions.
2. Provide an encode clock to the ADC via SMA connector J4. For best performance, a high-quality sine wave synthesizer with an external band-pass filter will provide a stable, low-phase-noise clock source. A crystal oscillator will also provide good performance. DC1057 includes an

on-board clock amplifier/buffer IC to provide a large-amplitude clock source to the ADC.

NOTE. A poor quality encode clock can significantly degrade the signal-to-noise ratio (SNR) of the driver-ADC combination.

Table 1: DC1057 Connectors and Descriptions

REFERENCE	FUNCTION
J1 (AIN+)	Analog Input (50Ω termination impedance)
J2 (AIN-)	Analog Input (by default, tied to ground via resistor R16 for single-ended-to-differential conversion)
J3 (40-pin conn)	Provides direct connection to DC718. CMOS Output Buffers provide parallel data output and clock signals (see schematic)
J4 (Encode Clock)	ADC Encode Clock. For best performance, use a high-quality low-jitter clock source.
JP1 (ENABLE)	Enable/Disable LT6411. Default is EN.

3. Apply an input signal to the board. DC1057 allows great flexibility in applying input signals (see the section on Applying Input Signals). For best results, use a low distortion, low noise signal generator with high order low-pass or band-

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pass filtering to avoid degrading the performance of the ADC driver and ADC.

4. Observe the ADC output with demo circuit DC718, a USB cable, a Windows computer, and Linear Technology's QuickEval-II data process-

ing software. See Figure 2 for the general board evaluation setup diagram.

NOTE. See the DC718 Quick Start Guide for instructions on using the DC718 QuickDAACS data acquisition demo board.

NOTE. Even a high-quality signal synthesizer will still have noise and harmonics that could be attenuated with a low-pass or band-pass filter. For good-quality high order filters, see TTE, Lark Engineering, or equivalent.

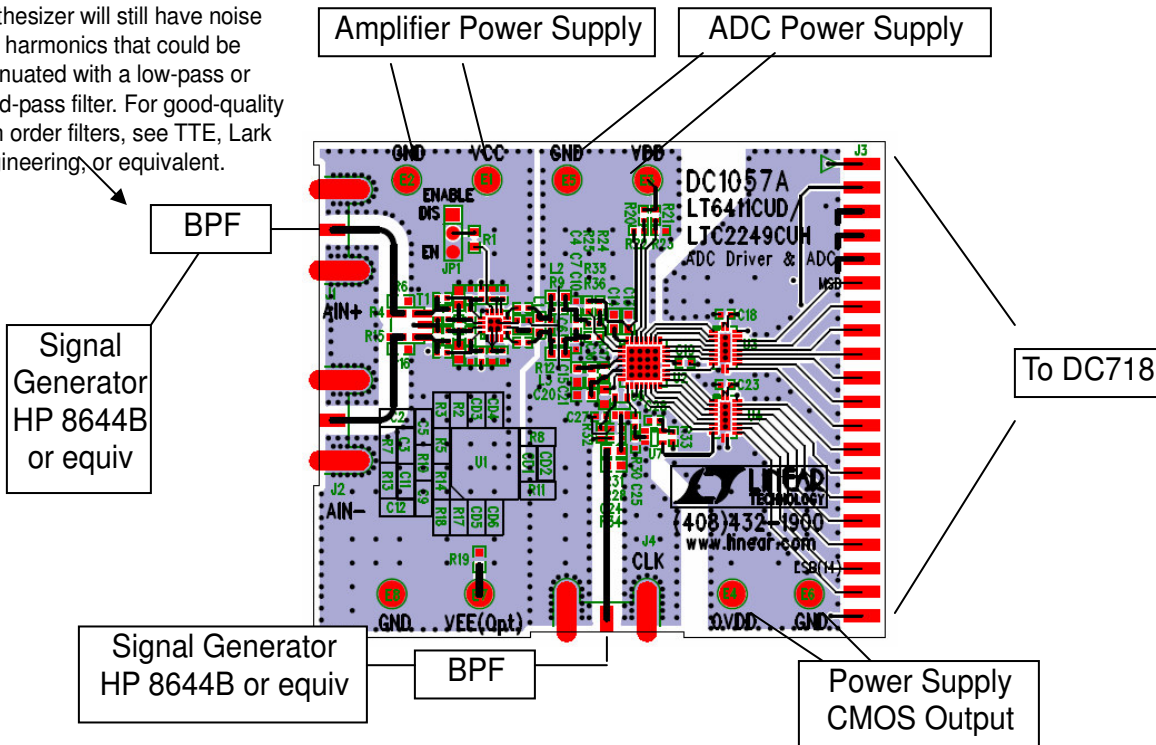


Figure 1. Proper Evaluation Equipment Setup

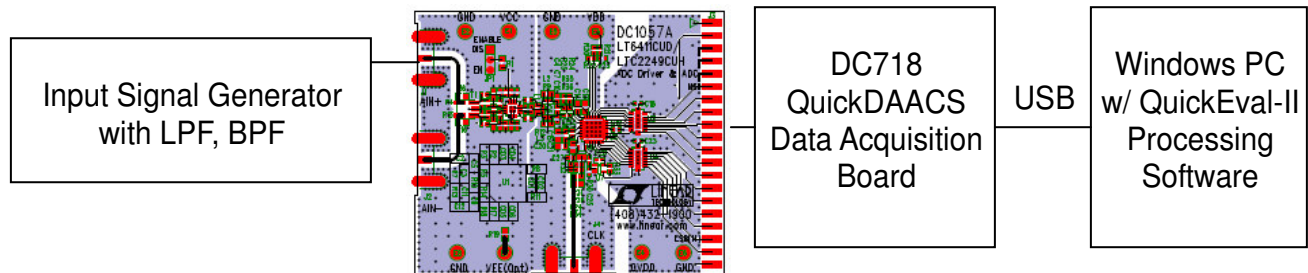


Figure 2. Evaluation Setup with DC718, Computer, and QuickEval-II Software

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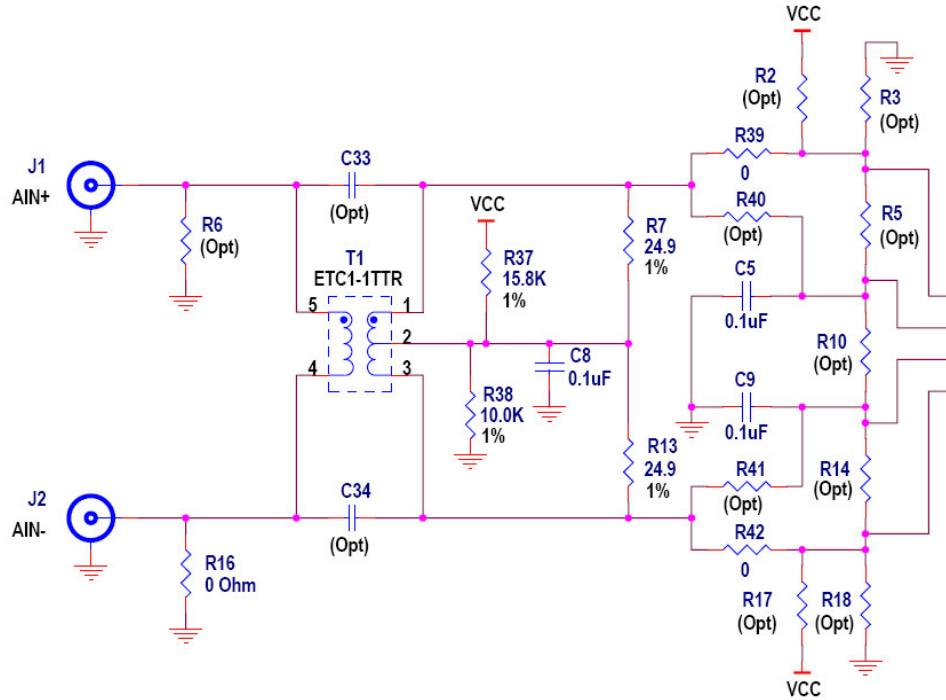


Figure 3. DC1057 Input Network, see Table 2 and text for configuration options

ADDITIONAL INFORMATION

Although the DC1057 demo board is ready to use, it has additional flexibility built in for various types of input networks, filtering configurations, and single-ended or differential inputs. Below is some information about configuring DC1057 to meet the specific needs of any application.

APPLYING INPUT SIGNALS

The input network consists of various components designed to allow either single-ended or differential inputs, transformer-coupled or DC-coupled. Table 2 and Figure 4 show some possible input configurations, and which components to install. Linear Technology's ADC driver families are generally characterized and designed for both single-ended and differential input drive, but for optimal performance differential input drive (or transformer-coupled drive) is recommended. By default, transformer drive is used on DC1057 so that only a single-ended input is needed. See the LT6411 data-

sheet for more comprehensive information on possible configurations.

Table 2: DC1057 Input Configuration Guide

CONFIGURATION	COMPONENTS NECESSARY
Single-Ended Input Transformer Drive Gain = +2 (default, not shown)	Install 0Ω jumper at R16 or R6. Install transformer T1. Install 25Ω at R7 and R13 for impedance matching. Establish DC bias by using R37 and R38 or R2/R3 and R17/R18. Tie feedback resistors to AC ground through 0.1μF at C5 and C9 (or replace with 0Ω resistors if using dual supplies).
Single-Ended Input Single-Ended Drive Gain = +2 (Figure 4a)	Install 0Ω jumper at R16. Install R6 for impedance matching. Remove T1, C5, C9. Install 0Ω at R5, R10, R39, R42. Install 0.1μF at C33, C34. Establish DC bias with R17, R18 resistors. Install 0Ω at R5, R10.

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Differential Input AC-Coupled Gain = +2 (Figure 4b)	Remove R16 and R6. Install 0Ω at R39, R42. Remove T1. Install 0.1μF at C33, C34. Install R7 and R13 for impedance matching. Establish DC bias by using R37 and R38 or R2/R3 and R17/R18. Tie feedback resistors to AC ground through 0.1μF at C5 and C9 (or replace with 0Ω resistors if using dual supplies).
Differential Input AC-Coupled Gain = +1 (Figure 4c)	Remove R16 and R6. Install 0Ω at R39, R42. Remove T1. Install 0.1μF at C33, C34. Install R7 and R13 for impedance matching. Establish DC bias by using R37 and R38 or R2/R3 and R17/R18. Install 0Ω at R5, R14 to establish gain of +1.
Differential Input AC-Coupled Gain = -1 (Figure 4d)	Remove R16 and R6. Remove T1. Install 0.1μF at C33, C34. Install R7 or R13 for impedance matching. Establish DC bias by using R2/R3 and R17/R18. Install 0Ω at R40, R41 to establish gain of -1.
Differential Input AC-Coupled Gain = +3 (Figure 4e)	Remove R16 and R6 Remove T1. Install 0.1μF at C33, C34. Install R7 or R13 for impedance matching. Establish DC bias by using R37 and R38 or R2/R3 and R17/R18. Install 0Ω jumpers in the positions shown in Figure 4e, to establish gain of +3.
Differential Input DC-Coupled* (Figure 4f)	Remove R16 and R6. Remove T1. Install 0Ω at R39, R42. Install R7 or R13 for impedance matching. Remove CIN+ and CIN-, replace with 0Ω. Install 0Ω jumpers at C5, C9.

NOTE. * When driving the ADC driver with a direct DC-coupled path, be aware of the increased input currents that may occur due to the output common-mode voltage and internal resistor networks.

The DC common-mode voltage requirements of Linear Technology's ADC drivers do not always extend to ground (the negative supply voltage). When replacing CIN+ and CIN- with 0Ω jumpers, make sure to level-shift the inputs so that the ADC driver's input common-mode voltage requirement is met.

Recommended 1:1 transformers for populating T1 are M-A/Com's ETC1-1-13 and ETC1-1T.

POWER SUPPLY BYPASS CAPACITANCE

Depending on the quality of the power supplies provided to DC1057, it may be desirable to add larger bulk capacitors at C1, C29, C30, and C31. This will not be necessary with clean, low-impedance power supplies.

FILTER NETWORKS

For narrowband input signals, L1 and C6 are included at the output of the ADC driver for easy band-pass filter design. In addition, there are extra pads for resistors, capacitors, and other filter network components at the output of the LT6411.

CHANGING THE ADC DRIVER'S OUTPUT COMMON-MODE VOLTAGE

The output common-mode voltage of the ADC driver must be set either at the input of the LT6411 (see Table 2), or by AC coupling the output of the LT6411. R24 and R25 are optional resistors connected to the VCM output of the ADC that can be installed to apply the proper common-mode voltage to the ADC inputs.

QUICKDAACS CIRCUITRY

Logic gate U6, installed on the back of DC1057, enables the CMOS output buffers when DC1057 is plugged into DC718, which pulls its input high. Device U5 is an EEPROM device that is used by the QuickEval software, and does not affect board operation or performance.

USING QUICKEVAL-II SOFTWARE

QuickEval-II, downloadable from Linear Technology's website <http://www.linear.com/>, processes data from the DC718 QuickDAACS board and displays FFT and signal analysis information on the computer screen. This section describes how to use the software to view the output from DC1057.

The first step is to select the correct input board. See Figure 5 From the Configure menu in the

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toolbar, select DC718 (QuickDAACs). The next step is to use the proper settings for the DC1057 output. See Figure 6 Select the correct device from the menu bar, and select the “Randomized” option

if the output randomizer is turned on (via JP4). After configuration is through, the program should be ready to collect and display data. See the Help file for instructions on general software use.

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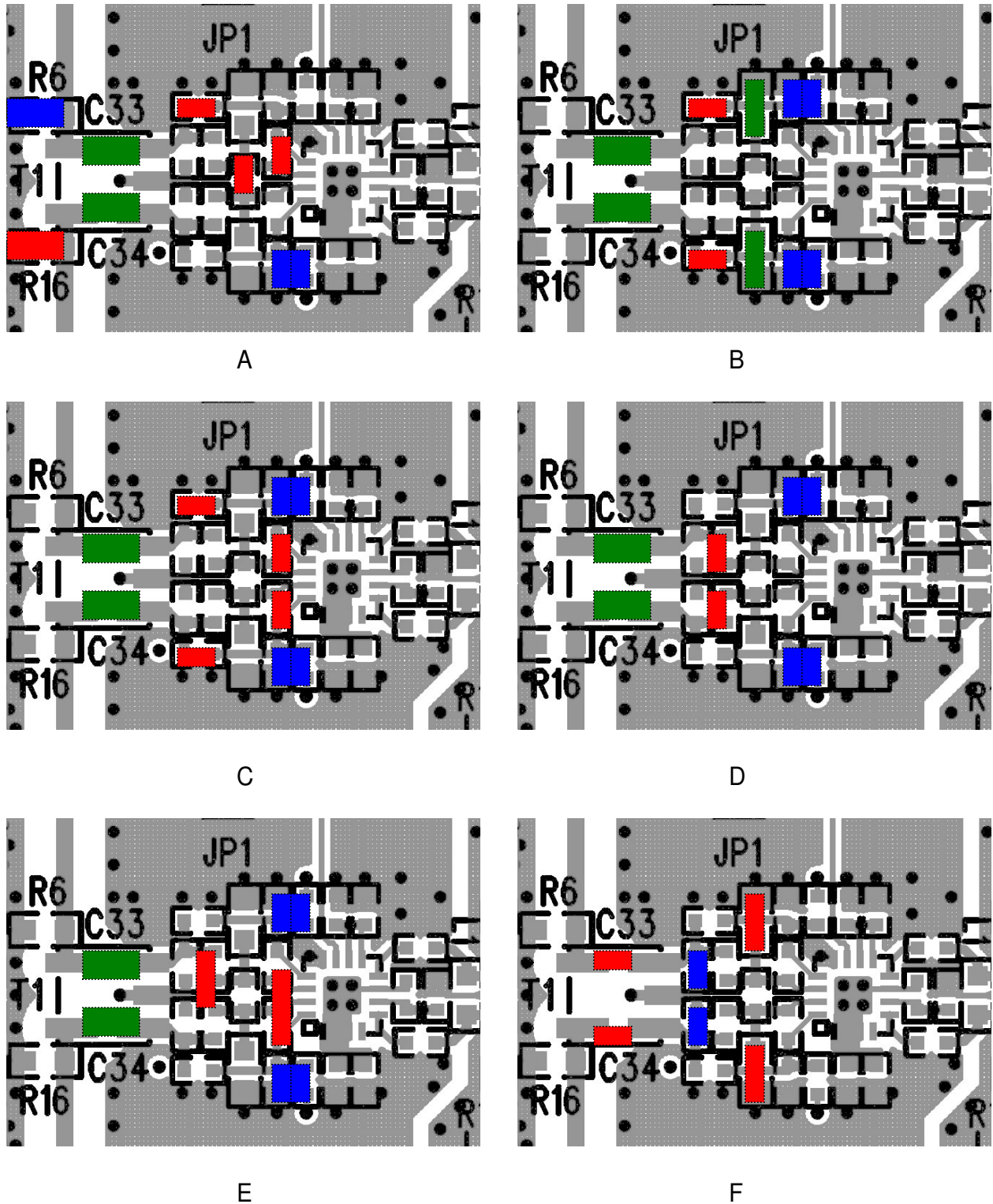


Figure 4. Pictures of DC1057 input network configurations. Blocks show where components should be mounted, according to Table 2.

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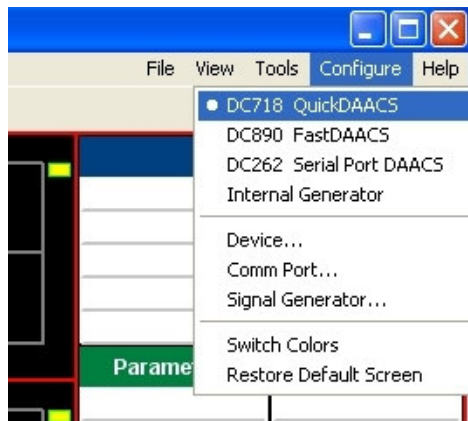


Figure 5. Selecting the correct input to QuickEval-II

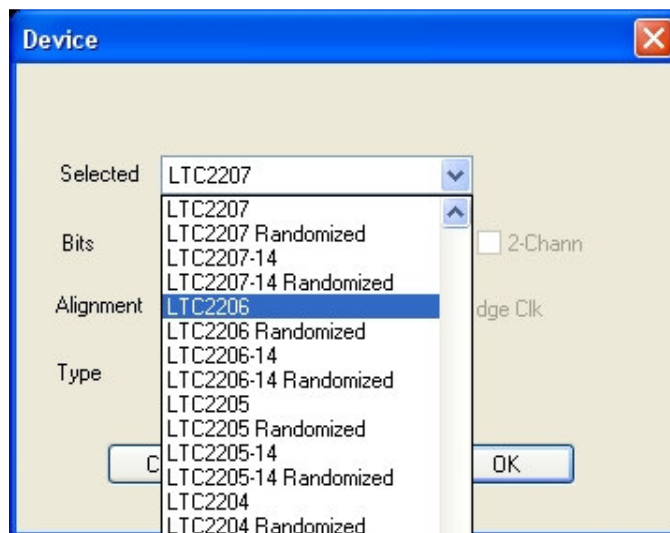
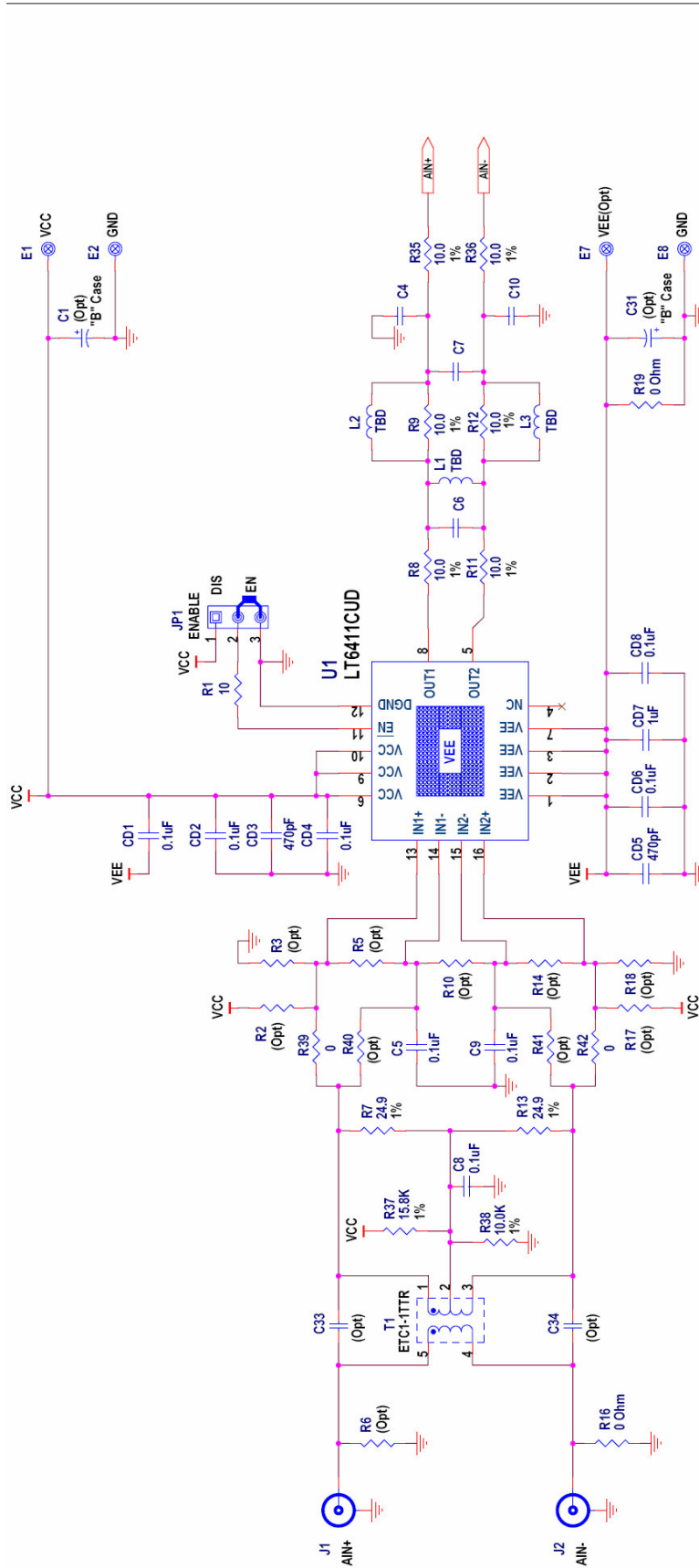


Figure 6. Entering the correct device information for your ADC. Select the correct device for your board.

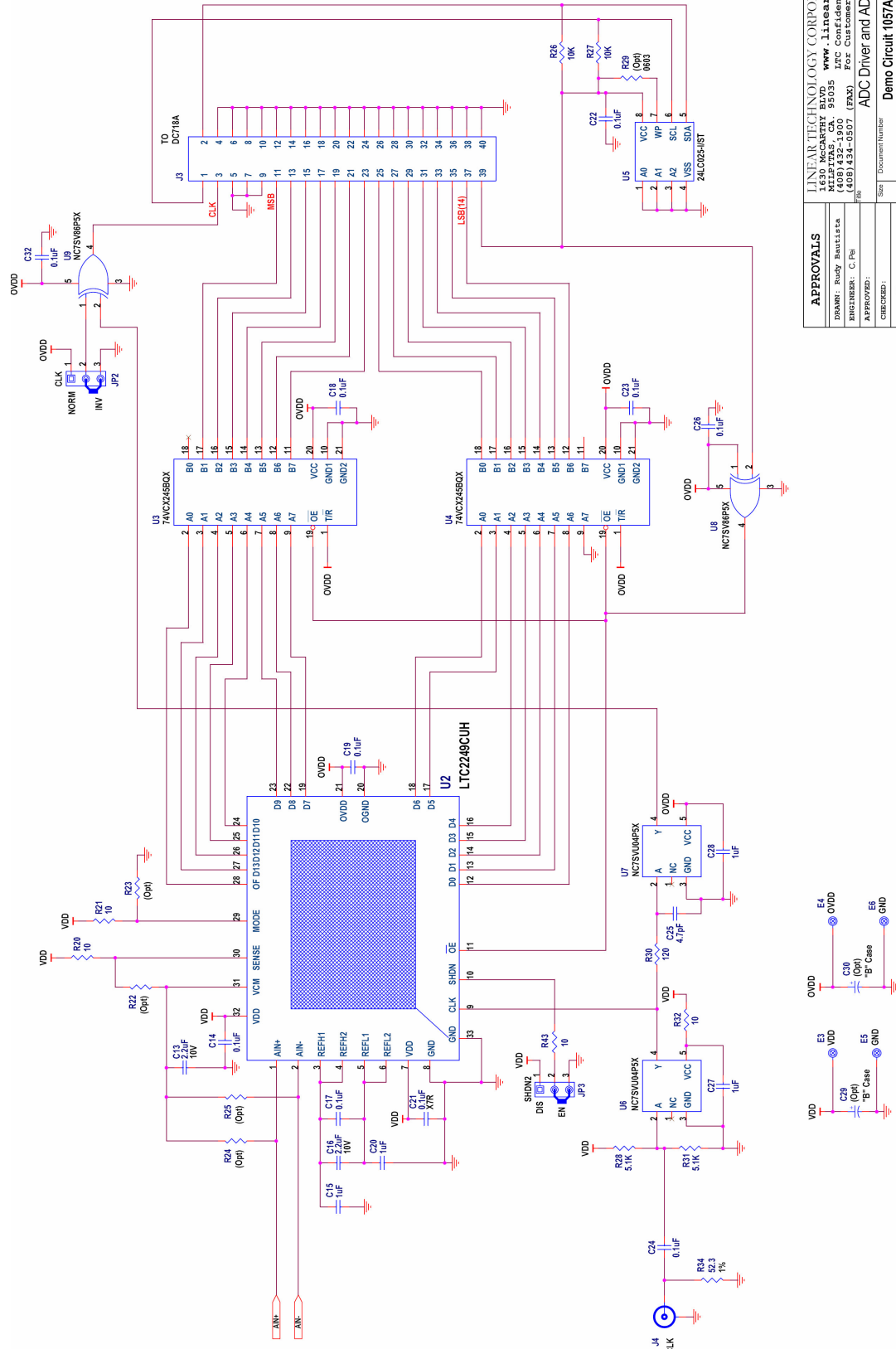
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DRAWN: Rudy Bautista	www.linear.com
ENGINEER: C Pei	LTC Confidential - For Customer Use Only
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APPROVALS	
DESIGNED BY: Rudy Bautista	DATE: 08/14/06
ENGINEER: C. Phi	DATE: 08/14/06
CHECKED: [Signature]	DATE: 08/14/06
APPROVED: [Signature]	DATE: 08/14/06
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