Microprocessor Reset Circuits with Capacitor-Adjustable Reset/Watchdog Timeout Delay

ADPL63164

General Description

The ADPL63164 low-power microprocessor (µP) supervisory circuits monitor single/dual system supply voltages from 1.575V to 5V and provide maximum adjustability for reset and watchdog functions. These devices assert a reset signal whenever the V_{CC} supply voltage or RESET IN falls below its reset threshold or when manual reset is pulled low. The reset output remains asserted for the reset timeout period after V_{CC} and RESET IN rise above the reset threshold. The reset function features immunity to power-supply transients.

The ADPL63164 has a ±2% factory-trimmed reset threshold voltage in approximately 100mV increments from 1.575V to 5V and/or adjustable reset threshold voltages using external resistors.

The reset and watchdog delays are adjustable with external capacitors. The ADPL63164 contains a watchdog select input that extends the watchdog timeout period by 128x.

The ADPL63164 is available with an open-drain active-low $\overline{\text{RESET}}$ output. The ADPL63164 is available in an 8-pin SOT23 package and is fully specified over the temperature range of -40°C to +125°C.

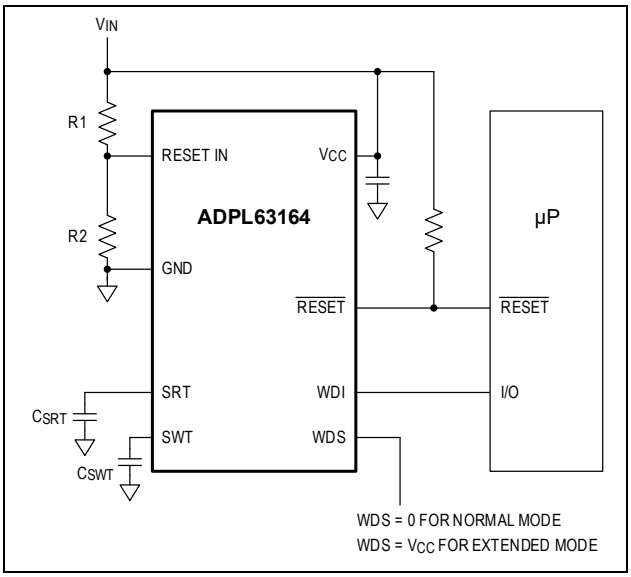
Applications

- Medical Equipment
- Automotive
- Intelligent Instruments
- Portable Equipment
- Battery-Powered Computers/Controllers
- Embedded Controllers
- Critical Microprocessor Monitoring
- Set Top Boxes
- Computers

Benefits and Features

- Configurable Reset and Watchdog Options Enables Wide Variety of Applications
  - Factory-Set Reset Threshold Options from 1.575V to 5V in ~100mV Increments
  - Adjustable Reset Threshold Options
  - Single/Dual Voltage Monitoring
  - Capacitor-Adjustable Reset Timeout
  - Capacitor-Adjustable Watchdog Timeout
  - Open-Drain $\overline{\text{RESET}}$ Output
- 4µA Supply Current Reduces System Power Consumption
- Integrated Power Supply Protection Increases Robustness
  - Power-Supply Transient Immunity
  - Guaranteed $\overline{\text{RESET}}$ Valid for V_{CC} ≥ 1.2V
- 8-Pin SOT23 Packages Saves Board Space

Typical Operating Circuit



19-101808; Rev 0; 1/24

Absolute Maximum Ratings

V_{CC} to GND ..... -0.3V to +6.0V

SRT, SWT, RESET IN, WDS, WDI, to GND..... -0.3V to V_{CC} + 0.3V

$\overline{RESET}$ (Open Drain) to GND ..... -0.3V to +6.0V

Input Current (All Pins) ..... ±20mA

Output Current ($\overline{RESET}$) ..... ±20mA

Continuous Power Dissipation (T_A = +70°C) 8-Pin SOT23 (derate 5.1mW/°C above +70°C) 408.2mW

Operating Temperature Range ..... -40°C to +125°C

Storage Temperature Range ..... -65°C to +150°C

Junction Temperature ..... +150°C

Lead Temperature (soldering, 10s) ..... +300°C

Soldering Temperature (reflow)..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Code	**K8+5, K8+5A**
Outline Number	*21-0078*
Land Pattern Number	*90-0176*
Thermal Resistance, Single-Layer Board	
Junction-to-Ambient (θ_{JA})	N/A
Junction-to-Case Thermal Resistance (θ_{JC})	800
Thermal Resistance, Four-Layer Board	
Junction-to-Ambient (θ_{JA})	196
Junction-to-Case Thermal Resistance (θ_{JC})	70

For the latest package outline information and land patterns (footprints), go to https://www.analog.com/en/design-center/packaging-quality-symbols-footprints/package-index.html. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to https://www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages.html.

Electrical Characteristics

(VCC = +1.7V to +5.5V, TA = TMIN to TMAX, unless otherwise specified. Typical values are at VCC = +5V and TA = +25°C) (Note 1)

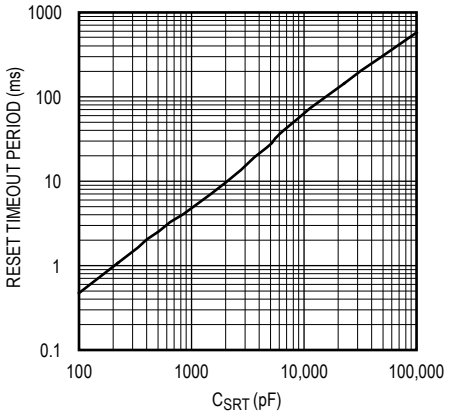
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	Reset output is guaranteed to be in a known state	1.2		5.5	V
		T_A = -40°C to 125°C	1.7		5.5	
Supply Current	I_{CC}	V_{CC} <= 5.5V		7	15	µA
		V_{CC} <= 3.3V		4.5	10	
		V_{CC} <= 2.0V		4	9	
V_{CC} Reset Threshold	V_{TH}	See *Table 1* ; T_A = -40°C to +125°C	V_{TH} - 2.5%		V_{TH} + 2.5%	V
Hysteresis	V_{HYST}			0.8		%
V_{CC} to RESET Delay		V_{CC} falling from V_{TH} + 100mV to V_{TH} - 100mV at 1mV/µs		20		µs
Reset Timeout Period	t_{RP}	C_{SRT} = 1500pF	5.692	7.59	9.487	ms
		C_{SRT} = 100pF		0.506		
SRT Ramp Current	I_{RAMP}	V_{SRT} = 0 to 1.23V; V_{CC} = 1.6V to 5V	180	250	320	nA
SRT Ramp Threshold	V_{RAMP}	V_{CC} = 1.6V to 5V (V_{RAMP} rising)	1.17	1.235	1.3	V
Normal Watchdog Timeout Period	t_{WD}	C_{SWT} = 1500pF	5.692	7.59	9.487	ms
		C_{SWT} = 100pF		0.506		
Extended Watchdog Timeout Period	t_{WD}	C_{SWT} = 1500pF	728.6	971.5	1214.4	ms
		C_{SWT} = 100pF		64.77		
SWT Ramp Current	I_{RAMP}	V_{SWT} = 0 to 1.23V; V_{CC} = 1.6V to 5V	180	250	320	nA
SWT Ramp Threshold	V_{RAMP}	V_{CC} = 1.6V to 5V (VRAMP rising)	1.17	1.235	1.3	V
$\overline{RESET}$ Output-Voltage Low (Asserted)	V_{OL}	V_{CC} ≥ 1.0V, I_{SINK} = 50µA			0.3	V
		V_{CC} ≥ 2.7V, I_{SINK} = 1.2mA			0.3	
		V_{CC} ≥ 4.5V, I_{SINK} = 3.2mA			0.4	
$\overline{RESET}$ Output Leakage Current	I_{LKG}	V_{CC} > V_{TH}, reset not asserted V_{RESET} = 5.5V			1.5	µA
DIGITAL INPUTS (WDI, WDS)						
Input Logic Levels	V_{IL}	V_{CC} ≥ 4.0V			0.8	V
	V_{IH}	V_{CC} ≥ 4.0V	2.4			
	V_{IL}	V_{CC} < 4.0V			0.2 x V_{CC}	
	V_{IH}		0.8 x V_{CC}			
WDI Minimum Pulse Width			300			ns
RESET IN						
RESET IN Threshold	$V_{RESET\ IN}$	T_A = -40°C to +125°C	1.21	1.235	1.26	V
RESET IN Leakage Current	$I_{RESET\ IN}$		-55	±1	55	nA
RESET IN to $\overline{RESET}$ Delay		RESET IN falling at 1mV/µs		20		µs

Note 1: Production testing done at T_A = +25°C. Over temperature limits are guaranteed by design.

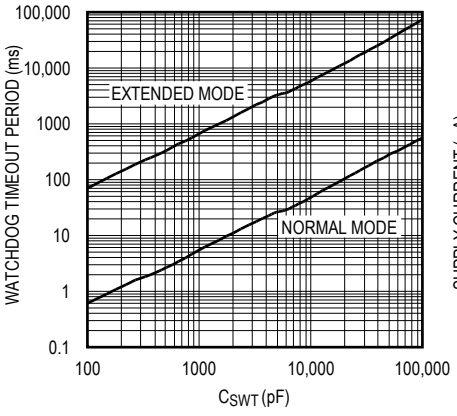
Typical Operating Characteristics

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

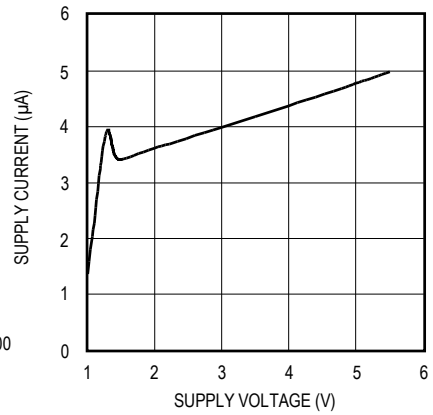
RESET TIMEOUT PERIOD vs. C_{SRT}



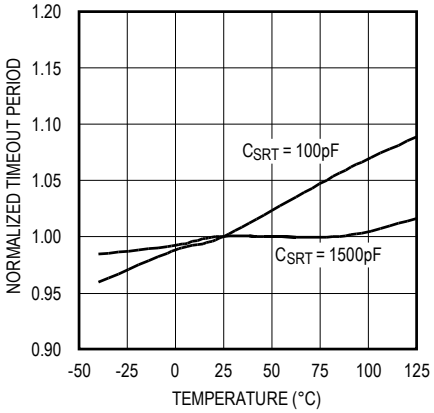
WATCHDOG TIMEOUT PERIOD vs. C_{SWT}



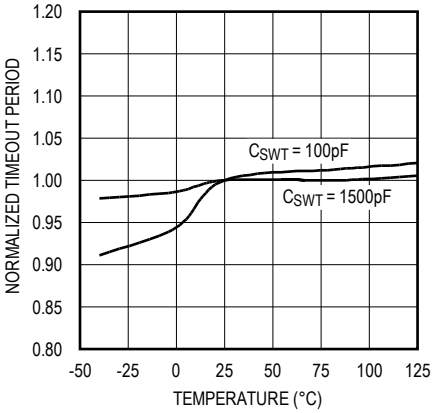
SUPPLY CURRENT vs. SUPPLY VOLTAGE



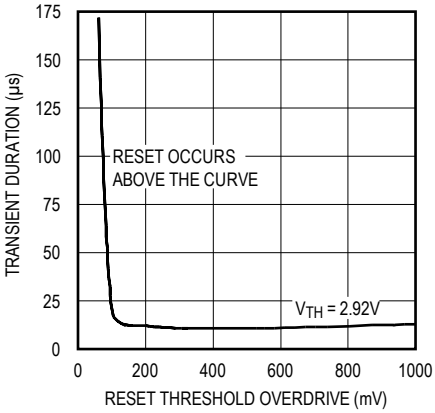
NORMALIZED RESET TIMEOUT PERIOD vs. TEMPERATURE



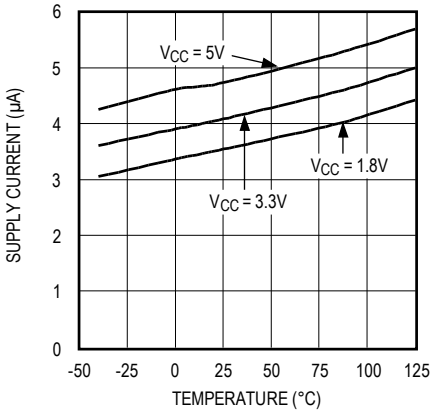
NORMALIZED WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



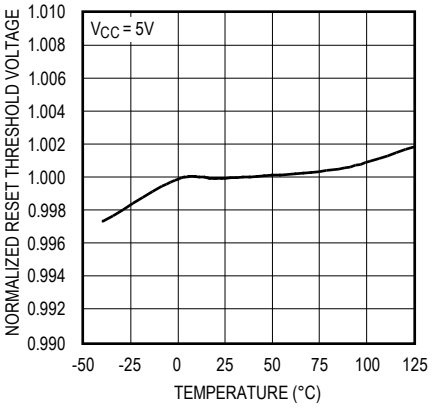
MAXIMUM TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE



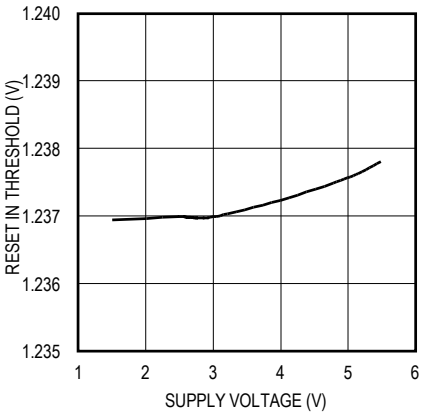
SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED RESET IN THRESHOLD VOLTAGE vs. TEMPERATURE

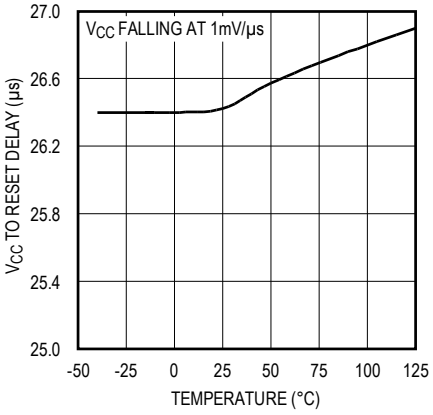


RESET IN THRESHOLD vs. SUPPLY VOLTAGE

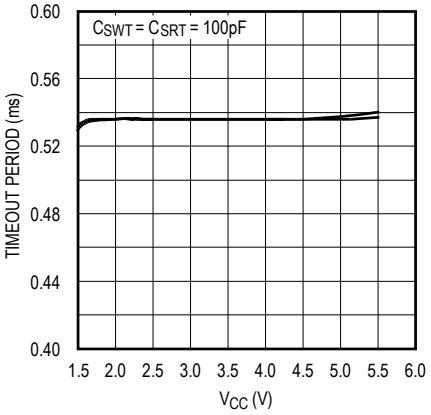


(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

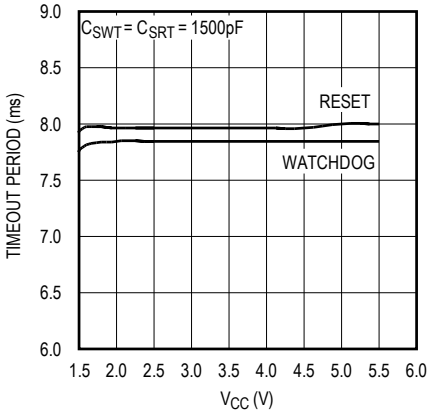
V_{CC} TO RESET DELAY vs. TEMPERATURE (V_{CC} FALLING)



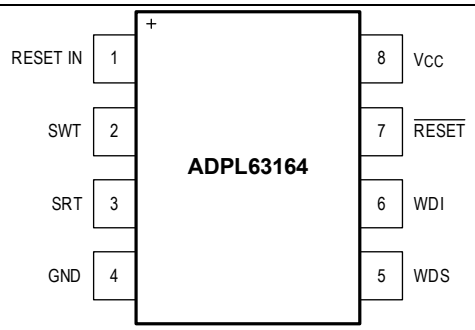
RESET AND WATCHDOG TIMEOUT PERIOD vs. SUPPLY VOLTAGE



RESET AND WATCHING TIMEOUT PERIOD vs. SUPPLY VOLTAGE



Pin Configurations



Pin Descriptions

PIN	NAME	FUNCTION
1	RESET IN	Reset Input. High-impedance input to the adjustable reset comparator. Connect RESET IN to the center point of an external resistor-divider to set the threshold of the externally monitored voltage.
2	SWT	Watchdog Timeout Input. Connect a capacitor between SWT and ground to set the basic watchdog timeout period (tWD). Determine the period by the formula $tWD = 4.94 \times 106 \times CSWT$ with tWD in seconds and CSWT in Farads. Extend the basic watchdog timeout period by using the WDS input. Connect SWT to ground to disable the watchdog timer function.
3	SRT	Reset Timeout Input. Connect a capacitor from SRT to GND to select the reset timeout period. Determine the period as follows: $tRP = 4.94 \times 106 \times CSRT$ with tRP in seconds and CSRT in Farads.
4	GND	Ground.
5	WDS	Watchdog Select Input. WDS selects the watchdog mode. Connect WDS to ground to select normal mode and the watchdog timeout period. Connect WDS to V_{CC} to select extended mode, multiplying the basic timeout period by a factor of 128. A change in the state of WDS clears the watchdog timer.
6	WDI	Watchdog Input. A falling transition must occur on WDI within the selected watchdog timeout period, or a reset pulse occurs. The watchdog timer clears when a transition occurs on WDI or whenever $\overline{RESET}$ is asserted. Connect SWT to ground to disable the watchdog timer function. WDI must not be left floating. Connect a 100k resistor from WDI to ground to ensure proper operation when watchdog function is not used.
7	$\overline{RESET}$	Open-Drain Reset Output. $\overline{RESET}$ asserts whenever V_{CC} or RESET IN drops below the selected reset threshold voltage (V_{TH} or $V_{RESET\ IN}$, respectively). $\overline{RESET}$ remains low for the reset timeout period after all reset conditions are deasserted, and then goes high. The watchdog timer triggers a reset pulse (tRP) whenever a watchdog fault occurs.
8	V_{CC}	Supply Voltage. V_{CC} is the power-supply input and the input for fixed threshold V_{CC} monitor.

Detailed Description

The ADPL63164 asserts a reset signal whenever the V_{CC} supply voltage or RESET IN falls below its reset threshold. The reset output remains asserted for the reset timeout period after V_{CC} and RESET IN rise above its respective reset threshold. A watchdog timer triggers a reset pulse whenever a watchdog fault occurs.

The reset and watchdog delays are adjustable with external capacitors. The ADPL63164 contains a watchdog select input that extends the watchdog timeout period to 128x.

Reset Output

The reset output is typically connected to the reset input of a microprocessor. A microprocessor's reset input starts or restarts the microprocessor in a known state. The ADPL63164 microprocessor supervisory circuits provide the reset logic to prevent code-execution errors during power-up, power-down, and brownout conditions (see *Typical Operating Circuit*).

$\overline{\text{RESET}}$ changes from high to low whenever the monitored voltage, RESET IN, and/or V_{CC} drop below the reset threshold voltages. Once $V_{RESET\ IN}$ and/or V_{CC} exceeds its respective reset threshold voltage(s), $\overline{\text{RESET}}$ remains low for the reset timeout period, then goes high.

$\overline{\text{RESET}}$ is guaranteed to be in the correct logic state for V_{CC} greater than 1V.

RESET IN Threshold

The ADPL63164 monitors the voltage on RESET IN using an adjustable reset threshold ($V_{RESET\ IN}$) set with an external resistor voltage-divider (see *Figure 1*). Use the following formula to calculate the externally monitored voltage (V_{MON_TH}):

$$V_{MON\_TH} = V_{RESET\ IN} \times (R1 + R2)/R2$$

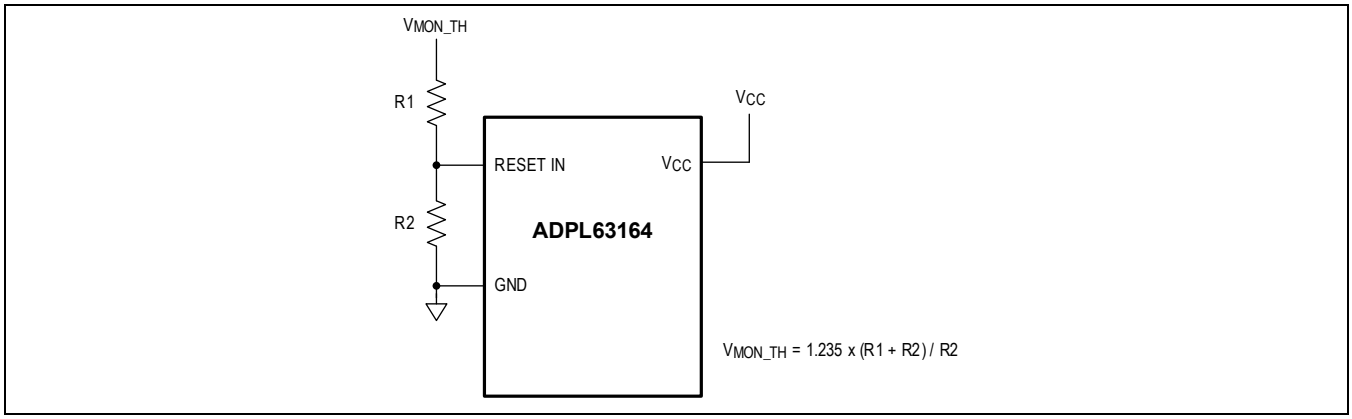


Figure 1. Calculating the Monitored Threshold Voltage (V_{MON_TH})

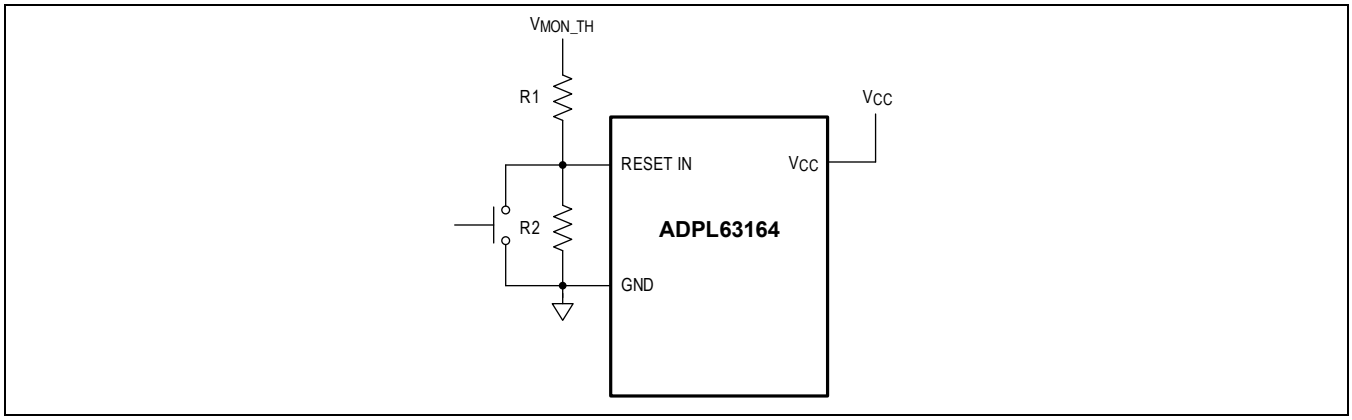


Figure 2. Adding an External Manual-Reset Function to the ADPL63164

where V_{MON_TH} is the desired reset threshold voltage and V_{TH} is the reset input threshold (1.235V). Resistors R1 and R2 can have very high values to minimize current consumption due to low leakage currents. Set R2 to some conveniently high value (500kΩ, for example) and calculate R1 based on the desired reset threshold voltage, using the following formula:

$$R1 = R2 \times \left(\frac{V_{MON\_TH}}{V_{RESET\ IN}} - 1\right)(\Omega)$$

Dual-Voltage Monitoring

The ADPL63164 contains both factory-trimmed threshold voltages and an adjustable reset threshold input, allowing the monitoring of two voltages, V_{CC} and V_{MON_TH} (see *Figure 1*). $\overline{RESET}$ is asserted when either of the voltages falls below its respective threshold voltages.

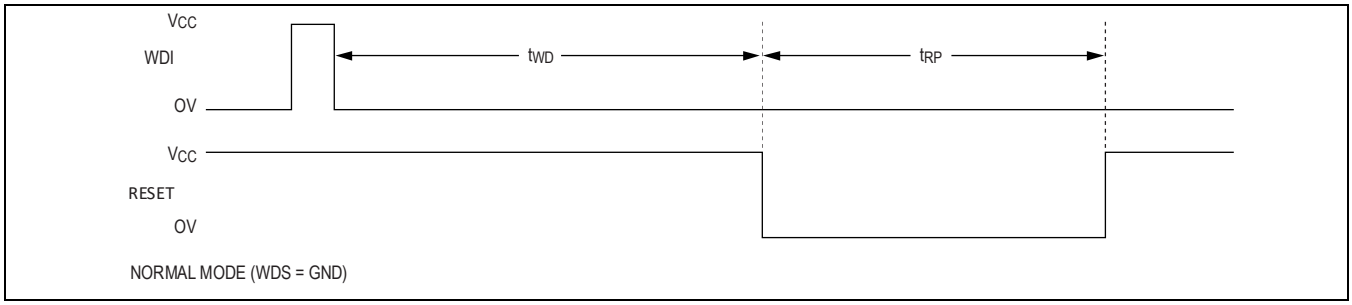
Manual Reset

A manual-reset option can easily be implemented with the ADPL63164 by connecting a normally open momentary switch in parallel with R2 (see *Figure 2*). When the switch is closed, the voltage on RESET IN goes to zero, initiating a reset. Reset remains asserted while the voltage at RESET IN is zero and for the reset timeout period after the switch is opened.

Watchdog Timer

The watchdog's circuit monitors the microprocessor's activity. If the microprocessor does not toggle the watchdog input (WDI) within t_{WD} (user-selected), $\overline{RESET}$ asserts for the reset timeout period. The internal watchdog timer is cleared by any event that asserts $\overline{RESET}$: by a falling transition at WDI (which can detect pulses as short as 300ns) or by a transition at WDS. The watchdog timer remains cleared while reset is asserted; as soon as reset is released, the timer starts counting.

The ADPL63164 features two modes of watchdog operation: normal mode and extended mode. In normal mode (see *0*), the watchdog timeout period is determined by the value of the capacitor connected between SWT and ground. In extended mode (see *Figure 3*), the watchdog timeout period is multiplied by 128. For example, in extended mode, a 0.1µF capacitor gives a watchdog timeout period of 65s (see the Extended Mode in Watchdog Timeout Period vs. C_{SWT} graph in the *Typical Operating Characteristics*). To disable the watchdog timer function, connect SWT to ground.



Watchdog Timing Diagram, WDS = GND

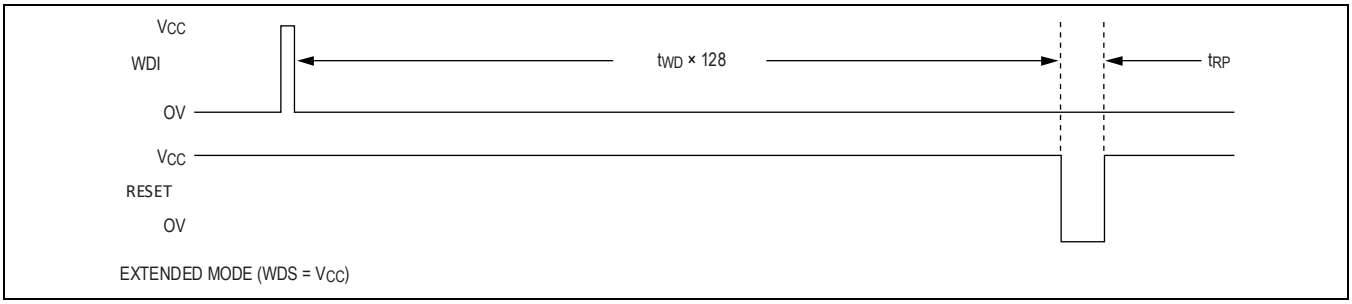


Figure 3. Watchdog Timing Diagram, WDS = V_{CC}

Applications Information

Selecting Reset/Watchdog Timeout Capacitor

The reset timeout period is adjustable to accommodate a variety of microprocessor applications. Adjust the reset timeout period (t_{RP}) by connecting a capacitor (C_{SRT}) between SRT and ground. Calculate the reset timeout capacitor as follows:

$$C_{SRT} = t_{RP}/(4.94 \times 10^6)$$

with t_{RP} in seconds and C_{SRT} in Farads.

The watchdog timeout period is adjustable to accommodate a variety of microprocessor applications. With this feature, the watchdog timeout can be optimized for software execution. The programmer can determine how often the watchdog timer should be serviced. Adjust the watchdog timeout period (t_{WD}) by connecting a specific value capacitor (C_{SWT}) between SWT and GND. Calculate the watchdog timeout capacitor as follows:

$$C_{SWT} = t_{WD}/(4.94 \times 106)$$

with t_{WD} in seconds and C_{SWT} in Farads.

C_{SRT} and C_{SWT} must be a low-leakage (< 10nA) type capacitor. Ceramic capacitors are recommended.

Transient Immunity

In addition to issuing a reset to the microprocessor during power-up, power-down, and brownout conditions, this supervisor is relatively immune to short-duration supply transients (glitches). The Maximum Transient Duration vs. Reset Threshold Overdrive graph in the *Typical Operating Characteristics* shows this relationship.

The area below the curves of the graph is the region in which these devices typically do not generate a reset pulse. This graph was generated using a falling pulse applied to V_{CC}, starting above the actual reset threshold (V_{TH}) and ending below it by the magnitude indicated (reset threshold overdrive). As the magnitude of the transient increases (farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts 50µs or less does not cause a reset pulse to be issued. For applications where the power supply to V_{CC} has high transient rates, dV/dt > 5V/50µS, an RC filter on V_{CC} is required. See *Figure 6*.

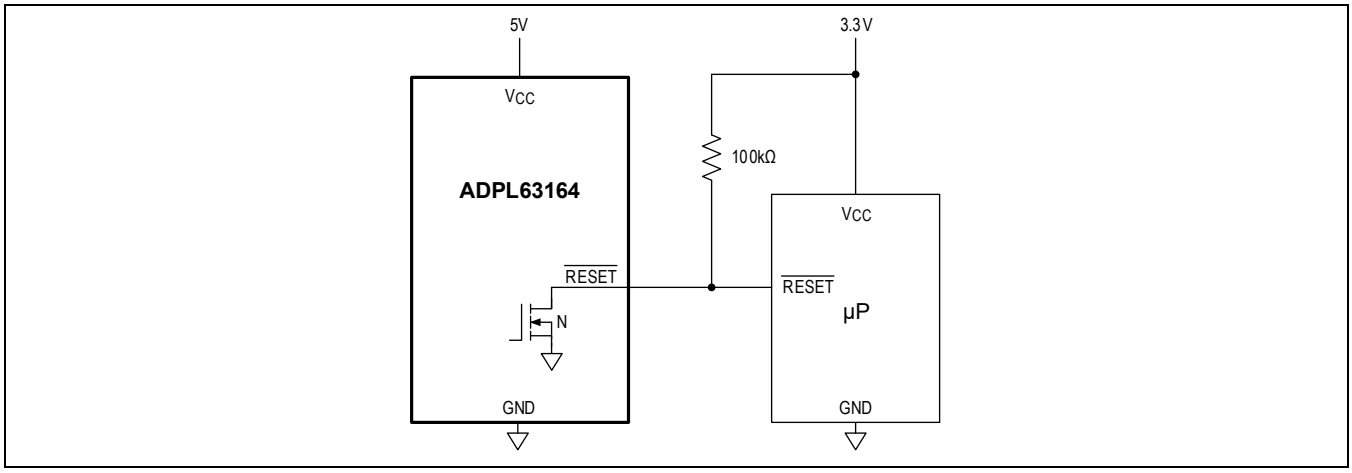


Figure 4. Interfacing to Other Voltage Levels

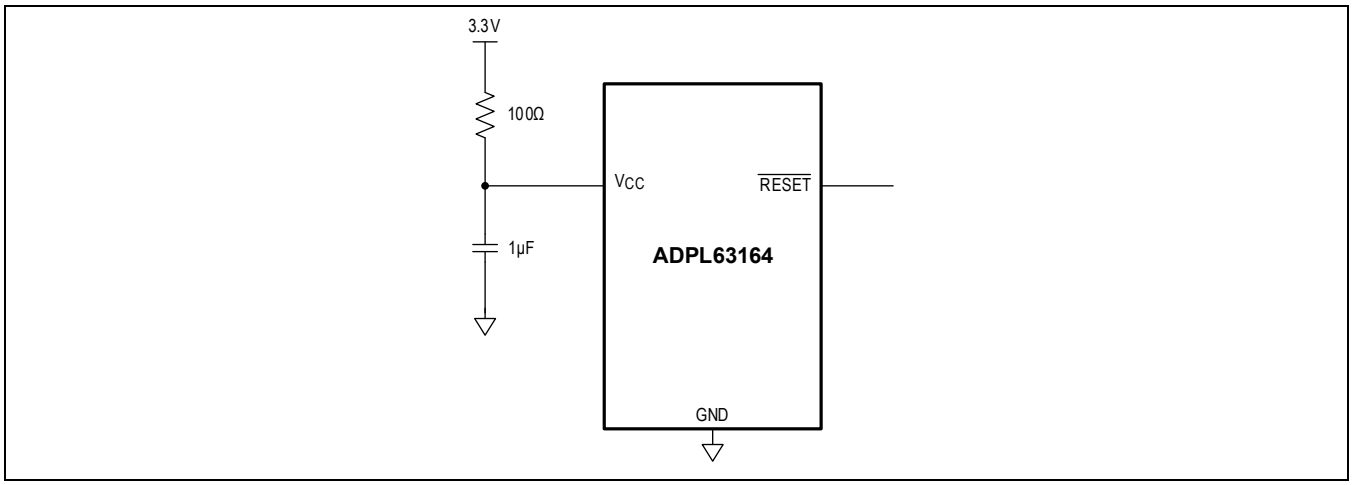


Figure 6. Application Circuit for High-Input Voltage Transient Applications

Interfacing to Other Voltages for Logic Compatibility

The open-drain $\overline{\text{RESET}}$ output can be used to interface to a microprocessor with other logic levels. As shown in *Figure 4*, the open-drain output can be connected to voltages from 0V to 6V.

Generally, the pull-up resistor connected to $\overline{\text{RESET}}$ connects to the supply voltage that is being monitored at the IC's V_{CC} pin. However, some systems can use the open-drain output to level-shift from the monitored supply to reset circuitry powered by some other supply. Note that as the supervisor's V_{CC} decreases toward 1V, so does the IC's ability to sink current at $\overline{\text{RESET}}$. Also, with any pull-up resistor, $\overline{\text{RESET}}$ is pulled high as V_{CC} decays toward zero. The voltage where this occurs depends on the pull-up resistor value and the voltage to which it is connected.

Table 1. Reset Threshold Voltage Suffix (T_A = -40°C to +125°C)

SUFFIX	MIN	TYP	MAX
50	4.875	5.000	5.125
49	4.778	4.900	5.023
48	4.680	4.800	4.920
47	4.583	4.700	4.818
46	4.509	4.625	4.741
45	4.388	4.500	4.613
44	4.266	4.375	4.484
43	4.193	4.300	4.408
42	4.095	4.200	4.305
41	3.998	4.100	4.203
40	3.900	4.000	4.100
39	3.803	3.900	3.998
38	3.705	3.800	3.895
37	3.608	3.700	3.793
36	3.510	3.600	3.690
35	3.413	3.500	3.588
34	3.315	3.400	3.485
33	3.218	3.300	3.383
32	3.120	3.200	3.280
31	2.998	3.075	3.152
30	2.925	3.000	3.075
29	2.852	2.925	2.998
28	2.730	2.800	2.870
27	2.633	2.700	2.768
26	2.559	2.625	2.691
25	2.438	2.500	2.563
24	2.340	2.400	2.460
23	2.255	2.313	2.371
22	2.133	2.188	2.243
21	2.048	2.100	2.153
20	1.950	2.000	2.050
19	1.853	1.900	1.948
18	1.755	1.800	1.845
17	1.623	1.665	1.707
16	1.536	1.575	1.614

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
ADPL63164AKA_ _+	-40°C to +125°C	8 SOT23
ADPL63164AKA_ _+T	-40°C to +125°C	8 SOT23
ADPL63164AKA31+	-40°C to +125°C	8 SOT23
ADPL63164AKA31+T	-40°C to +125°C	8 SOT23

Note: *"_ _" represents the two number suffix needed when ordering the reset threshold voltage value. The reset threshold voltages are available in approximately 100mV increments. Table 1 contains the suffix and reset factory-trimmed voltages. All devices are available in tape and reel only. There is a 2500-piece minimum order increment for standard versions (see Ordering Information). Sample stock is typically held on standard versions only. Nonstandard versions require a minimum order increment of 10,000 pieces. Contact factory for availability.*

+Denotes a lead(Pb)-free/RoHS-compliant package. T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/24	Initial release	—

Mouser Electronics

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Analog Devices Inc.:

ADPL63164AKA31+T