ADPL62933

Nanopower µP Supervisor with Manual Reset and Watchdog Timer

General Description

The ADPL62933 is an ultra-low-current (200nA, typ) microprocessor (µP) supervisory circuit that combines voltage monitoring, watchdog timer, and manual reset input functions in a 5- pin SOT23 package. This device asserts a reset signal whenever the monitored voltage drops below the factory-trimmed reset threshold voltage, manual reset is asserted, or the watchdog timer expires. The reset output remains asserted for a minimum timeout period after V_{CC} rises above the reset threshold and manual reset is deasserted. Factory-trimmed reset threshold voltages are offered from +1.575V to +4.625V in approximately 100mV increments (see the *Table 1*). Each device is offered with six minimum reset timeout options, ranging from 10ms to 1200ms.

The ADPL62933 offers a watchdog timer that monitors activity at the WDI input to prevent code execution errors. It also offers watchdog timeout options of 3.3s or 209s (typ). Open-drain, active-low reset outputs is available.

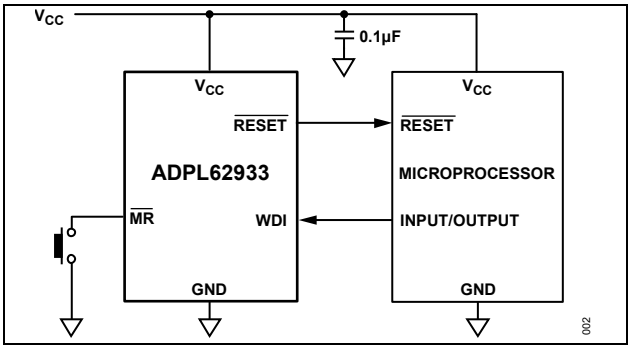
Applications

- Portable/Battery-Powered Equipment
- PDAs/Cell Phones
- MP3 Players/Pagers
- Glucose Monitors/Patient Monitors

Features

- Ultra-Low 170nA (typ) Supply Current
- Reset Thresholds from +1.575V to +4.625V in Approximately 100mV Increments
- Six Minimum Reset Timeout Period Options from 10ms to 1200ms
- Manual Reset Option
- Watchdog Timer Option
- Immune to Short V_{CC} Transients
- Guaranteed Reset Valid to V_{CC} = +1.1V
- Open-Drain $\overline{RESET}$ Output
- No External Components
- Small 5-Pin SOT23 Package

Typical Operating Circuit



Ordering Information ***appears at end of data sheet.***

19-101821; Rev 1; 01/24

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Absolute Maximum Ratings

V_{CC}, Open-Drain $\overline{RESET}$ to GND ..... -0.3V to +6.0V

$\overline{MR}$, WDI..... -0.3V to (V_{CC} + 0.3V)

Input Current, Output Current (all pins)..... ±20mA

Continuous Power Dissipation (T_A = +70°C) 5-Pin SOT23 (derate 7.1mW/°C above +70°C)..... 571mW

Operating Temperature Range ..... -40°C to +85°C

Junction Temperature ..... +150°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Code	U5+2
Outline Number	*21-0057*
Land Pattern Number	*90-0174*

For the latest package outline information and land patterns (footprints), go to http://www.analog.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to http://www.analog.com/thermal-tutorial.

Electrical Characteristics

(V_{CC} = 1.7V to 5.5V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{CC} = 2.5V, T_A = +25°C.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	Reset output is guaranteed to be in a known state		1.1		5.5	V
		T_A = -40°C to +85°C		1.7		5.5	
Supply Current	I_{CC}	V_{CC} > V_{TH}, no load, reset output deasserted (*Note 2*)	V_{CC} = 5.0V		220	410	nA
			V_{CC} = 3V		200	390	
		V_{CC} < V_{TH}, no load, reset output asserted			7	15	µA
V_{CC} Reset Threshold	V_{TH}	V_{CC} falling (see *Table 1*)		V_{TH} - 3%	V_{TH}	V_{TH} + 3%	V
Reset Threshold Hysteresis	V_{HYST}	Reset asserted to reset deasserted			0.5		%V_{TH}
Reset Timeout Period	t_{RP}	V_{CC} = V_{TH} + 150mV (*Figure 13* and *Figure 14*)	D1	10	15	25	ms
			D2	40	60	80	
			D3	150	225	300	
			D4	1200	1800	2400	
			D5	300	450	600	
			D6	600	900	1200	Ms
V_{CC} to Reset Delay	t_{RD}	V_{CC} falling from (V_{TH} + 100mV) to (V_{TH} - 100mV) at 10mV/µs			40		µs
$\overline{RESET}$ Output Voltage	V_{OL}	V_{CC} ≥ 1.1V, I_{SINK} = 50µA, $\overline{RESET}$ asserted, TA ≥ 0°C				0.3	V
		V_{CC} ≥ 1.2V, I_{SINK} = 100µA, $\overline{RESET}$ asserted				0.3	
		V_{CC} ≥ 2.12V, I_{SINK} = 1.2mA, $\overline{RESET}$ asserted				0.3	
Open-Drain $\overline{RESET}$ Leakage Current	I_{LKG}	$\overline{RESET}$ deasserted				30	nA
MANUAL RESET INPUT							
$\overline{MR}$ Input Voltage	V_{IH}			0.8 x V_{CC}			V
	V_{IL}					0.2 x V_{CC}	
$\overline{MR}$ Minimum Pulse Width	t_{MPW}			1			µs
$\overline{MR}$ Glitch Rejection					200		ns
$\overline{MR}$ to Reset Delay	t_{MRD}				250		ns
MR Pullup Resistance				5	10	20	kW
WATCHDOG TIMER							
WDI Input Voltage	V_{IH}			0.8 x V_{CC}			V
	V_{IL}					0.2 x V_{CC}	
WDI Input Current		WDI = GND or V_{CC}				20	nA
WDI Pulse Width	t_{WDI}	(*Note 3*)		150			ns

(V_{CC} = 1.7V to 5.5V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{CC} = 2.5V, T_A = +25°C.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Watchdog Timeout Period	t_{WD}	S	1.5	3.3	7.75	s
		L	95	209	487	

Note 1: Devices are tested at T_A = +25°C. Specifications for T_A = -40°C to +85°C are guaranteed by design.

Note 2: The watchdog period is 1s with t_{RISE} and t_{FALL} < 50ns.

Note 3: Guaranteed by design.

Typical Operating Characteristics

(V_{CC} = +2.5V, T_A = +25°C, unless otherwise noted.)

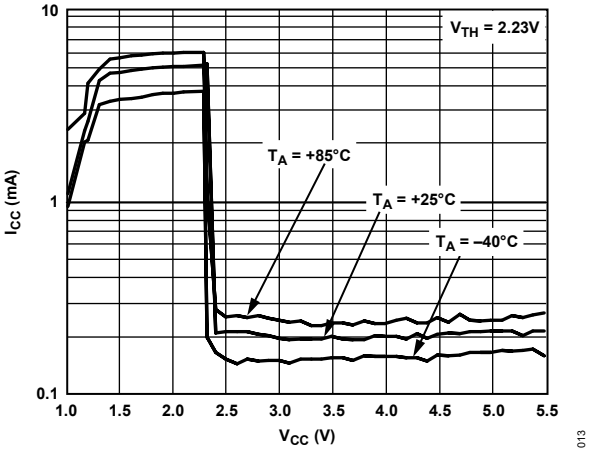


Figure 1. Supply Current vs. Supply Voltage

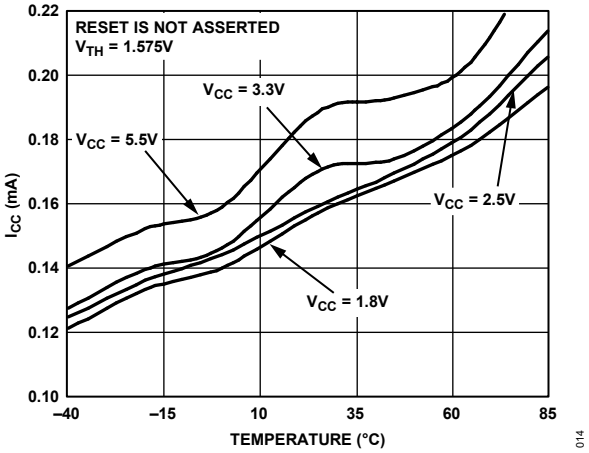


Figure 2. Supply Current vs. Temperature

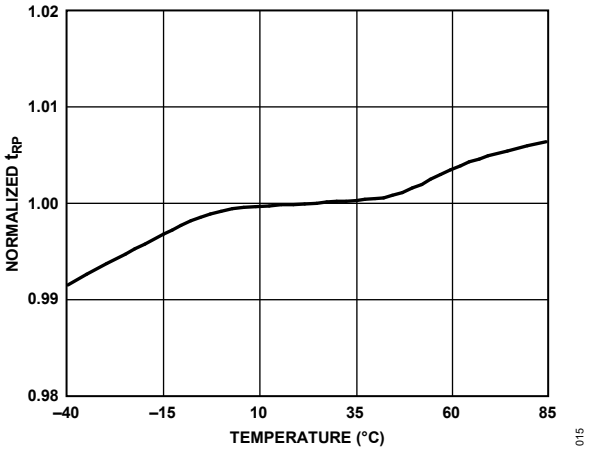


Figure 3. Normalized Reset Timeout Period vs. Temperature

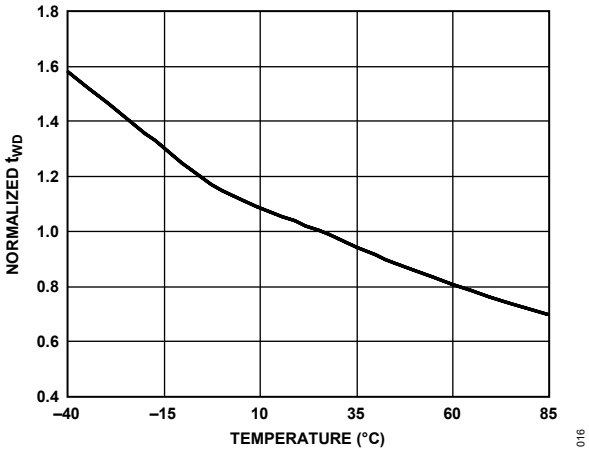


Figure 4. Normalized Watchdog Timeout Period vs. Temperature

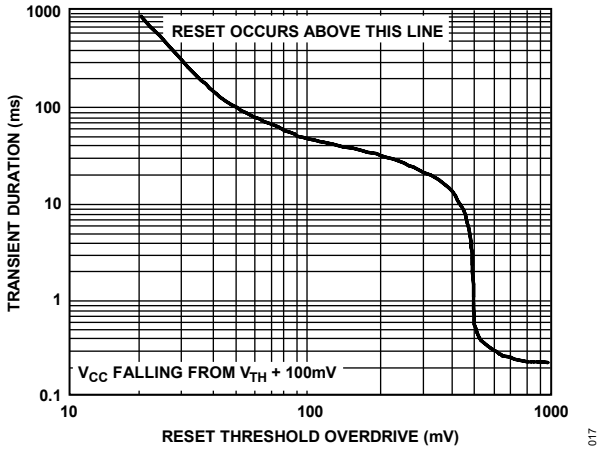


Figure 5. Maximum V_{cc} Transient Duration vs. Reset Threshold Overdrive

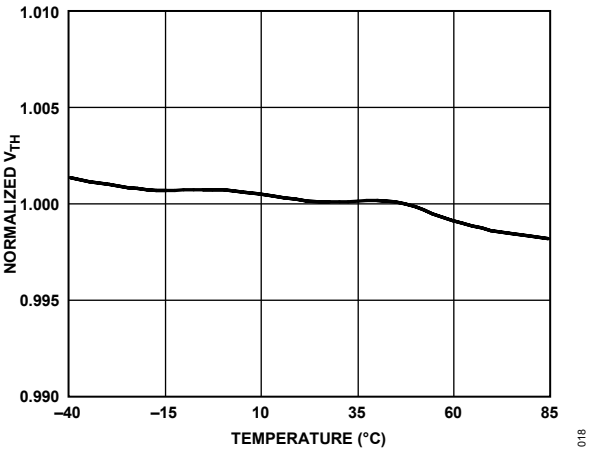


Figure 6. Normalized Reset Threshold Voltage vs. Temperature

(V_{CC} = +2.5V, T_A = +25°C, unless otherwise noted.)

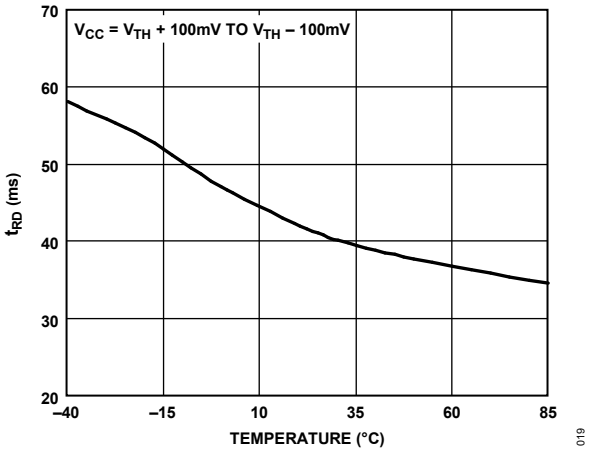


Figure 7. V_{cc} To Reset Delay vs. Temperature

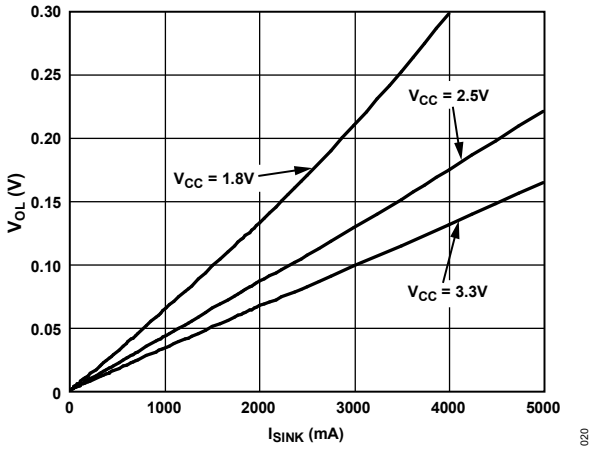


Figure 8. Output Low Voltage vs. Sink Current

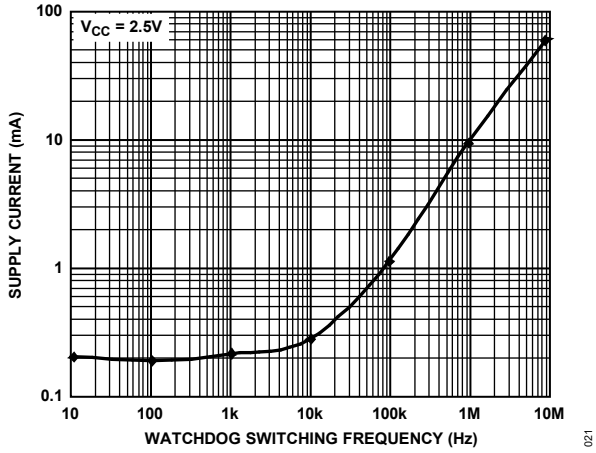


Figure 9. Supply Current vs. Watchdog Switching Frequency

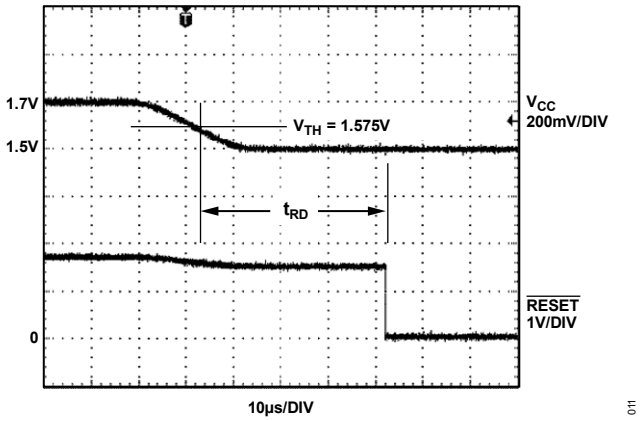


Figure 10. V_{cc} To Reset Delay

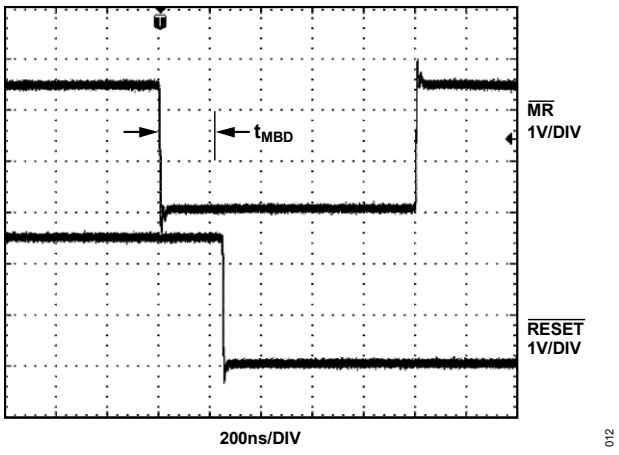
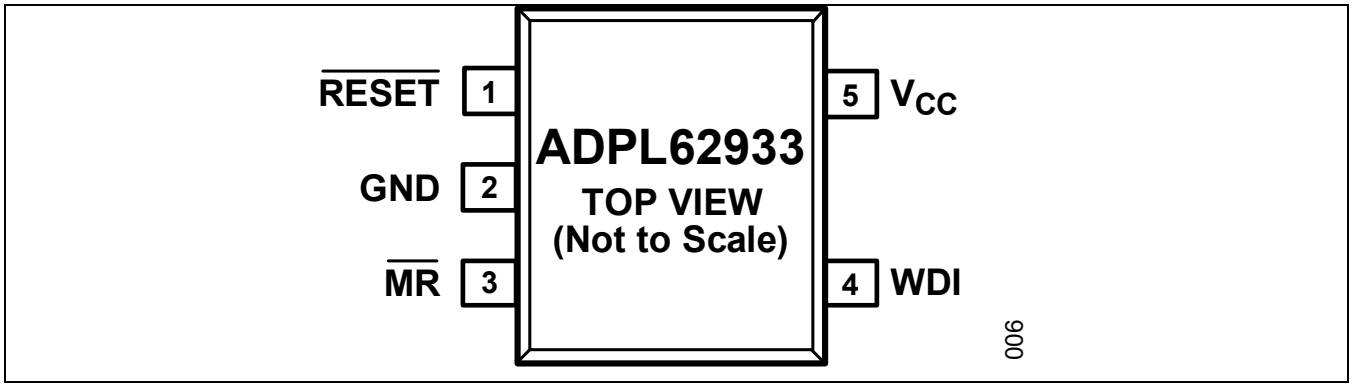


Figure 11. Manual Reset Delay

Pin Configurations



Pin Descriptions

PIN	NAME	FUNCTION
ADPL62933		
1	$\overline{\text{RESET}}$	Active-Low Open-Drain Reset Output. $\overline{\text{RESET}}$ transitions from high to low when V_{CC} drops below the selected reset threshold, $\overline{\text{MR}}$ is pulled low, or the watchdog timer expires. $\overline{\text{RESET}}$ remains low for the reset timeout period after V_{CC} exceeds the device reset threshold, MR deasserts, or after the watchog timer expires. Open-drain $\overline{\text{RESET}}$ outputs require an external pullup resistor.
2	GND	Ground.
3	$\overline{\text{MR}}$	Active-Low Manual Reset Input. Drive $\overline{\text{MR}}$ low to initiate a reset. The reset output remains asserted while $\overline{\text{MR}}$ is held low and for the reset timeout period after MR transitions high. Leave $\overline{\text{MR}}$ unconnected or connect to V_{CC} if unused. MR is internally pulled up to V_{CC} through 10kW.
4	WDI	Watchdog Input. If WDI remains high or low for longer than the watchdog timeout period, the internal watchdog timer expires, and a reset is triggered for the reset timeout period. The internal watchdog timer clears whenever reset is asserted, the manual reset is asserted, or WDI sees a rising or falling edge.
5	V_{CC}	Supply Voltage. Input for V_{CC} reset monitor. For noisy systems, bypass V_{CC} with a 0.1µF capacitor to GND.

Functional Diagrams

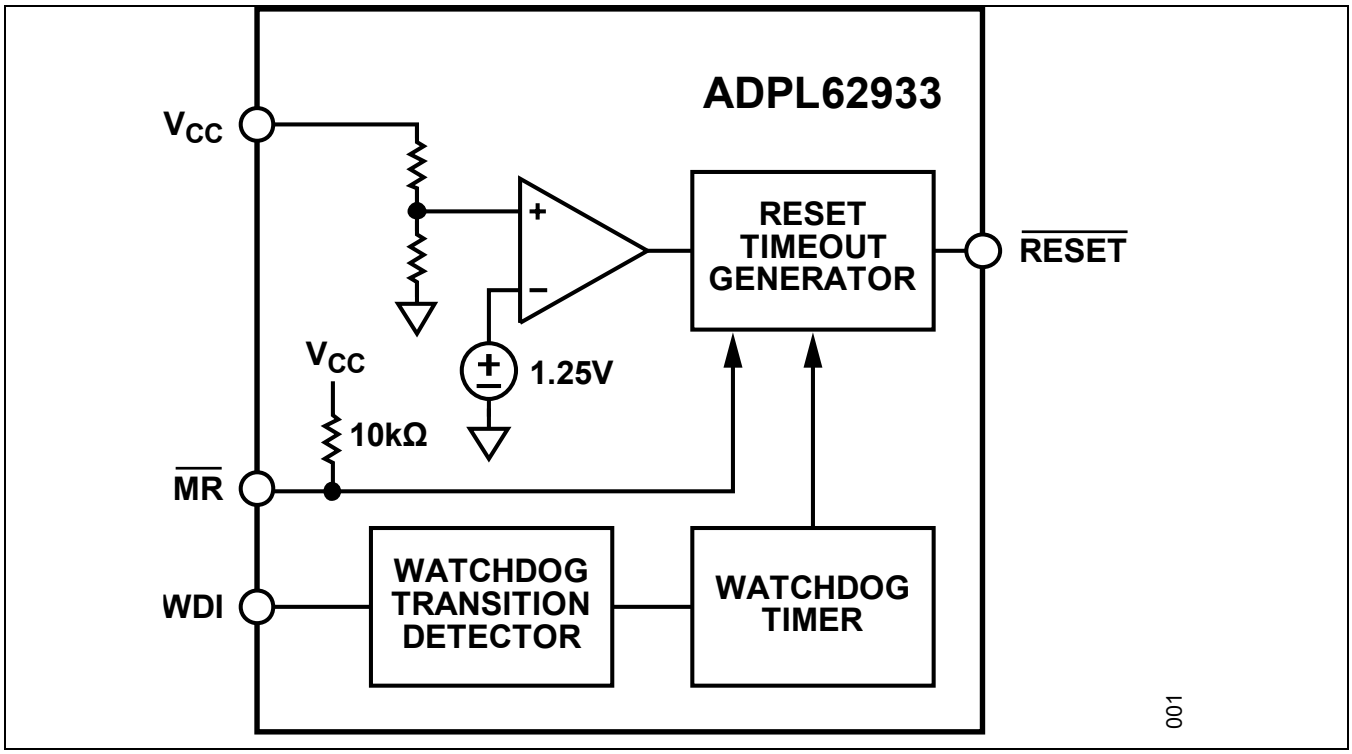


Figure 12. Functional Diagram

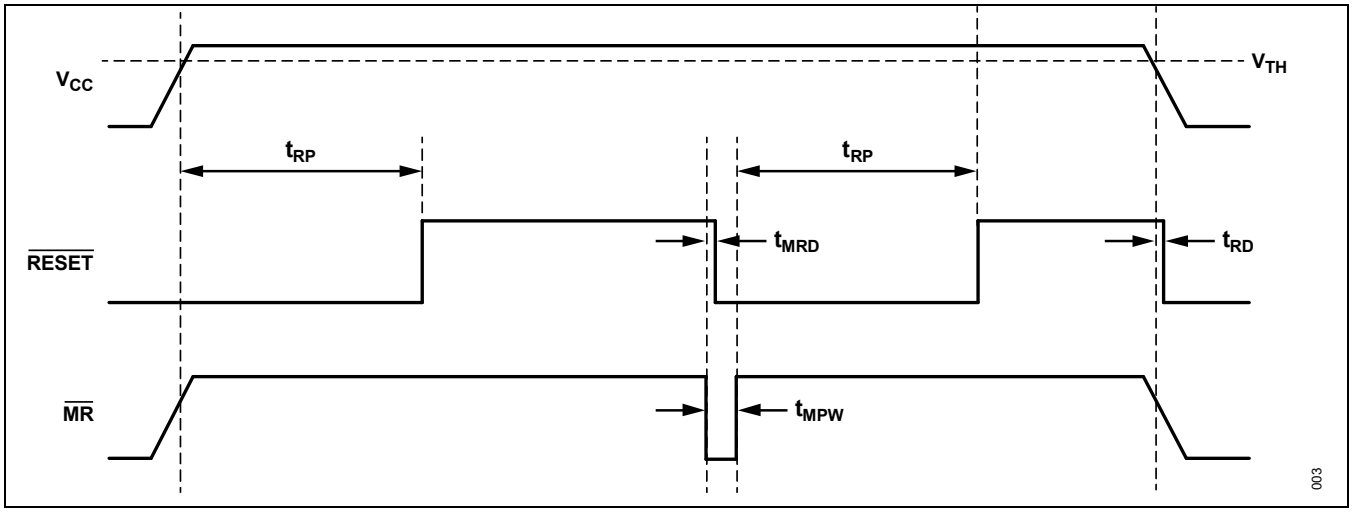


Figure 13. $\overline{RESET}$ Timing Relationship

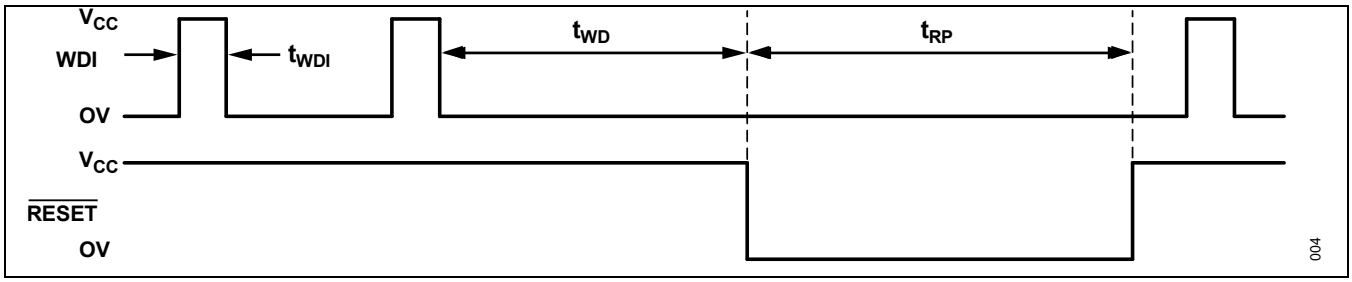


Figure 14. Detailed Watchdog Input Timing Relationship

Detailed Description

$\overline{\text{RESET}}$ Output

A µP's reset input starts the µP in a known state. The ADPL62933 µP supervisory circuits assert a reset to prevent code-execution errors during power-up, power-down, and brownout conditions. The ADPL62933 reset output is guaranteed to be valid for V_{CC} down to 1.1V.

Whenever V_{CC} falls below the reset threshold, the reset output asserts low for $\overline{\text{RESET}}$. Once V_{CC} exceeds the reset threshold, an internal timer keeps the reset output asserted for the specified reset timeout period, then after this interval the reset output deasserts (see *Figure 13*).

Manual Reset Input

Many µP-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. The ADPL62933 features an $\overline{\text{MR}}$ input. A logic low on $\overline{\text{MR}}$ asserts a reset. Reset remains asserted while MR is low and for the timeout period, t_{RP}, after $\overline{\text{MR}}$ returns high. The devices provide an internal 10kΩ pullup from MR to V_{CC}. Leave $\overline{\text{MR}}$ unconnected or connect to V_{CC} if unused. $\overline{\text{MR}}$ can be driven with CMOS logic levels or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{\text{MR}}$ to GND to implement a manual reset function; external debounce circuitry is not required. If $\overline{\text{MR}}$ is driven by long cables or the device is used in a noisy environment, connect a 0.1µF capacitor from $\overline{\text{MR}}$ to GND to provide additional noise immunity.

Watchdog Input

The ADPL62933's watchdog timer circuitry monitors the µP's activity. If the µP does not toggle (low-to-high or high-to-low) the watchdog input (WDI) within the watchdog timeout period (t_{WDI}), reset asserts for the reset timeout period (t_{RP}). The internal timer is cleared when reset asserts, when manual reset is asserted, or by a rising or falling edge on WDI. The watchdog input detects pulses as short as 150ns. While reset is asserted the watchdog timer does not count. As soon as reset deasserts, the watchdog timer resumes counting (see *Figure 14*).

Applications Information

Transient Immunity

In addition to issuing a reset to the µP during power-up, power-down, and brownout conditions, the ADPL62933 are relatively immune to short-duration supply transients, or glitches. The Maximum V_{CC} Transient Duration vs. Reset Threshold Overdrive graph in the Typical Operating Characteristics shows this relationship.

The area below the curve of the graph is the region in which these devices typically do not generate a reset pulse. This graph was generated using a falling pulse applied to V_{CC}, starting 100mV above the actual reset threshold, V_{TH}, and ending below this threshold (reset-threshold overdrive). As the magnitude of the transient increases, the maximum allowable pulse width decreases. Typically, a 100mV V_{CC} transient duration of 40µs or less does not cause a reset.

Interfacing to Other Voltages for Logic Compatibility

The open-drain $\overline{\text{RESET}}$ output can be used to interface to a µP with other logic levels. As shown in *Figure 15*, the open-drain output can be connected to voltages from 0 to 5.5V. Generally, the pullup resistor connected to $\overline{\text{RESET}}$ connects to the supply voltage that is being monitored at the IC's V_{CC} input. However, some systems use the open-drain output to level-shift from the monitored supply to reset circuitry powered by another supply voltage. Keep in mind that as the supervisor's V_{CC} decreases, so does the IC's ability to sink current at $\overline{\text{RESET}}$.

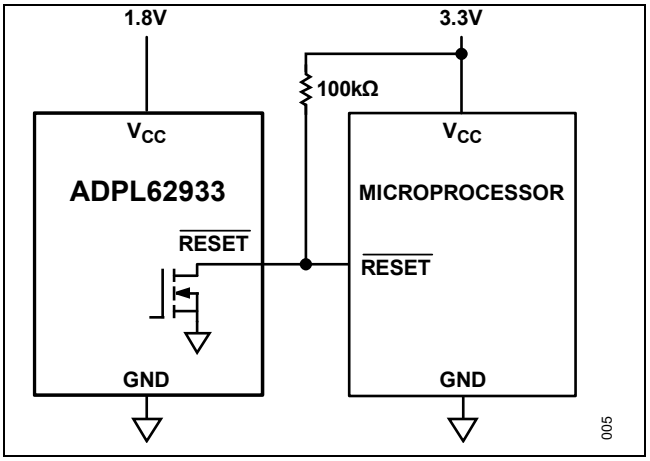


Figure 15. Interfacing with Other Voltage Levels

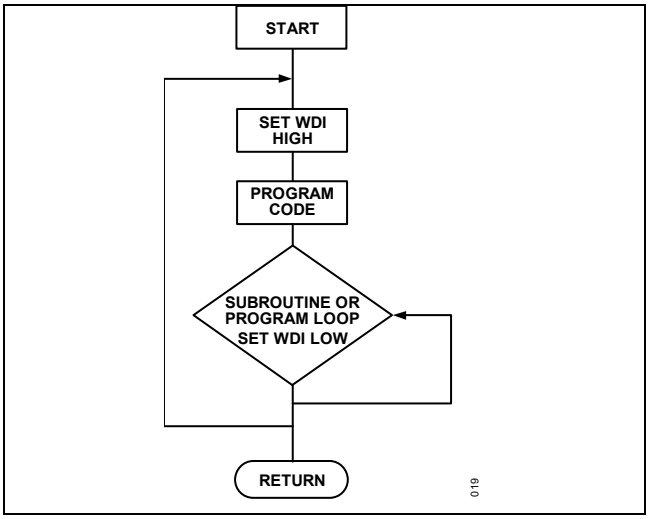


Figure 16. Watchdog Flow Diagram

Watchdog Software Considerations

One way to help the watchdog timer monitor software execution more closely is to set and reset the watchdog input at different points in the program, rather than pulsing the watchdog input high-low-high or low-high-low. This technique avoids a stuck loop, in which the watchdog timer would continue to be reset inside the loop, keeping the watchdog from timing out.

The *Figure 16* shows an example of a flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should hang in any subroutine, the problem would quickly be corrected, since the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued.

Table 1. Threshold Suffix Guide

SUFFIX	V_{CC} THRESHOLD FALLING			UNITS
	MIN	TYP	MAX	
46	4.486	4.625	4.764	V
45	4.365	4.500	4.635	
44	4.244	4.375	4.506	
43	4.171	4.300	4.408	
42	4.074	4.200	4.429	
41	3.977	4.100	4.326	
40	3.880	4.000	4.120	
39	3.783	3.900	4.017	
38	3.686	3.800	3.914	
37	3.589	3.700	3.811	
36	3.492	3.600	3.708	
35	3.395	3.500	3.605	
34	3.298	3.400	3.502	
33	3.201	3.300	3.399	
32	3.104	3.200	3.296	
31	2.983	3.075	3.167	
30	2.910	3.000	3.090	
29	2.837	2.925	3.013	
28	2.716	2.800	2.884	
27	2.619	2.700	2.781	
26	2.546	2.625	2.704	
25	2.425	2.500	2.575	
24	2.328	2.400	2.472	
23	2.244	2.313	2.382	
225	2.168	2.235	2.302	
22	2.122	2.188	2.254	
21	2.037	2.100	2.163	
20	1.940	2.000	2.060	
19	1.843	1.900	1.957	
18	1.746	1.800	1.854	
17	1.615	1.665	1.715	
16	1.528	1.575	1.622	

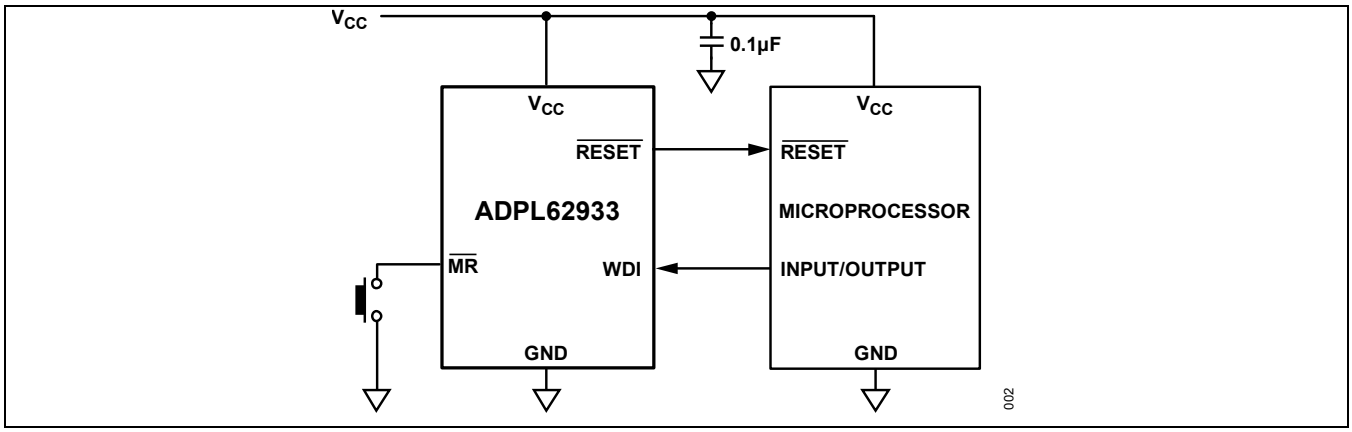
Table 2. Watchdog Timeout

SUFFIX	WATCHDOG TIMEOUT PERIOD			
	MIN	TYP	MAX	UNITS
S	1.5	3.3	7.75	s
L	95	209	487	

Table 3. Reset Timeout Periods

TIMEOUT OPTION	RESET TIMEOUT PERIODS			
	MIN	TYP	MAX	UNITS
D1	10	15	25	ms
D2	40	60	80	
D3	150	225	300	
D4	1200	1800	2400	
D5	300	450	600	
D6	600	900	1200	

Typical Application Circuits



Ordering Information

PART†	TEMP RANGE	PIN-PACKAGE
ADPL62933UK29D3S+	-40°C to +85°C	5 SOT23-5
ADPL62933UK29D3S+T	-40°C to +85°C	5 SOT23-5
ADPL62933UK_ _D_ _+	-40°C to +85°C	5 SOT23-5
ADPL62933UK_ _D_ _+T	-40°C to +85°C	5 SOT23-5

†Insert reset threshold suffix (see Table 1, Threshold Suffix Guide) after UK. Insert the number corresponding to the desired reset timeout period (see Table 3, Reset Timeout Period) after D. Insert the letter corresponding to the desired watchdog timeout period (S or L, see Table 2) into the blank following the reset timeout period suffix.

Note: *Sample stock is generally held on standard versions only (see Ordering Information). Standard versions have an order increment of 2500 pieces. Nonstandard versions have an order increment of 10,000 pieces. Contact factory for availability of nonstandard versions.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	01/24	Release to market intro	—

Mouser Electronics

Authorized Distributor

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