MAX14822

16-Channel High-Voltage Protected, Low-Power, Low-Noise Operational Amplifier

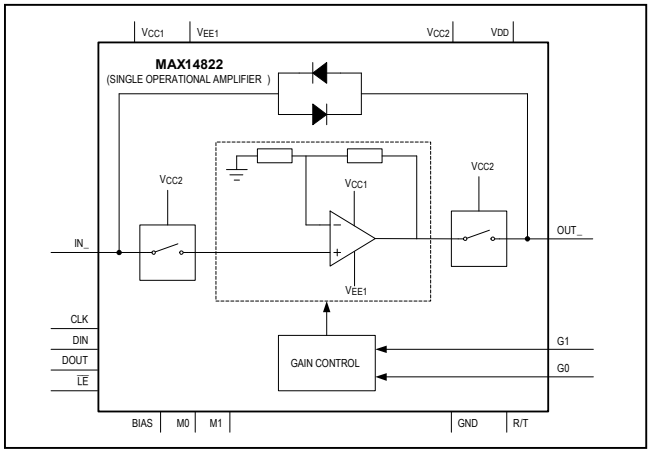
General Description

The MAX14822 is a 16-channel, high-voltage protected, low-noise, operational amplifier. This device is a fully integrated, very compact solution for in-probe amplification of echo signals coming from transducers in an ultrasound system. The use of in-probe buffering improves signal-to-noise ratio (SNR) for transducers featuring high-output impedance. This results in greater penetration depth and sensitivity. The device can be adopted in ultrasound probes without any changes in the system (scanner machine). Typical applications include high-impedance piezoelectric transducers (PZT) and capacitive micromachined ultrasonic transducers (CMUT), in-probe buffering, and amplification.

The device features 16 operational amplifiers with a small-signal output impedance of 22Ω (typ). The low-noise amplifier features > 45MHz (typ) -3dB bandwidth and very low voltage and current noise, ensuring excellent noise figure. Power dissipation of the device is extremely low to match the severe power consumption requirement of ultrasound probe electronics. The device provides high-voltage (HV) protection for inputs and outputs of the operational amplifiers. An integrated automatic HV switch protects each of the amplifier's channel outputs from HV bursts up to ±105V.

The MAX14822 is available in a small 7mm x 7mm CTBGA package and is specified over a 0°C to +70°C temperature range.

Functional Diagram



Benefits and Features

- High Channel-Count and Robust Integration Simplify Designs and Reduce Board Space
  - 16 Channels of Up to ±105V High-Voltage Protection
  - Ultrafast, Automatic High-Voltage Protected T/R Switch
  - Ultrafast Recovery Time After TX Burst 0.8µs (Typ)
  - OVP for Signals Greater Than ±1.39V (Typ)
- Flexible Programmability Options Enable Use in Many Diagnostic Applications
  - Global T/R Control Switch for Flexible Protection Strategies
  - Individual Channel TX, RX, or TX/RX control Through SPI
  - Operating Mode and Settings Programmable Through SPI or Hardware
  - Selectable Voltage Gain: 0dB, 3.5dB, 6dB, 9.5dB
  - 22Ω (Typ) Low-Signal Output Impedance
  - High Input Impedance
- Extremely Low Power Dissipation and Low Noise to Meet In-Probe Requirements
  - 5.9mW/ch, BIAS = 0 (Typ)
  - 8.6mW/ch, BIAS = 1 (Typ)
  - Programmable Bias Current (BIAS)
  - > 65MHz (typ) 3dB Bandwidth at 0dB Gain
  - > 45MHz (typ) 3dB Bandwidth at High Gain
  - Low Voltage and Current Noise
    - 1.54nV/√Hz, 1.67pA/√Hz (Typ) (BIAS = 0, Gain = 6dB)
    - 1.28nV/√Hz, 1.8pA/√Hz (Typ) (BIAS = 1, Gain = 6dB)

Applications

- Ultrasound Medical Imaging, PZT High-Impedance Probes
- Ultrasound Medical Imaging, CMUT Probes
- Ultrasound Industrial Imaging, PZT NDT Probes
- Other Applications (Non-Ultrasound)

Ordering Information **appears at end of data sheet.**

19-7580; Rev 0; 4/15

maxim integrated™

Absolute Maximum Ratings

(All voltages referenced to GND.)
$V_{OUT\_}$ ..... -110V to +110V
$V_{IN\_} - V_{OUT\_}$ (continuous) ..... -0.5V to +0.05V
$V_{IN\_}$ ..... -110V to +110V
V_{CC1} ..... -0.3V to +2V
V_{EE1} ..... -2V to +0.3V
V_{CC1} - V_{EE1} ..... -0.3V to +3.6V
V_{CC2}, V_{DD} ..... -0.3V to +5.6V

M0, M1, BIAS, G0, G1, R/T, $\overline{LE}$,
DIN, DOUT, CLK ..... -0.3V to +5.6V
64 CTBGA (derate 30.30mW/°C above +70°C):
Continuous Power Dissipation (T_A = +70°C) 2424.2mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

CTBGA
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1) ..... 33°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) (Note1) ..... 10°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{CC1} = -V_{EE1} = +1.37V to +1.6V, V_{CC2} = = +5V ±5%, V_{DD} = +2.375V to +5.25V, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC1} = -V_{EE1} = +1.4V, V_{CC2} = V_{DD} = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
Supply Voltage 1	V_{CC1}	V_{CC1} = -V_{EE1}		1.37	1.4	1.6	V
Supply Voltage 2	V_{CC2}			4.75	5	5.25	V
Supply Voltage 3	V_{DD}			2.375		5.25	V
Signal Range	V_{OUT}			-105		+105	V
Quiescent Supply Current From V_{CC1}	I_{CC1}	IN_ = 0, per channel	BIAS = 0		2.1	2.9	mA
			BIAS = 1		3.06	4.15	
Quiescent Supply Current From V_{EE1}	I_{EE1}	IN_ = 0, per channel	BIAS = 0		2.1	2.9	mA
			BIAS = 1		3.06	4.15	
Quiescent Supply Current From V_{CC1} in Transmit-Only Mode	I_{CC1T}	Total consumption for all channels. D (23:38) = 1	BIAS = 0		1.5		mA
			BIAS = 1		2.2		
Quiescent Supply Current from V_{EE1} in Transmit-Only Mode	I_{EE1T}	Total consumption for all channels. D (23:38) = 1	BIAS = 0		1.4		mA
			BIAS = 1		2.1		
Total Supply Quiescent Current From V_{CC2} in Receive Mode	I_{CC2R}	IN_ = 0			12	30	µA
Total Supply Quiescent Current From V_{CC2} in Transmit Mode	I_{CC2T}	M0 = M1 = 0, R/T = 0			3.4	5.4	mA

DC Electrical Characteristics (continued)

(V_{CC1} = -V_{EE1} = +1.37V to +1.6V, V_{CC2} = = +5V ±5%, V_{DD} = +2.375V to +5.25V, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC1} = -V_{EE1} = +1.4V, V_{CC2} = V_{DD} = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Total Supply Quiescent Current From V_{DD}	I_{DD}				3	5.1	µA
Quiescent Power Dissipation Per Channel in Receive Mode Only	P_{D1}	IN_ = 0	BIAS = 0		5.9	9.5	mW
			BIAS = 1		8.6	13.9	
Quiescent Power Dissipation Per Channel in Transmit-Only Mode Only	P_{D2}	M0 = 1, M1 = 0, IN_ = 0	BIAS = 0		0.25		mW
			BIAS = 1		0.38		
Additional Power Dissipation During Transmission (Per Channel)	P_{D3}	Bipolar TX pulses with ±60V amplitude dv/dt = 10V/ns, f_{SW} = 5MHz, 2 periods, PRF = 20kHz			3		mW
Supply Current in Shutdown Mode	I_{SDN}	From V_{CC2}				30	µA
		From V_{CC1}, V_{EE1}, V_{DD}				8	µA
HV PROTECTION							
HV Protection Output Switch Resistance	R_{OUT_SW}	V_{OUT} = 50mV T_A = +25°C			22		Ω
HV Protection Input Switch Resistance	R_{IN_SW}	V_{IN} = 50mV T_A = +25°C			22		Ω
Equivalent On Output Impedance	Z_{OUT}	f_{SW} = 5MHz, V_{IN} = 0			22		Ω
Off Output Current	I_{OFF}	V_{OUT} = +100V			1		mA
		V_{OUT} = -100V			1.4		
Large-Signal Input Capacitance	C_{O_OFF}	V_{OUT} = ±100V, 2MHz, M0 = M1 = 0, R/T = 0			15		pF
Equivalent DC Input Offset Bias	V_{OS}	Output DC offset referred to input. IN floating, six sigma.		-25		+20	mV
Positive OVP Threshold	V_{OVP+}	Output impedance ≥ 1kΩ, V_{CC2} = +5, T_A = +25°C		1.15	1.39	1.8	V
Negative OVP Threshold	V_{OVP-}	Output impedance ≥ 1kΩ, V_{CC2} = +5, T_A = +25ºC		-1.65	-1.25	-1.1	V
Transmission Diode On-Resistance	R_{ON}	I = 1A			1.5		Ω
Transmission Diode Drop	TX_{DROP}	I = 1mA		600	810	950	mV
LOW-NOISE AMPLIFIER							
Maximum Output Voltage Range	V_{OUT_P-P}	R_L = 1kΩ, THD < 2% (peak-to-peak), f_{SW} = 5MHz			800		mV_{P-P}

DC Electrical Characteristics (continued)

(V_{CC1} = -V_{EE1} = +1.37V to +1.6V, V_{CC2} = = +5V ±5%, V_{DD} = +2.375V to +5.25V, T_A = 0°C to +70°C unless otherwise noted. Typical values are at V_{CC1} = -V_{EE1} = +1.4V, V_{CC2} = V_{DD} = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Voltage Gain (No Load)	A_V	[G0:G1] = 00			0		dB
		[G0:G1] = 01		3.0	3.5	4.0	dB
		[G0:G1] = 10		5.5	6.0	6.5	dB
		[G0:G1] = 11		9.0	9.5	10.0	dB
Input Resistance	R_{IN1}	BIAS = 0			14.8		kΩ
		BIAS = 1			11.3		kΩ
Input Shunt Capacitance Between IN_ and GND	C_{IN}	2MHz, 100mV_{P-P}, R_L = 200Ω	[G0:G1] = 00		7.6		pF
			[G0:G1] = 01		7.1		
			[G0:G1] = 10		6.4		
			[G0:G1] = 11		5.2		
LOGIC DIGITAL							
Low-Level Input	V_{IL}					0.2 x V_{DD}	V
High-Level Input	V_{IH}			0.8 x V_{DD}			V
Logic Input Leakage	I_{LEAK}			-1		1	µA
Input Capacitance	C_{IN}				4		pF

AC Electrical Characteristics

(V_{CC1} = -V_{EE1} = +1.37V to +1.6V, V_{CC2} = = +5V ±5%, V_{DD} = +2.375V to +5.25V, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC1} = -V_{EE1} = +1.4V, V_{CC2} = V_{DD} = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Total Harmonic Distortion	THD	f_{SW} = 5MHz, R_L = 1kΩ, V_{IN} = 20mV_{P-P}, Gain = 6dB			-50		dB
-3dB Bandwidth	BW1	R_L = 200Ω, C_L = 40pF, V_{IN} = 20mV_{P-P}, T_A = +25°C, BIAS = 0	Gain = 0dB		68		MHz
			Gain = 3.5dB		55		
			Gain = 6dB		51		
			Gain = 9.5dB		46		
		R_L = 200Ω, C_L = 40pF, V_{IN} = 20mV_{P-P}, T_A = +25°C, BIAS = 1	Gain = 0dB		85		
			Gain = 3.5dB		71		
			Gain = 6dB		57		
			Gain = 9.5dB		51		
Input Voltage Noise	e_{NOISE}	Gain = 6dB	BIAS = 0		1.54		nV/√Hz
			BIAS = 1		1.28		
Input Current Noise	I_{NOISE}	Gain = 6dB	BIAS = 0		1.67		pA/√Hz
			BIAS = 1		1.80		

AC Electrical Characteristics (continued)

(V_{CC1} = -V_{EE1} = +1.37V to +1.6V, V_{CC2} = = +5V ±5%, V_{DD} = +2.375V to +5.25V, T_A = 0°C to +70°C unless otherwise noted. Typical values are at V_{CC1} = -V_{EE1} = +1.4V, V_{CC2} = V_{DD} = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Noise Figure	NF	R_{SOURCE} = 200Ω, Gain = 6dB	BIAS = 0		2.6		nV/dB
			BIAS = 1		2.1		
		R_{SOURCE} = 500Ω, Gain = 6dB	BIAS = 0		1.5		nV/dB
			BIAS = 1		1.3		
Transmit Large-Signal Insertion Loss	I_L	RMS(V_{OUT})/RMS(V_{SOURCE}), automatic protection excitation signal 120V_{P-P}, 5MHz one period, R_{SOURCE} = 100Ω			1		dB
HV Pulse Inversion	P_{INV_HV}	120V_{P-P}, f0 = 5MHz one period, R_{SOURCE} = 50Ω, automatic protection, ratio between the max of the harmonics of the sum signal in the bandwidth 2xf0 ±f0/2 and the fundamental	Auto		-41		dB
			Semiauto or manual		-41		
LV Pulse Inversion	P_{INV_LV}	10V_{P-P}, f0 = 5MHz one period, R_{SOURCE} = 50Ω, automatic protection, ratio between the max of the harmonics of the sum signal in the bandwidth 2xf0 ±f0/2 and the fundamental	Auto		-38		dB
			Semiauto or manual		-38		

AC Electrical Characteristics (continued)

(V_{CC1} = -V_{EE1} = +1.37V to +1.6V, V_{CC2} = = +5V ±5%, V_{DD} = +2.375V to +5.25V, T_A = 0°C to +70°C unless otherwise noted. Typical values are at V_{CC1} = -V_{EE1} = +1.4V, V_{CC2} = V_{DD} = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Channel Crosstalk	CT	f_{SW} = 5MHz, V_{OUT} = 0.2V_{P-P} (adjacent channels), R_{IN} = 200Ω, R_L = 50Ω	Gain = 0dB		-50		dB
			Gain = 9.5dB		-40		
Slew Rate	SR	R_L = 1kΩ, BIAS = 0			±27		V/µs
		R_L = 1kΩ, BIAS = 1			±39		V/µs
Power-Supply Rejection Ratio	PSRR-V_{CC1}	f_{SW} = 5MHz, 10mV_{P-P}, R_{IN} = 200Ω, R_L = 50Ω	Gain = 0dB		-49		dB
			Gain = 9.5dB		-42.5		
	PSRR-V_{EE1}	f_{SW} = 5MHz, 10mV_{P-P}, R_{IN} = 200Ω, R_L = 50Ω	Gain = 0dB		-42		
			Gain = 9.5dB		-43		
	PSRR-V_{CC2}	f_{SW} = 5MHz, 10mV_{P-P}, R_{IN} = 200Ω, R_L = 50Ω	Gain = 0dB		-44.5		
			Gain = 9.5dB		-37		
Recovery Time After A Transmitted Pulse	t_R	V_{CC2} = +5V, ±5V ≤ pulse amplitude ≤ ±60V, M0, M1 = 10 or 11, Figure 1, T_A = +25°C			0.8		µs
Recovery Time with D(22) = 1	t_{R2}	V_{CC2} = +5V, D(22)=1, ±5V ≤ pulse amplitude ≤ ±60V M0, M1 = 10 or 11, PWM = 1, Figure 1, T_A = +25°C			1.45		µs
R/T High-to-Low Setup Time	T_{RT_SET}	From R/T low, protection switches in high-Z, M0, M1 = 01 or 11				1	µs
R/T Low-to-High Setup Time	T_{TR_SET}	From R/T high, protection switches on, T_A = +25°C, M0, M1 = 01			0.8		µs
R/T Minimum Pulse Width	T_{PULSE}	M0, M1 = 11, semiautomatic protection		100			ns

AC Electrical Characteristics (continued)

(V_{CC1} = -V_{EE1} = +1.37V to +1.6V, V_{CC2} = = +5V ±5%, V_{DD} = +2.375V to +5.25V, T_A = 0°C to +70°C unless otherwise noted. Typical values are at V_{CC1} = -V_{EE1} = +1.4V, V_{CC2} = V_{DD} = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
R/T High-to-Low Glitch	V_{GLITCH}	100Ω load, measured at node IN		110		mV
R/T Low-to-High Glitch	$V_{GLITCH2}$	100Ω load, measured at node IN		150		mV
Enable Time From Shutdown to Normal Operation	T_{EN}				500	µs
Disable Time From Shutdown to Normal Operation	T_{DIS}				1	µs
Settling Time After SPI Programming Time	T_{SET1}	From $\overline{LE}$ falling-edge to fully settled			4	µs
M0, M1, G0, G1, Settling Time	T_{SET2}	From M0, M1, G0, G1, change to fully settled			4	µs
BIAS Settling Time	T_{BIAS}	From BIAS change to fully settled			80	µs
M0, M1, G0, G1, BIAS Rise/Fall Glitches	$V_{GLITCH3}$	100Ω Load, measured at node IN		20		mV
SPI TIMING						
Maximum Operating CLK Frequency	fclk	V_{DD} = +5V, Figure 4			50	MHz
D_{IN} to CLK Setup Time	t_{DS}	Figure 4	2.5			ns
D_{IN} to CLK Hold Time	t_{DH}	Figure 4	2.5			ns
CLK to $\overline{LE}$ Hold Time	t_{CH}	Figure 4	2.5			ns
CLK to $\overline{LE}$ Setup Time	t_{CS}	Figure 4	3.5			ns
$\overline{LE}$ Low Pulse Width	t_{WL}	Figure 4	10			ns
CLK to D_{OUT} Delay	t_{DO}	C_L = 10pF, V_{DD} = +5V			16.5	ns

Note 2: All specifications are 100% tested at T_A = +25°C, unless otherwise noted

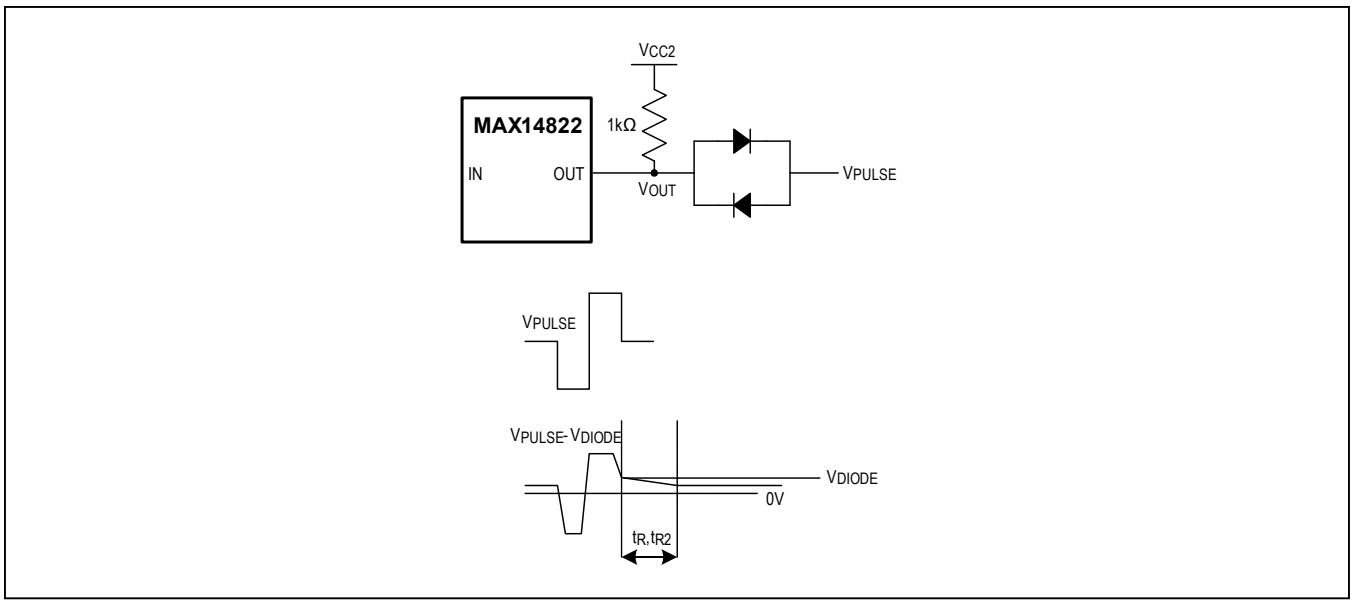
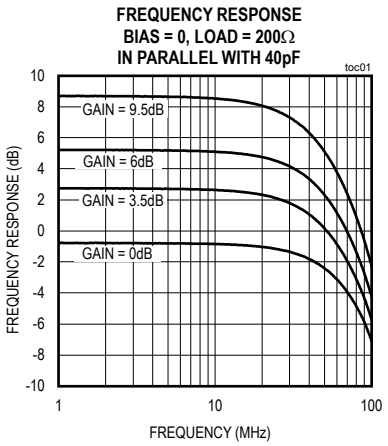
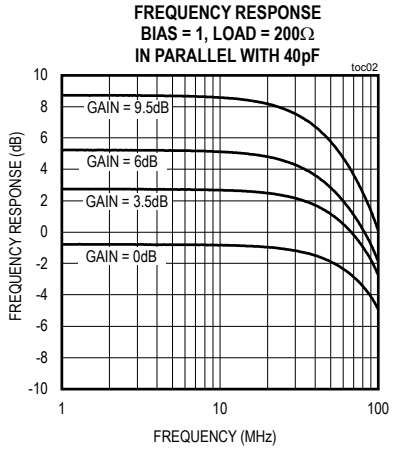


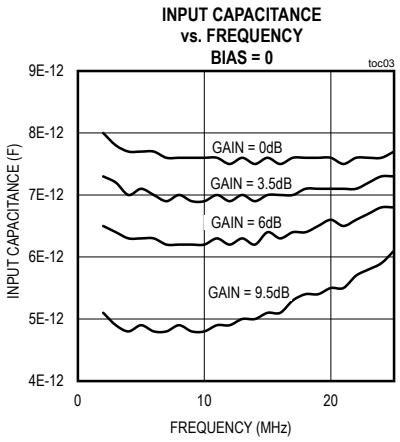
Figure 1. Recovery Time Diagram

Typical Operating Characteristics

(V_{CC1} = -V_{DD} = +1.4V, V_{CC2} = V_{VDD} = +5V, T_A = +25°C, R/T, unless otherwise noted.)



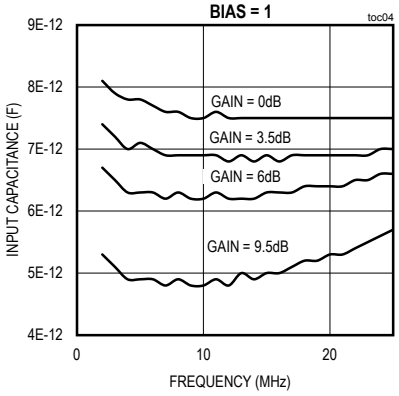




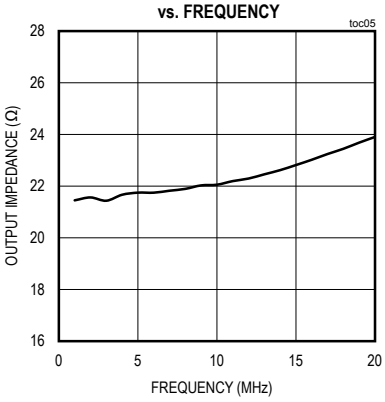
Typical Operating Characteristics (continued)

(V_{CC1} = -V_{DD} = +1.4V, V_{CC2} = V_{VDD} = +5V, T_A = +25°C, R/T, unless otherwise noted.)

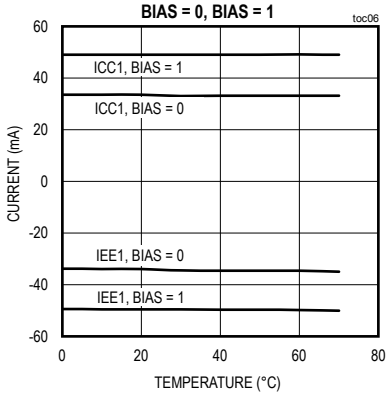
INPUT CAPACITANCE vs. FREQUENCY BIAS = 1



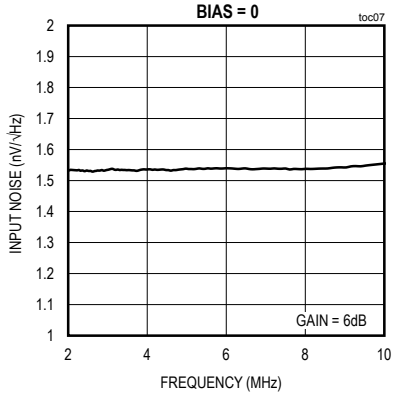
OUTPUT IMPEDANCE vs. FREQUENCY



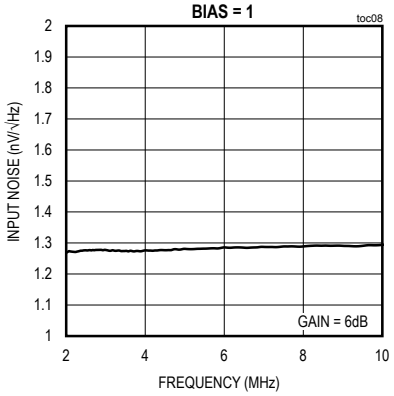
I_{CC1} AND I_{EE1} vs. TEMPERATURE BIAS = 0, BIAS = 1



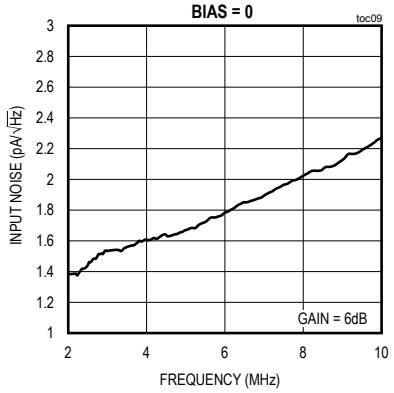
EQUIVALENT VOLTAGE INPUT NOISE vs. FREQUENCY BIAS = 0



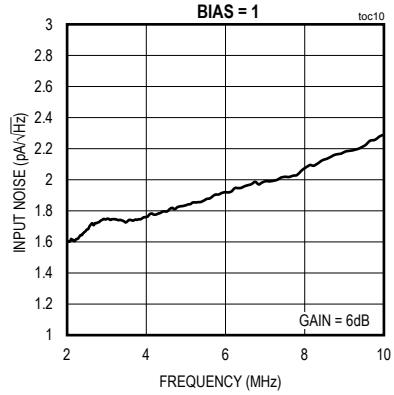
EQUIVALENT VOLTAGE INPUT NOISE vs. FREQUENCY BIAS = 1



EQUIVALENT CURRENT INPUT NOISE vs. FREQUENCY BIAS = 0



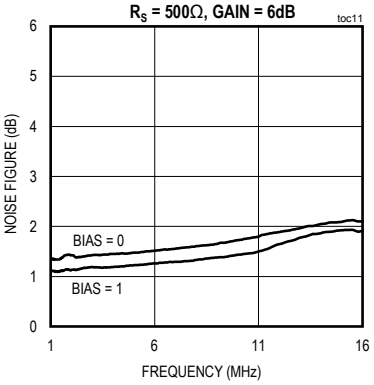
EQUIVALENT CURRENT INPUT NOISE vs. FREQUENCY BIAS = 1



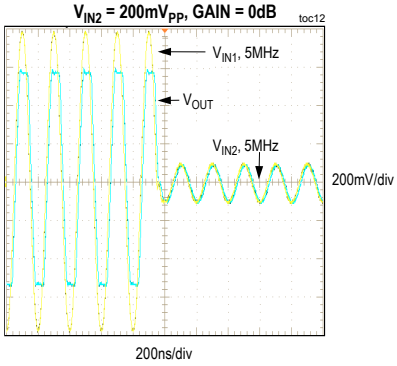
Typical Operating Characteristics (continued)

(V_{CC1} = -V_{DD} = +1.4V, V_{CC2} = V_{VDD} = +5V, T_A = +25°C, R/T, unless otherwise noted.)

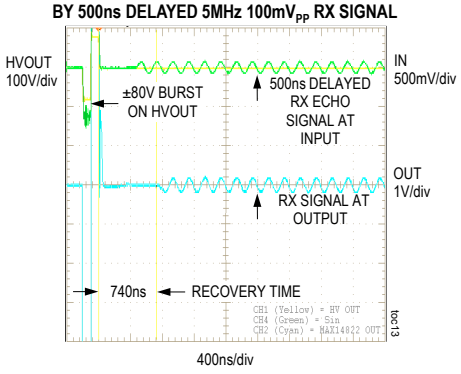
NOISE FIGURE vs. FREQUENCY
R_S = 500Ω, GAIN = 6dB



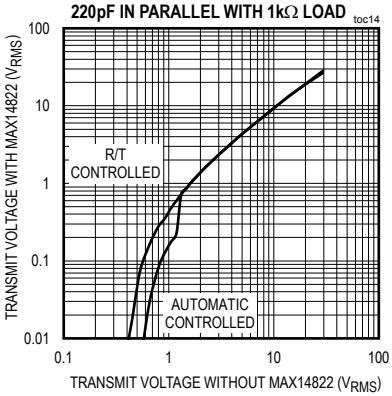
LARGE-SIGNAL RECOVERY
SINUSOIDAL SIGNAL, V_{IN1} = 1.6V_{PP}, V_{IN2} = 200mV_{PP}, GAIN = 0dB



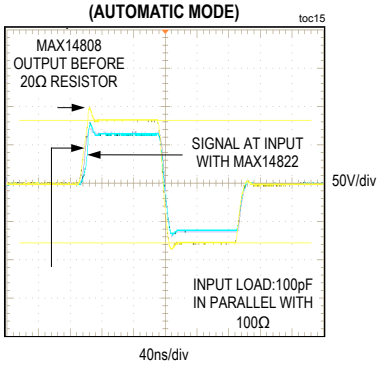
RECOVERY AFTER HV BURST
AUTOMATIC MODE, 5MHz HV BURST FOLLOWED BY 500ns DELAYED 5MHz 100mV_{PP} RX SIGNAL



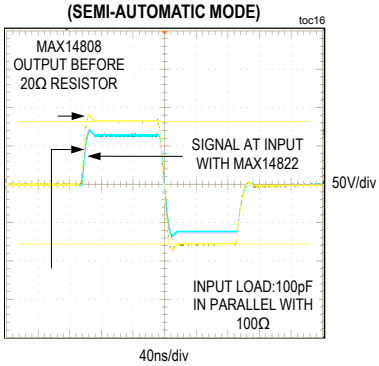
TX INSERTION LOSS vs. AMPLITUDE
5MHz 50Ω SOURCE, 220pF IN PARALLEL WITH 1kΩ LOAD



TRANSMIT RESPONSE WITH AND WITHOUT MAX14822 (AUTOMATIC MODE)



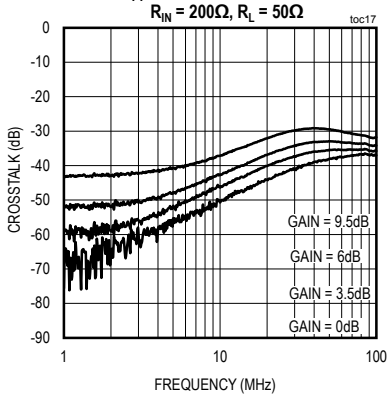
TRANSMIT RESPONSE WITH AND WITHOUT MAX14822 (SEMI-AUTOMATIC MODE)



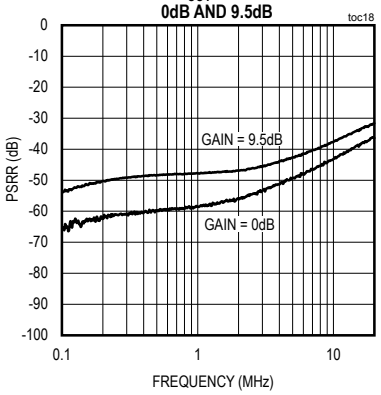
Typical Operating Characteristics (continued)

(V_{CC1} = -V_{DD} = +1.4V, V_{CC2} = V_{VDD} = +5V, T_A = +25°C, R/T, unless otherwise noted.)

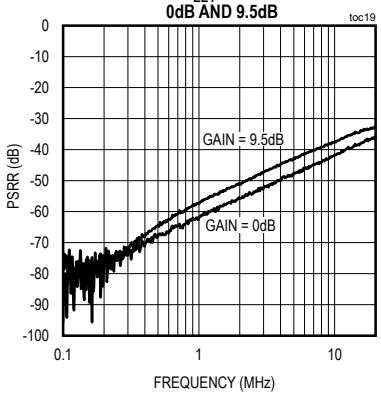
CH1 vs. CH2 CROSSTALK
0.2V_{PP} TONE ADJACENT SIGNALS
R_{IN} = 200Ω, R_L = 50Ω



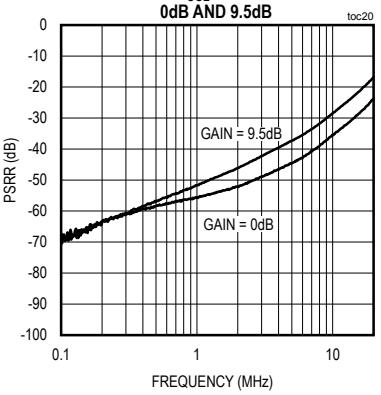
V_{CC1} PSRR
0dB AND 9.5dB



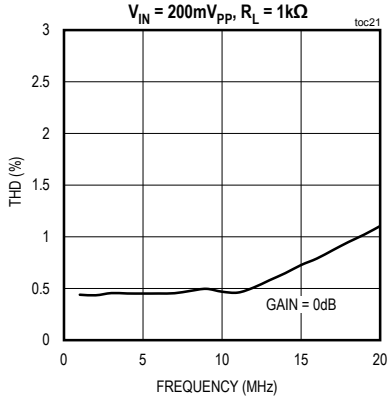
V_{EE1} PSRR
0dB AND 9.5dB



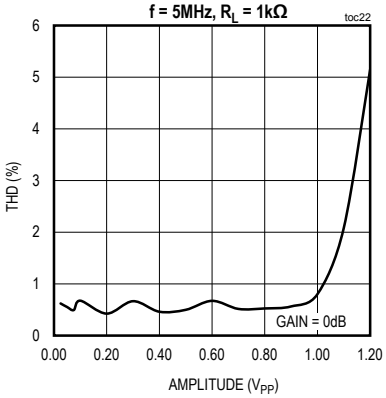
V_{CC2} PSRR
0dB AND 9.5dB



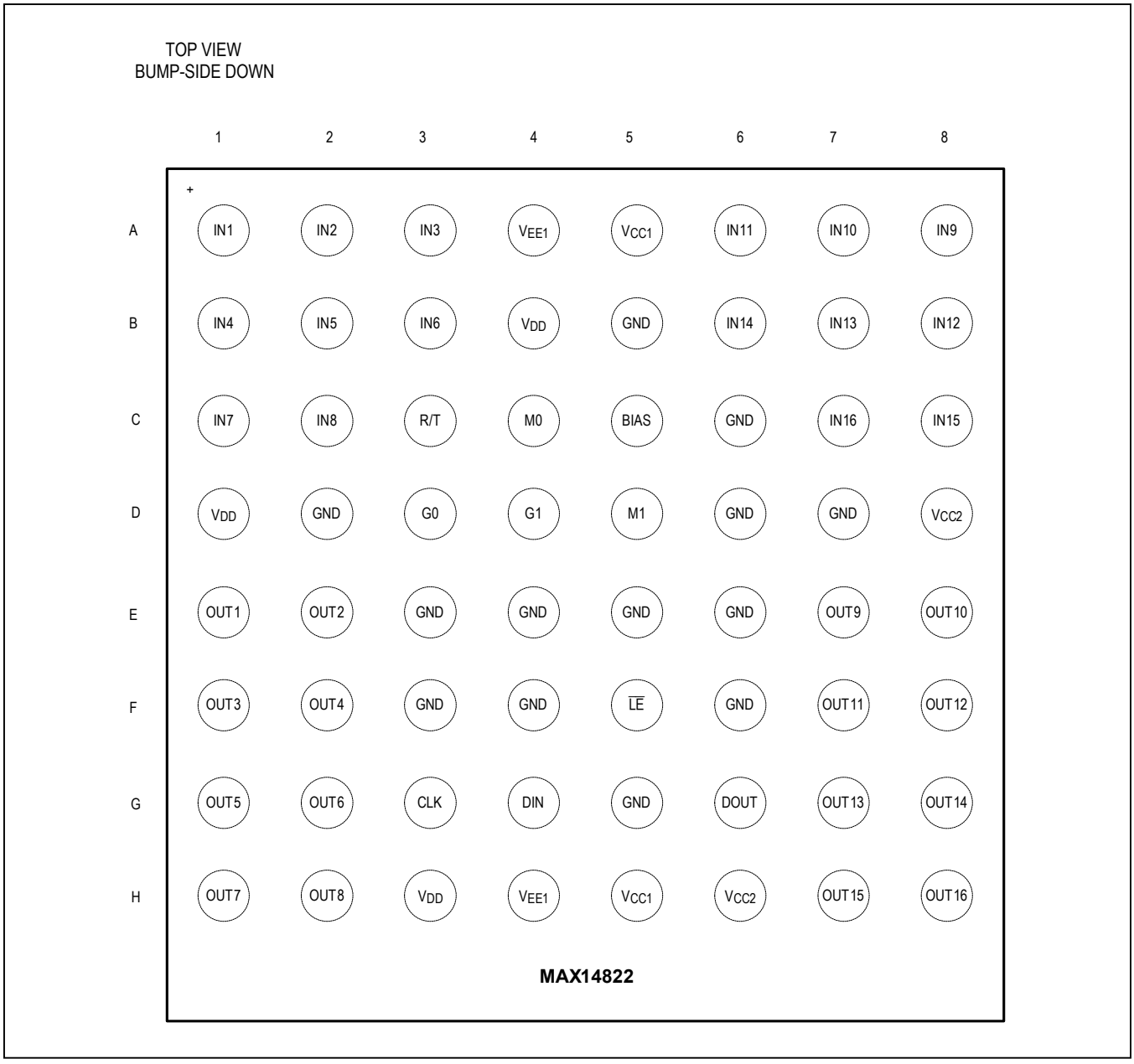
THD vs. FREQUENCY
V_{IN} = 200mV_{PP}, R_L = 1kΩ



THD vs. INPUT AMPLITUDE
f = 5MHz, R_L = 1kΩ



Bump Configuration



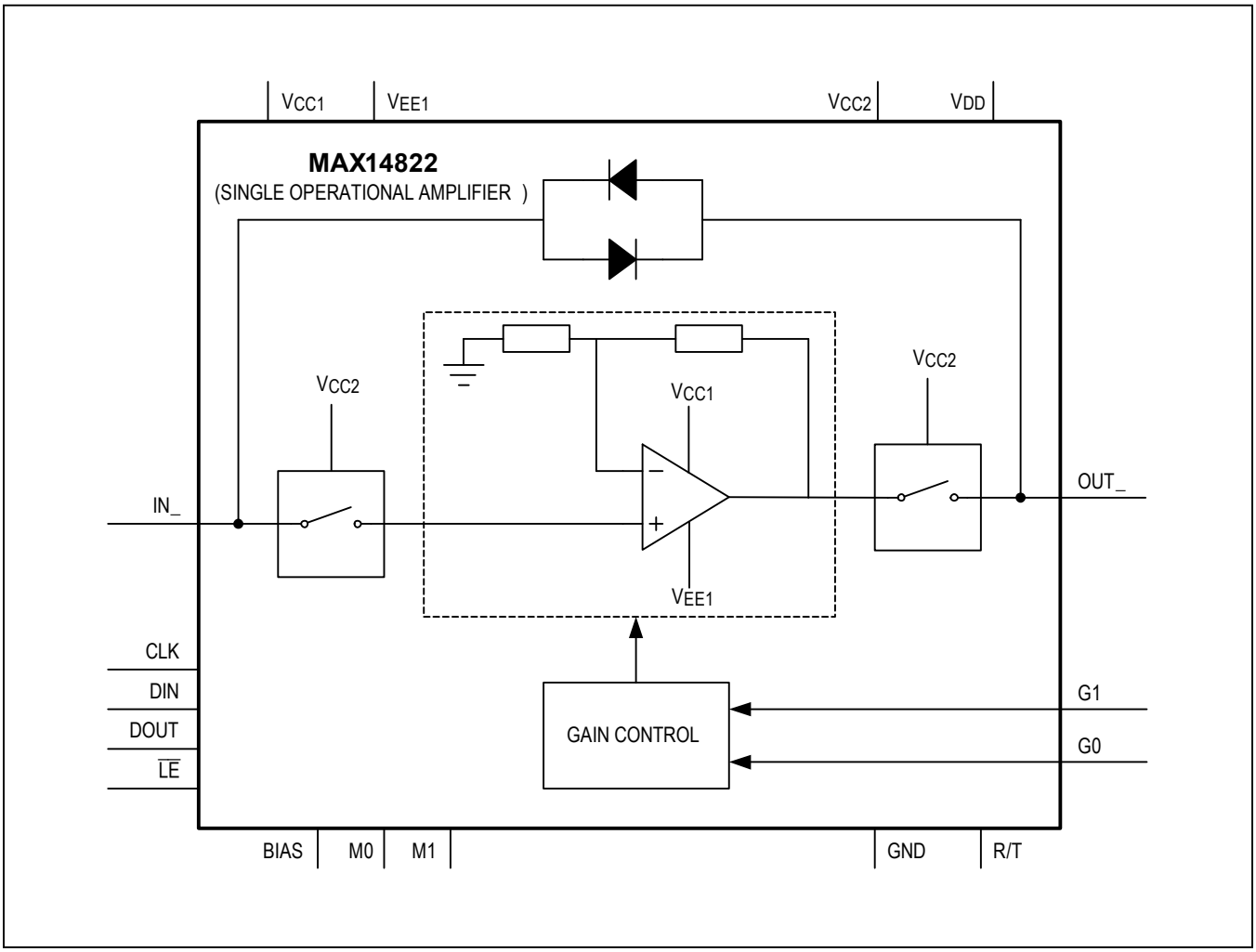
Bump Description

PIN	NAME	FUNCTION
A1	IN1	LNA Input. Connect IN1 to the transducer.
A2	IN2	LNA Input. Connect IN2 to the transducer.
A3	IN3	LNA Input. Connect IN3 to the transducer.
A4	V_{EE1}	Negative LNA Voltage Supply (-1.4V, typ). Bypass with 100nF or greater ceramic capacitor to GND.
A5	V_{CC1}	Positive LNA Voltage Supply (+1.4V, typ). Bypass with 100nF or greater ceramic capacitor to GND.
A6	IN11	LNA Input. Connect IN11 to the transducer.
A7	IN10	LNA Input. Connect IN10 to the transducer.
A8	IN9	LNA Input. Connect IN9 to the transducer.
B1	IN4	LNA Input. Connect IN4 to the transducer.
B2	IN5	LNA Input. Connect IN5 to the transducer.
B3	IN6	LNA Input. Connect IN6 to the transducer.
B4	V_{DD}	Positive Voltage Supply for Digital Inputs (+5V, typ.). Bypass with 100nF or greater ceramic capacitor to GND.
B5	GND	
B6	IN14	LNA Input. Connect IN14 to the transducer.
B7	IN13	LNA Input. Connect IN13 to the transducer.
B8	IN12	LNA Input. Connect IN12 to the transducer.
C1	IN7	LNA Input. Connect IN7 to the transducer.
C2	IN8	LNA Input. Connect IN8 to the transducer.
C3	R/T	Digital CMOS Control Input. Control the status of HV protections.
C4	M0	Digital CMOS Control Input. Together with M1 controls the operating mode of the MAX14822.
C5	BIAS	Digital CMOS Control Input. Connect BIAS to GND for low-bias operation. Connect BIAS to V_{DD} for high-bias operation.
C6	GND	Ground
C7	IN16	LNA Input. Connect IN16 to the transducer.
C8	IN15	LNA Input. Connect IN15 to the transducer.
D1	V_{DD}	Positive Voltage Supply for CMOS Input Interface (+5V, typ.). Bypass with 100nF or greater ceramic capacitor to GND.
D2	GND	Ground
D3	G0	Digital CMOS Control Input. Control the LNA gain.
D4	G1	Digital CMOS Control Input. Control the LNA gain.
D5	M1	Digital CMOS Control Input. Together with M0 controls the operating mode of the MAX14822.
D6	GND	Ground
D7	GND	Ground
D8	V_{CC2}	Positive Protection Switch Voltage Supply (+5V, typ). Bypass with 100nF or greater ceramic capacitance to GND.

Bump Description (continued)

PIN	NAME	FUNCTION
E1	OUT1	LNA Output. Connect OUT1 to the cable.
E2	OUT2	LNA Output. Connect OUT2 to the cable.
E3	GND	Ground
E4	GND	Ground
E5	GND	Ground
E6	GND	Ground
E7	OUT9	LNA Output. Connect OUT9 to the cable.
E8	OUT10	LNA Output. Connect OUT10 to the cable.
F1	OUT3	LNA Output. Connect OUT3 to the cable.
F2	OUT4	LNA Output. Connect OUT4 to the cable.
F3	GND	Ground
F4	GND	Ground
F5	$\overline{LE}$	SPI Digital Control Pin. If the SPI is not used, connect this pin to V_{DD}.
F6	GND	Ground
F7	OUT11	LNA Output. Connect OUT11 to the cable.
F8	OUT12	LNA Output. Connect OUT12 to the cable.
G1	OUT5	LNA Output. Connect OUT5 to the cable.
G2	OUT6	LNA Output. Connect OUT6 to the cable.
G3	CLK	SPI Digital Control Pin. If the SPI is not used, connect this pin to GND.
G4	DIN	SPI Digital Control Pin. If the SPI is not used, connect this pin to GND.
G5	GND	Ground
G6	DOUT	SPI Digital Control Pin. If the SPI is not used, leave this pin unconnected.
G7	OUT13	LNA Output. Connect OUT13 to the cable.
G8	OUT14	LNA Output. Connect OUT14 to the cable.
H1	OUT7	LNA Output. Connect OUT7 to the cable.
H2	OUT8	LNA Output. Connect OUT8 to the cable.
H3	V_{DD}	Positive Voltage Supply for CMOS Input Interface (+5V, typ). Bypass with 100nF or greater ceramic capacitance to GND.
H4	V_{EE1}	Negative LNA Voltage Supply (-1.4V, typ). Bypass with 100nF or greater ceramic capacitance to GND.
H5	V_{CC1}	Positive LNA Voltage Supply (+1.4V, typ). Bypass with 100nF or greater ceramic capacitance to GND.
H6	V_{CC2}	Positive Protection switches Voltage Supply (+5V, typ). Bypass with 100nF ceramic capacitance to GND.
H7	OUT15	LNA Output. Connect OUT15 to the cable.
H8	OUT16	LNA Output. Connect OUT16 to the cable.

Functional Diagram



Detailed Description

The MAX14822 is a 16-channel high-voltage-protected, low-noise, operational amplifier. This device is a fully integrated, very compact solution for in-probe amplification of echo signals coming from transducers in an ultrasound system. The use of in-probe buffering improves signal-to-noise ratio (SNR) for transducers featuring high-output impedance. This results in greater penetration depth and sensitivity. The device can be adopted in ultrasound probes without any changes in the system (scanner machine). Typical applications include high-impedance piezoelectric transducers (PZT), capacitive micromachined ultrasonic transducers (CMUT), in-probe buffering, and amplification.

The device features 16 operational amplifiers configured in a non-inverting configuration. The small-signal output impedance of these operational amplifiers is 20Ω (typ) for matching the typical cable impedance. The low-noise amplifier features > 45MHz (typ) -3dB bandwidth and very low voltage and current noise, ensuring excellent noise figure. The output signals of these operational amplifiers are limited with diodes in an antiparallel configuration to GND.

The device provides high-voltage (HV) protection for the inputs and outputs of the operational amplifiers. An integrated automatic HV switch protects the input and output of the amplifier from HV bursts. Transmitted bursts reach the transducer through a pair of integrated antiparallel diodes. Each channel is able to sustain transmission bursts up to ±105V. The HV protection is automatically activated as soon as the TX voltage is greater than -1.39V (typ) or less than +1.25V (typ); no dedicated TX/RX signal is normally required. The device also features the ability to control the status of the protection switches through the use of a digital control input (R/T) to minimize transmitted burst attach distortion and transmission losses. Various control strategies are supported (refer to the Protection and Operating Modes section).

Power dissipation of the device is extremely low in order to match the severe power-consumption requirement of ultrasound probe electronics. The device features a dedicated digital input that enables selection of the bias current between two values. A higher bias current corresponds to a lower equivalent voltage noise at the expense of greater power consumption.

The device also features two control inputs (G0 and G1) that allow the voltage gain to be programmed to four fixed values in order to tailor the part for transducers featuring different sensitivity levels.

Protection and Operating Modes

The MAX14822 digital CMOS inputs (M0 and M1), or the SPI register bits (D(1) and D(2)), can be used to set the desired operating mode. The content of the LSB in the SPI register (D(0)) determines whether the operating mode is software or hardware-controlled. Refer to Table 1 and Table 5 for configuration details of the five operating modes.

Shutdown Mode (M0 = M1 = 0, R/T = 1)

Shutdown mode corresponds to the lowest power dissipation mode. In this mode, all the LNAs are shut down. HV protection switches are on and automatically protected.

Transmission Mode (M0 = M1 = 0, R/T = 0)

When the device is transmission mode, all the LNAs are shut down and all protection switches are open. In this mode, only transmission is supported. We recommend entering in this modality for transmit channels in Continuous Wave Doppler (CWD) mode.

Fully Automatic Protection Mode (M0 = 1, M1 = 0)

In fully automatic protection mode, the device input and output protection switches do not require a dedicated control signal. The protection switches are controlled by means of window comparators that sense the voltage on pin OUT_ and activate/deactivate the switches of the corresponding channels accordingly. In this operating mode, the R/T control signal is ignored.

Although the active protection switches are extremely fast, the non-zero turn-off time could cause attach distortion of the transmit burst. The extent of such a distortion depends on the equivalent output impedance of the transmitter and the amplitude and frequency of the transmit burst. Moreover, transmit power dissipation and insertion losses during transmission could be slightly affected. In case these issues limit the performance in fully automatic mode, the semiautomatic protection, or the externally controlled protection, method should be used.

Semiautomatic Protection Mode (M0 = 1, M1 = 1)

In semiautomatic mode, the MAX14822 input and output protection switches can be controlled such that a low pulse on the R/T digital input sets all the protection switches off (open) in advance of the transmit burst. Then, by sensing the cable voltage, each channel can individually recognize that the transmit burst is over and will automatically go back to the receive configuration (switches on).

This protection strategy removes the limitations of the fully automatic protection approach (attach distortion and

TX insertion losses). The R/T is normally a global signal for all the channels in the probe head.

As shown in Figure 2 and Figure 3, a negative pulse at the R/T input sets the device in transmit mode. When in transmit mode, all the protection switches are open and each channel monitors the OUT_ (cable) pin to detect transmit activity. As soon as the transmit burst is detected ($|V_{OUT}| > V_{TH}$) and then subsides ($|V_{OUT}| < V_{TH}$), each channel independently returns to receive mode (switches closed) and is ready to listen for ultrasound echoes. In cases where the transmit aperture is narrower than the receive window, it is still possible to use the semiautomatic protection feature by preprogramming the SPI register D[3:18] (refer to Table 4).

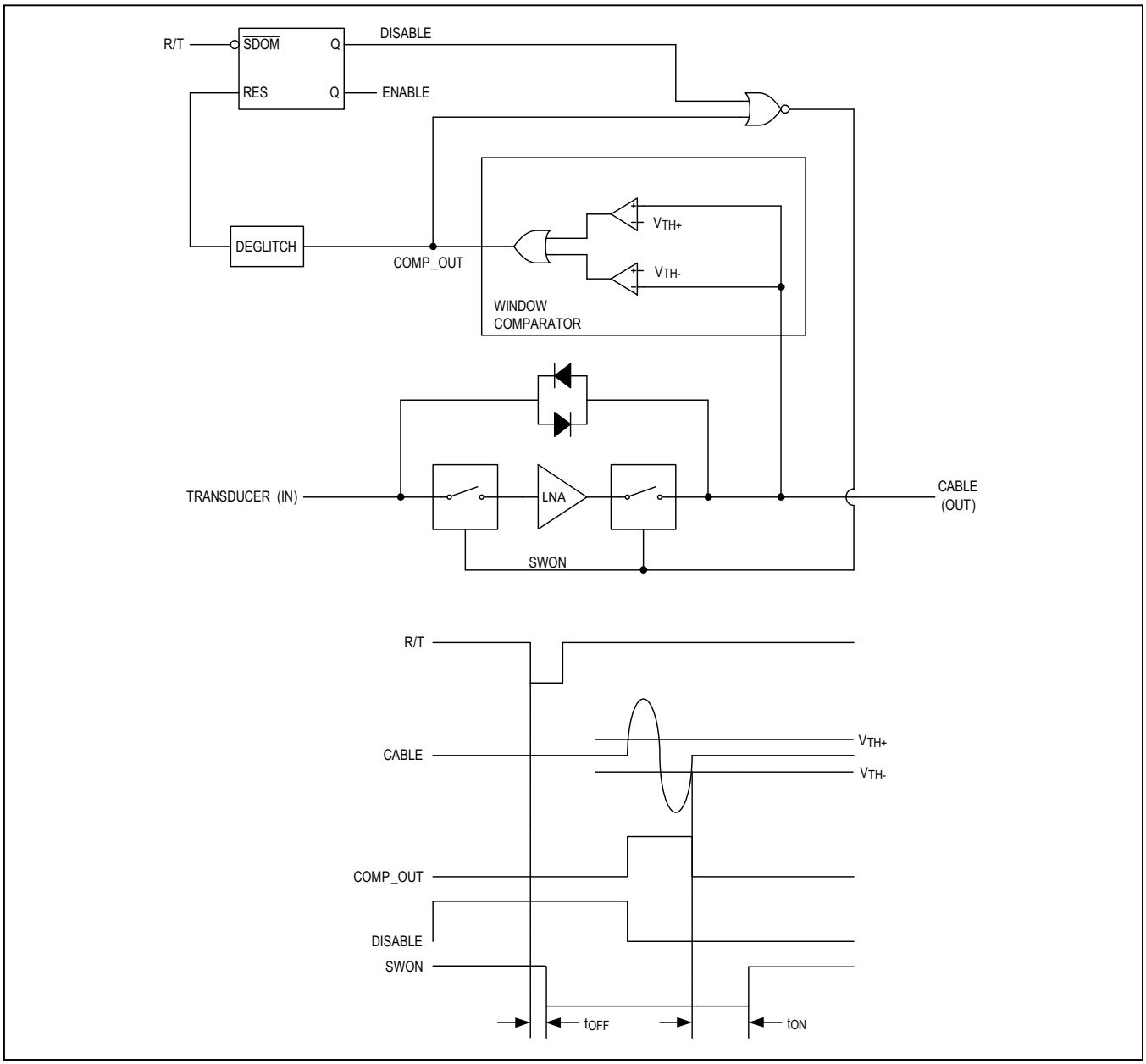


Figure 2. Semiautomatic Protection Functionality

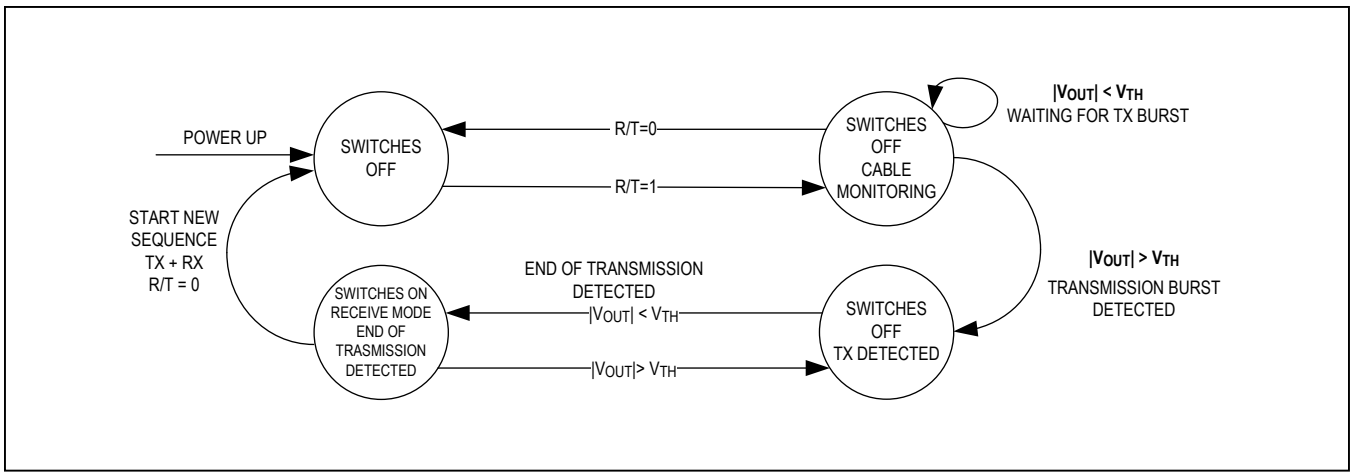


Figure 3. Semiautomatic Protection Diagram

Externally Controlled Protection Mode (M0 = 0, M1 = 1)

The device input and output protection switches are controlled by the status of the R/T digital input in this mode. When R/T is low, all channels are configured in transmit mode and protection switches are off (open). Channels are allowed to enter receive mode only if R/T is high and the condition $|V_{OUT}| < V_{TH}$ is satisfied.

Selectable Fixed Gain (G0, G1)

Either the digital CMOS inputs (G0 and G1) or the SPI register bits (D(19), D(20)) can be used to set the desired gain. Whether the operating mode is software/hardware-controlled depends on the content of the LSB in the SPI register (D(0))

Voltage gain can be programmed between four fixed values (0dB, 3.5dB, 6dB, 9.5dB). Whilte high voltage gain results in better system SNR, worse input linear dynamic range should be expected. The MAX14822 voltage gain value must be set taking into account the compatibility with the limited dynamic range of the system analog front-end.

Turn-On Time Increase

It is possible to program the turn-on time (T_{ON}) of the HV protections through bit D(22). When D(22) is set low (default), T_{ON} is set to minimum value. When bit D(22) is set high, T_{ON} is programmed to 1.45µs. Setting D(22) high ensures that the HV protection switches are kept off for 3 level-coded HV bursts (PWM).

SPI Programming

The device features a 50MHz SPI interface and can be programmed through an SPI interface. Serial data are clocked in on the rising-edge of the CLK. A full programming word consists of 39 bits. The MSB (D(38)) is entered first and the LSB D(0) is entered last.

Provided that D(0) = 1, gain, bias and operating mode settings can be programmed through SPI (see Table 4).

If D(0) = 0 (default), these settings are hardware-controlled by dedicated digital CMOS inputs.

Two subsets of the SPI data register (TXONLY, RXONLY) allow declaring each channel individually as a transmit channel only, a receive channel only, or a transmit/receive channel (default).

1) Transmit/receive mode (default). The channel is intended to be used both in transmit and receive. The automatic and semiautomatic protection, as well as the externally controlled protection scheme, can be used. To declare the channel a transmit/receive channel, the corresponding bits in the RXONLY D(3:18) and TXONLY D(23:38) subsets of the SPI register must be set low.
2) Receive-Only Mode. The channel is intended to be used in receive only. The semiautomatic and the externally controlled protection are disabled for that specific channel. Note that:
    a. the automatic protection is always active,
    b. transmit is still possible since the transmit path (anti-parallel diodes) is not open.

    To declare a receive-only channel, the corresponding bit in the RXONLY D(3:18) SPI register subset must be set high.
3) Transmit-Only Mode. The channel is intended to be used in transmit-only. The corresponding LNA is shut down. Protection switches are on and protected accordingly to the programmed protection scheme (refer to Table 5). Use this feature to save power whenever channels are unused or are used in transmission only. To declare the individual channel as transmit-only channel the corresponding bit in the TXONLY D(23:38) SPI register subset must be set high.

Refer to Table 4 for details.

Register Map and Logic Table

The operating mode, gain, and BIAS settings can be set either by hardware (HW) or software (SW) (SPI register), depending on the content of the LSB into the SPI register (D(0)). The D(0) default value is set at 0. As a consequence, at power-up, all the settings are controlled through hardware by the corresponding digital inputs (M0, M1, GAIN, BIAS). If the SPI is not used (or D(0) remains set at 0), the MAX14822 status is HW controlled. If the SPI is used and D0 is set at 1, the MAX14822 operating mode is software-controlled through SPI.

The naming used in the tables below refer to the internal control signals independent from the device being hardware or software-controlled.

Table 1. M0 and M1 Protection Mode Setting

M0	M1	OPERATING MODE
0	0	Shutdown mode (R/T=1) or transmission mode (R/T=0). See Table 5.
0	1	Normal operation. Externally controlled protection mode
1	0	Normal operation. Fully automatic protection mode
1	1	Normal operation. Semiautomatic protection mode

Table 2. G0 and G1 Gain Control Settings

G0	G1	GAIN (dB)
0	0	0dB
0	1	3.5dB
1	0	6dB
1	1	9.5dB

Table 3. BIAS Control Settings

BIAS	POWER DISSIPATION (mW/channel)	en (nV/√Hz)	in (pA/√Hz)
0	5.9	1.54	1.67
1	8.6	1.28	1.80

Table 4. SPI Register Map

D[0:38]	BIT NAME	DESCRIPTION
0	HW/SW	D[0] = 0 device setting is HW controlled (CMOS input M0, M1, G0, G1, BIAS pins). D[0] = 1 device setting is SW controlled through SPI (bits D(1), D(2), D(19), D(20), D(21)).
1	M0	Set operating mode (refer to Table 1). Active if D(0) = 1 only.
2	M1	Set operating mode (refer to Table 1). Active if D(0) = 1 only.
D[3:18]	RXONLY	When set high, the R/T feature is disabled for that particular channel (e.g., D(3) → CH(0), D(4) → CH(1) etc.), which is considered receive-only mode. This applies to both the semiautomatic and externally controlled mode. This is required whenever the part is programmed in semiautomatic mode (refer to Table 1) and a subset of channels is supposed to receive only (RXONLY). When set low (default), the R/T feature is enabled according to the programmed operating mode (see Table 5).
19	G0	Set device voltage gain (see Table 2). Active if D(0) = 1 only.
20	G1	Set device voltage gain (see Table2). Active if D(0) = 1 only.
21	BIAS	Set bias operating mode (see Table 3). Active if D(0) = 1 only.
22	T_{ON}	Set device T_{ON}. When D(22) = 1, T_{ON} is set at 1.45µs.
D[23:38]	TXONLY	When set high, the corresponding receive channel (e.g., D(23) → CH(0), D(24) → CH(1) etc.) is disabled. The LNA is shut down. Protection switches are on and protected according to the programmed protection scheme (see Table 1 and Table 5). Use this feature to save power whenever channels are unused, or are used in transmit-only mode. When set low (default) the corresponding channel (e.g., D(23) → CH(0), D(24) → CH(1) etc.) is enabled for both receive and transmit. LNA are on and protection switches operating according to Table 1 and Table 5.

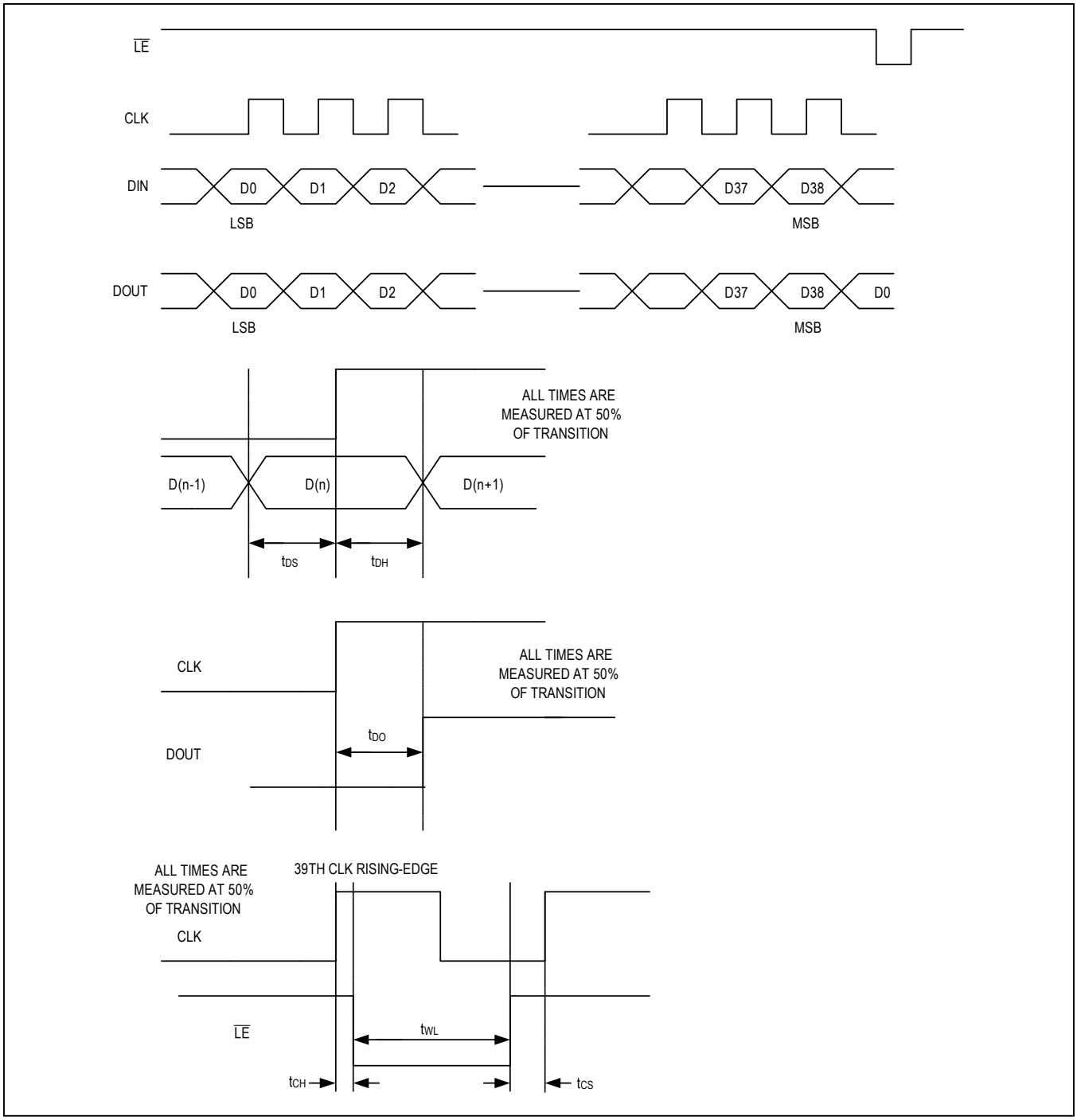


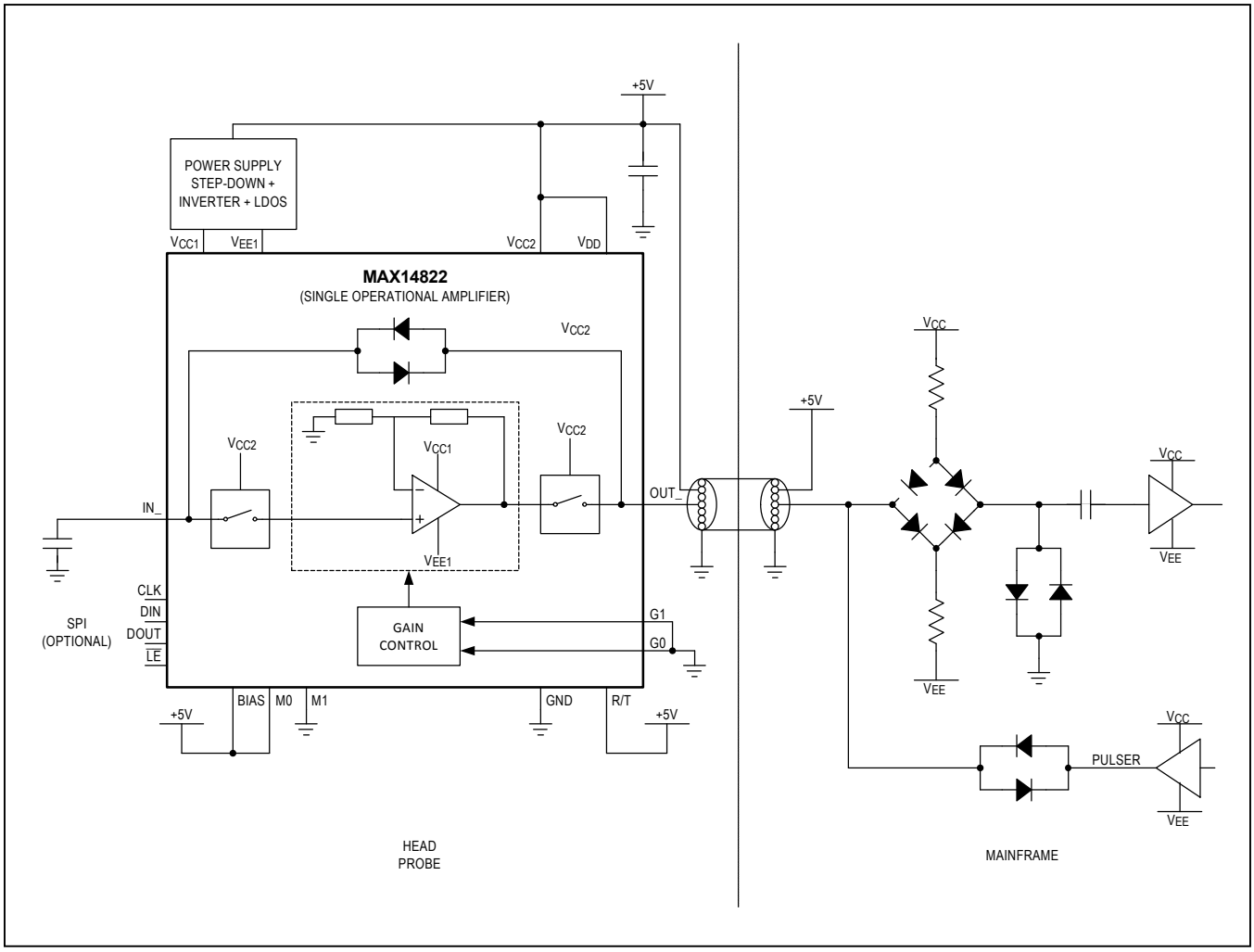
Figure 4. SPI Timing Diagram

Table 5. Protection and Operating Mode

	M0	M1	R/T	CABLE VOLTAGE	SWITCHES	AMPLIFIER
SHUTDOWN	0	0	1	$\|V_{OUT}\| < V_{TH}$	ON	Shutdown
	0	0	1	$\|V_{OUT}\| > V_{TH}$	OFF	Shutdown
TRANSMISSION MODE	0	0	0	X	OFF	Shutdown
AUTOMATIC PROTECTION MODE	1	0	X	$\|V_{OUT}\| < V_{TH}$	ON	Active
	1	0	X	$\|V_{OUT}\| > V_{TH}$	OFF	Active
SEMIAUTOMATIC PROTECTION MODE (NOTE 3)	1	1	0	X	OFF	Active
	1	1	1	$\|V_{OUT}\| > V_{TH}$	OFF	Active
	1	1	1	$\|V_{OUT}\| < V_{TH}$ before a transmit burst is detected.	OFF	Active
	1	1	1	$\|V_{OUT}\| < V_{TH}$ after a transmit burst is detected	ON	Active
EXTERNALLY CONTROLLED PROTECTION MODE	0	1	0	X	OFF	Active
	0	1	1	$\|V_{OUT}\| > V_{TH}$	OFF	Active
	0	1	1	$\|V_{OUT}\| < V_{TH}$	ON	Active

Note 3: Switches are off (open) when entering semiautomatic mode from any other modes, or after power-up.

Typical Application Circuit



Application Information

The device does not require special power-up/power-down sequencing for the voltage supplies V_{CC1}, V_{EE1}, V_{CC2}, and V_{DD}. The user must ensure that no transmit activity is present on OUT_ pins during power-up and power-down.

Low-dropout (LDOs) linear regulators are recommended for the LNA supplies. LDOs must feature good noise and PSRR performances. LDOs can be placed in the connector or inside the probe head. The in-probe approach is preferred because of the benefits of local regulation, provided that the total power consumption inside the probe head remains acceptable.

Use HV PCB electrical rules when routing the inputs and outputs of the MAX14822.

The following PCB layout rules are recommended for optimal operation with the MAX14822:

1) Minimize capacitive coupling between the device's IN and OUT traces on the PCB. Parasitic capacitances between these two pins can affect the device stability.
2) Keep input traces as short as possible. Specifically, parasitic inductance of these traces must be minimized.
3) When possible, avoid using multiple throughputs for the input traces. Vias result in additional series inductances.

Protection Strategy

Fully automatic protection mode does not require an external control signal and works in most applications. However, the nonidealities of the protection switches could result in transmit insertion losses and distortions, especially for extremely low amplitude transmit bursts.

To improve the transmit insertion loss and the transmit pulse distortion, the semiautomatic (or the externally controlled) protection mode should be considered.

For CWD operation, all the transmit channels must be set in Transmit mode" so that power consumption and transmit efficiency is optimized.

Compatibility

The device has been designed to be fully compatible with existing ultrasound scanners. Depending on the probe sensitivity, high gain pre-amplification inside the probe head could overdrive the input stage of the analog front-end (AFE) at system-side and cause saturation and image artifacts. In these cases, a lower gain setting for the device (0dB or 3.5dB) is recommended.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14822CXB+	0°C to +70°C	64 CTBGA

Chip Information

PROCESS: BCDMOS/BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
64 CTBGA	X6477MK+2	21-0461	90-0384

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/15	Initial release	—

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