19-2332; Rev 2; 9/08

3V/5V, 12-Bit, Serial Voltage-Output Dual DACs with Internal Reference

General Description

The MAX5230/MAX5231 low-power, dual 12-bit voltage-output digital-to-analog converters (DACs) feature an internal 10ppm/°C precision bandgap voltage reference and precision output amplifiers. The MAX5231 operates on a single 5V supply with an internal 2.5V reference and features a 4.095V full-scale output range. The MAX5230 operates on a single 3V supply with an internal 1.25V reference and features a 2.0475V full-scale output range. The MAX5231 consumes only 470µA while the MAX5230 consumes only 420µA of supply current. Both devices feature low-power (2µA) software- and hardware-enabled shutdown modes.

The MAX5230/MAX5231 feature a 13.5MHz SPI™-, QSPI™-, and MICROWIRE™-compatible 3-wire serial interface. An additional data output (DOUT) allows for daisy-chaining and read back. Each DAC has a double-buffered digital input. The MAX5230/MAX5231 feature two software-selectable shutdown output impedances: 1kΩ or 200kΩ. A power-up reset feature sets DAC outputs at ground or at the midscale DAC code.

The MAX5230/MAX5231 are specified over the extended temperature range (-40°C to +85°C) and are available in 16-pin QSOP packages.

Applications

Industrial Process Controls

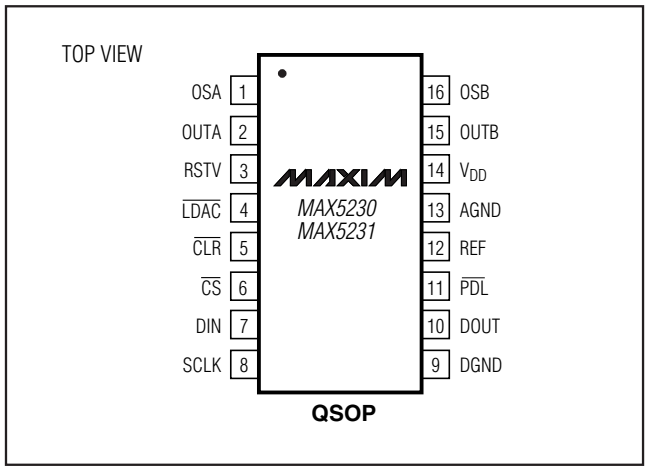
Automatic Test Equipment

Digital Offset and Gain Adjustment

Motion Control

µP-Controlled Systems

Pin Configuration



Features

- **Internal 10ppm/°C Precision Bandgap Reference**
  2.465V (MAX5231)
  1.234V (MAX5230)
- **Single-Supply Operation**
  5V (MAX5231)
  3V (MAX5230)
- **Low Supply Current**
  470µA (MAX5231)
  420µA (MAX5230)
- **13.5MHz SPI/QSPI/MICROWIRE-Compatible, 3-Wire Serial Interface**
- **Pin-Programmable Power-Up Reset State to Zero or Midscale Output Voltage**
- **Programmable Shutdown Modes with 1kΩ or 200kΩ Internal Output Loads**
- **Recalls Output State Prior to Shutdown or Reset**
- **Buffered Output Drives 5kΩ || 100pF Loads**
- **Space-Saving 16-Pin QSOP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	INL (LSB)
MAX5230AEEE+	-40°C to +85°C	16 QSOP	±0.5
MAX5230BEEE+	-40°C to +85°C	16 QSOP	±1
MAX5231AEEE+	-40°C to +85°C	16 QSOP	±0.5
MAX5231BEEE+	-40°C to +85°C	16 QSOP	±1

+Denotes a lead-free/RoHS-compliant package.

Functional Diagram appears at end of data sheet.

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MICROWIRE is a trademark of National Semiconductor, Corp.

3V/5V, 12-Bit, Serial Voltage-Output Dual DACs with Internal Reference

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND, DGND .....-0.3V to +6V
AGND to DGND.....-0.3V to +0.3V
Digital Inputs to DGND.....-0.3V to +6V
Digital Output (DOUT) to DGND.....-0.3V to V_{DD} + 0.3V
OUT_ to AGND .....-0.3V to V_{DD} + 0.3V
OS_ to AGND.....-4V to V_{DD} + 0.3V
Maximum Current into Any Pin.....50mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.3mW/°C above +70°C).....667mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX5231

(V_{DD} = +4.5V to +5.5V, OS_ = AGND = DGND = 0, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution	N		12			Bits
Integral Nonlinearity (Note 1)	INL	MAX5231A			±0.5	LSB
		MAX5231B			±1	
Differential Nonlinearity	DNL				±1	LSB
Offset Error (Note 2)	V_{OS}				±3	mV
Offset-Temperature Coefficient (Note 3)	TCV_{OS}			8		µV/°C
Full-Scale Voltage	V_{FS}	Code = FFF hex, T_A = +25°C	4.070	4.095	4.120	V
Full-Scale Temperature Coefficient	TCV_{FS}	MAX5231 (Notes 3 and 6)		10	55	ppm/°C
Power-Supply Rejection	PSR	4.5V ≤ V_{DD} ≤ 5.5V		175	500	µV
DC Crosstalk (Note 4)					100	µV
REFERENCE						
Output Voltage	V_{REF}			2.465		V
Output-Voltage Temperature Coefficient	TCV_{REF}	MAX5231 (Note 3)		10		ppm/°C
Reference External Load Regulation	V_{OUT}/I_{OUT}	0 ≤ I_{OUT} ≤ 100µA (sourcing)		0.1	2	µV/µA
Reference Short-Circuit Current				4		mA
DIGITAL INPUTS						
Input High Voltage	V_{IH}		0.7 x V_{DD}			V
Input Low Voltage	V_{IL}				0.3 x V_{DD}	V
Input Hysteresis	V_{HYS}			200		mV
Input Leakage Current	I_{IN}	Digital inputs = 0 or V_{DD}			±1	µA
Input Capacitance	C_{IN}			8		pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = 2mA	4.25			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA			0.2	V
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate	SR			0.6		V/µs

ELECTRICAL CHARACTERISTICS—MAX5231 (continued)

(V_{DD} = +4.5V to +5.5V, OS_ = AGND = DGND = 0, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage-Output Settling Time		To ±0.5LSB, V_{STEP} = ±4V (V_{DD} - 0.25V) ≥ V_{OUT} ≥ 0.25V		10		µs
Output-Voltage Swing (Note 5)				0 to V_{DD}		V
OS_ Input Resistance	R_{OS}		83	121		kΩ
Time Required for Output to Settle After Turning on V_{DD} (Note 6)				95	400	µs
Time Required for Output to Settle After Exiting Full Power-Down (Note 6)				95	400	µs
Time Required for Output to Settle After Exiting DAC Power-Down (Note 6)				12	160	µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, f_{SCLK} = 100kHz, V_{SCLK} = $5V_{P-P}$		5		nV-s
Major-Carry Glitch Energy				90		nV-s
POWER SUPPLIES						
Power-Supply Voltage	V_{DD}		4.5		5.5	V
Power-Supply Current (Note 7)	I_{DD}			470	525	µA
Power-Supply Current in Power-Down and Shutdown Modes (Note 7)		Full power-down mode		1.4	5	µA
		One DAC shutdown mode		350	390	
		Both DACs shutdown mode		235	260	

ELECTRICAL CHARACTERISTICS—MAX5230

(V_{DD} = +2.7V to +3.6V, OS_ = AGND = DGND = 0, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution	N		12			Bits
Integral Nonlinearity (Note 1)	INL	MAX5230A			±0.5	LSB
		MAX5230B			±1	
Differential Nonlinearity	DNL				±1	LSB
Offset Error (Note 2)	V_{OS}				±3	mV
Offset-Temperature Coefficient (Note 3)	TCV_{OS}			8		µV/°C
Full-Scale Voltage	V_{FS}	Code = FFF hex, T_A = +25°C	2.0350	2.0475	2.0600	V
Full-Scale Temperature Coefficient	TCV_{FS}	MAX5230 (Notes 3 and 6)		10	55	ppm/°C
Power-Supply Rejection	PSR	2.7V ≤ V_{DD} ≤ 3.6V		175	500	µV
DC Crosstalk (Note 4)					100	µV
REFERENCE						
Output Voltage	V_{REF}			1.234		V
Output-Voltage Temperature Coefficient	TCV_{REF}	MAX5230 (Note 3)		10		ppm/°C

3V/5V, 12-Bit, Serial Voltage-Output Dual DACs with Internal Reference

ELECTRICAL CHARACTERISTICS—MAX5230 (continued)

(V_{DD} = +2.7V to +3.6V, OS_ = AGND = DGND = 0, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reference External Load Regulation	V_{OUT}/I_{OUT}	0 ≤ I_{OUT} ≤ 100µA (sourcing)		0.1	2	µV/µA
Reference Short-Circuit Current				4		mA
DIGITAL INPUTS						
Input High Voltage	V_{IH}		0.7 x V_{DD}			V
Input Low Voltage	V_{IL}				0.3 x V_{DD}	V
Input Hysteresis	V_{HYS}			200		mV
Input Leakage Current	I_{IN}	Digital inputs = 0 or V_{DD}			±1	µA
Input Capacitance	C_{IN}			8		pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = 2mA	2.3			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA			0.25	V
DYNAMIC PERFORMANCE						
Voltage-Output Slew Rate	SR			0.6		V/µs
Voltage-Output Settling Time		To ±0.5 LSB, V_{STEP} = ±2V (V_{DD} - 0.25V) ≥ V_{OUT} ≥ 0.25V		10		µs
Output-Voltage Swing (Note 5)				0 to V_{DD}		V
OS_ Input Resistance	R_{OS}		83	121		kΩ
Time Required for Output to Settle After Turning on V_{DD} (Note 6)				95	400	µs
Time Required for Output to Settle After Exiting Full Power-Down (Note 6)				95	400	µs
Time Required for Output to Settle After Exiting DAC Power-Down (Note 6)				12	160	µs
Digital Feedthrough		$\overline{CS}$ =V_{DD}, f_{SCLK} = 100kHz, V_{SCLK} = $3V_{P-P}$		5		nV-s
Major-Carry Glitch Energy				90		nV-s

ELECTRICAL CHARACTERISTICS—MAX5230 (continued)

(V_{DD} = +2.7V to +3.6V, OS_ = AGND = DGND = 0, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Power-Supply Voltage	V_{DD}		2.7		3.6	V
Power-Supply Current (Note 7)	I_{DD}			420	475	µA
Power-Supply Current in Power-Down and Shutdown Modes (Note 7)		Full power-down mode		0.9	5	µA
		One DAC shutdown mode		320	360	
		Both DACs shutdown mode		220	245	

Note 1: Accuracy is guaranteed as shown in the following table:

V_{DD} (V)	ACCURACY GUARANTEED	
	FROM CODE	TO CODE
3	20	4095
5	10	4095

Note 2: Offset is measured at the code closest to 10mV.

Note 3: Temperature coefficient is determined by the box method in which the maximum ΔV_{OUT} over the temperature range is divided by ΔT.

Note 4: DC crosstalk is measured as follows: set DAC A to midscale, and DAC B to zero, and measure DAC A output; then change DAC B to full scale, and measure ΔV_{OUT} for DAC A. Repeat the same measurement with DAC A and DAC B interchanged. DC crosstalk is the maximum ΔV_{OUT} measured.

Note 5: Accuracy is better than 1LSB for $V_{OUT\_}$ = 10mV to V_{DD} - 180mV.

Note 6: Guaranteed by design, not production tested.

Note 7: R_{LOAD} = ∞ and digital inputs are at either V_{DD} or DGND.

TIMING CHARACTERISTICS—MAX5231

(V_{DD} = +4.5V to +5.5V, AGND = DGND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Figures 1 and 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Period	t_{CP}		74			ns
SCLK Pulse Width High	t_{CH}		30			ns
SCLK Pulse Width Low	t_{CL}		30			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		30			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		30			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to DOUT Valid Propagation Delay Time	t_{DO1}	C_{LOAD} = 200pF		45	100	ns
		C_{LOAD} = 100pF		30		
SCLK Fall to DOUT Valid Propagation Delay Time	t_{DO2}	C_{LOAD} = 200pF		45	100	ns
		C_{LOAD} = 100pF		30		
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		10			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		30			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		75			ns
$\overline{LDAC}$ Pulse Width Low	t_{LDL}		30			ns
$\overline{CS}$ Rise to $\overline{LDAC}$ Rise Hold Time	t_{CSLD}	(Note 8)	40			ns

3V/5V, 12-Bit, Serial Voltage-Output Dual DACs with Internal Reference

TIMING CHARACTERISTICS—MAX5230

(V_{DD} = +2.7V to +3.6V, AGND = DGND = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Figures 1 and 2)

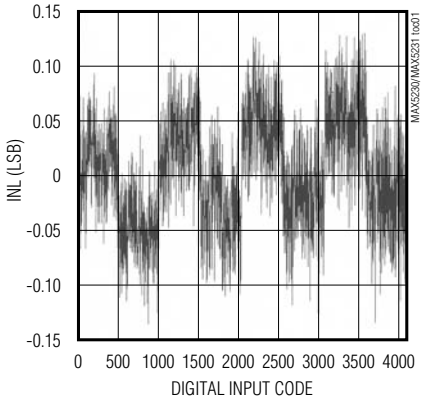
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Period	t_{CP}		74			ns
SCLK Pulse Width High	t_{CH}		30			ns
SCLK Pulse Width Low	t_{CL}		30			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		30			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		30			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to DOUT Valid Propagation Delay Time	t_{DO1}	C_{LOAD} = 200pF		60	200	ns
		C_{LOAD} = 100pF		45		
SCLK Fall to DOUT Valid Propagation Delay Time	t_{DO2}	C_{LOAD} = 200pF		60	200	ns
		C_{LOAD} = 100pF		45		
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		10			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		30			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		75			ns
$\overline{LDAC}$ Pulse Width Low	t_{LDL}		30			ns
$\overline{CS}$ Rise to $\overline{LDAC}$ Rise Hold Time	t_{CSLD}	(Note 8)	75			ns

Note 8: This timing requirement applies only to $\overline{CS}$ rising edges, which execute commands modifying the DAC input register contents.

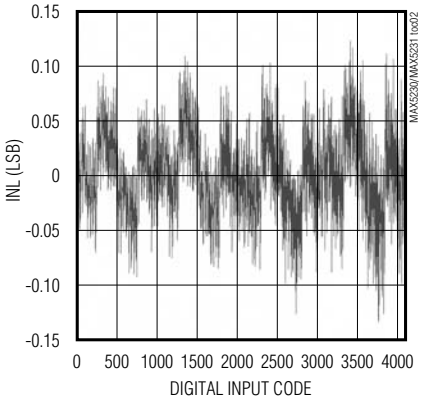
Typical Operating Characteristics

(V_{DD} = +3V (MAX5230), V_{DD} = +5V (MAX5231), R_L = 5kΩ, C_L = 100pF, OS_ = AGND, both DACs enabled with full-scale output code, T_A = +25°C, unless otherwise noted.)

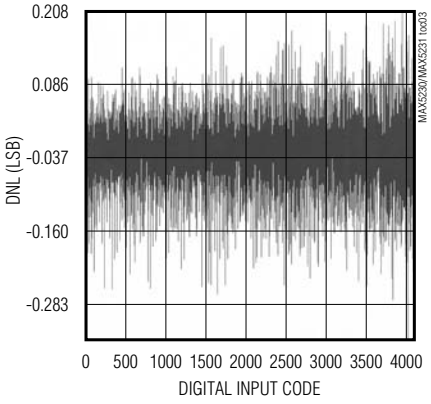
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE (MAX5230)



INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE (MAX5231)



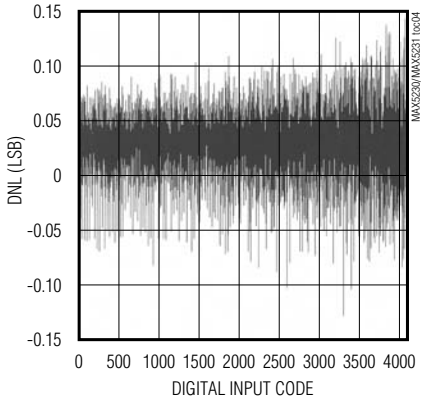
DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE (MAX5230)



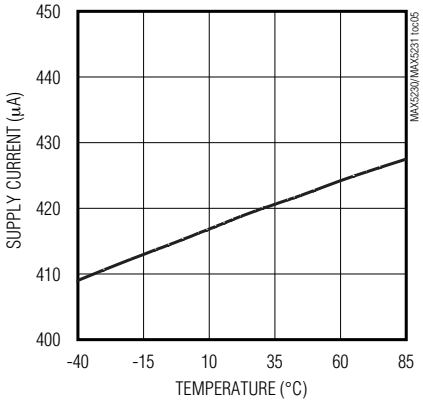
Typical Operating Characteristics (continued)

(V_{DD} = +3V (MAX5230), V_{DD} = +5V (MAX5231), R_L = 5kΩ, C_L = 100pF, OS_ = AGND, both DACs enabled with full-scale output code, T_A = +25°C, unless otherwise noted.)

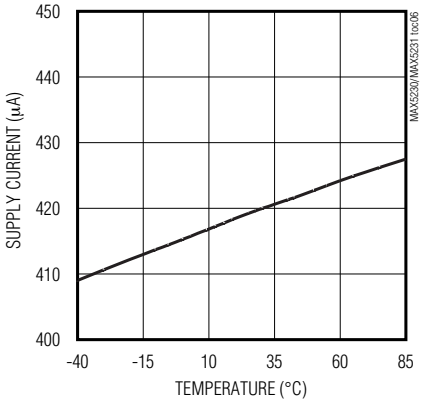
DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE (MAX5231)



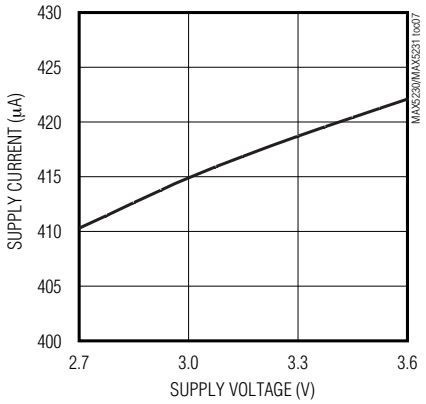
SUPPLY CURRENT vs. TEMPERATURE (MAX5230)



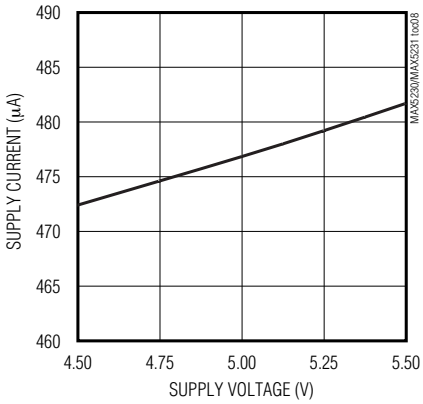
SUPPLY CURRENT vs. TEMPERATURE (MAX5231)



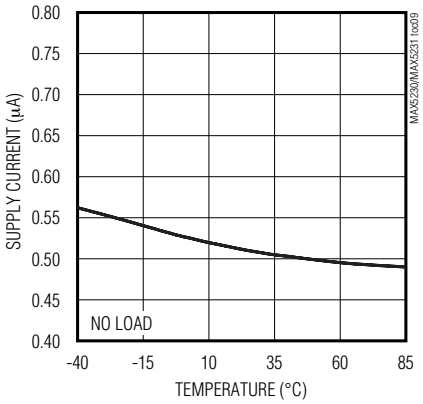
SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX5230)



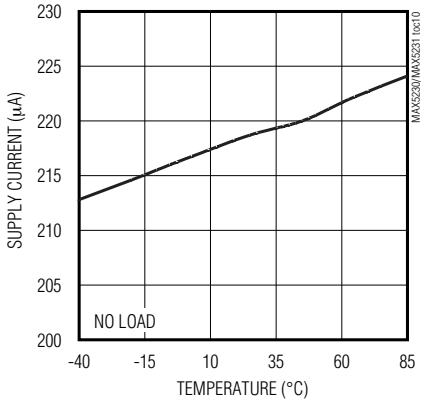
SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX5231)



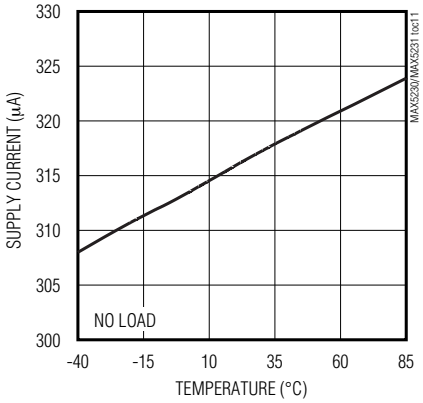
FULL POWER-DOWN SUPPLY CURRENT vs. TEMPERATURE (MAX5230)



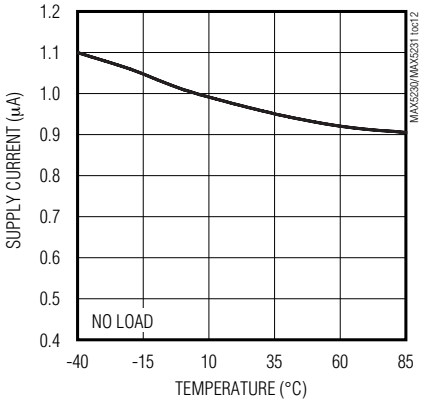
TWO-DACs SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE (MAX5230)



ONE-DAC SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE (MAX5230)



FULL POWER-DOWN SUPPLY CURRENT vs. TEMPERATURE (MAX5231)

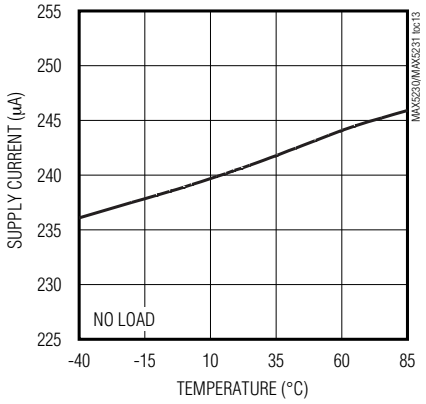


3V/5V, 12-Bit, Serial Voltage-Output Dual DACs with Internal Reference

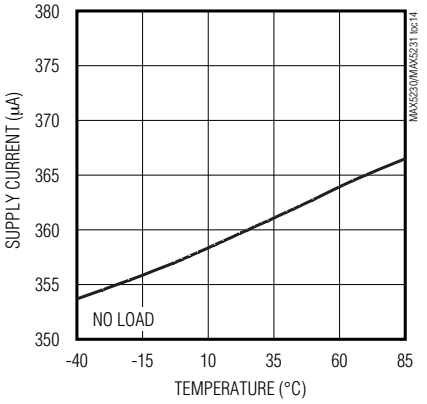
Typical Operating Characteristics (continued)

(V_{DD} = +3V (MAX5230), V_{DD} = +5V (MAX5231), R_L = 5kΩ, C_L = 100pF, OS_ = AGND, both DACs enabled with full-scale output code, T_A = +25°C, unless otherwise noted.)

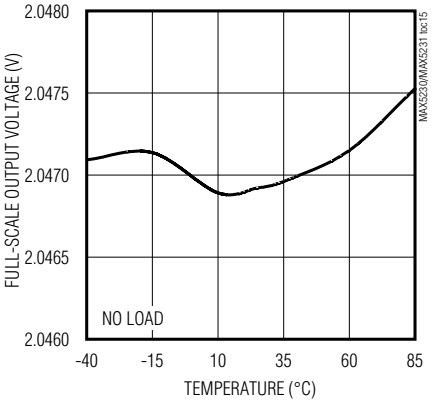
TWO-DACs SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE (MAX5231)



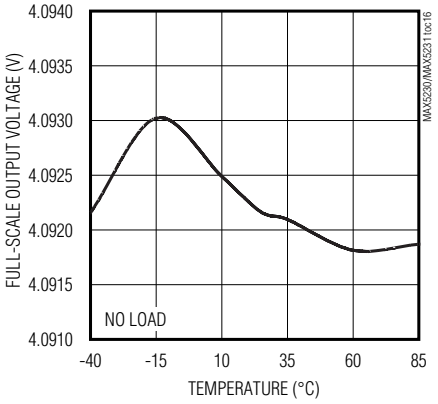
ONE-DAC SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE (MAX5231)



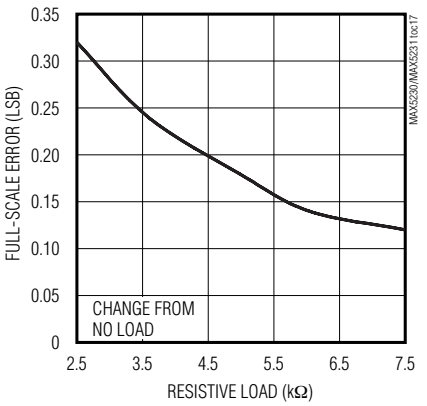
FULL-SCALE OUTPUT VOLTAGE vs. TEMPERATURE (MAX5230)



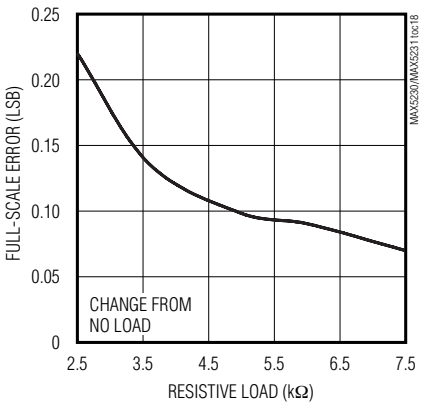
FULL-SCALE OUTPUT VOLTAGE vs. TEMPERATURE (MAX5231)



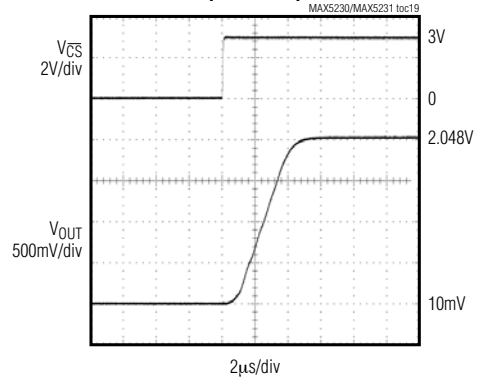
FULL-SCALE ERROR vs. RESISTIVE LOAD (MAX5230)



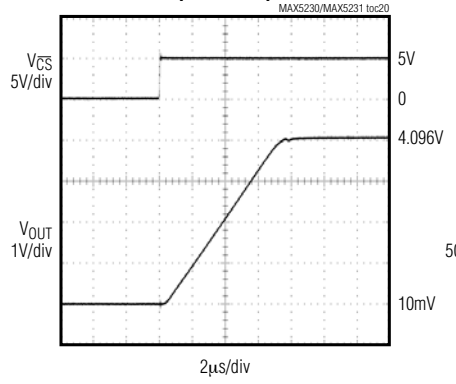
FULL-SCALE ERROR vs. RESISTIVE LOAD (MAX5231)



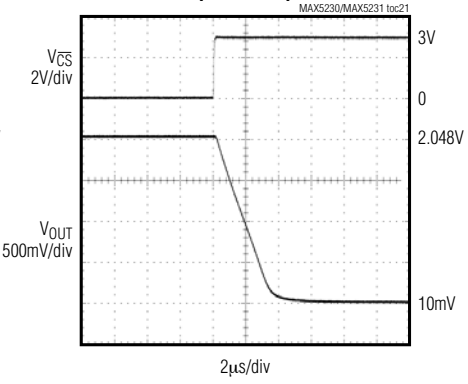
DYNAMIC RESPONSE RISE TIME (MAX5230)



DYNAMIC RESPONSE RISE TIME (MAX5231)



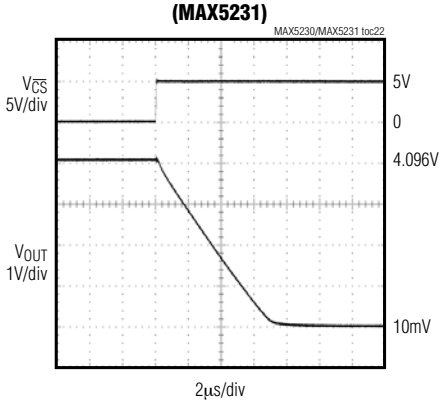
DYNAMIC RESPONSE FALL TIME (MAX5230)



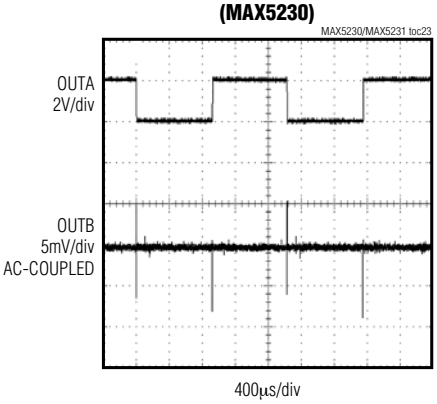
Typical Operating Characteristics (continued)

(V_{DD} = +3V (MAX5230), V_{DD} = +5V (MAX5231), R_L = 5kΩ, C_L = 100pF, OS_ = AGND, both DACs enabled with full-scale output code, T_A = +25°C, unless otherwise noted.)

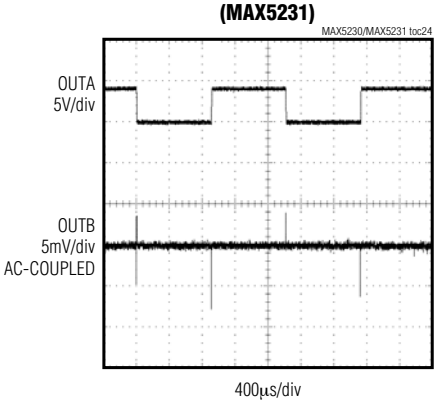
DYNAMIC RESPONSE FALL TIME (MAX5231)



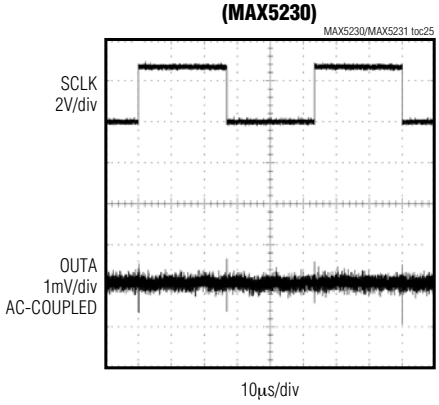
ANALOG CROSSTALK (MAX5230)



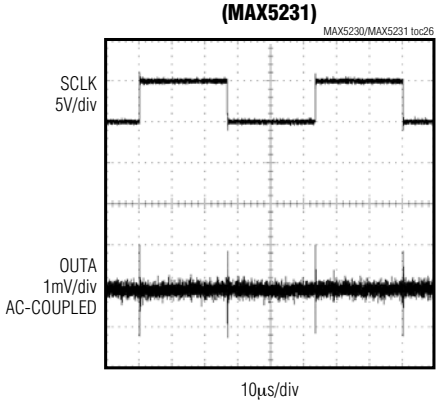
ANALOG CROSSTALK (MAX5231)



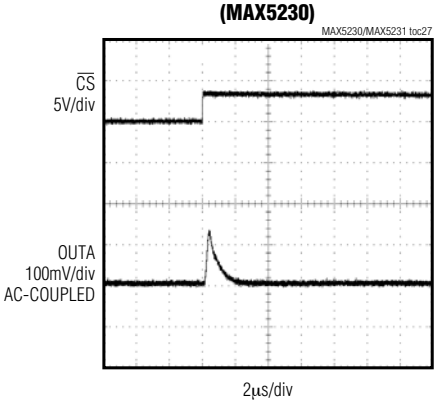
DIGITAL FEEDTHROUGH (MAX5230)



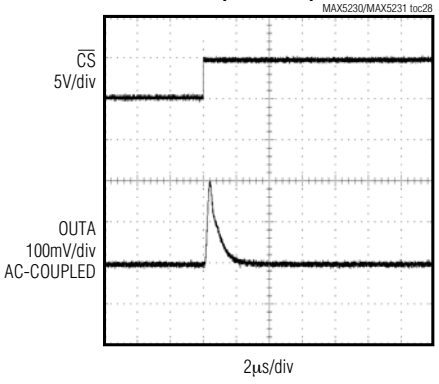
DIGITAL FEEDTHROUGH (MAX5231)



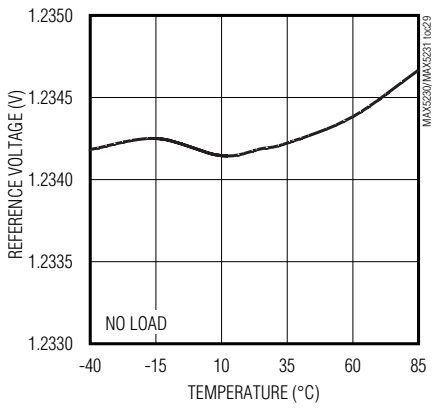
MAJOR-CARRY TRANSITION (MAX5230)



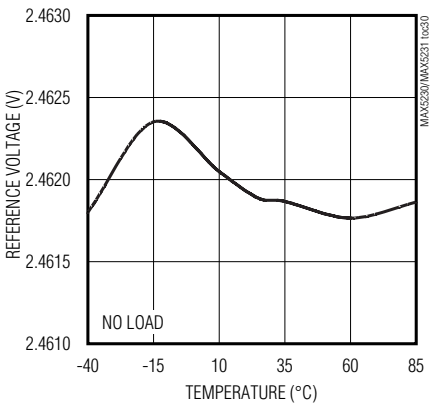
MAJOR-CARRY TRANSITION (MAX5231)



REFERENCE VOLTAGE vs. TEMPERATURE (MAX5230)



REFERENCE VOLTAGE vs. TEMPERATURE (MAX5231)



3V/5V, 12-Bit, Serial Voltage-Output Dual DACs with Internal Reference

Pin Description

PIN	NAME	FUNCTION
1	OSA	DAC A Offset Adjust
2	OUTA	DAC A Output
3	RSTV	Reset Value Input 1: Connect to V_{DD} to select midscale as the reset value. 0: Connect to DGND to select zero as the reset value.
4	$\overline{LDAC}$	Load DACs A and B
5	$\overline{CLR}$	Clear Input. Both DAC outputs go to zero or midscale. Clears both DAC internal registers (input register and DAC register) to its predetermined (RSTV) state.
6	$\overline{CS}$	Chip-Select Input
7	DIN	Serial Data Input. Data is clocked in on the rising edge of SCLK.
8	SCLK	Serial Clock Input
9	DGND	Digital Ground
10	DOUT	Serial Data Output
11	$\overline{PDL}$	Power-Down Lockout. Disables shutdown of both DACs when low.
12	REF	Reference Output. Reference provides a 2.465V (MAX5231) or 1.234V (MAX5230) nominal output.
13	AGND	Analog Ground
14	V_{DD}	Positive Power Supply. Bypass V_{DD} with a 0.1µF capacitor in parallel with a 4.7µF capacitor to AGND, and bypass V_{DD} with a 0.1µF capacitor to DGND.
15	OUTB	DAC B Output
16	OSB	DAC B Offset Adjust

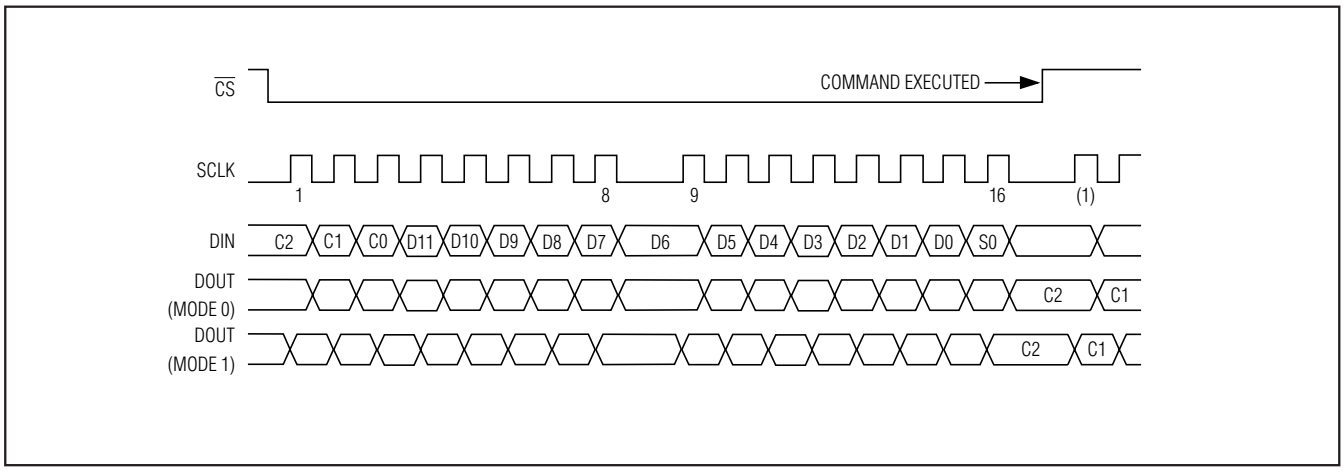


Figure 1. Serial Interface Timing

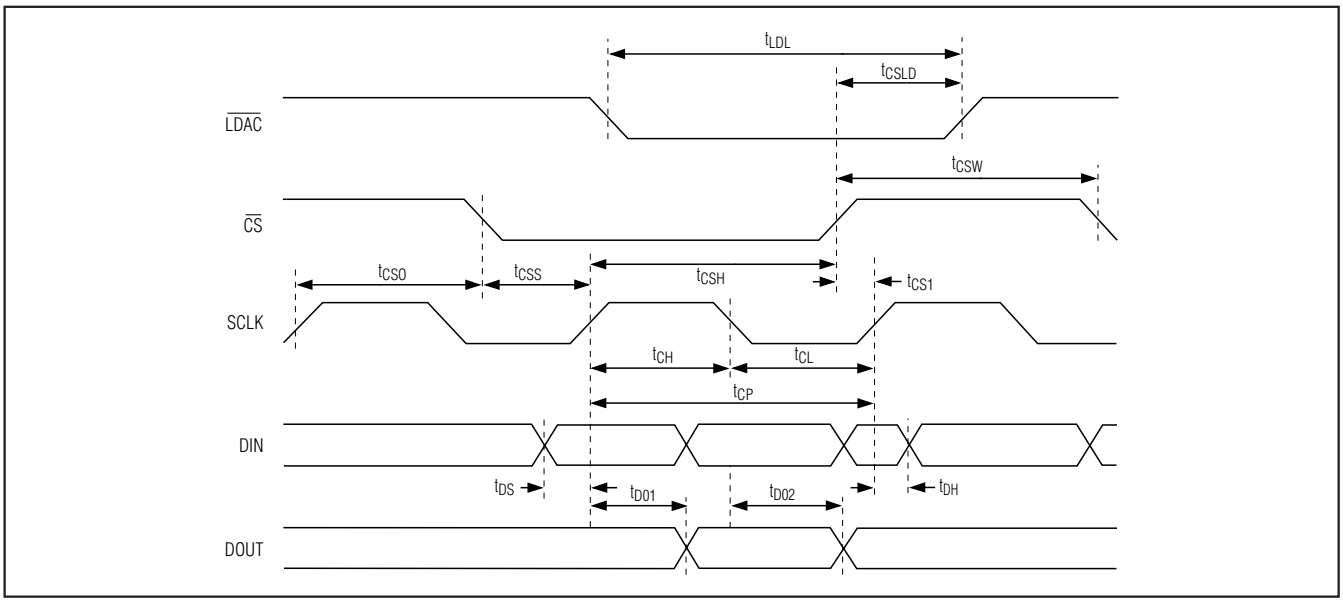


Figure 2. Detailed Serial Interface Timing

Detailed Description

The MAX5230/MAX5231 12-bit, voltage-output DACs are easily configured with a 3-wire SPI-, QSPI-, MICROWIRE-compatible serial interface. The devices include a 16-bit data-in/data-out shift register and have an input consisting of an input register and a DAC register. In addition, these devices employ precision trimmed internal resistors to produce a gain of 1.6384V/V, maximizing the output voltage swing, and a programmable-shutdown output impedance of 1kΩ or 200kΩ The full-scale output voltage is 4.095V for the MAX5231 and 2.0475V for the MAX5230. These devices produce a weighted output voltage proportional to the digital input code with an inverted rail-to-rail ladder network (Figure 3).

Internal Reference

The MAX5230/MAX5231 use an on-board precision bandgap reference to generate an output voltage of 1.234V (MAX5230) or 2.465V (MAX5231). With a low temperature coefficient of only 10ppm/°C, REF can source up to 100µA and is stable for capacitive loads less than 35pF.

Output Amplifiers

The output amplifiers have internal resistors that provide for a gain of 1.6384V/V when OS_ is connected to AGND. The output amplifiers have a typical slew rate of 0.6V/µs and settle to 1/2LSB within 10µs with a load of 5kΩ in parallel with 100pF. Use the serial interface to set the shutdown output impedance of the amplifiers to 1kΩ or 200kΩ.

OS_ can be used to produce an offset voltage at the output. For instance, to achieve a 1V offset, apply -1V to OS_ to produce an output range from 1V to (1V + V_{FS}/V_{REF}). Note that the DAC's output range is still limited by the maximum output voltage specification.

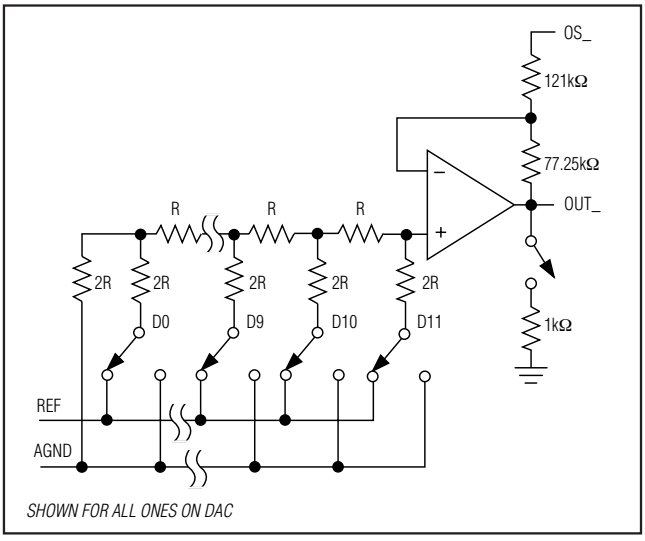


Figure 3. Simplified DAC Circuit Diagram

3V/5V, 12-Bit, Serial Voltage-Output Dual DACs with Internal Reference

Table 1. Serial Data Format

MSB <----------16-bits of serial data----------> LSB		
3 Control Bits	MSB .. 12 Data Bits ... LSB	Sub-Bit
C2…C0	D11 .....D0	S0

Serial Interface

The 3-wire serial interface (SPI, QSPI, MICROWIRE compatible) used in the MAX5230/MAX5231 allows for complete control of DAC operations (Figures 4 and 5). Figures 1 and 2 show the timing for the serial interface. The serial word consists of 3 control bits followed by 12 data bits (MSB first) and 1 sub-bit as described in Tables 1, 2, and 3. When the 3 control bits are all zero or all 1, D11–D8 are used as additional control bits, allowing for greater DAC functionality.

The digital inputs allow any of the following: loading the input register(s) without updating the DAC register(s), updating the DAC register(s) from the input register(s), or updating the input and DAC register(s) simultaneously. The control bits and D11–D8 allow the DACs to operate independently.

Send the 16-bit data as one 16-bit word (QSPI) or two 8-bit packets (SPI, MICROWIRE), with $\overline{CS}$ low during this period. The control bits and D11–D8 determine which registers update and the state of the registers when exiting shutdown. The 3-bit control and D11–D8 determine the following:

- Registers to be updated
- Selection of the power-down and shutdown modes

The general timing diagram of Figure 1 illustrates data acquisition. Driving $\overline{CS}$ low enables the device to receive data. Otherwise the interface control circuitry is disabled. With $\overline{CS}$ low, data at DIN is clocked into the register on the rising edge of SCLK. As $\overline{CS}$ goes high, data is latched into the input and/or DAC registers, depending on the control bits and D11–D8. The maximum clock frequency guaranteed for proper operation is 13.5MHz. Figure 2 depicts a more detailed timing diagram of the serial interface.

Table 2. Serial-Interface Programming Commands

16-BIT SERIAL WORD					FUNCTION
C2	C1	C0	D11.....D0	S0*	
0	0	1	12-bit DAC data	0	Load input register A; DAC registers are unchanged.
0	1	0	12-bit DAC data	0	Load input register A; all DAC registers are updated.
0	1	1	12-bit DAC data	0	Load all DAC registers from the shift register (start up both DACs with new data, and load the input registers).
1	0	0	X X X X X X X X X X X X	0	Update both DAC registers from their respective input registers (start up both DACs with data previously stored in the input registers).
1	0	1	12-bit DAC data	0	Load input register B; DAC registers are unchanged.
1	1	0	12-bit DAC data	0	Load input register B; all DAC registers are updated.
1	1	1	P1A P1B X X X X X X X X X X	0	Shut down both DACs, respectively, according to bits P1A and P1B (see Table 3). Internal bias and reference remain active.
0	0	0	0 0 1 X X X X X X X X X	0	Update DAC register A from input register A (start up DAC A with data previously stored in input register A).
0	0	0	0 1 1 P1A P1B X X X X X X X	0	Full Power-Down. Power down the main bias generator and shut down both DACs, respectively, according to bits P1A and P1B (see Table 3).
0	0	0	1 0 1 X X X X X X X X X	0	Update DAC register B from input register B (start up DAC B with data previously stored in input register B).
0	0	0	1 1 0 P1A X X X X X X X X	0	Shut down DAC A according to bit P1A (see Table 3).
0	0	0	1 1 1 P1B X X X X X X X X	0	Shut down DAC B according to bit P1B (see Table 3).
0	0	0	1 0 0 0 X X X X X X X X	0	Mode 0. DOUT clocked out on SCLK falling edge (default).
0	0	0	1 0 0 1 X X X X X X X X	0	Mode 1. DOUT clocked out on SCLK rising edge.

X = Don't care.
* S0 must be zero for proper operation.

Power-Down and Shutdown Modes

As described in Tables 2 and 3, several serial interface commands put one or both of the DACs into shutdown mode. Shutdown modes are completely independent for each DAC. In shutdown, the amplifier output becomes high impedance, and OUT_ terminates to OS_ through the 200kΩ (typ) gain resistors. Optionally (see Tables 2 and 3), OUT_ can have an additional termination of 1kΩ to AGND.

Full power-down mode shuts down the main bias generator, reference, and both DACs. The shutdown impedance of the DAC outputs can still be controlled independently, as described in Tables 2 and 3.

A serial interface command exits shutdown mode and updates a DAC register. Each DAC can exit shutdown at the same time or independently (see Tables 2 and 3). For example, if both DACs are shut down, updating the DAC A register causes DAC A to power up, while DAC B remains shut down. In full power-down mode, powering up either DAC also powers up the main bias generator and reference. To change from full power-down to both DACs shutdown requires the waking of at least one DAC between states.

When powering up the MAX5230/MAX5231 (powering V_{DD}), allow 400µs (max) for the output to stabilize. When exiting full power-down mode, also allow 400µs (max) for the output to stabilize. When exiting DAC shutdown mode, allow 160µs (max) for the output to stabilize.

Reset Value (RSTV) and Clear ($\overline{CLR}$) Inputs

Driving $\overline{CLR}$ low asynchronously forces both DAC outputs and all the internal registers (input registers and DAC registers) for both DACs to either zero or midscale, depending on the level at RSTV. RSTV = DGND sets the zero value, and RSTV, = V_{DD} sets the midscale value.

The internal power-on reset circuit sets the DAC outputs and internal registers to either zero or midscale when power is first applied to the device, depending on the level at RSTV as described in the preceding paragraph. The DAC outputs are enabled after power is first applied. In order to obtain the midscale value on power-up (RSTV = V_{DD}), the voltage on RSTV must rise simultaneously with the V_{DD} supply.

Table 3. P1 Shutdown Modes

P1 (A/B)	SHUTDOWN MODE
0	Shut down with internal 1kΩ load to GND
1	Shut down with internal 200kΩ load to GND

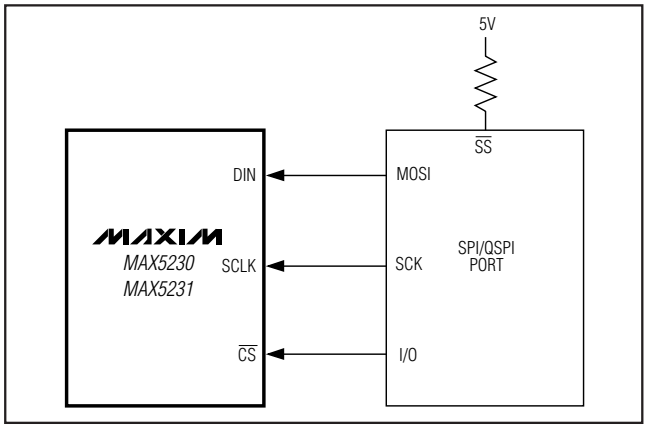


Figure 4. SPI/QSPI Interface Connections

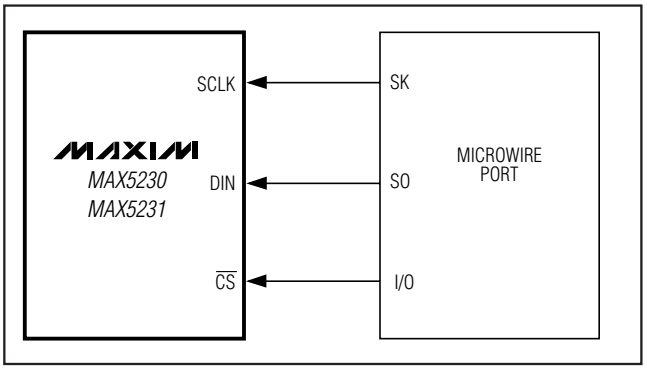


Figure 5. Connections for MICROWIRE

Load DAC Input ($\overline{LDAC}$)

Asserting $\overline{LDAC}$ asynchronously loads the DAC registers from their corresponding input registers (DACs that are shut down remain shut down). The $\overline{LDAC}$ input is totally asynchronous and does not require any activity on $\overline{CS}$, SCLK, or DIN in order to take effect. If $\overline{LDAC}$ is asserted coincident with a rising edge of $\overline{CS}$, which executes a serial command modifying the value of either DAC input register, then $\overline{LDAC}$ must remain asserted for at least 30ns following the $\overline{CS}$ rising edge. This requirement applies only for serial commands that modify the value of the DAC input registers.

Power-Down Lockout Input ($\overline{PDL}$)

Driving $\overline{PDL}$ low disables shutdown of either DAC. When $\overline{PDL}$ is low, serial commands to shut down either DAC are ignored. When either DAC is in shutdown mode, a high-to-low transition on $\overline{PDL}$ brings the DACs and the reference out of shutdown with DAC outputs set to the state prior to shutdown.

3V/5V, 12-Bit, Serial Voltage-Output Dual DACs with Internal Reference

Applications Information

Definitions

Integral Nonlinearity (INL)

Integral nonlinearity (Figure 6a) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit (closest approximation to the actual transfer curve) or a line drawn between the endpoints of the transfer function, once offset and gain errors have been nullified. For a DAC, the deviations are measured at every single step.

Differential Nonlinearity (DNL)

Differential nonlinearity (Figure 6b) is the difference between an actual step height and the ideal value of 1LSB. If the magnitude of the DNL is less than 1LSB, the DAC guarantees no missing codes and is monotonic.

Offset Error

The offset error (Figure 6c) is the difference between the ideal and the actual offset point. For a DAC, the offset point is the step value when the digital input is zero. This error affects all codes by the same amount and can usually be compensated for by trimming.

Gain Error

Gain error (Figure 6d) is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

Settling Time

The settling time is the amount of time required from the start of a transition, until the DAC output settles to its new output value within the converter's specified accuracy.

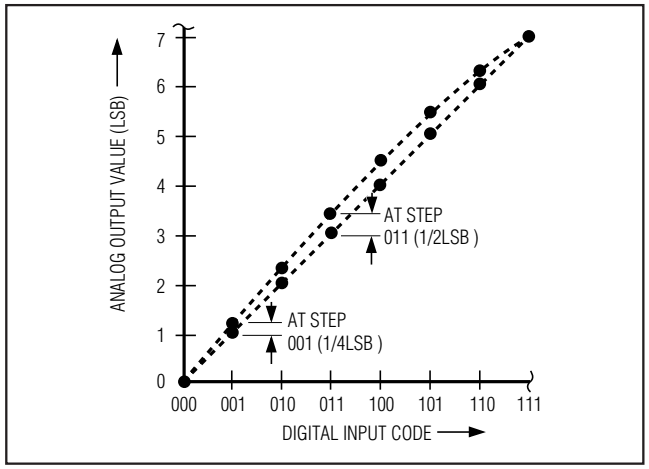


Figure 6a. Integral Nonlinearity

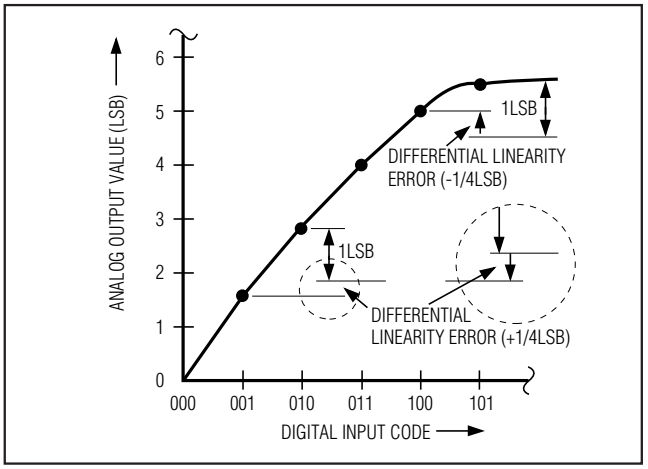


Figure 6b. Differential Nonlinearity

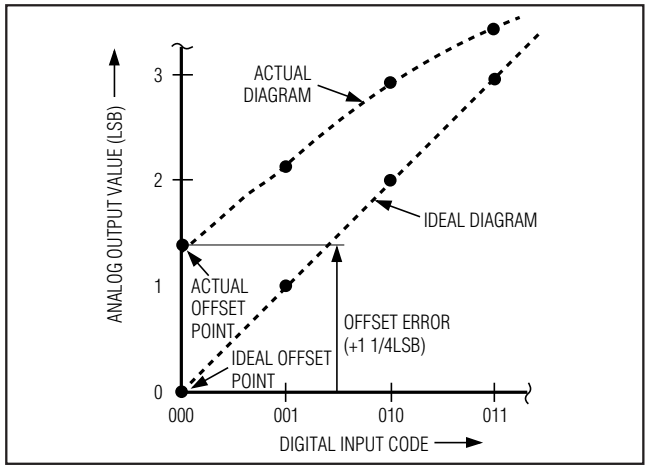


Figure 6c. Offset Error

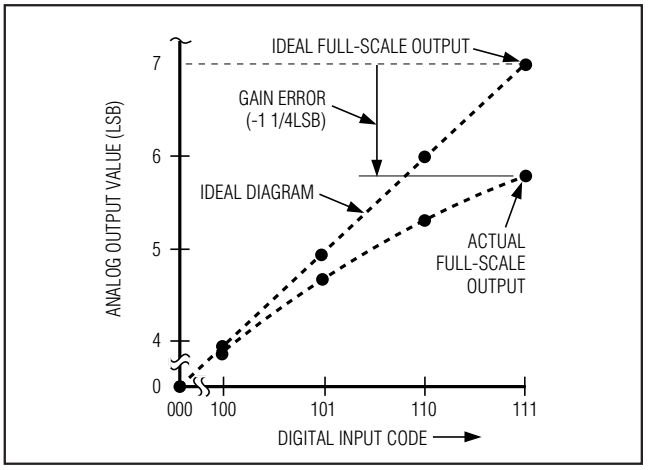


Figure 6d. Gain Error

Table 4. Unipolar Code Table

DAC CONTENTS		ANALOG OUTPUT (V)	
MSB	LSB	MAX5230	MAX5231
1111 1111 1	111 (0)	2.04750	4.0950
1000 0000 0	001 (0)	1.02425	2.0485
1000 0000 0	000 (0)	1.02375	2.0475
0111 1111 1	111 (0)	1.02325	2.0465
0000 0000	001 (0)	0.00050	0.0010
0000 0000 0	000 (0)	0	0

Digital Feedthrough

Digital feedthrough is noise generated on the DAC's output when any digital input transitions. Proper board layout and grounding significantly reduce this noise, but there is always some feedthrough caused by the DAC itself.

Unipolar Output

Figure 7 shows the MAX5230/MAX5231 configured for unipolar, rail-to-rail operation. The MAX5231 produces a 0 to 4.095V output, while the MAX5230 produces 0 to 2.0475V output. Table 4 lists the unipolar output codes.

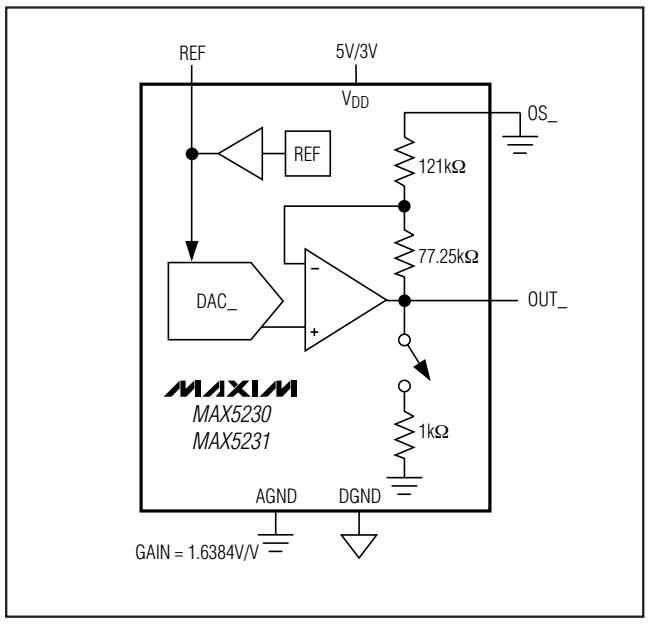


Figure 7. Unipolar Output Circuit (Rail-to-Rail)

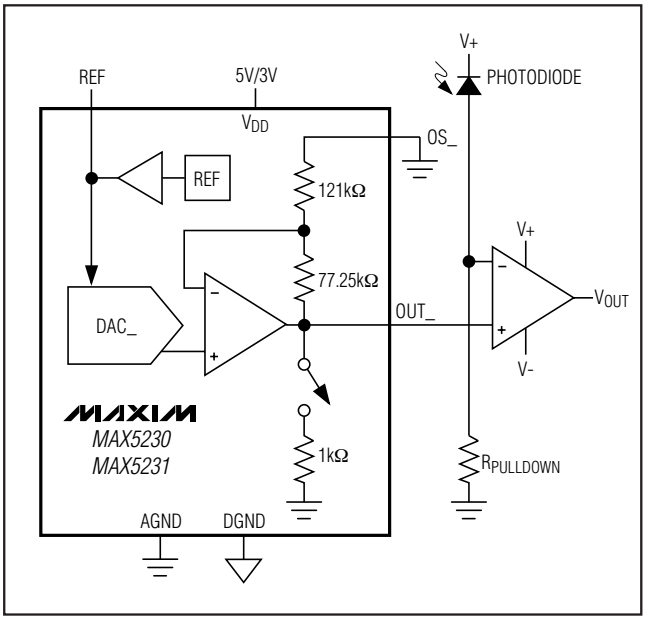


Figure 8. Digital Calibration

Digital Calibration and Threshold Selection

Figure 8 shows the MAX5230/MAX5231 in a digital calibration application. With a bright light value applied to the photodiode (on), the DAC is digitally ramped until it trips the comparator. The microprocessor (µP) stores this "high" calibration value. Repeat the process with a dim light (off) to obtain the dark current calibration. The µP then programs the DAC to set an output voltage at the midpoint of the two calibrated values. Applications include tachometers, motion sensing, automatic readers, and liquid clarity analysis.

Sharing a Common DIN Line

Several MAX5230/MAX5231s may share one common DIN signal line (Figure 9). In this configuration, the data bus is common to all devices; data is not shifted through a daisy-chain. The SCLK and DIN lines are shared by all devices, but each IC needs its own dedicated $\overline{CS}$ line.

Daisy-Chaining Devices

Any number of MAX5230/MAX5231s can be daisy-chained by connecting the serial data output (DOUT) of one device to the digital input (DIN) of the following device in the chain (Figure 10).

3V/5V, 12-Bit, Serial Voltage-Output Dual DACs with Internal Reference

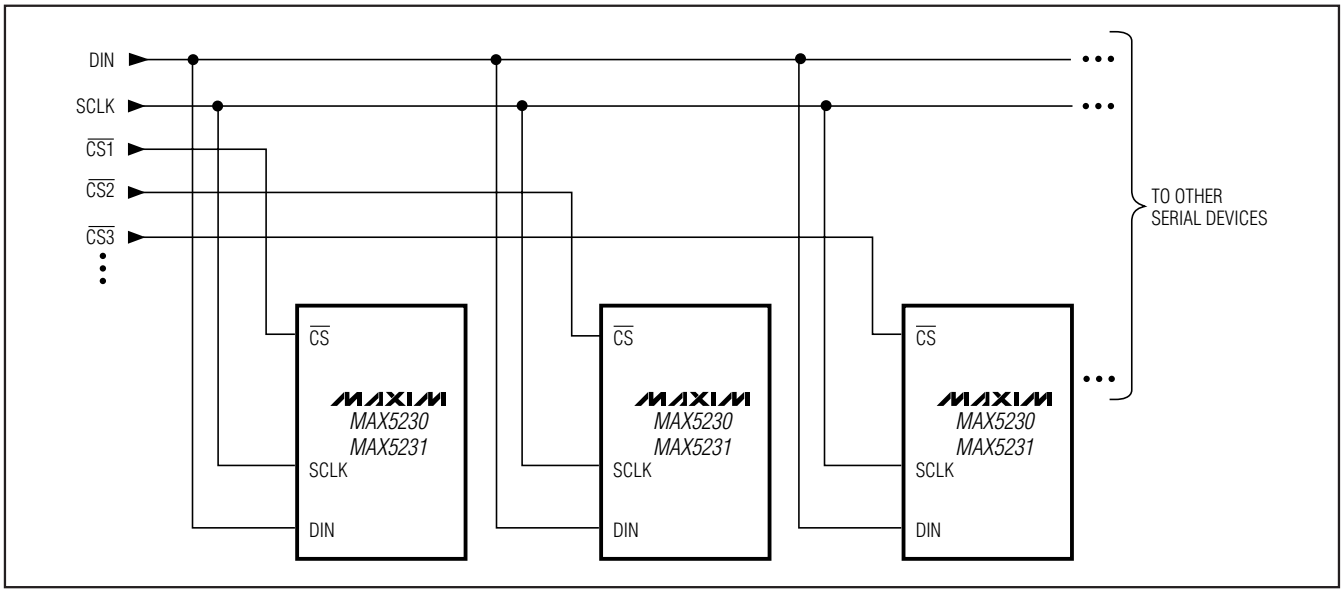


Figure 9. Multiple MAX5230/MAX5231s Sharing a Common DIN Line

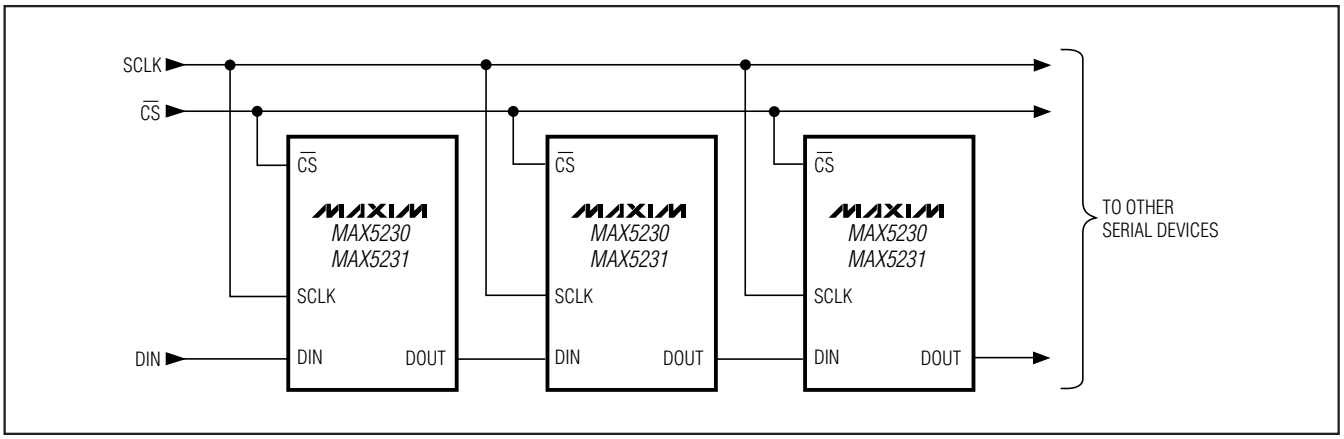


Figure 10. Daisy-Chaining MAX5230/MAX5231 Devices

Power-Supply and Bypassing Considerations

On power-up, the input and DAC registers are cleared to either zero (RSTV = DGND) or midscale (RSTV = V_{DD}). Bypass V_{DD} with a 4.7µF capacitor in parallel with a 0.1µF capacitor to AGND, and bypass V_{DD} with a 0.1µF capacitor to DGND. Minimize lead lengths to reduce lead inductance.

Grounding and Layout Considerations

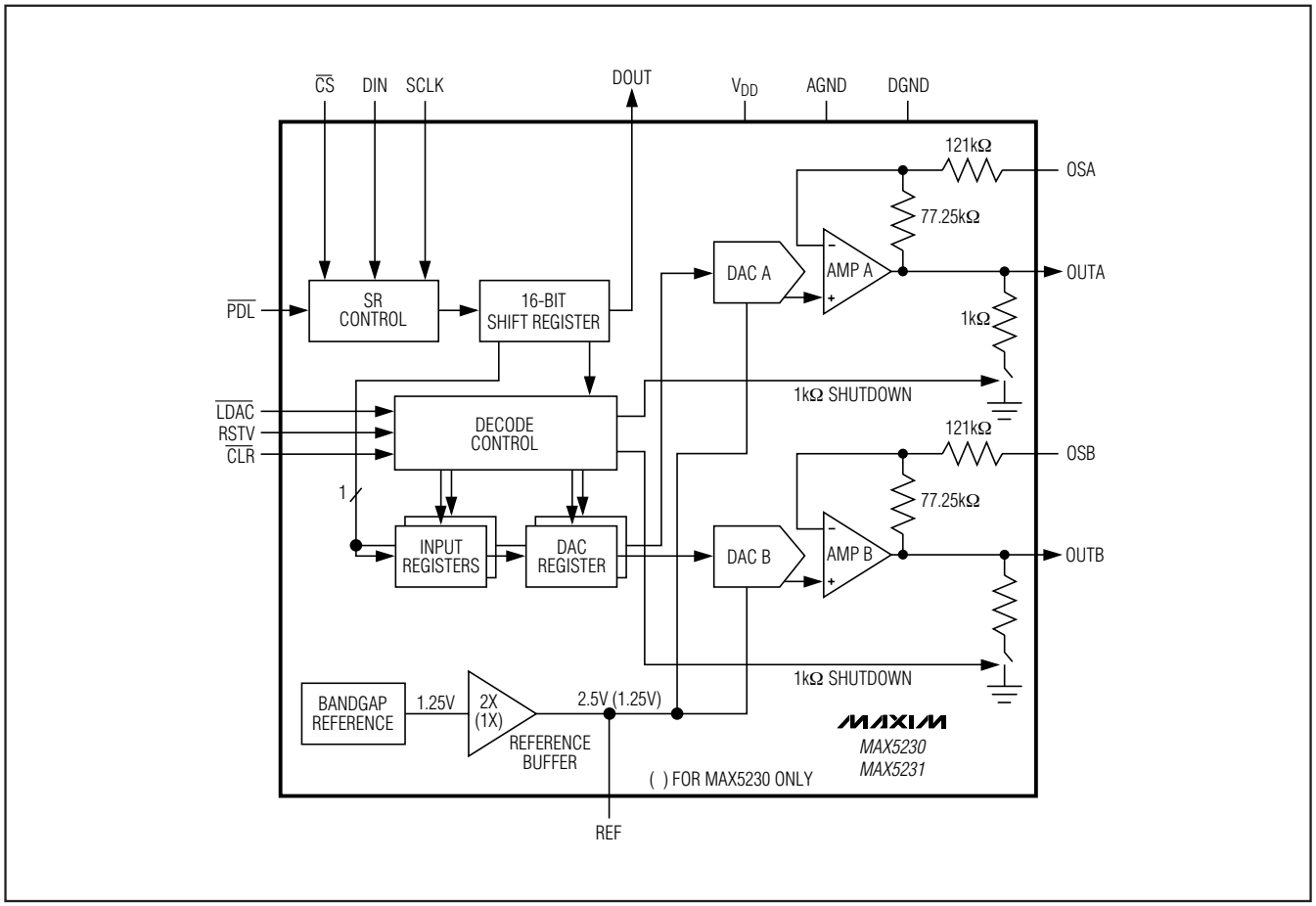
Digital and AC transient signals on AGND or DGND can create noise at the output. Connect AGND and DGND to the highest quality ground available. Use proper grounding techniques, such as a multilayer board with a low-inductance ground plane or star connect all ground return paths back to the MAX5230/MAX5231 AGND. Carefully lay out the traces between channels to reduce AC cross-coupling and crosstalk. Wire-wrapped boards and sockets are not recommended. If noise becomes an issue, shielding may be required.

Chip Information

TRANSISTOR COUNT: 4745

PROCESS: BiCMOS

Functional Diagram



Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
16 QSOP	E16-5	**21-0055**

3V/5V, 12-Bit, Serial Voltage-Output Dual DACs with Internal Reference

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	9/08	Changed specification	1, 2, 3, 11

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