



# Current-Mode PWM Controllers with an Error Amplifier for Isolated/Nonisolated Power Supplies

## General Description

The MAX5052/MAX5053 current-mode PWM controllers contain all the control circuitry required for the design of wide-input-voltage isolated and nonisolated power supplies. The MAX5052 is well suited for universal input (rectified 85VAC to 265VAC) or telecom (-36VDC to -72VDC) power supplies. The MAX5053 is well suited for low-input-voltage (10.8VDC to 24VDC) power supplies.

The MAX5052/MAX5053 contain an internal error amplifier that regulates the tertiary winding output voltage. This implements a primary-side regulated, isolated power supply, eliminating the need for an optocoupler. An input undervoltage lockout (UVLO) is provided for programming the input-supply start voltage and to ensure proper operation during brownout conditions. The input-supply start voltage is externally programmable with a voltage-divider. To shutdown the device, the UVLO pin is pulled low. Internal digital soft-start reduces output voltage overshoot. The internal thermal shutdown circuit protects the device in the event the junction temperature exceeds +130°C.

The MAX5052 has an internal bootstrap UVLO with large hysteresis that requires a minimum voltage of 23.6V for startup. The MAX5053 does not have the internal bootstrap UVLO and can be biased directly from a minimum voltage of 10.8V.

The 262kHz switching frequency is internally trimmed to  $\pm 12\%$  accuracy; this allows the optimization of the magnetic and filter components resulting in compact, cost-effective power supplies. The MAX5052A/MAX5053A are offered with a 50% maximum duty-cycle limit. The MAX5052B/MAX5053B are offered with a 75% maximum duty-cycle limit. These devices are available in 8-pin  $\mu$ MAX packages and operate over the -40°C to +85°C temperature range.

## Applications

Universal Input AC Power Supplies	Industrial Power Conversion
Isolated Telecom Power Supplies	Isolated Keep-Alive Circuits
Networking Systems	12V Boost Regulators
Computer Systems/Servers	12V SEPIC Regulators

Functional Diagram/Typical Operating Circuit/Selector Guide appear at end of data sheet.

## Features

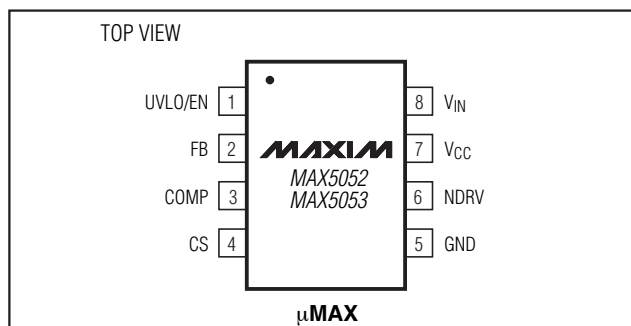
- ◆ Available in a Tiny 8-Pin  $\mu$ MAX Package
- ◆ Current-Mode Control
- ◆ 50W Output Power
- ◆ Universal Offline Input Voltage Range Rectified 85VAC to 265VAC (MAX5052)
- ◆  $V_{IN}$  Directly Driven from 10.8V to 24V Input (MAX5053)
- ◆ Digital Soft-Start
- ◆ Programmable Input Startup Voltage
- ◆ Internal Bootstrap UVLO with Large Hysteresis (MAX5052)
- ◆ Internal Error Amplifier with 1% Accurate Reference
- ◆ Thermal Shutdown
- ◆ 45 $\mu$ A (typ) Startup Supply Current
- ◆ 1.4mA (typ) Operating Supply Current
- ◆ Fixed Switching Frequency of 262kHz  $\pm 12\%$
- ◆ 50% Maximum Duty-Cycle Limit (MAX5052A/MAX5053A)
- ◆ 75% Maximum Duty-Cycle Limit (MAX5052B/MAX5053B)
- ◆ 60ns Cycle-by-Cycle Current-Limit Response Time

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5052AEUA	-40°C to +85°C	8 $\mu$ MAX
MAX5052BEUA	-40°C to +85°C	8 $\mu$ MAX
MAX5053AEUA	-40°C to +85°C	8 $\mu$ MAX
MAX5053BEUA	-40°C to +85°C	8 $\mu$ MAX

**Warning:** The MAX5052/MAX5053 are designed to work with high voltages. Exercise caution.

## Pin Configuration



# Current-Mode PWM Controllers with an Error Amplifier for Isolated/Nonisolated Power Supplies

## ABSOLUTE MAXIMUM RATINGS

$V_{IN}$  to GND .....-0.3V to +30V  
 $V_{CC}$  to GND .....-0.3V to +13V  
 FB, COMP, UVLO, CS to GND .....-0.3V to +6V  
 $NDRV$  to GND.....-0.3V to ( $V_{CC} + 0.3V$ )  
 Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )  
     8-Pin  $\mu\text{MAX}$  (derate 4.5mW/ $^\circ\text{C}$  above  $+70^\circ\text{C}$ ) .....362mW

Operating Temperature Range .....-40 $^\circ\text{C}$  to +85 $^\circ\text{C}$   
 Storage Temperature Range .....-65 $^\circ\text{C}$  to +150 $^\circ\text{C}$   
 Junction Temperature .....+150 $^\circ\text{C}$   
 Lead Temperature (soldering, 10s) .....+300 $^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

( $V_{IN} = +12V$  (for MAX5052,  $V_{IN}$  must first be brought up to 23.6V for startup), 10nF bypass capacitors at  $V_{IN}$  and  $V_{CC}$ ,  $C_{NDRV} = 0$ ,  $V_{UVLO} = +1.4V$ ,  $V_{FB} = +1.0V$ ,  $V_{COMP}$  = floating,  $V_{CS} = 0V$ , typical values are measured at  $T_A = +25^\circ\text{C}$ ,  $T_A = -40^\circ\text{C}$  to +85 $^\circ\text{C}$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UNDERVOLTAGE LOCKOUT/STARTUP						
Bootstrap UVLO Wake-Up Level	V <sub>SUVR</sub>	V <sub>IN</sub> rising (MAX5052 only)	19.68	21.6	23.60	V
Bootstrap UVLO Shutdown Level	V <sub>SUVF</sub>	V <sub>IN</sub> falling (MAX5052 only)	9.05	9.74	10.43	V
UVLO/EN Wake-Up Threshold	V <sub>ULR2</sub>	UVLO/EN rising	1.188	1.28	1.371	V
UVLO/EN Shutdown Threshold	V <sub>ULF2</sub>	UVLO/EN falling	1.168	1.23	1.291	V
UVLO/EN Input Current	I <sub>UVLO</sub>	T <sub>J</sub> = +125°C		25		nA
UVLO/EN Hysteresis				50		mV
V <sub>IN</sub> Supply Current In Undervoltage Lockout	I <sub>START</sub>	V <sub>IN</sub> = +19V, for MAX5052 only when in bootstrap UVLO		45	90	μA
V <sub>IN</sub> Range	V <sub>IN</sub>		10.8		24	V
UVLO/EN Propagation Delay	t <sub>EXTR</sub>	UVLO/EN steps up from +1.1V to +1.4V		12		μs
	t <sub>EXTF</sub>	UVLO/EN steps down from +1.4V to +1.1V		1.8		
Bootstrap UVLO Propagation Delay	t <sub>BUVR</sub>	V <sub>IN</sub> steps up from +9V to +24V		5		μs
	t <sub>BUVF</sub>	V <sub>IN</sub> steps down from +24V to +9V		1		
INTERNAL SUPPLY						
V <sub>CC</sub> Regulator Set Point	V <sub>CCSP</sub>	V <sub>IN</sub> = +10.8V to +24V, sinking 1μA to 20mA from V <sub>CC</sub>	7		10.5	V
V <sub>IN</sub> Supply Current After Startup	I <sub>IN</sub>	V <sub>IN</sub> = +24V		1.4	2.5	mA
Shutdown Supply Current		UVLO/EN = low			90	μA
GATE DRIVER						
Driver Output Impedance	R <sub>ON(LOW)</sub>	Measured at NDRV sinking, 100mA		2	4	Ω
	R <sub>ON(HIGH)</sub>	Measured at NDRV sourcing, 20mA		4	12	
Driver Peak Sink Current				1		A
Driver Peak Source Current				0.65		A
PWM COMPARATOR						
Comparator Offset Voltage	V <sub>OPWM</sub>	V <sub>COMP</sub> - V <sub>CS</sub>	1.15	1.38	1.70	V
CS Input Bias Current	I <sub>CS</sub>	V <sub>CS</sub> = 0V	-2		+2	μA
Comparator Propagation Delay	t <sub>PWM</sub>	V <sub>CS</sub> = +0.1V		60		ns
Minimum On-Time	t <sub>ON(MIN)</sub>			150		ns

# Current-Mode PWM Controllers with an Error Amplifier for Isolated/Nonisolated Power Supplies

MAX5052/MAX5053

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{IN} = +12V$  (for MAX5052,  $V_{IN}$  must first be brought up to 23.6V for startup), 10nF bypass capacitors at  $V_{IN}$  and  $V_{CC}$ ,  $C_{NDRV} = 0$ ,  $V_{UVLO} = +1.4V$ ,  $V_{FB} = +1.0V$ ,  $V_{COMP}$  = floating,  $V_{CS} = 0V$ , typical values are measured at  $T_A = +25^{\circ}C$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT-LIMIT COMPARATOR						
Current-Limit Trip Threshold	V <sub>CS</sub>		262	291	320	mV
CS Input Bias Current	I <sub>CS</sub>	V <sub>CS</sub> = 0V	-2		+2	μA
Propagation Delay From Comparator Input to NDRV	t <sub>PWM</sub>	50mV overdrive		60		ns
Switching Frequency	f <sub>SW</sub>		230	262	290	kHz
Maximum Duty Cycle	D <sub>MAX</sub>	MAX505_A		50	50.5	%
		MAX505_B		75	76	
V <sub>IN</sub> CLAMP VOLTAGE						
V <sub>IN</sub> Clamp Voltage	V <sub>INC</sub>	2mA sink current, MAX5052 only (Note 3)	24.1	26.1	29.0	V
ERROR AMPLIFIER						
Voltage Gain		R <sub>LOAD</sub> = 100kΩ		80		dB
Unity-Gain Bandwidth		R <sub>LOAD</sub> = 100kΩ, C <sub>LOAD</sub> = 200pF		2		MHz
Phase Margin		R <sub>LOAD</sub> = 100kΩ, C <sub>LOAD</sub> = 200pF		65		degrees
FB Input Offset Voltage					3	mV
COMP Pin Clamp Voltage		High	2.2		3.5	V
		Low	0.4		1.1	
Source Current			0.5			mA
Sink Current			0.5			mA
Reference Voltage	V <sub>REF</sub>	(Note 2)	1.218	1.230	1.242	V
Input Bias Current					50	nA
COMP Short-Circuit Current				8		mA
THERMAL SHUTDOWN						
Thermal-Shutdown Temperature				130		°C
Thermal Hysteresis				25		°C
DIGITAL SOFT-START						
Soft-Start Duration				15,872		clock cycles
Reference Voltage Steps During Soft-Start				31		steps
Reference Voltage Step				40		mV

**Note 1:** All devices are 100% tested at  $T_A = +85^{\circ}C$ . All limits over temperature are guaranteed by characterization.

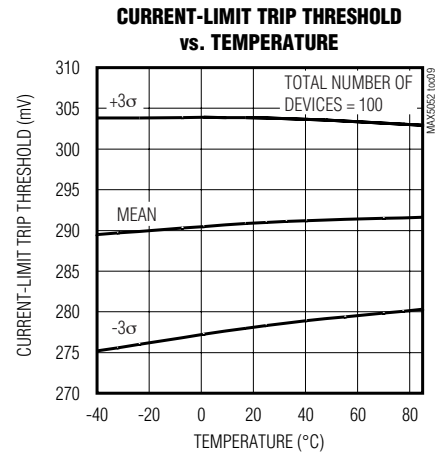
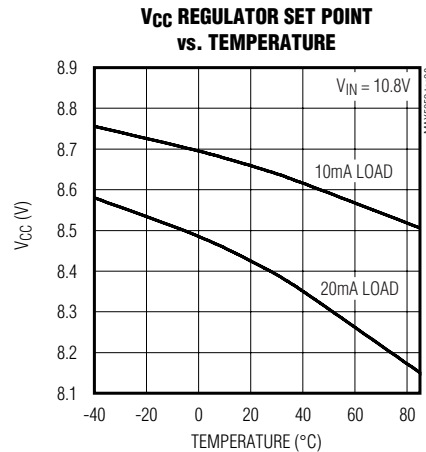
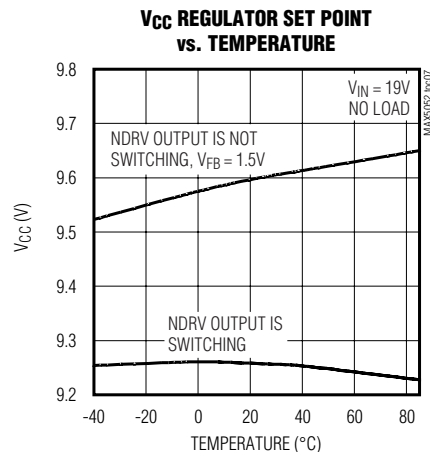
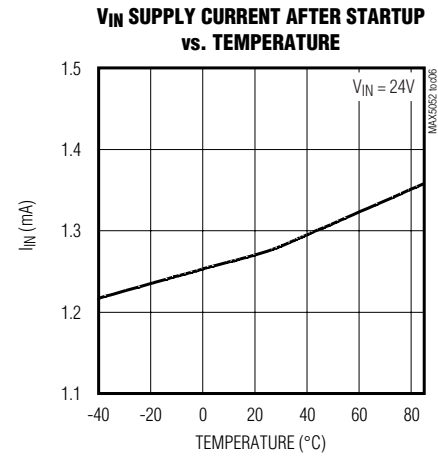
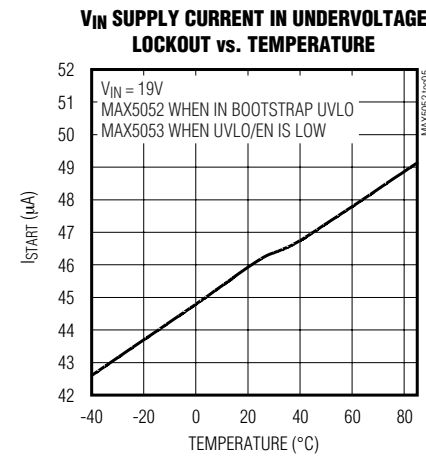
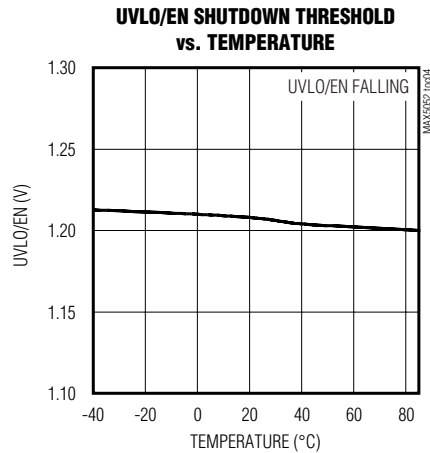
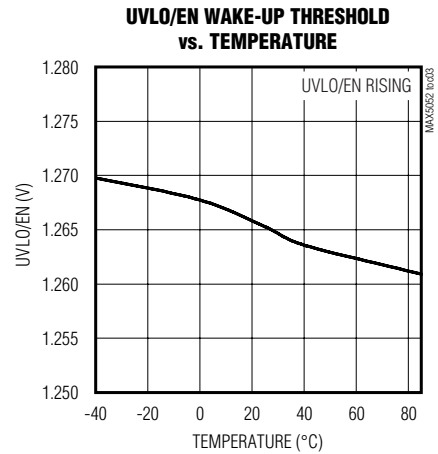
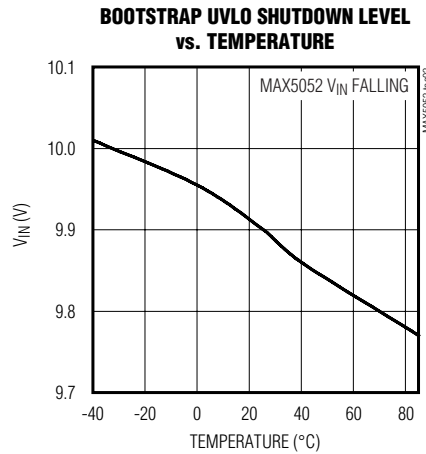
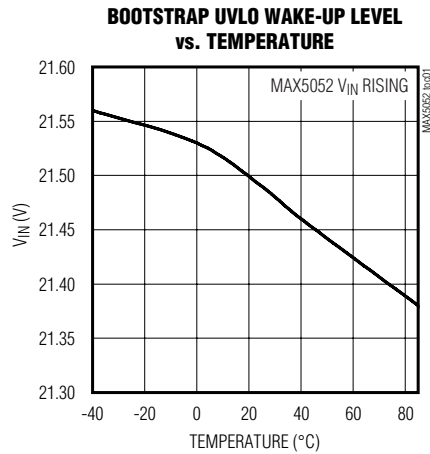
**Note 2:**  $V_{REF}$  is measured with FB connected to the COMP pin (see *Functional Diagram*).

**Note 3:** The MAX5052 is intended for use in universal input power supplies. The internal clamp circuit is used to prevent the bootstrap capacitor (C1 in Figure 1) from charging to a voltage beyond the absolute maximum rating of the device when EN/UVLO is low. The maximum current to  $V_{IN}$  (hence to clamp) when UVLO is low (device in shutdown) must be externally limited to 2mA, max. Clamp currents higher than 2mA may result in clamp voltage higher than 30V, thus exceeding the absolute maximum rating for  $V_{IN}$ . For the MAX5053, do not exceed the 24V maximum operating voltage of the device.

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## Typical Operating Characteristics

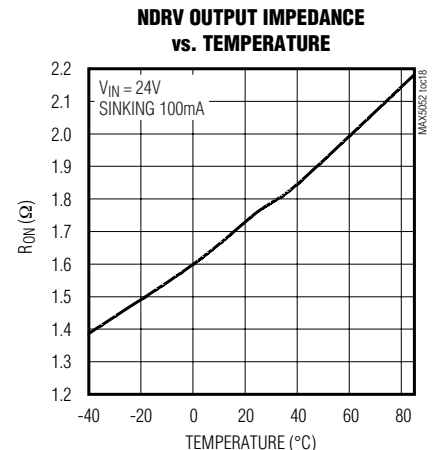
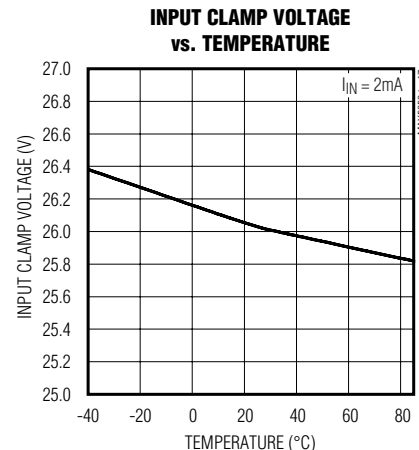
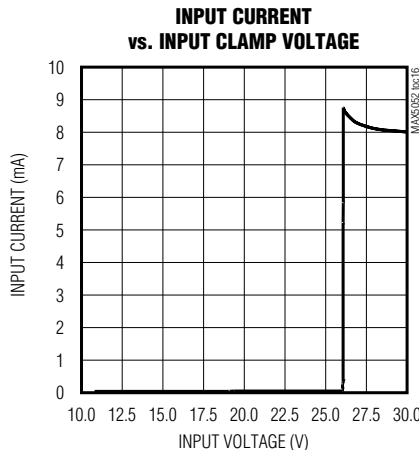
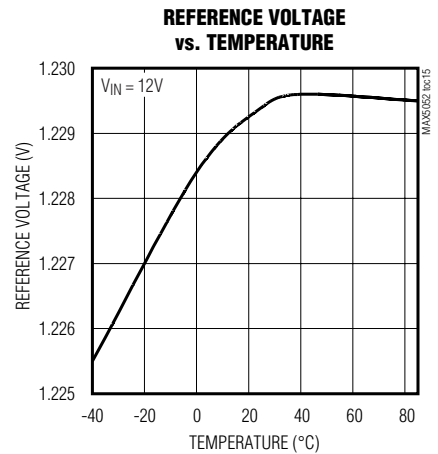
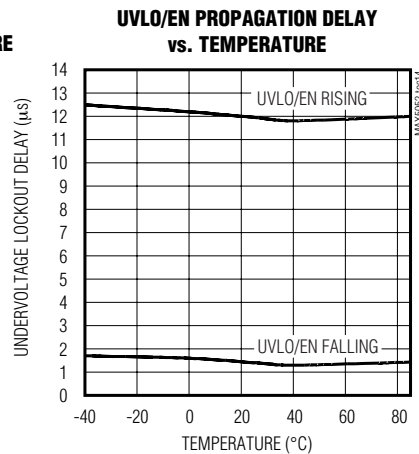
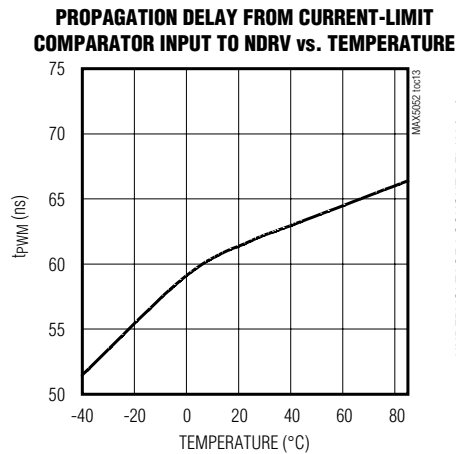
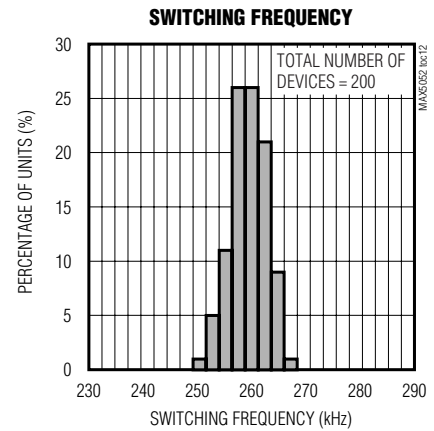
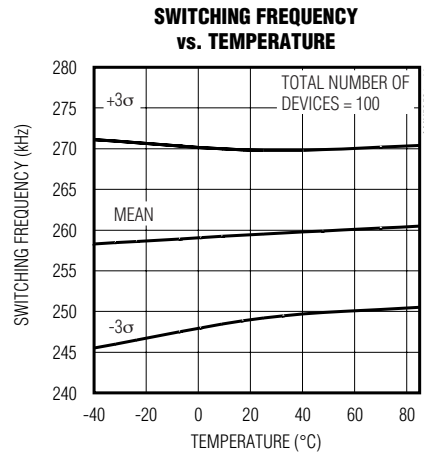
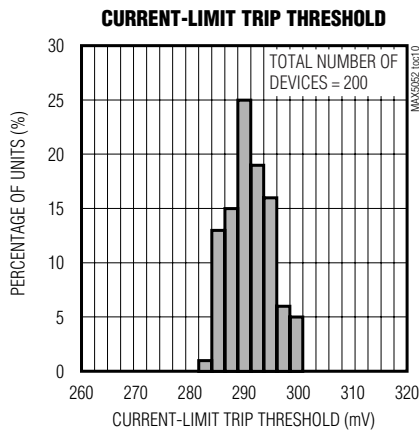
(UVLO = +1.4V,  $V_{FB}$  = +1V,  $V_{COMP}$  = floating,  $V_{CS}$  = 0V,  $T_A$  = +25°C, unless otherwise noted.)



# Current-Mode PWM Controllers with an Error Amplifier for Isolated/Nonisolated Power Supplies

## Typical Operating Characteristics (continued)

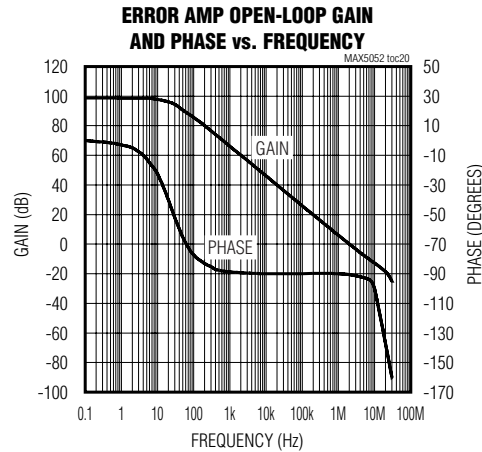
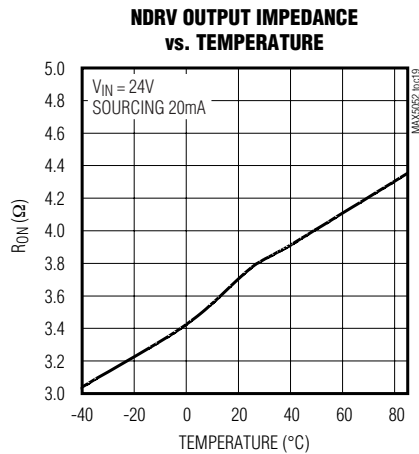
(UVLO = +1.4V, V<sub>FB</sub> = +1V, V<sub>COMP</sub> = floating, V<sub>CS</sub> = 0V, T<sub>A</sub> = +25°C, unless otherwise noted.)



# Current-Mode PWM Controllers with an Error Amplifier for Isolated/Nonisolated Power Supplies

## Typical Operating Characteristics (continued)

(UVLO = +1.4V, V<sub>FB</sub> = +1V, V<sub>COMP</sub> = floating, V<sub>CS</sub> = 0V, T<sub>A</sub> = +25°C, unless otherwise noted.)



## Pin Description

PIN	NAME	FUNCTION
1	UVLO/EN	Externally Programmable Undervoltage Lockout. UVLO programs the input start voltage. Connect UVLO to GND to disable the device.
2	FB	Error-Amplifier Inverting Input
3	COMP	Error-Amplifier Output
4	CS	Current-Sense Connection for PWM Regulation and Overcurrent Protection. Connect to high side of sense resistor. An RC filter may be necessary to eliminate leading-edge spikes.
5	GND	Power-Supply Ground
6	NDRV	External N-Channel MOSFET Gate Connection
7	V <sub>CC</sub>	Gate-Drive Supply. Internally regulated down from V <sub>IN</sub> . Decouple with a 10nF or larger capacitor to GND.
8	V <sub>IN</sub>	IC Supply. Decouple with a 10nF or larger capacitor to GND. For bootstrapped operation (MAX5052) connect a startup resistor from the input supply line to V <sub>IN</sub> . Connect the bias winding supply to this point as well (see the <i>Typical Operating Circuit</i> ). For the MAX5053, connect V <sub>IN</sub> directly to 10.8V to 24V supply.

## Detailed Description

The MAX5052/MAX5053 are current-mode PWM controllers that have been specifically designed for use in isolated and nonisolated power-supply applications. A bootstrap UVLO with a large hysteresis (11.9V), very low startup current, and low operating current result in efficient universal-input power supplies. In addition to the internal bootstrap UVLO, these devices also offer programmable input startup voltage programmed through the UVLO/EN pin. This feature is useful in preventing the power supply from entering a brownout condition, in case the input voltage drops below its minimum value. This is important since switching power

supplies increases their input supply current as the input voltage drops in order to keep the output power constant. The MAX5052 is well suited for universal input (rectified 85VAC to 265VAC) or telecom (-36VDC to -72VDC) power supplies. The MAX5053 is well suited for low-input-voltage (10.8VDC to 24VDC) power supplies.

Power supplies designed with the MAX5052 use a high-value startup resistor, R<sub>1</sub>, that charges a reservoir capacitor, C<sub>1</sub> (see Figure 1). During this initial period, while the voltage is less than the internal bootstrap UVLO threshold, the device typically consumes only 45μA of quiescent current. This low startup current and the large bootstrap UVLO hysteresis helps to minimize

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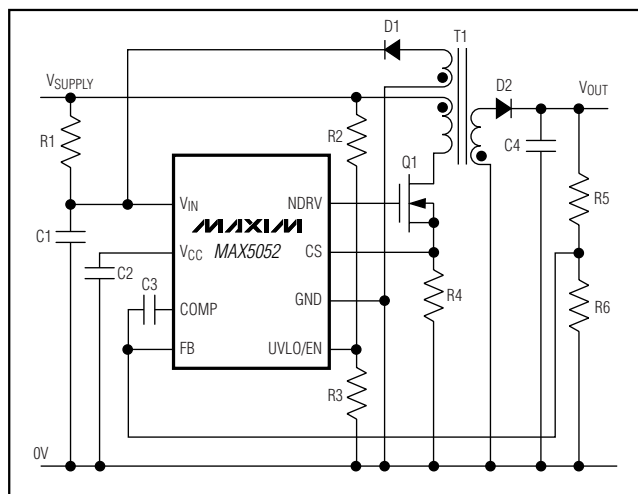


Figure 1. Nonisolated Power Supply with Programmable Input-Supply Start Voltage

the power dissipation across R1 even at the high end of the universal AC input voltage (265VAC).

The MAX5052/MAX5053 include a cycle-by-cycle current limit that turns off the gate drive to the external MOSFET during an overcurrent condition. When using the MAX5052 in the bootstrapped mode (if the power-supply output is shorted), the tertiary winding voltage drops below the 10V threshold causing the UVLO to turn off the gate drive to the external power MOSFET. This reinitiates a startup sequence with soft-start.

## MAX5052/MAX5053 Undervoltage Lockout

The MAX5052/MAX5053 have an input voltage UVLO/EN pin. The threshold for this UVLO is 1.28V. Before any operation can commence, the voltage on this pin has to exceed 1.28V. The UVLO circuit keeps the CPWM comparator, ILIM comparator, oscillator, and output driver shut down to reduce current consumption (see the *Functional Diagram*).

Use this UVLO function to program the input-supply start voltage. For example, a reasonable start voltage for a 36V to 72V telecom range might be set at 34V. Calculate the divider resistor values, R2 and R3 (see Figure 1) by using the following formulas:

$$R3 = \frac{V_{ULR2} \times V_{IN}}{500 \times I_{UVLO}(V_{IN} - V_{ULR2})}$$

The value of R3 is calculated to minimize the voltage-drop error across R2 as a result of the input bias current of the UVLO/EN pin.  $V_{ULR2} = 1.28V$ ,  $I_{UVLO} = 50nA$

(max).  $V_{IN}$  is the value of the input-supply voltage where the power supply must start.

$$R2 = \frac{V_{IN} - V_{ULR2}}{V_{ULR2}} \times R3$$

where  $I_{UVLO}$  is the UVLO/EN pin input current (50nA), and  $V_{ULR2}$  is the UVLO/EN wake-up threshold.

## MAX5052 Bootstrap Undervoltage Lockout

In addition to the externally programmable UVLO function offered in both the MAX5052 and MAX5053, the MAX5052 has an additional internal bootstrap UVLO that is very useful when designing high-voltage power supplies (see the *Functional Diagram*). This allows the device to bootstrap itself during initial power-up. The MAX5052 attempts to start when  $V_{IN}$  exceeds the bootstrap UVLO threshold of 21.6V.

During startup, the UVLO circuit keeps the CPWM comparator, ILIM comparator, oscillator, and output driver shut down to reduce current consumption. Once  $V_{IN}$  reaches 21.6V, the UVLO circuit turns on both the CPWM and ILIM comparators, as well as the oscillator, and allows the output driver to switch. If  $V_{IN}$  drops below 9.7V, the UVLO circuit will shut down the CPWM comparator, ILIM comparator, oscillator, and output driver returning the MAX5052/MAX5053 to the startup mode.

## MAX5052 Startup Operation

Normally  $V_{IN}$  is derived from a tertiary winding of the transformer. However, at startup there is no energy delivered through the transformer, hence, a special bootstrap sequence is required. Figure 2 shows the voltages on  $V_{IN}$  and  $V_{CC}$  during startup. Initially, both  $V_{IN}$  and  $V_{CC}$  are 0V. After the line voltage is applied, C1 charges through the startup resistor, R1, to an intermediate voltage. At this point, the internal regulator begins charging C2 (see Figure 1). The MAX5052 uses only 45μA of the current supplied by R1, and the remaining input current charges C1 and C2. The charging of C2 stops when the  $V_{CC}$  voltage reaches approximately 9.5V, while the voltage across C1 continues rising until it reaches the wake-up level of 21.6V. Once  $V_{IN}$  exceeds the bootstrap UVLO threshold, NDRV begins switching the MOSFET and transfers energy to the secondary and tertiary outputs. If the voltage on the tertiary output builds to higher than 9.9V (the bootstrap UVLO lower threshold), then startup has been accomplished and sustained operation commences.

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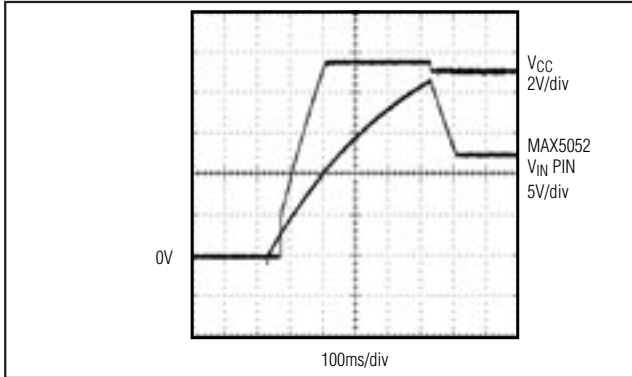


Figure 2.  $V_{IN}$  and  $V_{CC}$  During Startup when Using the MAX5052 in Bootstrapped Mode (Figure 1)

If  $V_{IN}$  drops below 9.9V before startup is complete, the device goes back to low-current UVLO. In this case, increase the value of  $C1$  in order to store enough energy to allow for the voltage at tertiary winding to build up.

## Startup Time Considerations For Power Supplies Using the MAX5052

The  $V_{IN}$  bypass capacitor,  $C1$ , supplies current immediately after wake up (see Figure 1). The size of  $C1$  and the connection configuration of the tertiary winding determine the number of cycles available for startup. Large values of  $C1$  increase the startup time but also supply gate charge for more cycles during initial start-up. If the value of  $C1$  is too small,  $V_{IN}$  drops below 9.9V because NDRV does not have enough time to switch and build up sufficient voltage across the tertiary output which powers the device. The device goes back into UVLO and does not start. Use a low-leakage capacitor for  $C1$  and  $C2$ .

As a rule of thumb, offline power supplies keep typical startup times to less than 500ms even in low-line conditions (85VAC input for universal offline or 36VDC for telecom applications). Size the startup resistor,  $R1$ , to supply both the maximum startup bias of the device (90 $\mu$ A) and the charging current for  $C1$  and  $C2$ . The bypass capacitor,  $C2$ , must charge to 9.5V and  $C1$  to 24V, all within the desired time period of 500ms. Because of the internal 60ms soft-start time of the MAX5052,  $C1$  must store enough charge to deliver current to the device for at least this much time. To calculate the approximate amount of capacitance required, use the following formula:

$$I_g = Q_{gtot} \times f_{sw}$$

$$C1 = \frac{(I_{IN} + I_g)(t_{ss})}{V_{hyst}}$$

where  $I_{IN}$  is the MAX5052's internal supply current after startup (1.4mA),  $Q_{gtot}$  is the total gate charge for Q1,  $f_{sw}$  is the MAX5052's switching frequency (262kHz),  $V_{hyst}$  is the bootstrap UVLO hysteresis (12V) and  $t_{ss}$  is the internal soft-start time (60ms).

For example:

$$I_g = (8nC)(262kHz) \approx 2.1mA$$

$$C1 = \frac{(1.4mA + 2.1mA)(60ms)}{(12V)} = 17.5\mu F$$

choose 15 $\mu$ F standard value.

Assuming  $C1 > C2$ , calculate the value of  $R1$  as follows:

$$I_{C1} = \frac{V_{SUVR} \times C1}{(500ms)}$$

$$R1 = \frac{V_{IN(MIN)} - V_{SUVR}}{I_{C1} + I_{START}}$$

where  $V_{IN(MIN)}$  is the minimum input supply voltage for the application (36V for telecom),  $V_{SUVR}$  is the bootstrap UVLO wake-up level (23.6V max.),  $I_{START}$  is the  $V_{IN}$  supply current at startup (90 $\mu$ A, max).

For example:

$$I_{C1} = \frac{(24V)(15\mu F)}{(500ms)} = 0.72mA$$

$$R1 = \frac{(36V) - (12V)}{(0.72mA) + (90\mu A)} = 29.6k\Omega$$

choose 32k $\Omega$  standard value.

Choose a higher value for  $R1$  than the one calculated above if longer startup time can be tolerated in order to minimize power loss on this resistor.

The above startup method is applicable to a circuit similar to the one shown in Figure 1. In this circuit, the tertiary winding has the same phase as the output windings. Thus, the voltage on the tertiary winding at any given time is proportional to the output voltage and goes through the same soft-start period as the output voltage. The minimum discharge voltage of  $C1$  from 22V to 10V must be greater than the soft-start time of 60ms.

Another method for bootstrapping the power supply is to have a separate bias winding than the one used for regulating the output voltage and to connect the bias winding so that it is in phase with the MOSFET ON time (see Figure 3). The amount of capacitance required is much

# Current-Mode PWM Controllers with an Error Amplifier for Isolated/Nonisolated Power Supplies

MAX5052/MAX5053

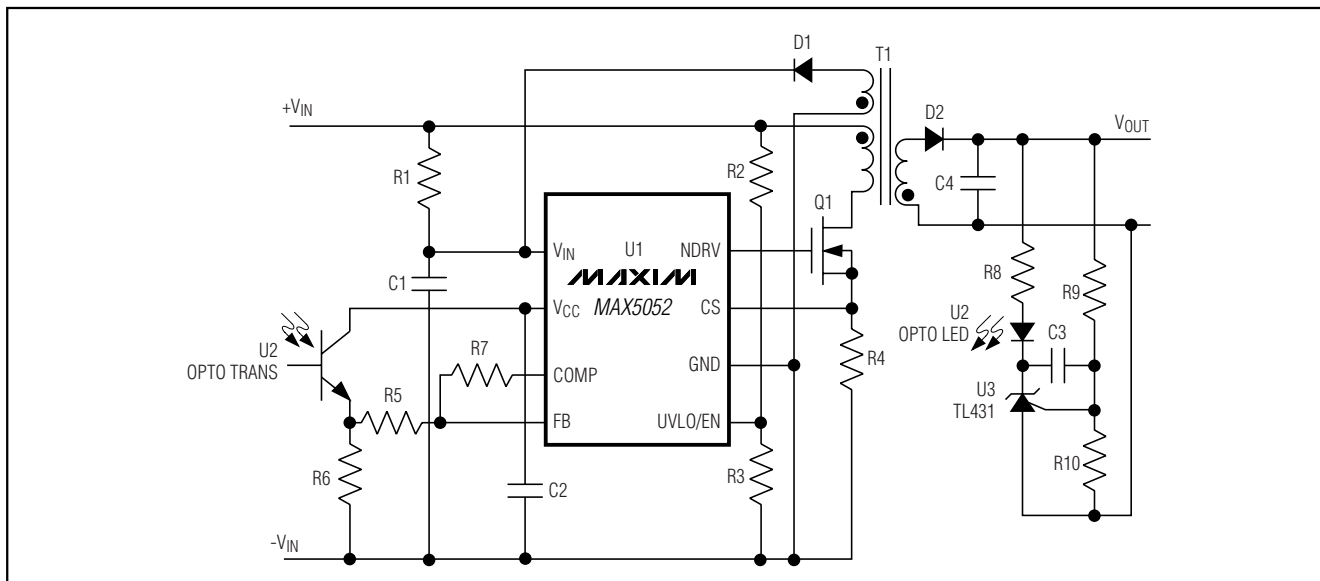


Figure 3. Secondary-Side Regulated, Isolated Power Supply

smaller. However, in this mode, the input voltage range has to be roughly 2:1. Another consideration is if the bias winding is in phase with the output, then the power supply hiccups and soft-start under output short-circuit conditions. Whereas, this property is lost if the bias winding is in phase with the MOSFET ON time.

## Soft-Start

The MAX5052/MAX5053 soft-start feature allows the load voltage to ramp up in a controlled manner, eliminating output voltage overshoot. Soft-start begins after UVLO is deasserted. The voltage applied to the noninverting node of the amplifier ramps from 0 to 1.23V in over a 60ms soft-start timeout period. Figure 4 shows the 5V output of the power-supply circuit in Figure 5 during startup. Note the staircase increase of the output voltage. This is a result of the digital soft-starting technique used. Unlike other devices, the MAX5052/MAX5053 reference voltage to the internal amplifier is soft-started; this method results in superior control of the output voltage under heavy- and light-load conditions.

## N-Channel MOSFET Switch Driver

The NDRV pin drives an external N-channel MOSFET. The NDRV output is supplied by the internal regulator (V<sub>CC</sub>), which is internally set to approximately 9.5V. For the universal input voltage range, the MOSFET used must be able to withstand the DC level of the high-line input voltage plus the reflected voltage at the primary of the transformer. For most offline applications that use the discontinuous flyback topology, this requires a MOSFET rated at 600V. NDRV can source/sink in excess of the

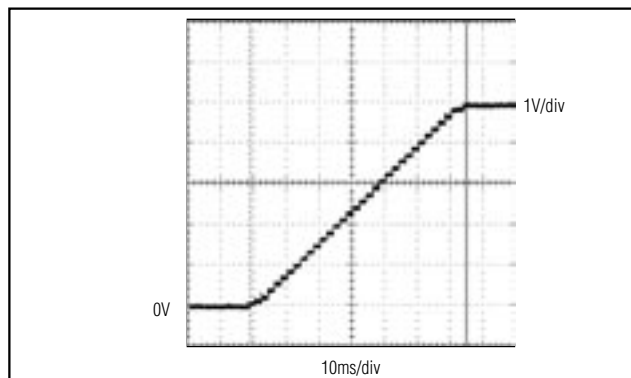


Figure 4. Output Voltage Soft-Start During Initial Startup for the Circuit of Figure 5

650mA/1000mA peak current, so select a MOSFET that yields acceptable conduction and switching losses.

## Internal Oscillator

The internal oscillator switches at 1.048MHz and is divided down to 262kHz by two D flip-flops. The MAX5052A/MAX5053A invert the Q output of the last D flip-flop to provide a duty cycle of 50% (Figure 6). The MAX5052B/MAX5053B perform a logic NAND operation on the Q outputs of both D flip-flops to provide a duty cycle of 75%.

# Current-Mode PWM Controllers with an Error Amplifier for Isolated/Nonisolated Power Supplies

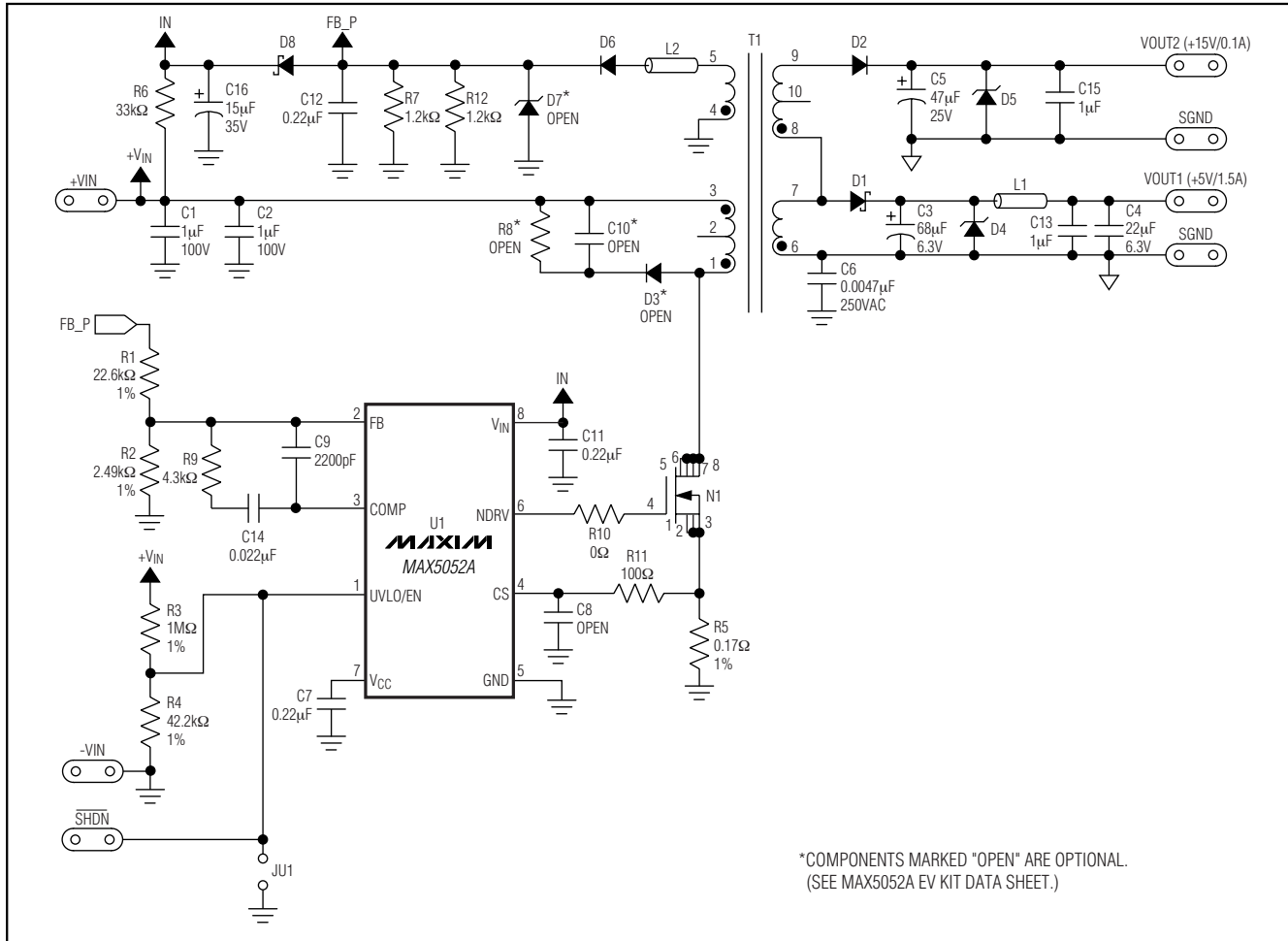


Figure 5. Primary Regulated, Dual-Output, Isolated Telecom Power Supply

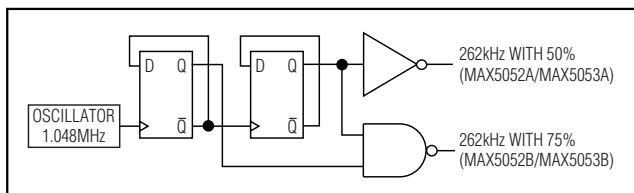


Figure 6. Internal Oscillator

## Internal Error Amplifier

The MAX5052/MAX5053 include an internal error amplifier that can be used to regulate the output voltage in the case of a nonisolated power supply (see Figure 1). Calculate the output voltage using the following equation:

$$V_{OUT} = \left(1 + \frac{R5}{R6}\right) V_{REF}$$

where  $V_{REF} = 1.23V$ . The amplifier's noninverting input is internally connected to a digital soft-start circuit that gradually increases the reference voltage during start-up and is applied to this pin. This forces the output voltage to come up in an orderly and well-defined manner under all load conditions.

The error amplifier may also be used to regulate the tertiary winding output which implements a primary-side regulated, isolated power supply (see Figure 5). Calculate the output voltage using the following equation:

$$V_{OUT1} = \frac{N_S}{N_T} \left[ \left(1 + \frac{R1}{R2}\right) V_{REF} + V_{D6} \right] - V_{D1}$$

where  $N_S$  is the number of secondary turns for  $V_{OUT1}$ ,  $N_T$  is the number of tertiary winding turns, and both  $V_{D6}$  and  $V_{D1}$  are the diode drops at the respective outputs.

# Current-Mode PWM Controllers with an Error Amplifier for Isolated/Nonisolated Power Supplies

## Current Limit

The current-sense resistor ( $R_{CS}$ ), connected between the source of the MOSFET and ground, sets the current limit. The CS input has a voltage-trip level ( $V_{CS}$ ) of 291mV. Use the following equation to calculate the value of  $R_{CS}$ :

$$R_{CS} = \frac{V_{CS}}{I_{PRI}}$$

Where  $I_{PRI}$  is the peak current in the primary that flows through the MOSFET.

When the voltage produced by this current (through the current-sense resistor) exceeds the current-limit comparator threshold, the MOSFET driver (NDRV) quickly terminates the current ON-cycle, typically within 60ns. In most cases, a small RC filter is required to filter out the leading-edge spike on the sense waveform. Set the corner frequency at a few megahertz.

## Applications Information

### Primary Regulated, Isolated Telecom Power Supply

Figure 5 shows a complete design of a dual-output power supply with a telecom voltage range of 36V to 72V. An important aspect of this power supply is its primary-side regulation. This regulation, through the tertiary winding, also acts as bias winding for the MAX5052.

In the circuit of Figure 5, cross-regulation has been improved (tertiary and 5V outputs) by using chip inductors, L1 and L2, and R7||R2. R7||R2 presents enough loading on the tertiary winding output to allow  $\pm 5\%$  load regulation on the 5V output over a load current range from 150mA to 1.5A.

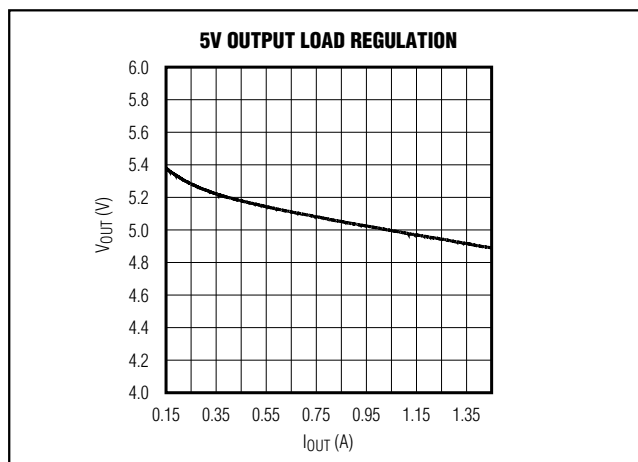


Figure 7. Output Voltage Regulation for the Figure 5 Circuit

## Layout Recommendations

All printed circuit board traces carrying switching currents must be kept as short as possible, and the current loops they form must be minimized. The pins of the  $\mu$ MAX package have been placed to allow easy interfacing to the external MOSFET.

For universal AC input design, all applicable safety regulations must be followed. Offline power supplies may require UL, VDE, and other similar agency approvals. These agencies can be contacted for the latest layout and component rules.

Typically there are two sources of noise emission in a switching power supply: high di/dt loops and high dv/dt surfaces. For example, traces that carry the drain current often form high di/dt loops. Similarly, the heatsink of the MOSFET presents a dv/dt source, thus the surface area of the heatsink must be minimized as much as possible.

To achieve best performance, a star ground connection is recommended to avoid ground loops. For example, the ground returns for the power-line input filter, power MOSFET switch, and sense resistor should be routed separately through wide copper traces to meet at a single-system ground connection.

## Chip Information

TRANSISTOR COUNT: 1449

PROCESS: BiCMOS

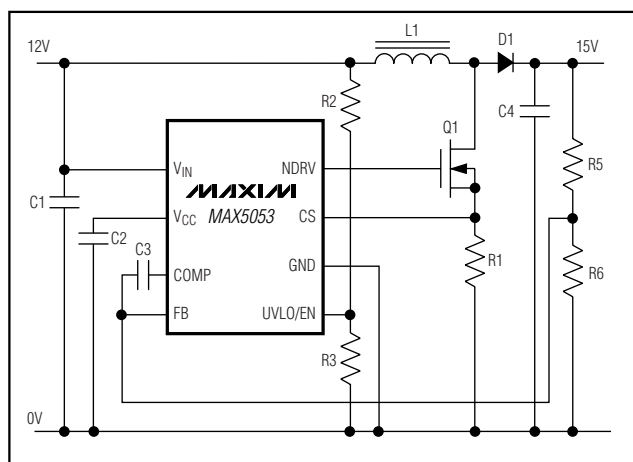
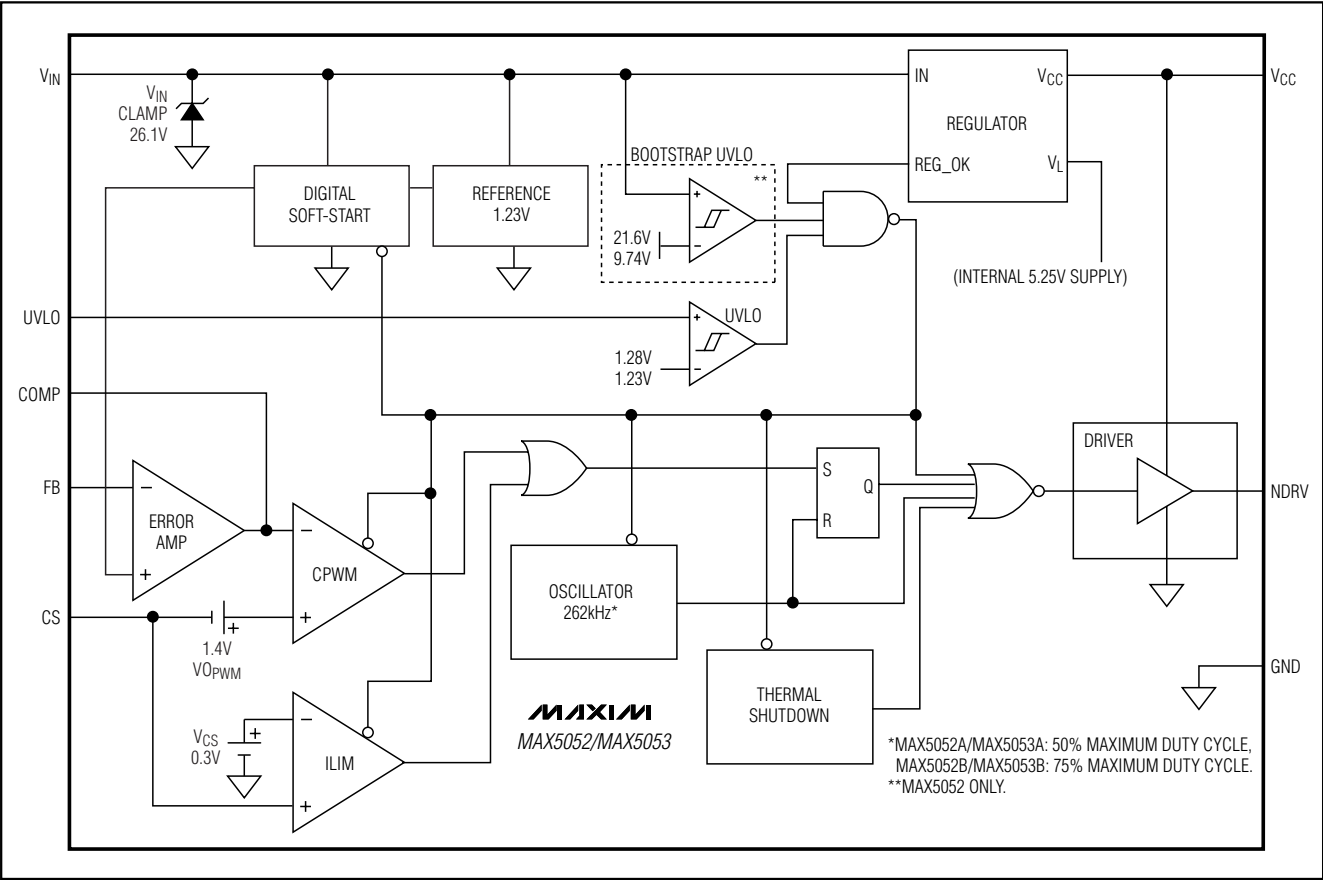


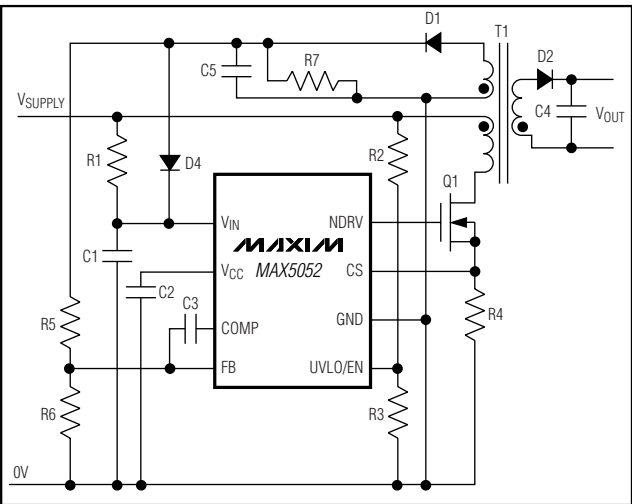
Figure 8. 12V to 15V Out Boost Regulator

# Current-Mode PWM Controllers with an Error Amplifier for Isolated/Nonisolated Power Supplies

Functional Diagram



Typical Operating Circuit



Selector Guide

PART	BOOTSTRAP UVLO	STARTUP VOLTAGE	MAX DUTY CYCLE
MAX5052A	Yes	22V	50%
MAX5052B	Yes	22 V	75%
MAX5053A	No	10.8V*	50%
MAX5053B	No	10.8V*	75%

\*The MAX5053 does not have an internal bootstrap UVLO. The MAX5053 starts operation as long as the VCC pin is higher than 7V (the guaranteed output with a VIN pin voltage of 10.8V) and the UVLO/EN pin is high.

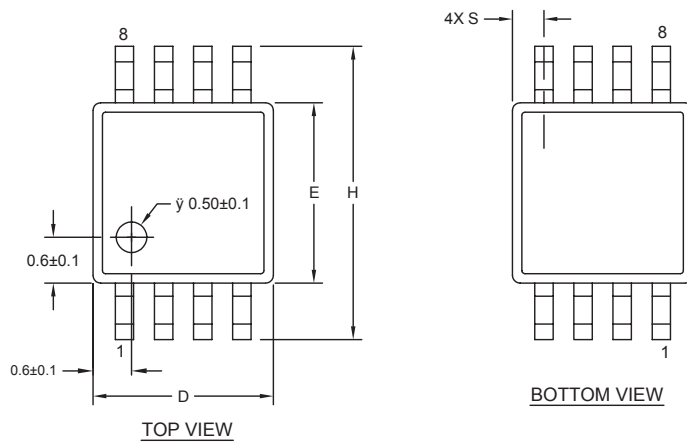
# Current-Mode PWM Controllers with an Error Amplifier for Isolated/Nonisolated Power Supplies

## Package Information

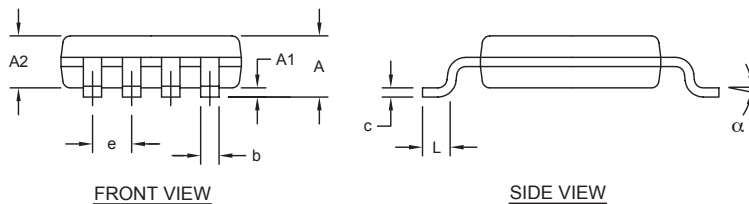
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

MAX5052/MAX5053

8LUMAXD.EPS



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°
S	0.0207 BSC		0.5250 BSC	



### NOTES:

1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-AA.

 <b>DALLAS</b> SEMICONDUCTOR			
PROPRIETARY INFORMATION			
TITLE:  PACKAGE OUTLINE, 8L uMAX/uSOP			
APPROVAL	DOCUMENT CONTROL NO.  21-0036	REV.  J	1/ 1

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