19-1424; Rev 0; 1/99

MAXIM

# Low-Voltage, High-Isolation, Dual 2-Channel RF/Video Multiplexer



## General Description

The MAX4589 low-voltage, dual 2-channel multiplexer is designed for RF and video signal processing at frequencies up to 200MHz in 50Ω and 75Ω systems. On-chip functions are controlled through either a parallel interface or an SPI™/QSPI™/MICROWIRE™ serial interface.

Each channel of the MAX4589 is designed using a "T" switch configuration, ensuring excellent high-frequency off-isolation. The MAX4589 has low on-resistance of 60Ω max, with an on-resistance match across all channels of 4Ω max. Additionally, on-resistance is flat across the specified signal range (2Ω max). The off-leakage current is under 1nA at $T_A$ = +25°C, and less than 10nA at $T_A$ = +85°C.

The MAX4589 operates from single +2.7V to +12V or dual ±2.7V to ±6V supplies. When operating with a positive supply of +5V, the inputs maintain TTL/CMOS-level compatibility. The MAX4589 is available in 20-pin DIP, wide SO, and SSOP packages.

## Applications

RF Switching

Video Signal Routing

High-Speed Data Acquisition

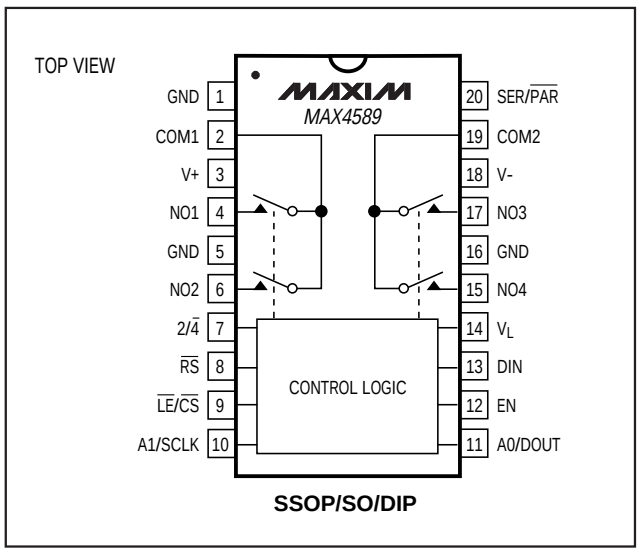
Automatic Test Equipment

Networking

## Features

- **Low Insertion Loss: < -2.5dB up to 100MHz**
- **High Off-Isolation: -74dB at 10MHz**
- **Low Crosstalk: < -70dB up to 10MHz**
- **20MHz -0.1dB Signal Bandwidth**
- **200MHz -3dB Signal Bandwidth**
- **60Ω (max) On-Resistance with ±5V Supplies**
- **4Ω (max) On-Resistance Matching with ±5V Supplies**
- **2Ω (max) On-Resistance Flatness with ±5V Supplies**
- **+2.7V to +12V Single-Supply Operation ±2.7V to ±6V Dual-Supply Operation**
- **Low Power Consumption: <20µW**
- **Rail-to-Rail®, Bidirectional Signal Handling**
- **Parallel or SPI/QSPI/MICROWIRE-Compatible Serial Interface**
- **>±2kV ESD Protection per Method 3015.7**
- **TTL/CMOS-Compatible Inputs with $V_L$ = +5V**

## Pin Configuration




**SSOP/SO/DIP**

## Ordering Information

| PART | TEMP. RANGE | PIN-PACKAGE |
|---|---|---|
| MAX4589CAP | 0°C to +70°C | 20 SSOP |
| MAX4589CWP | 0°C to +70°C | 20 Wide SO |
| MAX4589CPP | 0°C to +70°C | 20 Plastic DIP |
| MAX4589EAP | -40°C to +85°C | 20 SSOP |
| MAX4589EWP | -40°C to +85°C | 20 Wide SO |
| MAX4589EPP | -40°C to +85°C | 20 Plastic DIP |

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*Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.*

# Low-Voltage, High-Isolation, Dual 2-Channel RF/Video Multiplexer

## ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND)
V+ .....-0.3V to +13V
$V_L$ .....-0.3V to (V+ + 0.3V) or 7V (whichever is lower)
V- .....-13V to +0.3V
V+ to V-.....-0.3V to +13V
$V_{NO\_}$, $V_{COM\_}$ to GND (Note 1).....(V- - 0.3V) to (V+ + 0.3V)
2/$\overline{4}$, $\overline{RS}$, $\overline{LE}$, $\overline{CS}$, A1/SCLK, ____
A0/DOUT, EN, DIN, SER/$\overline{PAR}$ to GND .....-0.3V to (V+ + 0.3V)
Continuous Current into Any Terminal.....±20mA
Peak Current into Any Terminal
(pulsed at 1ms, 10% duty cycle).....±40mA

ESD per Method 3015.7.....±2kV
Continuous Power Dissipation ($T_A$ = +70°C)
SSOP (derate 9.1mW/°C above +70°C).....727mW
Wide SO (derate 10mW/°C above +70°C).....800mW
Plastic DIP (derate 11.1mW/°C above +70°C) .....889mW
Operating Temperature Ranges
MAX4589C_ P.....0°C to +70°C
MAX4589E_ P.....-40°C to +85°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (soldering, 10sec).....+300°C

**Note 1:** Voltages on these pins exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current rating.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = $V_L$ = +4.5V to +5.5V, V- = -4.5V to -5.5V, $V_{INH}$ = +2.4V, $V_{INL}$ = +0.8V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C, V+ = $V_L$ = +5V, V- = -5V.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | $T_A$ | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| Analog Signal Range (Note 3) | $V_{COM\_}$, $V_{NO\_}$ | | | V- | | V+ | V |
| On-Resistance | $R_{ON}$ | V+ = 5V, V- = -5V, $V_{NO\_}$ = ±2V, $I_{COM\_}$ = 4mA | +25°C | | 40 | 60 | Ω |
| | | | C, E | | | 75 | |
| On-Resistance Match Between Channels (Note 4) | $\Delta R_{ON}$ | V+ = 5V, V- = 5V, $V_{NO\_}$ = ±2V, $I_{COM\_}$ = 4mA | +25°C | | 1 | 4 | Ω |
| | | | C, E | | | 5 | |
| On-Resistance Flatness (Note 5) | $R_{FLAT(ON)}$ | V+ = 5V; V- = -5V; $V_{NO\_}$ = 1V, 0, -1V; $I_{COM\_}$ = 4mA | +25°C | | 0.5 | 2.5 | Ω |
| | | | C, E | | | 3 | |
| NO_ Off-Leakage Current (Note 6) | $I_{NO\_(OFF)}$ | V+ = 5.5V, V- = -5.5V, $V_{COM\_}$ = ±4.5V, $V_{NO\_}$ = ∓4.5V | +25°C | -1 | 0.01 | 1 | nA |
| | | | C, E | -10 | | 10 | |
| COM_ Off-Leakage Current (Note 6) | $I_{COM\_(OFF)}$ | V+ = 5.5V, V- = -5.5V, $V_{COM\_}$ = ±4.5V, $V_{NO\_}$ = ∓4.5V | +25°C | -2 | 0.01 | 2 | nA |
| | | | C, E | -20 | | 20 | |
| COM_ On-Leakage Current (Note 6) | $I_{COM\_(ON)}$ | V+ = 5.5V, V- = -5.5V, $V_{COM\_}$ = ±4.5V, $V_{NO\_}$ = floating | +25°C | -2 | 0.01 | 2 | nA |
| | | | C, E | -20 | | 20 | |
| **LOGIC INPUTS (2/$\overline{4}$, $\overline{RS}$, $\overline{LE}$/$\overline{CS}$, A1/SCLK, AO/DOUT, EN, DIN, SER/$\overline{PAR}$)** | | | | | | | |
| Input Logic Threshold High | $V_{INH}$ | | C, E | 2.4 | 1.7 | | V |
| Input Logic Threshold Low | $V_{INL}$ | | C, E | | 1.5 | 0.8 | V |
| Input Threshold Hysteresis | | | | | 0.2 | | V |
| Input Current | $I_{IN}$ | $V_{IN\_}$ = 0 or $V_L$ | C, E | -1 | 0.03 | 1 | µA |

## ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = $V_L$ = +4.5V to +5.5V, V- = -4.5V to -5.5V, $V_{INH}$ = +2.4V, $V_{INL}$ = +0.8V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C, V+ = $V_L$ = +5V, V- = -5V.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | $T_A$ | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **LOGIC OUTPUT (SERIAL INTERFACE)** | | | | | | | | |
| DOUT Logic Low Output | $V_{OL}$ | $I_{SINK}$ = 3.2mA | | C, E | | | 0.4 | V |
| DOUT Logic High Output | $V_{OH}$ | $I_{SOURCE}$ = -1mA | | C, E | $V_L$ - 1 | | | V |
| **SWITCH DYNAMIC CHARACTERISTICS** | | | | | | | | |
| Turn-On Time | $t_{ON}$ | $V_{NO\_}$ = 3V, V+ = 4.5V, V- = -4.5V, Figure 1 | | +25°C | | 380 | 550 | ns |
| | | | | C, E | | | 600 | |
| Turn-Off Time | $t_{OFF}$ | $V_{NO\_}$ = 3V, V+ = 4.5V, V- = -4.5V, Figure 1 | | +25°C | | 150 | 300 | ns |
| | | | | C, E | | | 350 | |
| Break-Before-Make Time Delay (Note 3) | $t_{BBM}$ | $V_{NO\_}$ = 3V, V+ = 5.5V, V- = -5.5V, Figure 2 | | C, E | 10 | 180 | | ns |
| Charge Injection | Q | $C_L$ = 1.0nF, $V_{NO\_}$ = 0, $R_S$ = 0, Figure 3 | | +25°C | | 15 | | pC |
| NO_ Off-Capacitance | $C_{NO\_(OFF)}$ | $V_{NO\_}$ = 0, $f_{IN}$ = 1MHz, Figure 4 | | +25°C | | 2 | | pF |
| COM_ Off-Capacitance | $C_{COM\_(OFF)}$ | $V_{COM\_}$ = 0, $f_{IN}$ = 1MHz, Figure 4 | | +25°C | | 4 | | pF |
| COM_ On-Capacitance | $C_{COM\_(ON)}$ | $V_{COM\_}$ = 0, $f_{IN}$ = 1MHz, Figure 4 | | +25°C | | 6 | | pF |
| Off-Isolation (Note 7) | $V_{ISO}$ | $V_{NO\_}$ = 1$V_{RMS}$, f = 10MHz, all channels off, Figure 5 | | +25°C | | -74 | | dB |
| Channel-to-Channel Crosstalk | $V_{CT}$ | $V_{NO\_}$ = 1$V_{RMS}$, f = 10MHz, Figure 5 | | +25°C | | -70 | | dB |
| -3dB Bandwidth | BW | Figure 5 | 2-channel mode | +25°C | | 200 | | MHz |
| | | | 4-channel mode | | | 150 | | |
| -0.1dB Bandwidth | BW | Figure 5 | 2-channel mode | +25°C | | 20 | | MHz |
| | | | 4-channel mode | | | 15 | | |
| **PARALLEL-INTERFACE TIMING** | | | | | | | | |
| A_, EN to $\overline{LE}$ Rise Setup Time | $t_{DS}$ | Figure 6 | | C, E | 80 | | | ns |
| A_, EN to $\overline{LE}$ Rise Hold Time | $t_{DH}$ | Figure 6 | | C, E | 0 | | | ns |
| $\overline{LE}$ Low Pulse Width | $t_L$ | Figure 6 | | C, E | 80 | | | ns |
| $\overline{RS}$ Low Pulse Width | $t_{RS}$ | Figure 6 | | C, E | 80 | | | ns |
| **SERIAL-INTERFACE TIMING** | | | | | | | | |
| Operating Frequency | $f_{CLK}$ | Figure 7 | | C, E | | | 6.25 | MHz |
| SCLK Pulse Width High | $t_{CH}$ | Figure 7 | | C, E | 80 | | | ns |
| SCLK Pulse Width Low | $t_{CL}$ | Figure 7 | | C, E | 80 | | | ns |
| DIN to SCLK Rise Setup Time | $t_{DS}$ | Figure 7 | | C, E | 60 | | | ns |
| DIN to SCLK Rise Hold Time | $t_{DH}$ | Figure 7 | | C, E | 0 | | | ns |

# Low-Voltage, High-Isolation, Dual 2-Channel RF/Video Multiplexer

## ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = $V_L$ = +4.5V to +5.5V, V- = -4.5V to -5.5V, $V_{INH}$ = +2.4V, $V_{INL}$ = +0.8V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C, V+ = $V_L$ = +5V, V- = -5V.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | $T_A$ | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $\overline{CS}$ Fall to SCLK Rise Setup Time | $t_{CSS0}$ | Figure 7 | C, E | 50 | | | ns |
| $\overline{CS}$ Fall to SCLK Rise Hold Time | $t_{CSS1}$ | Figure 7 | C, E | 80 | | | ns |
| $\overline{CS}$ Rise to SCLK Rise Hold Time | $t_{CSH1}$ | Figure 7 | C, E | 0 | | | ns |
| $\overline{CS}$ Rise to SCLK Rise Setup Time | $t_{CSS1}$ | Figure 7 | C, E | 80 | | | ns |
| SCLK Rise to DOUT Valid | $t_{DO}$ | $C_L$ = 50pF, Figure 7 | C, E | | | 150 | ns |
| $\overline{RS}$ Low Pulse Width | $t_{RS}$ | Figure 6 | C, E | 80 | | | ns |
| **POWER SUPPLY** | | | | | | | |
| Power-Supply Range | V+, V- | | | ±2.7 | | ±6 | V |
| | $V_L$ | | | +2.7 | | V+ | |
| V+ Supply Current | I+ | V- = -5.5V, V+ = 5.5V | +25°C | -1 | 0.0001 | 1 | µA |
| | | | C, E | -10 | | 10 | |
| V- Supply Current | I- | V- = -5.5V, V+ = 5.5V | +25°C | -1 | 0.0001 | 1 | µA |
| | | | C, E | -10 | | 10 | |
| $V_L$ Supply Current | $I_L$ | $V_L$ = 5.5V, all $V_{IN\_}$ = 0 or $V_L$ | C, E | -10 | 2 | 10 | µA |

## ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = $V_L$ = +4.5V to +5.5V, V- = 0, $V_{INH}$ = +2.4V, $V_{INL}$ = +0.8V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C, V+ = $V_L$ = +5V.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | $T_A$ | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| Analog Signal Range (Note 3) | $V_{COM\_}$, $V_{NO}$ | | | 0 | | V+ | V |
| On-Resistance | $R_{ON}$ | V+ = 5V, $V_{NO\_}$ = 3V, $I_{COM\_}$ = 4mA | +25°C | | 80 | 120 | Ω |
| | | | C, E | | | 150 | |
| On-Resistance Match Between Channels (Note 4) | $\Delta R_{ON}$ | V+ = 5V, $V_{NO\_}$ = 3V, $I_{COM\_}$ = 4mA | +25°C | | 1 | 8 | Ω |
| | | | C, E | | | 10 | |
| On-Resistance Flatness (Note 5) | $R_{FLAT(ON)}$ | V+ = 5V; $I_{COM\_}$ = 4mA; $V_{NO\_}$ = 2V, 3V, 4V | +25°C | | 4 | 10 | Ω |
| | | | C, E | | | 12 | |
| NO_ Off-Leakage Current (Notes 6, 8) | $I_{NO\_(OFF)}$ | V+ = 5.5V; $V_{COM\_}$ = 4.5V, 1V; $V_{NO\_}$ = 1V, 4.5V | +25°C | -1 | 0.005 | 1 | nA |
| | | | C, E | -10 | | 10 | |
| COM_ Off-Leakage Current (Notes 6, 8) | $I_{COM\_(OFF)}$ | V+ = 5.5V; $V_{COM\_}$ = 4.5V, 1V; $V_{NO\_}$ = 1V, 4.5V | +25°C | -2 | 0.005 | 2 | nA |
| | | | C, E | -20 | | 20 | |
| COM_ On-Leakage Current (Notes 6, 8) | $I_{COM\_(ON)}$ | V+ = 5.5V; $V_{COM\_}$ = 4.5V 1V; $V_{NO\_}$ = 4.5V, 1V, or floating | +25°C | -2 | 0.005 | 2 | nA |
| | | | C, E | -20 | | 20 | |

## ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = $V_L$ = +4.5V to +5.5V, V- = 0, $V_{INH}$ = +2.4V, $V_{INL}$ = +0.8V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C, V+ = $V_L$ = +5V.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | $T_A$ | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **LOGIC INPUTS (2/$\overline{4}$, $\overline{RS}$, $\overline{LE}$/$\overline{CS}$, A1/SCLK, AO/DOUT, EN, DIN, SER/$\overline{PAR}$** | | | | | | | | |
| Input Logic Threshold High | $V_{INH}$ | | | C, E | 2.4 | 1.7 | | V |
| Input Logic Threshold Low | $V_{INL}$ | | | C, E | | 1.5 | 0.8 | V |
| Input Threshold Hysteresis | | | | | | 0.2 | | V |
| Input Current | $I_{IN}$ | $V_{IN}$ = 0 or $V_L$ | | C, E | -1 | | 1 | µA |
| **LOGIC OUTPUT (SERIAL INTERFACE)** | | | | | | | | |
| DOUT Logic Low Output | $V_{OL}$ | $I_{SINK}$ = 3.2mA | | C, E | | | 0.4 | V |
| DOUT Logic High Output | $V_{OH}$ | $I_{SOURCE}$ = -1mA | | C, E | $V_L$ - 1 | | | V |
| **SWITCH DYNAMIC CHARACTERISTICS** | | | | | | | | |
| Turn-On Time | $t_{ON}$ | $V_{NO\_}$ = 3V, V+ = 4.5V, Figure 1 | | +25°C | | 550 | 800 | ns |
| | | | | C, E | | | 900 | |
| Turn-Off Time | $t_{OFF}$ | $V_{NO\_}$ = 3V, V+ = 4.5V, Figure 1 | | +25°C | | 150 | 300 | ns |
| | | | | C, E | | | 350 | |
| Break-Before-Make Time Delay (Note 3) | $t_{BBM}$ | $V_{NO\_}$ = 3V, V+ = 5.5V, Figure 2 | | C, E | 10 | 200 | | ns |
| Charge Injection | Q | $C_L$ = 1.0nF, $V_{NO\_}$ = 2.5V, $R_S$ = 0, Figure 3 | | +25°C | | 5 | | pC |
| Off-Isolation | $V_{ISO}$ | $V_{NO\_}$ = $1V_{RMS}$, f = 10MHz, all channels off, Figure 5 | | +25°C | | -65 | | dB |
| Channel-to-Channel Crosstalk | $V_{CT}$ | $V_{NO\_}$ = $1V_{RMS}$, f = 10MHz, Figure 5 | | +25°C | | -70 | | dB |
| -3dB Bandwidth | BW | Figure 5 | 2-channel mode | +25°C | | 100 | | MHz |
| | | | 4-channel mode | | | 75 | | |
| -0.1dB Bandwidth | BW | Figure 5 | 2-channel mode | +25°C | | 10 | | MHz |
| | | | 4-channel mode | | | 7 | | |
| **PARALLEL-INTERFACE TIMING** | | | | | | | | |
| A_, EN to $\overline{LE}$ Rise Setup Time | $t_{DS}$ | Figure 6 | | C, E | 80 | | | ns |
| A_, EN to $\overline{LE}$ Rise Hold Time | $t_{DH}$ | Figure 6 | | C, E | 0 | | | ns |
| $\overline{LE}$ Low Pulse Width | $t_L$ | Figure 6 | | C, E | 80 | | | ns |
| $\overline{RS}$ Low Pulse Width | $t_{RS}$ | Figure 6 | | C, E | 80 | | | ns |

# Low-Voltage, High-Isolation, Dual 2-Channel RF/Video Multiplexer

## ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = $V_L$ = +4.5V to +5.5V, V- = 0, $V_{INH}$ = +2.4V, $V_{INL}$ = +0.8V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C, V+ = $V_L$ = +5V.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | $T_A$ | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **SERIAL-INTERFACE TIMING** | | | | | | | |
| Operating Frequency | $f_{CLK}$ | Figure 7 | C, E | | | 6.25 | ns |
| SCLK Pulse Width High | $t_{CH}$ | Figure 7 | C, E | 80 | | | ns |
| SCLK Pulse Width Low | $t_{CL}$ | Figure 7 | C, E | 80 | | | ns |
| DIN to SCLK Rise Setup Time | $t_{DS}$ | Figure 7 | C, E | 60 | | | ns |
| DIN to SCLK Rise Hold Time | $t_{DH}$ | Figure 7 | C, E | 0 | | | ns |
| $\overline{CS}$ Fall to SCLK Rise Setup Time | $t_{CSS0}$ | Figure 7 | C, E | 50 | | | ns |
| $\overline{CS}$ Rise to SCLK Rise Hold Time | $t_{CSH1}$ | Figure 7 | C, E | 0 | | | ns |
| $\overline{CS}$ Rise to SCLK Rise Setup Time | $t_{CSS1}$ | Figure 7 | C, E | 80 | | | ns |
| $\overline{CS}$ Fall to SCLK Rise Hold Time | $t_{CSS1}$ | Figure 7 | C, E | 80 | | | ns |
| SCLK Rise to DOUT Valid | $t_{DO}$ | $C_L$ = 50pF, Figure 7 | C, E | | | 150 | ns |
| $\overline{RS}$ Low Pulse Width | $t_{RS}$ | Figure 6 | C, E | 80 | | | ns |
| **POWER SUPPLY** | | | | | | | |
| Power-Supply Range | V+ | | | 2.7 | | 12 | V |
| | $V_L$ | V+ ≤ 6.5V | | 2.7 | | V+ | V |
| | | V+ > 6.5V | | 2.7 | | 6.5 | |
| V+ Supply Current | I+ | V+= 5.5V, $V_{IN}$ = 0 or $V_L$ | +25°C | -1 | | 1 | µA |
| | | | C, E | -10 | | 10 | |
| $V_L$ Supply Current | $I_L$ | $V_L$ = 5.5V, all $V_{IN\_}$ = 0 or $V_L$ | C, E | -10 | 2 | 10 | µA |

## ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = $V_L$ = +2.7V to +3.6V, V- = 0, $V_{INH}$ = +2V, $V_{INL}$ = +0.5V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C, V+ = $V_L$ = +3V.)

| PARAMETER | SYMBOL | CONDITIONS | $T_A$ | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| Analog Signal Range (Note 3) | $V_{COM\_}$,$V_{NO}$ | | | 0 | | V+ | V |
| On-Resistance | $R_{ON}$ | V+ = 2.7V, $V_{NO\_}$ = 1V, $I_{COM\_}$ = 1mA | +25°C | | 240 | 350 | Ω |
| | | | C, E | | | 450 | |
| **LOGIC INPUT (2/$\overline{4}$, $\overline{RS}$, $\overline{LE}$/$\overline{CS}$, A1/SCLK, AO/DOUT, EN, DIN, SER/$\overline{PAR}$** | | | | | | | |
| Input Logic Threshold High | $V_{INH}$ | | C, E | 2.0 | | | V |
| Input Logic Threshold Low | $V_{INL}$ | | C, E | | | 0.5 | V |
| Input Current | $I_{IN}$ | $V_{IN\_}$ = 0 or $V_L$ | C, E | -1 | | 1 | µA |
| **SWITCH DYNAMIC CHARACTERISTICS** | | | | | | | |
| Turn-On Time | $t_{ON}$ | $V_{NO\_\_}$ = 1.5V, V+ = 2.7V, Figure 1 | +25°C | | 700 | 1000 | ns |
| | | | C, E | | | 1200 | |
| Turn-Off Time | $t_{OFF}$ | $V_{NO\_\_}$ = 1.5V, V+ = 2.7V, Figure 1 | +25°C | | 250 | 400 | ns |
| | | | C, E | | | 500 | |
| Break-Before-Make Time Delay (Note 3) | $t_{BBM}$ | $V_{NO\_\_}$ = 1.5V, V+ = 3.6V, Figure 2 | C, E | 10 | 350 | | ns |

## ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = $V_L$ = +2.7V to +3.6V, V- = 0, $V_{INH}$ = +2V, $V_{INL}$ = +0.5V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C, V+ = $V_L$ = +3V.)

| PARAMETER | SYMBOL | CONDITIONS | $T_A$ | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **PARALLEL-INTERFACE TIMING** | | | | | | | |
| A_, EN to $\overline{LE}$ Rise Setup Time | $t_{DS}$ | Figure 6 | C, E | 200 | | | ns |
| A_, EN to $\overline{LE}$ Rise Hold Time | $t_{DH}$ | Figure 6 | C, E | 0 | | | ns |
| $\overline{LE}$ Low Pulse Width | $t_L$ | Figure 6 | C, E | 200 | | | ns |
| $\overline{RS}$ Low Pulse Width | $t_{RS}$ | Figure 6 | C, E | 80 | | | ns |
| **SERIAL-INTERFACE TIMING** | | | | | | | |
| Operating Frequency | $f_{CLK}$ | Figure 7 | C, E | | | 2.1 | MHz |
| SCLK Pulse Width High | $t_{CH}$ | Figure 7 | C, E | 200 | | | ns |
| SCLK Pulse Width Low | $t_{CL}$ | Figure 7 | C, E | 200 | | | ns |
| DIN to SCLK Rise Setup Time | $t_{DS}$ | Figure 7 | C, E | 100 | | | ns |
| DIN to SCLK Rise Hold Time | $t_{DH}$ | Figure 7 | C, E | 0 | | | ns |
| $\overline{CS}$ Fall to SCLK Rise Setup Time | $t_{CSS0}$ | Figure 7 | C, E | 100 | | | ns |
| $\overline{CS}$ Rise to SCLK Rise Hold Time | $t_{CSH1}$ | Figure 7 | C, E | 0 | | | ns |
| $\overline{CS}$ Rise to SCLK Rise Setup Time | $t_{CSS1}$ | Figure 7 | C, E | 200 | | | ns |
| $\overline{CS}$ Fall to SCLK Rise Hold Time | $t_{CSS1}$ | Figure 7 | C, E | 200 | | | ns |
| SCLK Rise to DOUT Valid | $t_{DO}$ | $C_L$ = 50pF, Figure 7 | C, E | | | 250 | ns |
| $\overline{RS}$ Low Pulse Width | $t_{RS}$ | Figure 6 | C, E | 80 | | | ns |
| **POWER SUPPLY** | | | | | | | |
| V+ Supply Current | I+ | V+ = 3.6V, $V_{IN}$ = 0 or $V_L$ | +25°C | -1 | | 1 | µA |
| | | | C, E | -10 | | 10 | |
| $V_L$ Supply Current | $I_L$ | $V_L$ = 3.6V, all $V_{IN}$ = 0 or $V_L$ | C, E | -10 | 1 | 10 | µA |

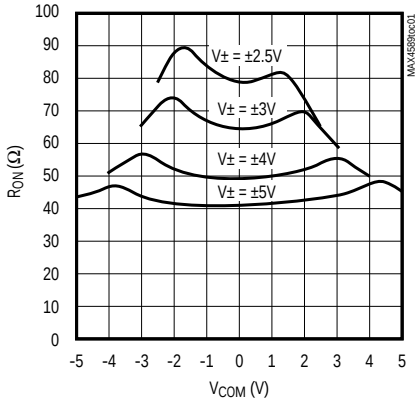
**Note 2:** The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
**Note 3:** Guaranteed by design.
**Note 4:** $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.
**Note 5:** Resistance flatness is defined as the difference between the maximum and the minimum value of on-resistance as measured over the specified analog-signal range.
**Note 6:** Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at $T_A$ = +25°C.
**Note 7:** Off-isolation = 20log10 [$V_{COM\_}$ / $V_{NO\_}$], $V_{COM\_}$ = output, $V_{NO\_}$ = input to off switch.
**Note 8:** Leakage testing for single-supply operation is guaranteed by testing with dual supplies.

# Low-Voltage, High-Isolation, Dual 2-Channel RF/Video Multiplexer

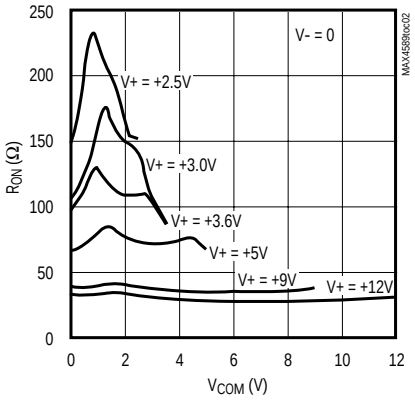
## Typical Operating Characteristics

(V+ = $V_L$ = +5V, V- = -5V, $T_A$ = +25°C, unless otherwise specified.)

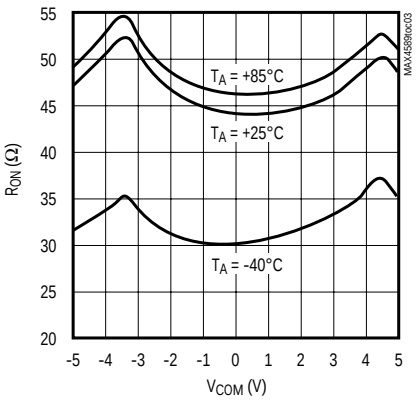
**ON-RESISTANCE vs. $V_{COM}$ (DUAL SUPPLIES)**



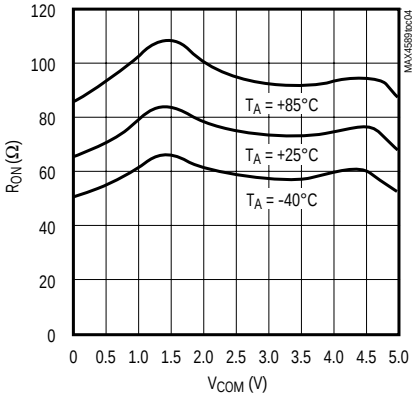

**ON-RESISTANCE vs. $V_{COM}$ (SINGLE SUPPLY)**



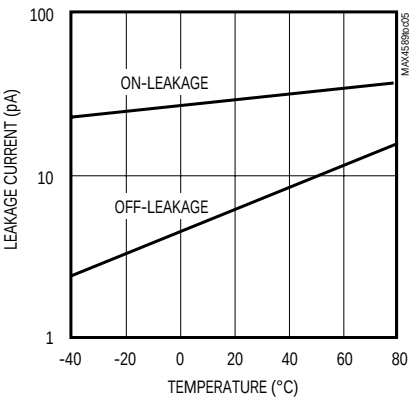

**ON-RESISTANCE vs. $V_{COM}$ AND TEMPERATURE (DUAL SUPPLIES)**



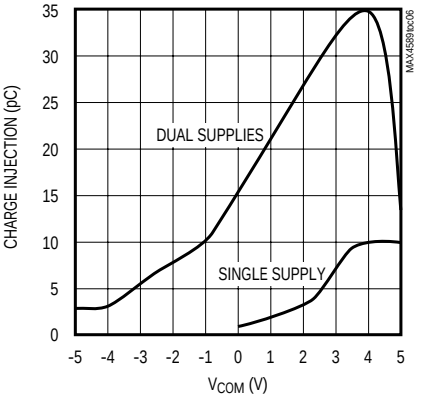

**ON-RESISTANCE vs. $V_{COM}$ AND TEMPERATURE (SINGLE SUPPLY)**



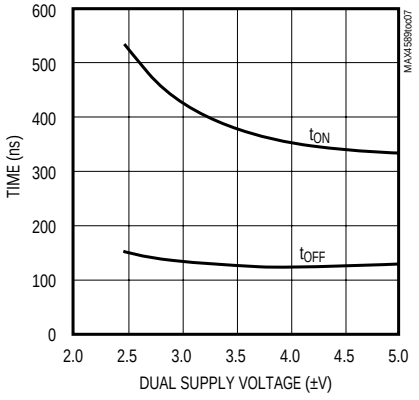

**ON/OFF-LEAKAGE CURRENT vs. TEMPERATURE**



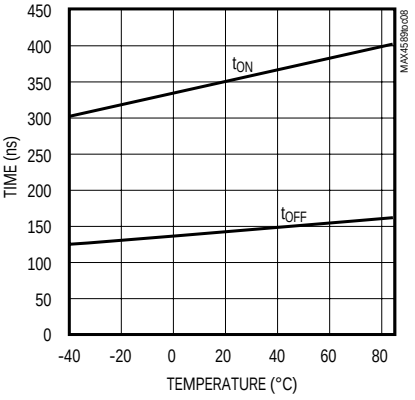

**CHARGE INJECTION vs. $V_{COM}$**



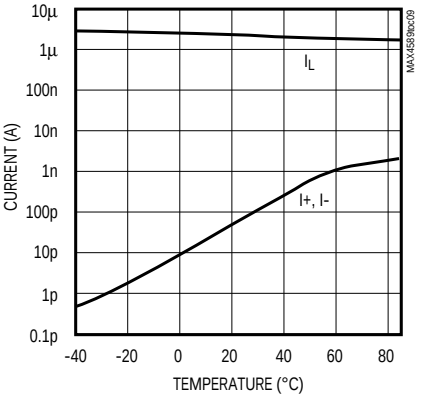

**$t_{ON}$, $t_{OFF}$ vs. SUPPLY VOLTAGE**




**$t_{ON}$, $t_{OFF}$ vs. TEMPERATURE**



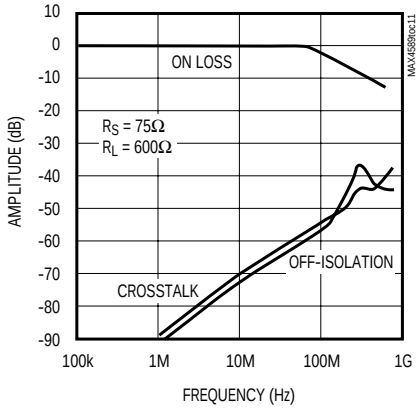

**POWER-SUPPLY CURRENT vs. TEMPERATURE**



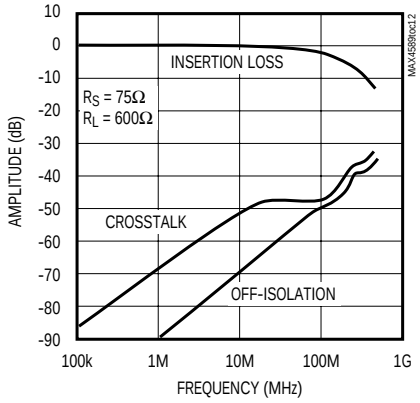
## Typical Operating Characteristics (continued)

(V+ = $V_L$ = +5V, V- = -5V, $T_A$ = +25°C, unless otherwise specified.)

**INSERTION LOSS, OFF-ISOLATION, AND CROSSTALK vs. FREQUENCY (DUAL SUPPLIES)**




**INSERTION LOSS, OFF-ISOLATION, AND CROSSTALK vs. FREQUENCY (SINGLE SUPPLY)**



# Low-Voltage, High-Isolation, Dual 2-Channel RF/Video Multiplexer

## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1, 5, 16 | GND | Ground. Connect to ground plane. See *Grounding* section. |
| 2 | COM1 | Analog Switch Common Terminal. See *Truth Tables*. |
| 3 | V+ | Analog Positive Supply Voltage Input |
| 4 | NO1 | Normally Open Analog Input Terminal. See *Truth Tables*. |
| 6 | NO2 | Normally Open Analog Input Terminal. See *Truth Tables*. |
| 7 | 2/$\overline{4}$ | Multiplexer Configuration Control. Connect to $V_L$ to select dual 2-channel mode. Connect to GND for single 4-channel multiplexer operation. See *Truth Tables*. |
| 8 | $\overline{RS}$ | Active-Low Reset Input. In serial mode, drive $\overline{RS}$ low to force the latches and shift registers to the power-on reset state and force all switches open. In parallel mode, drive $\overline{RS}$ low to force the latches to the power-on reset state and force switches open. See *Truth Tables*. |
| 9 | $\overline{LE}$/$\overline{CS}$ | In parallel mode this pin is the transparent Latch Enable. In the serial mode, this pin is the Chip-Select input. See *Truth Tables*. |
| 10 | A1/SCLK | In parallel mode, A1/SCLK is the most significant address bit. If 2/$\overline{4}$ is high, A1/SCLK is ignored. In the serial mode, A1/SCLK is the serial shift clock input. Data is loaded on the rising edge of SCLK. See *Truth Tables*. |
| 11 | A0/DOUT | In parallel mode, this pin is the least significant address bit. In serial mode, DOUT is the output from the internal 4-bit shift register. DOUT is intended for daisy-chain cascading. DOUT is not three-stated by $\overline{CS}$. See *Serial Operation*. |
| 12 | EN | Switch Enable. Drive EN low to force all channels off. Drive high to allow normal multiplexer operation. Operates asynchronously in serial mode. In parallel mode, EN is latched when the $\overline{LE}$ signal is high. |
| 13 | DIN | Serial Data Input. In serial mode, data is loaded on the rising edge of SCLK. Connect to $V_L$ or GND in parallel mode. |
| 14 | $V_L$ | Logic Supply Input. Powers the DOUT driver and other digital circuitry. $V_L$ sets both the input threshold levels and the output logic levels. |
| 15 | NO4 | Normally Open Analog Input Terminal. See *Truth Tables*. |
| 17 | NO3 | Normally Open Analog Input Terminal. See *Truth Tables*. |
| 18 | V- | Analog Negative Supply Voltage Input. Connect to GND for single-supply operation. |
| 19 | COM2 | Analog Switch Common Terminal. See *Truth Tables*. |
| 20 | SER/$\overline{PAR}$ | Interface Select Input. Drive low for parallel data interface operation. Drive high for serial data interface operation and to enable the DOUT driver. |

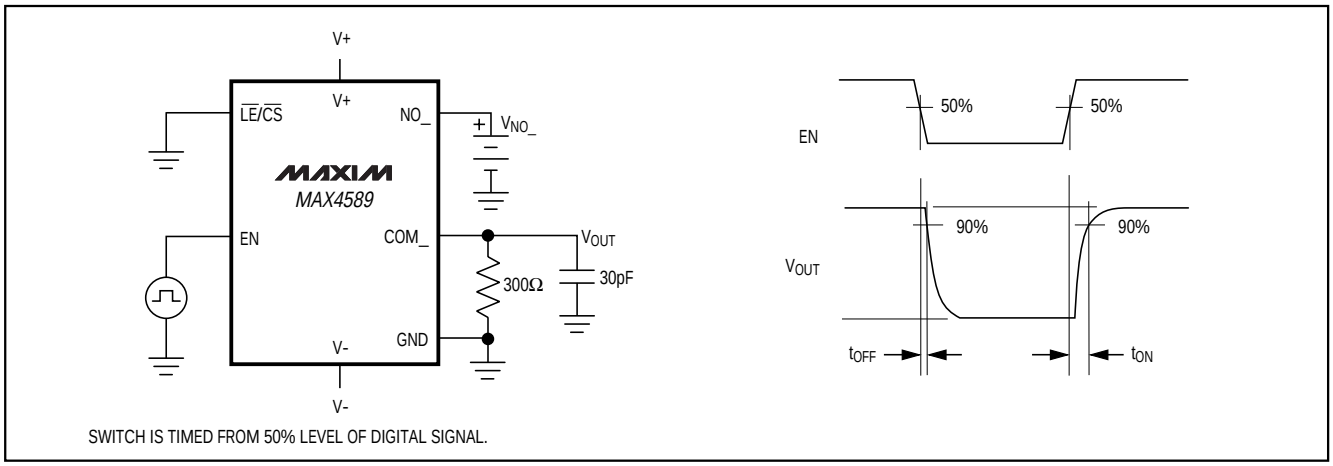



*Figure 1. Turn-On/Turn-Off Time*

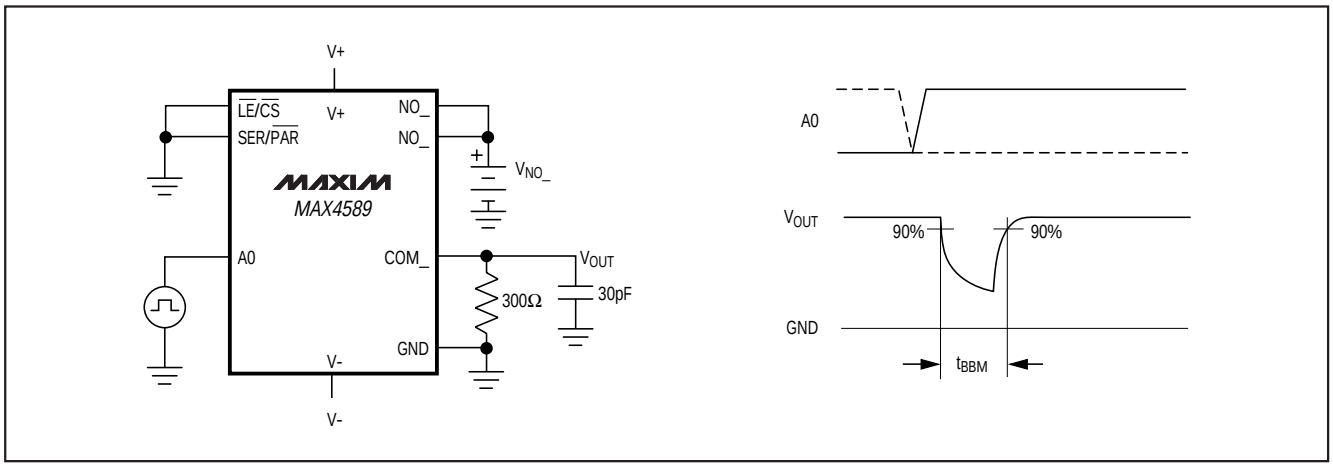



*Figure 2. Break-Before-Make Time Delay*

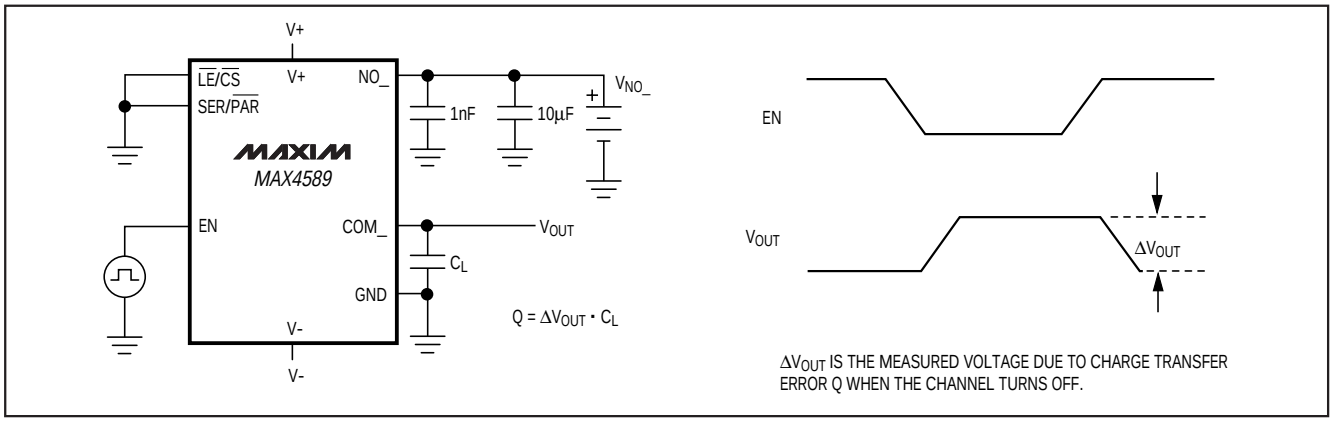



*Figure 3. Charge Injection*

# Low-Voltage, High-Isolation, Dual 2-Channel RF/Video Multiplexer

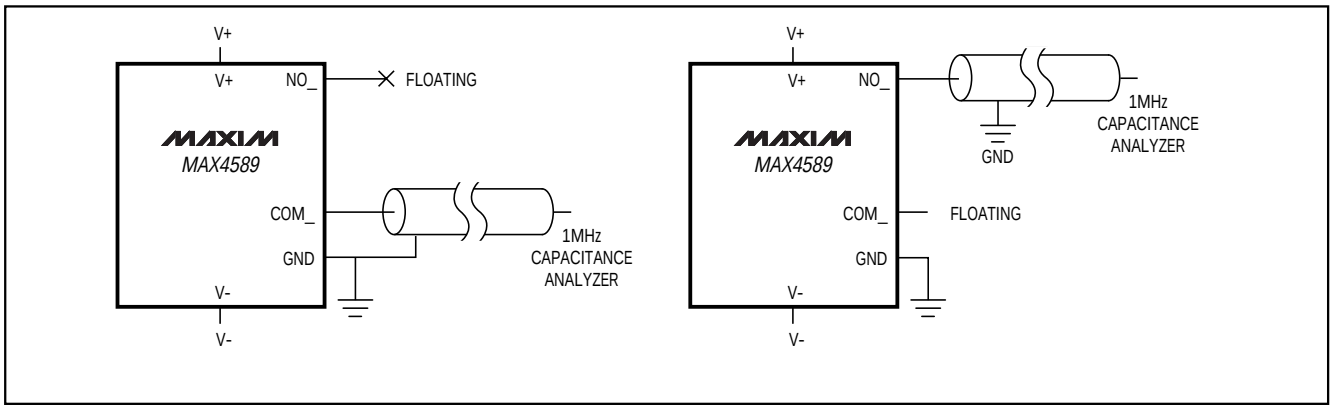



*Figure 4. NO_, COM_ Capacitance*

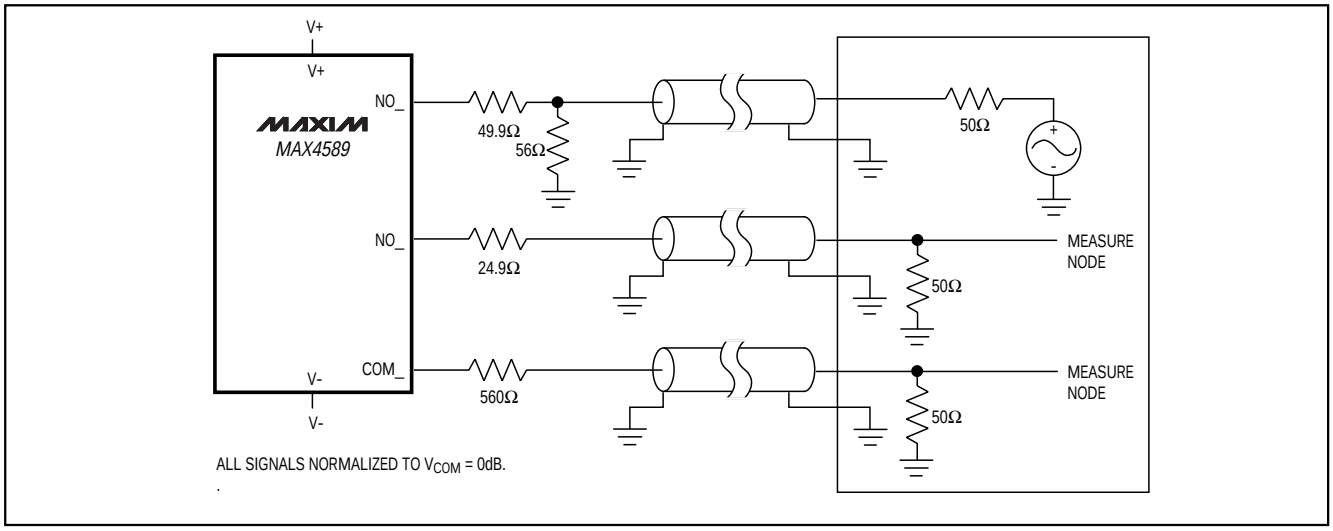



*Figure 5. Off-Isolation, Crosstalk, and Bandwidth*

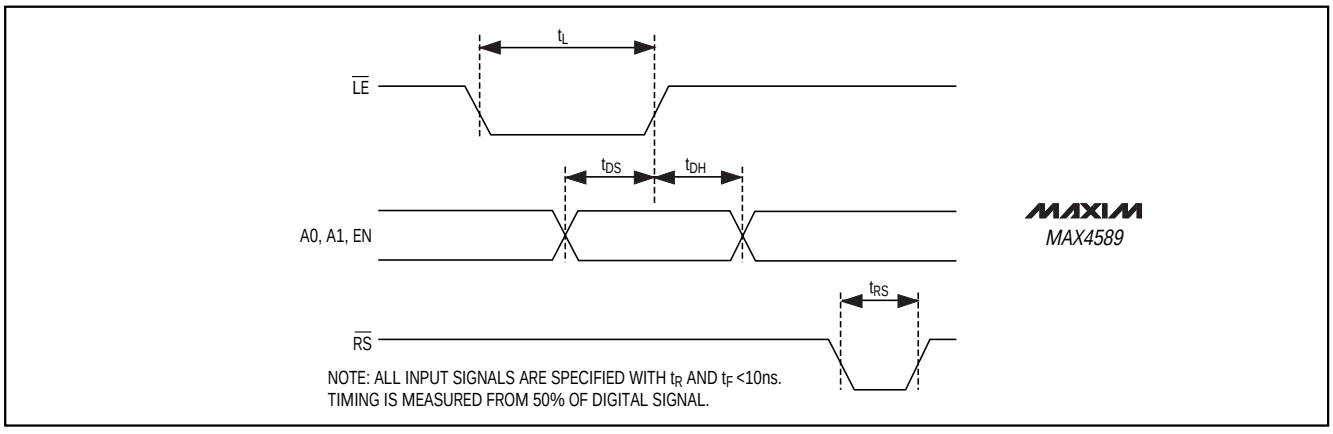



*Figure 6. Parallel Timing Diagram*

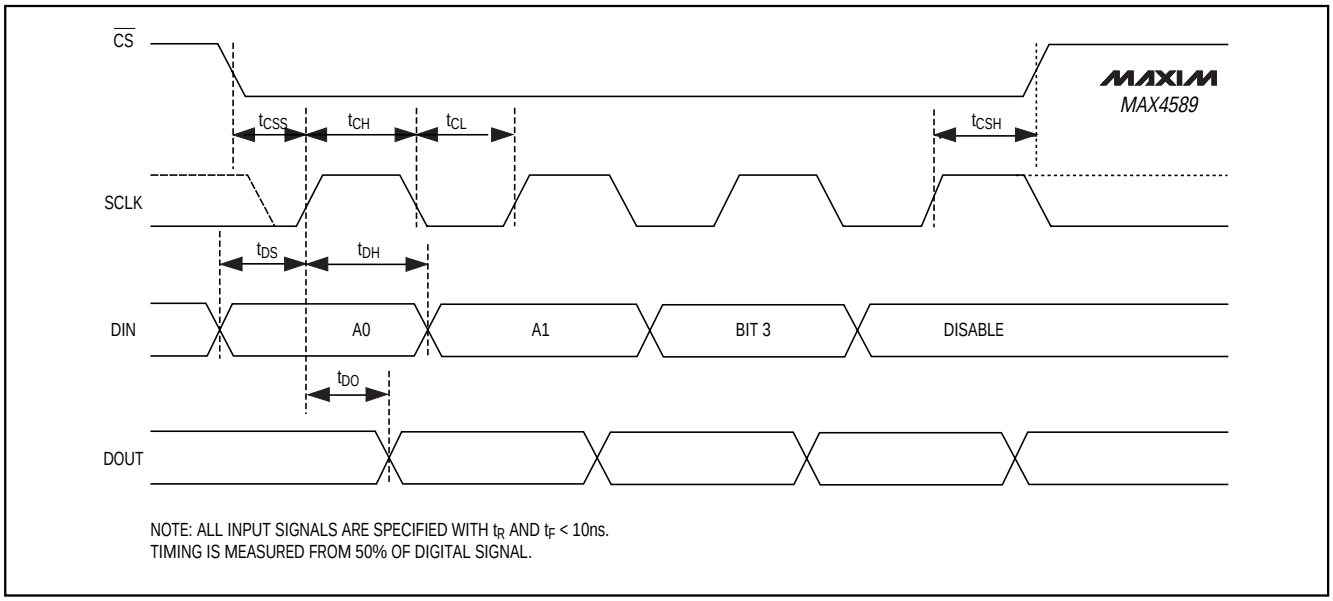



*Figure 7. Serial Timing Diagram*

## Detailed Description

### Logic-Level Translators

The MAX4589 is constructed of high-frequency "T" switches, as shown in Figure 8. The logic-level inputs are translated by amplifier A1 into a V+ to V- logic signal that drives the internal control logic. The internal control logic drives the gates of N-channel MOSFETs N1 and N2 from V+ to V-, turning them fully on or off. The same signal drives inverter A2 (which drives the P-channel MOSFETs P1 and P2, turning them fully on or off) from V+ to V-, and turns the N-channel MOSFET N3 on and off. The logic-level threshold is determined by $V_L$ and GND.

### Switch On Condition

When the switch is on, MOSFETs N1, N2, P1, and P2 are on and MOSFET N3 is off (Figure 8). The signal path is COM_ to NO_, and because both N-channel and P-channel MOSFETs act as pure resistances, it is symmetrical (i.e., signals pass in either direction). The off MOSFET, N3, has no DC conduction, but has a small amount of capacitance to GND. The MAX4589's construction allows an exceptional 200MHz -3dB bandwidth.

Frequency response in 75Ω systems is reasonably flat up to 50MHz, with typically 2.5dB of insertion loss. Higher-impedance circuits show even lower attenuation (and vice versa), but slightly lower bandwidth due to the increased effect of the internal and external capacitance and the switch's on-resistance.

The MAX4589 is optimized for ±5V operation. Using lower supply voltages or a single supply increases switching time, on-resistance (and therefore on-state attenuation), and nonlinearity.

### Switch Off Condition

When the switch is off, MOSFETs N1, N2, P1, and P2 are off and MOSFET N3 is on (Figure 8). The signal path is through the parasitic off-capacitances of N1, N2, P1, and P2, but it is shunted to ground by N3. This forms a highpass filter whose exact characteristics are dependent on the source and load impedances. In 75Ω systems, and below 1MHz, the attenuation exceeds 80dB. This value decreases with increasing frequency and increasing circuit impedances. External capacitance and board layout dominate overall performance.

# Low-Voltage, High-Isolation, Dual 2-Channel RF/Video Multiplexer

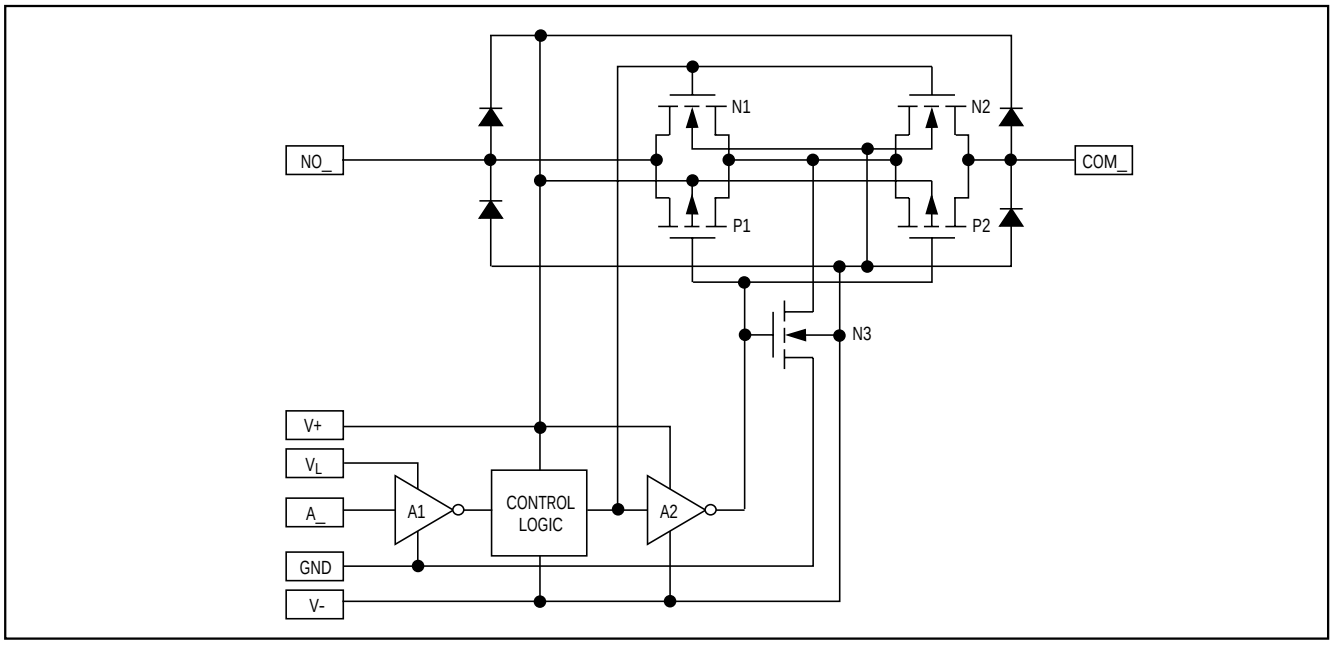



*Figure 8. T-Switch Construction*

## Applications Information

### Power-Supply Considerations

#### *Overview*

The MAX4589 construction is typical of many CMOS analog switches. It has four supply pins: V+, V-, $V_L$, and GND. V+ and V- are used to drive the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD-protection diodes are internally connected between each analog signal pin and both V+ and V-. If the voltage on any pin exceeds V+ or V-, one of these diodes conducts. During normal operation these reverse-biased ESD diodes leak, forming the only current drawn from V- and V+.

Virtually all the analog leakage current is through the ESD diodes. Although the ESD diodes on a given signal pin are identical, and therefore fairly well balanced, they are reverse-biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages vary as the signal varies. The difference in the two diode leakages from the signal path to the V+ and V- pins constitutes the analog signal-path leakage current. All analog leakage current flows to the supply terminals, not to the other switch terminal. This explains how both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog signal paths and GND. The analog signal paths consist of an N-channel and P-channel MOSFET with their sources and drains paralleled and their gates driven out of phase to V+ and V- by the logic-level translators.

$V_L$ and GND power the internal logic and logic-level translators, and set the input logic thresholds. The logic-level translators convert the logic levels to switched V+ and V- signals to drive the gates of the analog switches. Therefore, the gate-to-source and gate-to-drain impedances are the only connection between the logic supplies and the analog supplies.

#### *Bipolar-Supply Operation*

The MAX4589 operates with bipolar supplies between ±2.7V and ±6V. The V+ and V- supplies are not required to be symmetrical, but their sum cannot exceed the absolute maximum rating of 13.0V. **Do not connect the MAX4589 V+ pin to +3V and connect the logic-level input pins to TTL logic-level signals. This exceeds the absolute maximum ratings, and may cause damage to the part and/or external circuits.**

**CAUTION: The absolute maximum V+ to V- differential voltage is 13.0V. Typical "±6-Volt" or "12-Volt" supplies with ±10% tolerances can be as high as 13.2V. This voltage can damage the MAX4589. Even ±5% tolerance supplies may have overshoot or noise spikes that exceed 13.0V.**

### Single-Supply Operation

The MAX4589 operates from a single supply between +2.7V and +12V when V- is connected to GND. Observe all of the precautions listed in the *Bipolar-Supply Operation* section. Note, however, that these parts are optimized for ±5V operation, and AC and DC characteristics are degraded significantly when operating at less than ±5V. As the overall supply voltage (V+ to V-) is reduced, switching speed, on-resistance, off-isolation, and distortion are degraded (see *Typical Operating Characteristics*).

Single-supply operation also limits signal levels and interferes with grounded signals. When V- = GND, AC signals are limited to 300mV below GND. Voltages below this level are clipped by the internal ESD-protection diodes, and the parts can be damaged if excessive current flows.

### Power Off

When power to the MAX4589 is off (i.e., V+ = 0 and V- = 0), the *Absolute Maximum Ratings* still apply. This means that none of the MAX4589 pins can exceed ±0.3V. Voltages beyond ±0.3V cause the internal ESD-protection diodes to conduct, with potentially catastrophic consequences.

### Power-Supply Sequencing

When applying power to the MAX4589, follow this sequence: V+, V-, $V_L$, then logic inputs. Apply signals on the analog NO_ and COM_ pins any time after V+ and V- are set. Turning on all pins simultaneously is acceptable only if the circuit design guarantees concurrent power-up.

The power-down sequence is the opposite of the power-up sequence. That is, the $V_L$ and logic inputs must go to zero potential before (or simultaneously with) the V- then V+ supplies. Always observe the *Absolute Maximum Ratings* to ensure proper operation.

## Grounding

### DC Ground Considerations

Satisfactory high-frequency operation requires that careful consideration be given to grounding. **For most applications, a ground plane is strongly recommended and the GND pin must connect to it with solid copper.** While the V+ and V- power-supply pins are common to all switches in a given package, each input pair is separated with ground pins that are not internally connected to each other. This contributes to the overall high-frequency performance by reducing channel-to-channel crosstalk.

The digital inputs have voltage thresholds determined by $V_L$ and GND. (V- does not influence the logic-level threshold.) With $V_L$ = +5V and GND = 0, the threshold is about 1.6V, ensuring compatibility with TTL- and CMOS-logic drivers.

### AC Ground and Bypassing

**A ground plane is mandatory for satisfactory high-frequency operation.** Prototyping using hand wiring or wire-wrap boards is not recommended. Make the ground plane solid metal underneath the device, without interruptions. Avoid routing traces under the device itself. For DIP packages, this applies to both sides of a two-sided board. Failure to observe this has a minimal effect on the “on” characteristics of the switch at high frequencies, but it will degrade the off-isolation and crosstalk.

When using the SO package of the MAX4589 on PC boards with a buried ground plane, connect the GND pins to the ground plane with a separate via. Do not share this via with any other ground path. Providing a ground via on both sides of the SMT land further enhances the off-isolation by lowering the parasitic inductance. With the DIP package, connect the through-holes directly to the buried plane or thermally relieve them, as required, to meet manufacturability requirements. Again, do not use these through-hole pads as the current path for any other components.

Bypass the V+ and V- pins to the ground plane with surface-mount 0.1µF capacitors. Locate these capacitors as close as possible to the pins on the same side of the board as the device. Do not use feedthroughs or vias for bypass capacitors. If board layout dictates that the bypass capacitors are mounted on the opposite side of the PC board, use short feedthroughs or vias, directly under the V+ and V- pins. Use multiple vias if possible. If V- = GND, connect it directly to the ground plane with solid copper. Keep all traces short.

### Signal Routing

Keep all signal traces as short as possible. Separate all signal traces from each other, and keep them away from any other traces that could induce interference. Separating the signal traces with generously sized ground wires also helps minimize interference. Routing signals via coaxial cable, terminated as close to the MAX4589 as possible, provides the highest isolation.

### Board Layout

IC sockets degrade high-frequency performance and are not recommended if signal bandwidth exceeds 5MHz. Surface-mount parts, having shorter internal lead frames, provide the best high-frequency performance. Keep all bypass capacitors close to the device, and separate all signal leads with ground planes. Use

vias to connect the ground planes on each side of the board. Logic-level signal routing is not critical.

### Impedance Matching

The MAX4589 is intended for use in 75Ω systems, where the inputs are terminated external to the IC and the COM terminals are connected to an impedance of 600Ω or higher. The MAX4589 operates in 50Ω and 75Ω systems with terminations through the IC. However, variations in on-resistance and on-resistance flatness cause nonlinearities.

### Crosstalk and Off-Isolation

The graphs shown in the *Typical Operating Characteristics* for crosstalk and off-isolation are taken on adjacent channels. The adjacent channel is the worst-case condition. For example, NO1 has the worst off-isolation to COM1 due to its close proximity. Choosing channels wisely necessitates separating the most sensitive channels from the most offensive. Conversely, the above information also applies to the NO3 and NO4 inputs to the COM2 pin.

### Power-On Reset (POR)

The MAX4589 has internal circuitry to guarantee that all switches are off on power-up (POR). This is equivalent to the state resulting from asserting $\overline{RS}$ during normal operation.

### Serial Operation

The serial mode is activated by driving the SER/$\overline{PAR}$ input pin to a logic high. The data is then entered using a 4-bit SPI/MICROWIRE write operation. Systems that must write longer data streams can ignore all but the last four bits. Refer to Figure 7 for a detailed diagram of the serial-interface logic. The first bit loaded is A0, then A1, then an unused bit, followed by the disable bit.

There are four flip-flops in the input shift register. The output of the 4th shift register is output on DOUT on the rising edge of A1/SCLK. This allows cascading of multiple MAX4589s using only one chip-select line. For example, one 16-bit write programs the shift registers of four cascaded MAX4589s. The data from the shift register is moved to the internal control latches only upon the rising edge of $\overline{CS}$, so all four MAX4589s change state simultaneously. $\overline{RS}$ has the same effect as the internal power-on reset (POR) signal. The POR state is A0 = A1 = 0 and disable = 1.

In serial mode, 2/$\overline{4}$ is not used. Connect it to GND or $V_L$; do not leave 2/$\overline{4}$ unconnected.

### Parallel Operation

The parallel mode is activated by driving SER/$\overline{PAR}$ to a logic low. The MAX4589 is then programmed by a latched parallel bus scheme. Refer to Figure 6 for a detailed diagram of the parallel-interface logic. If 2/$\overline{4}$ is high, A1 is disabled and the MAX4589 is configured as a dual 1-of-2 multiplexer. If 2/$\overline{4}$ is low, the MAX4589 is configured as a 1-of-4 multiplexer. It is best to hard-wire 2/$\overline{4}$ to a known state for the desired mode of operation, or to use a dedicated microcontroller port pin.

## Truth Tables

### Parallel Operation

| SER/$\overline{PAR}$ | A1 | A0 | EN | $\overline{LE}$ | $\overline{RS}$ | 2/$\overline{4}$ | SWITCH STATES |
|---|---|---|---|---|---|---|---|
| 0 | x | x | x | 1 | 1 | x | Maintain previous state. |
| x | x | x | x | x | 0 | x | All switches off, latches are cleared. |
| 1 | x | x | x | x | 1 | x | Serial Mode. Refer to *Serial Operation Truth Table*. |
| 0 | x | x | 0 | 0 | 1 | x | All switches off. |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | Connect NO1 to COM1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | Connect NO2 to COM1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | Connect NO3 to COM2 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | Connect NO4 to COM2 |
| 0 | x | 0 | 1 | 0 | 1 | 1 | Connect NO1 to COM1and NO3 to COM2 |
| 0 | x | 1 | 1 | 0 | 1 | 1 | Connect NO2 to COM1and NO4 to COM2 |

*x = Don't Care.*

***Note:*** *2/$\overline{4}$ is not latched when $\overline{LE}$ is high. When $\overline{LE}$ is low, all latches are transparent. A1, A0 and EN are latched. Connect COM1 to COM2 externally for 1-of-4 single-ended operation.*

### Serial Operation

| SER/$\overline{PAR}$ | $\overline{CS}$ | SCLK | DIN | EN | $\overline{RS}$ | DOUT | SWITCH STATES |
|---|---|---|---|---|---|---|---|
| 1 | x | x | x | x | 0 | 0 | All switches off, latches and shift register are cleared. This is the Power-On Reset (POR) state. |
| 0 | x | x | x | x | x | High-Z | Parallel Mode. Refer to *Parallel Operation Truth Table*. |
| 1 | x | x | x | 0 | 1 | * | All switches off. |
| 1 | 1 | x | x | 1 | 1 | * | Chip unselected. |
| 1 | 0 | ⌐ | x | 1 | 1 | * | Input shift register loads one bit from DIN. DOUT updates on rising edge of SCLK. |
| 1 | ⌐ | x | x | 1 | 1 | * | Contents of shift register transferred to control latches. |

*x = Don't Care.*

**DOUT is delayed by 4 clock cycles from DIN.*

# Low-Voltage, High-Isolation, Dual 2-Channel RF/Video Multiplexer

## Truth Tables (continued)

### Control Bit and 2/$\overline{4}$ Logic

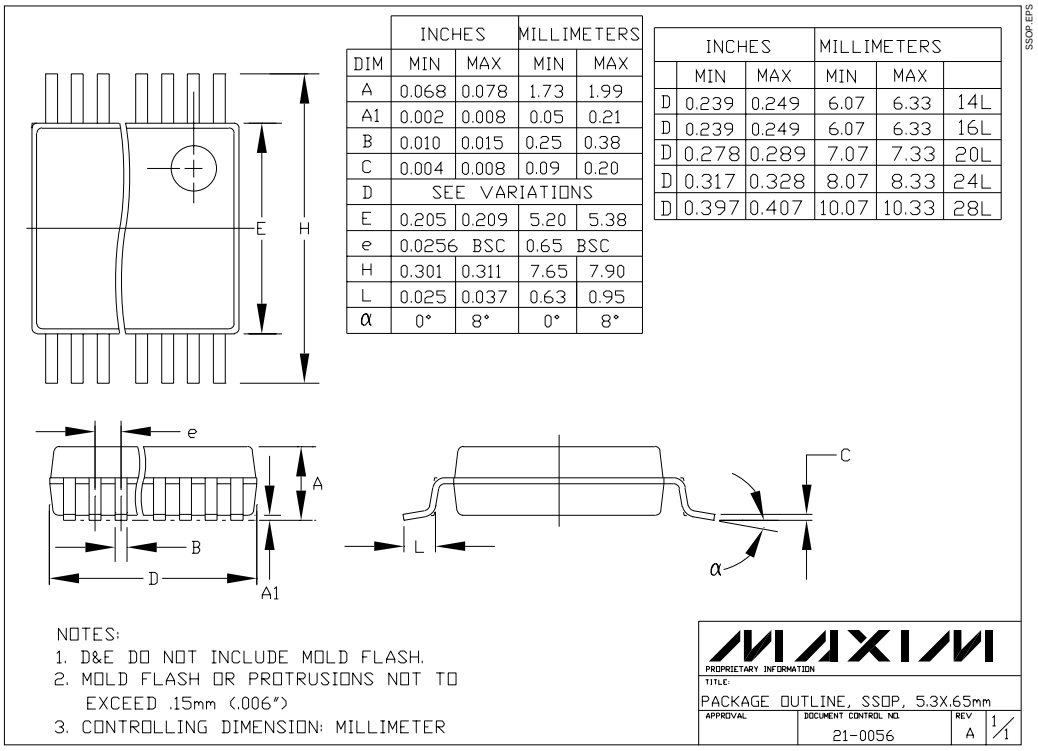
| DISABLE BIT | BIT 3 | A1 BIT | A0 BIT | 2/$\overline{4}$ PIN | SWITCH STATES |
|---|---|---|---|---|---|
| 1 | x | x | x | x | All switches off. |
| 0 | x | 0 | 0 | 0 | Connects NO1 to COM1 |
| 0 | x | 0 | 1 | 0 | Connects NO2 to COM1 |
| 0 | x | 1 | 0 | 0 | Connects NO3 to COM2 |
| 0 | x | 1 | 1 | 0 | Connects NO4 to COM2 |
| 0 | x | x | 0 | 1 | Connects NO1 to COM1 and NO3 to COM2 |
| 0 | x | x | 1 | 1 | Connects NO2 to COM1 and NO4 to COM2 |

*x = Don't Care.*

***Note:*** *A0, A1, BIT 3, and DISABLE are the 4 bits latched into the MAX4589 with a MICROWIRE/SPI write, respectively. A0 is the LSB (first bit clocked in), BIT 3 is not used, and DISABLE is the MSB (last bit clocked in).*

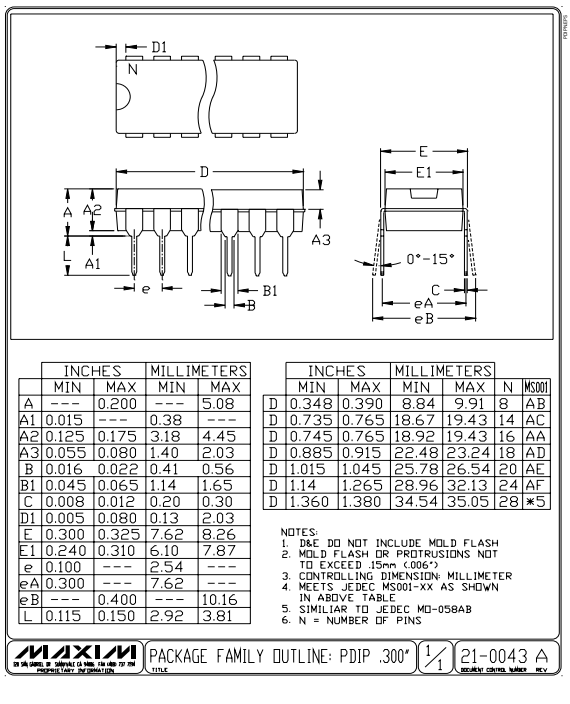
## Chip Information

TRANSISTOR COUNT: 853




| DIM | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX |
|---|---|---|---|---|
| A | 0.068 | 0.078 | 1.73 | 1.99 |
| A1 | 0.002 | 0.008 | 0.05 | 0.21 |
| B | 0.010 | 0.015 | 0.25 | 0.38 |
| C | 0.004 | 0.008 | 0.09 | 0.20 |
| D | SEE VARIATIONS | | | |
| E | 0.205 | 0.209 | 5.20 | 5.38 |
| e | 0.0256 BSC | | 0.65 BSC | |
| H | 0.301 | 0.311 | 7.65 | 7.90 |
| L | 0.025 | 0.037 | 0.63 | 0.95 |
| α | 0° | 8° | 0° | 8° |

| | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX | |
|---|---|---|---|---|---|
| D | 0.239 | 0.249 | 6.07 | 6.33 | 14L |
| D | 0.239 | 0.249 | 6.07 | 6.33 | 16L |
| D | 0.278 | 0.289 | 7.07 | 7.33 | 20L |
| D | 0.317 | 0.328 | 8.07 | 8.33 | 24L |
| D | 0.397 | 0.407 | 10.07 | 10.33 | 28L |




| | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX |
|---|---|---|---|---|
| A | --- | 0.200 | --- | 5.08 |
| A1 | 0.015 | --- | 0.38 | --- |
| A2 | 0.125 | 0.175 | 3.18 | 4.45 |
| A3 | 0.055 | 0.080 | 1.40 | 2.03 |
| B | 0.016 | 0.022 | 0.41 | 0.56 |
| B1 | 0.045 | 0.065 | 1.14 | 1.65 |
| C | 0.008 | 0.012 | 0.20 | 0.30 |
| D1 | 0.005 | 0.080 | 0.13 | 2.03 |
| E | 0.300 | 0.325 | 7.62 | 8.26 |
| E1 | 0.240 | 0.310 | 6.10 | 7.87 |
| e | 0.100 | --- | 2.54 | --- |
| eA | 0.300 | --- | 7.62 | --- |
| eB | --- | 0.400 | --- | 10.16 |
| L | 0.115 | 0.150 | 2.92 | 3.81 |

| | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX | N | MS001 |
|---|---|---|---|---|---|---|
| D | 0.348 | 0.390 | 8.84 | 9.91 | 8 | AB |
| D | 0.735 | 0.765 | 18.67 | 19.43 | 14 | AC |
| D | 0.745 | 0.765 | 18.92 | 19.43 | 16 | AA |
| D | 0.885 | 0.915 | 22.48 | 23.24 | 18 | AD |
| D | 1.015 | 1.045 | 25.78 | 26.54 | 20 | AE |
| D | 1.14 | 1.265 | 28.96 | 32.13 | 24 | AF |
| D | 1.360 | 1.380 | 34.54 | 35.05 | 28 | *5 |

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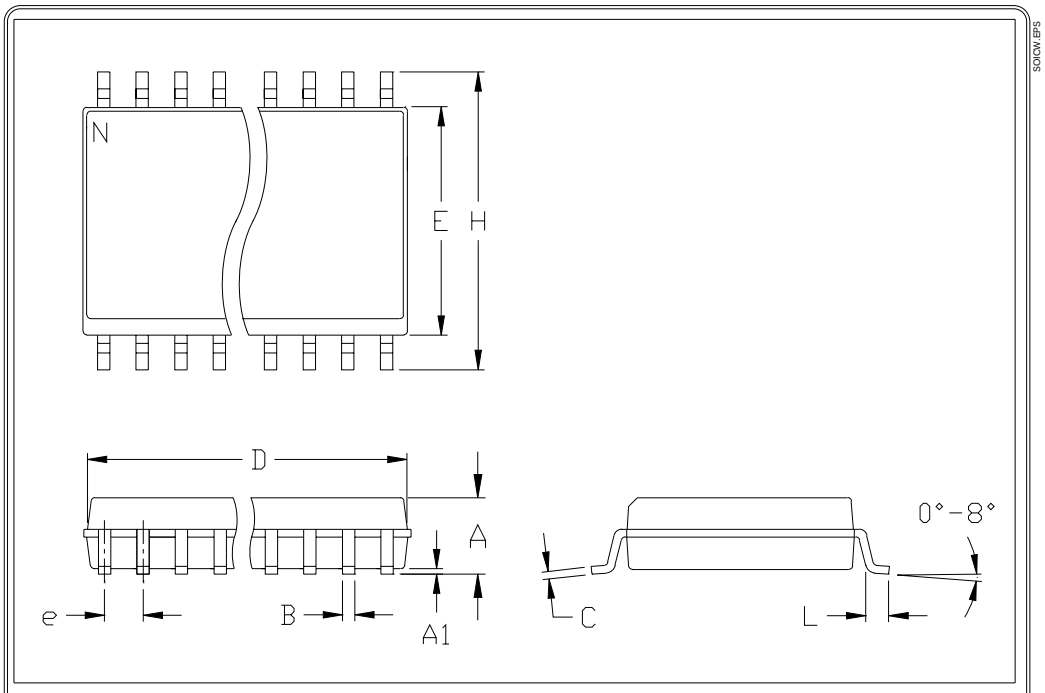
## Package Information (continued)




| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.093 | 0.104 | 2.35 | 2.65 |
| A1 | 0.004 | 0.012 | 0.10 | 0.30 |
| B | 0.014 | 0.019 | 0.35 | 0.49 |
| C | 0.009 | 0.013 | 0.23 | 0.32 |
| e | 0.050 | | 1.27 | |
| E | 0.291 | 0.299 | 7.40 | 7.60 |
| H | 0.394 | 0.419 | 10.00 | 10.65 |
| h | 0.010 | 0.030 | 0.25 | 0.75 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |

| | INCHES | | MILLIMETERS | | | |
|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | N | MS013 |
| D | 0.398 | 0.413 | 10.10 | 10.50 | 16 | AA |
| D | 0.447 | 0.463 | 11.35 | 11.75 | 18 | AB |
| D | 0.496 | 0.512 | 12.60 | 13.00 | 20 | AC |
| D | 0.598 | 0.614 | 15.20 | 15.60 | 24 | AD |
| D | 0.697 | 0.713 | 17.70 | 18.10 | 28 | AE |

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS013-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

| MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION | TITLE: PACKAGE FAMILY OUTLINE: SOIC .300" | 1/1 | DOCUMENT CONTROL NUMBER: 21-0042 A REV |
|---|---|---|---|

# Mouser Electronics

Authorized Distributor

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