*Click **here** to ask an associate for production status of specific part numbers.*

MAX22515 IO-Link Transceiver with Integrated Protection

General Description

The MAX22515 low-power industrial transceiver can operate as either an IO-Link device or an IO-Link master transceiver in industrial applications. The MAX22515 features a selectable control interface (pin mode or I^2C), two integrated linear regulators, and integrated surge protection for robust communication. The transceiver includes one C/Q input-output channel and one digital input (DI) channel.

The device features a flexible control interface. Pin-control logic inputs allow for operation with switching sensors that do not use a microcontroller. For sensors that use a microcontroller, an I^2C interface is available providing extensive configuration and diagnostics. Additionally, an integrated oscillator simplifies the clock generation for IO-Link devices.

The MAX22515 features extensive integrated protection to ensure robust communication in harsh industrial environments. All IO-Link line interface pins (V_{24}, C/Q, DI, and GND) are reverse voltage protected, short-circuit protected, hot-plug protected, and feature integrated ±1.2kV/500Ω surge protection.

The MAX22515 is available in a tiny WLP package (2.5mm x 2.0mm) or a 24-pin TQFN-EP package (4mm x 4mm) and operates over the -40ºC to +125ºC temperature range.

Applications

- IO-Link Sensor and Actuator Devices
- Industrial Sensors
- IO-Link Masters

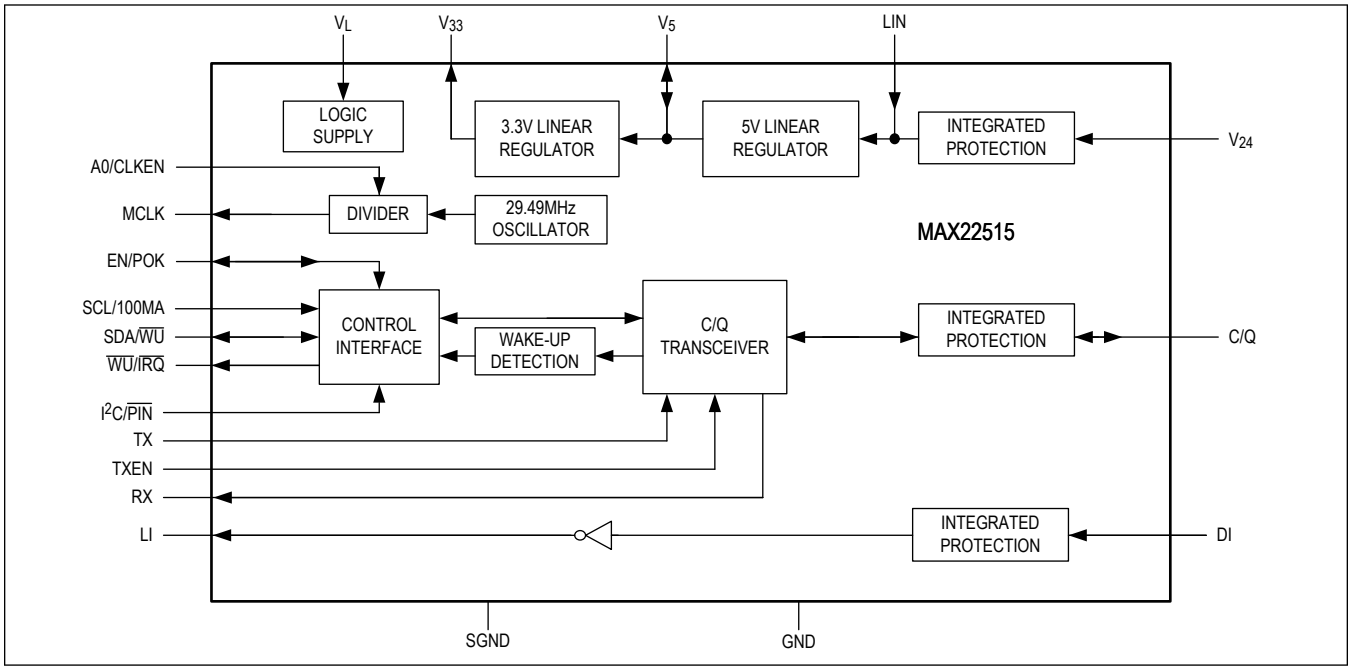
Benefits and Features

- High Configurability and Integration Reduces SKU
  - Operates from 8V to 36V
  - Auxiliary Digital Input (DI)
  - I^2C or Pin Mode Control
  - Selectable C/Q Driver Current: 50mA to 250mA
  - Selectable C/Q Driver Slew Rate (I^2C Mode)
  - Integrated Oscillator for IO-Link Communication
  - IO-Link Wake-Up Detection and Wake-Up
  - Generation
  - Integrated Linear Regulators: 3.3V and 5V
  - Compatible Register Set to MAX22513
  - Able to Communicate at COM1, COM2, and COM3 Data Rates
- Integrated Protection Enables Robust Systems
  - ±1.2kV/500Ω Surge Protection on V_{24}, C/Q, DI, and GND
  - Reverse Polarity Protection on V_{24}, C/Q, DI, and GND
  - Hot-Plug Protection on Supply Input (V_{24})
  - Glitch Filters for Improved Burst Resilience
  - Selectable Driver Overcurrent Configuration
  - -40°C to +125°C Operating Temperature Range
  - Fast Demagnetization of Inductive Loads
- Optimized for Small Designs
  - Low Power Dissipation: 2Ω (typ) C/Q Driver On-Resistance
  - 1.3mA (typ) Supply Current
  - Available in Two Tiny Packages:
    - 20-Bump WLP (2.5mm x 2.0mm)
    - 24-Pin TQFN-EP (4mm x 4mm)

***Ordering Information** appears at end of data sheet.*

19-100567; Rev 7; 4/21

Simplified Block Diagram



Absolute Maximum Ratings

All voltages referenced to GND, unless otherwise noted. .....
V_{24} (Continuous) ..... -36V to +36V
V_{24} (Peak, 100µs) ..... -52V to +65V
LIN (LIN is connected to V_{24}, Continuous)..... -36V to +36V
LIN (LIN is connected to V_{24}, Peak)..... -52V to +65V
LIN ..... max(-0.3V, V_5 - 0.3V) to V_{24}
C/Q (Continuous) ..... max(-36V, V_{24} - 36V) to min(+36V, (V_{24} + 36V)
C/Q (Peak, 100µs).....max(-52V, V_{24} - 52V) to min (+52V, V_{24} + 52V)
DI (Continuous) ..... -36V to +36V
DI (Peak, 100µs) ..... -52V to +52V
V_5, V_L ..... -0.3V to +6V
V_{33}.....-0.3V to (V_5 + 0.3V)
LOGIC PINS
I^2C/$\overline{PIN}$, EN/$\overline{POK}$, CLKEN, SCL/100MA,.....
SDA/$\overline{WU}$, $\overline{WU}$/$\overline{IRQ}$, TXEN, TX ..... -0.3V to +6V
MCLK, RX, LI ..... -0.3V to (V_L+0.3)V
SGND..... -0.3V to +0.3V
Continuous Current into V_{24} and GND .....±1A
Continuous Current into LIN .....±100mA
Continuous Current into C/Q.....±500mA
Continuous Current into V_5 and V_{33}.....±60mA
Continuous Current into Any Other Pin.....±50mA
Continuous Power Dissipation 24-Pin TQFN (T_A = +70ºC)
(derate at 27.8mW/ºC above +70ºC).....2222mW
20-bump WLP (T_A = +70ºC)
(derate at 21.35mW°/C above +70ºC).....1700mW
Operating Temperature Range .....-40ºC to +125ºC
Maximum Junction Temperature .....+160ºC
Storage Temperature Range .....-65ºC to +150ºC
Soldering Temperature (TQFN only, 10 sec).....+300ºC
Bump Reflow Temperature .....+260ºC

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

24 TQFN-EP

Package Code	T2444+4
Outline Number	21-0139
Land Pattern Number	90-0022
THERMAL RESISTANCE, SINGLE-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	48°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	3°C/W
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	36°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	3°C/W

20 (5 x 4) WLP

Package Code	W201L2+1
Outline Number	21-100314
Land Pattern Number	Refer to *Application Note 1891*
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	46.83°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics—DC

(V_{24} = 8V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, All logic inputs at V_L or GND, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS / POWER SUPPLY							
V_{24} Supply Voltage	V_{24}			8		36	V
V_{24} Undervoltage Lockout Threshold	V_{24UVLO}	V_{24} rising		6.9	7.5	8	V
		V_{24} falling		6.4	6.9	7.5	
V_{24} Undervoltage Lockout Threshold Hysteresis	V_{24UVLO_HYST}				500		mV
V_{24} Low Voltage Warning Threshold	V_{24_W}	V_{24} falling		14.5	15.3	16.3	V
V_{24} Supply Current	I_{24}	V_5 powered externally, no load on C/Q	C/Q is high impedance		16	30	µA
			C/Q is in push-pull and is high or low		285	400	
V_5 Supply Voltage	V_5	LIN = V_5, V_5 supplied externally		4.5		5.5	V
V_5 Undervoltage Lockout Threshold	V_{5UVLO}	V_5 rising				3.5	V
		V_5 falling		3			
V_5 Supply Current	I_5	LIN = V_5, V_5 is powered externally, no load on V_{33}, no load on C/Q	C/Q is high impedance, V_{33} is disabled, MCLK is disabled		560	850	µA
		LIN = V_5, V_5 is powered externally, no load on V_{33}, no load on C/Q	C/Q is in push-pull mode and is high or low, V_{33} is enabled, MCLK is disabled		1.08	1.5	mA
			C/Q is in push-pull mode and is high or low, V_{33} is enabled, MCLK is enabled		1.5	2.2	
V_L Logic Level Supply Voltage	V_L			2.5		5.5	V
V_L Undervoltage Threshold	V_{LUVLO}	V_L rising		0.5	0.85	1.2	V
V_L Logic Level Supply Current	I_{VL}	All logic inputs at GND or V_L, no load on any logic output	MCLK disabled		1	10	µA
			MCLK enabled, f = 29.49MHz		800		
			MCLK enabled, 10pF load on MCLK, V_L = 3.3V, f = 29.49MHz		1.56		mA
DC ELECTRICAL CHARACTERISTICS / 5V LINEAR REGULATOR (V_5)							
V_5 Input Supply Voltage	V_{LIN}			8		36	V
V_5 Output Voltage	V_5	8V ≤ V_{LIN} ≤ 36V, no load on V_5		4.9	5	5.1	V
V_5 Load Regulation	ΔV_{5_LDR}	V_{LIN} = 24V, 1mA ≤ I_{LOAD} ≤ 50mA			0.8	2	%

Electrical Characteristics—DC (continued)

(V_{24} = 8V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, All logic inputs at V_L or GND, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_5 Line Regulation	ΔV_{5_LNR}	8V ≤ V_{LIN} ≤ 36V, I_{LOAD} = 1mA			0.007	0.3	mV/V
V_5 Power Supply Rejection Ratio (PSRR)	$PSRR_{V5}$	f = 100kHz, I_{LOAD} = 20mA			-65		dB
V_5 Load Capacitance	C_{V5}	External capacitance required on V_5		0.8	1		µF
DC ELECTRICAL CHARACTERISTICS / 3.3V LINEAR REGULATOR (V_{33})							
V_{33} Output Voltage	V_{33}	No load		3.22	3.32	3.42	V
V_{33} Load Regulation	ΔV_{33_LR}	1mA ≤ I_{LOAD} ≤ 50mA			0.1	0.8	%
V_{33} Load Capacitance	C_{V33}	External capacitance required on V_{33}		0.8	1		µF
DC ELECTRICAL CHARACTERISTICS / C/Q DRIVER							
C/Q Driver On-Resistance	R_{OH}	High-side enabled, CL[1:0] = 11, I_{LOAD} = -200mA (Note 3)			2.65	4.6	Ω
	R_{OL}	Low-side enabled, CL[1:0] = 11, I_{LOAD} = +200mA (Note 3)			2.2	4.2	
C/Q Driver Current Limit	I_{CL}	V_{DROP} = 3V (Note 4)	CL[1:0] = 00	50	66	80	mA
			CL[1:0] = 01 (I^2C mode) or SDA/100MA = high (pin mode)	100	120	140	
			CL[1:0] = 10 (I^2C mode) or SDA/100MA = low (pin mode)	210	240	270	
			CL[1:0] = 11	260	300	340	
C/Q Leakage Current	I_{LEAK_CQ}	I^2C mode only, V_{24} = 24V, (V_{24} - 36V) ≤ $V_{C/Q}$ ≤ 36V, C/Q driver and receiver disabled (CQ_EN = 0, RXDIS = 1)		-40		+30	µA
		C/Q driver disabled (CQ_EN = 0), V_{24} = 24V, 0 ≤ $V_{C/Q}$ ≤ (V_{24} - 0.5V)		-2		+2	
C/Q Output Reverse Current	I_{REV_CQ}	C/Q driver enabled (TXEN = high, CQ_EN = 1) and in push-pull (CQ_PP = 1), $V_{C/Q}$ = (V_{24} + 5V) or (V_{GND} - 5V)		-90		+300	µA
C/Q Weak Pulldown Current	I_{PD}	I^2C mode only, $V_{C/Q}$ > 5V, TXEN = low, CQ_EN = 1, CQ_PD = 1, CQ_PU = 0 (Note 5)		+230	+320	+400	µA
C/Q Weak Pullup Current	I_{PU}	I^2C mode only,$V_{C/Q}$ = (V24 - 5V), TXEN = low, CQ_EN = 1, CQ_PD = 0, CQ_PU = 1 (Note 5)		-400	-300	-230	µA
DC ELECTRICAL CHARACTERISTICS / C/Q, DI RECEIVER							
Input Voltage Range	V_{IN}	For valid RX/LI logic		V_{24}-36		36	V
Input Threshold High	V_{TH}	TXEN = low	V_{24} ≥ 18V	10.8		12.5	V
			V_{24} < 18V	57.5		72	% of V_{24}

Electrical Characteristics—DC (continued)

(V_{24} = 8V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, All logic inputs at V_L or GND, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Threshold Low	V_{TL}	TXEN = low	$V_{24} \geq 18V$	8.8		10.5	V
			$V_{24} < 18V$	45		63	% of V_{24}
Input Hysteresis	V_{HYS}	TXEN = low	$V_{24} \geq 18V$		2		V
			$V_{24} < 18V$		11		% of V_{24}
C/Q Input Capacitance	C_{IN_CQ}	Driver disabled, CQ_EN = 0, RXDIS = 0, CQ_PD = 0, CQ_PU = 0, f = 100kHz			45		pF
DI Input Capacitance	C_{IN_DI}	DIDIS = 0, LIDIS = 0, f = 100kHz			4		pF
DI Input Current	I_{DI_IN}	V_{24} = 24V, DI receiver enabled, (V_{24} - 36V) ≤ V_{DI} ≤ 36V		-10		+15	µA
DC ELECTRICAL CHARACTERISTICS / LOGIC INPUTS (A0/CLKEN, SCL/100MA, SDA/$\overline{WU}$, TXEN, TX, I²C/$\overline{PIN}$, EN/POK)							
Logic Input Voltage Low	V_{IL}					0.2 x V_L	V
Logic Input Voltage High	V_{IH}			0.7 x V_L			V
Logic Input Leakage Current	I_{LEAK}	A0/CLKEN, SCL/100MA, SDA/$\overline{WU}$, TXEN, TX, I²C/$\overline{PIN}$, Logic input = GND or VL		-1		+1	µA
EN/POK Input Pullup Resistance	R_{PU}	EN/POK		60	100	140	kΩ
DC ELECTRICAL CHARACTERISTICS / LOGIC OUTPUTS ($\overline{WU}$/$\overline{IRQ}$, MCLK, SDA/$\overline{WU}$, RX, LI)							
Logic Output Voltage Low	V_{OL}	LI, RX, MCLK, SDA/$\overline{WU}$, I_{LOAD} = +5mA				0.15	V
Logic Output Voltage High	V_{OH}	LI, RX, MCLK, I_{LOAD} = -5mA		V_L - 0.2			V
Open-Drain High Impedance Leakage Current	I_{LK_OD}	$\overline{WU}$/$\overline{IRQ}$, output not asserted		-1		+1	µA
Logic Output Leakage Current	I_{LKG_OUT}	RX, LI, MCLK, DIDIS = 1, RXDIS = 1, MCLKDIS = 1, Logic output = GND or V_L		-1		+1	µA
SDA/WU Leakage Current	I_{LK_SDA}			-1		+1	µA
DC ELECTRICAL CHARACTERISTICS / THERMAL MANAGEMENT							
C/Q Driver Shutdown Temperature	T_{SHUT_D}	Driver temperature rising, C/Q driver fault bit is set and driver is disabled			+150		°C
C/Q Driver Shutdown Hysteresis	T_{SHUT_DHYS}	Driver temperature falling, C/Q driver is automatically reenabled			10		°C
IC Thermal Warning Threshold	T_{WRN}	Die temperature rising, THERMW and THERMWINT bits are set			+140		°C
IC Thermal Warning Threshold Hysteresis	T_{WRN_HYS}	Die temperature falling, THERMW bit is cleared			15		°C
IC Junction Thermal Shutdown Threshold	T_{SHUT_IC}	Die temperature rising			+160		°C
IC Junction Thermal Shutdown Hysteresis	T_{SHUT_ICHYS}	Die temperature falling			15		°C

Electrical Characteristics—AC

(V_{24} = 8V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, All logic inputs at V_L or GND, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS / C/Q DRIVER							
C/Q Driver Low-to-High Propagation Delay	t_{PDLH_PP}	CQSLEW[1:0] = 00, Figure 1	Push-pull or PNP mode		0.5	0.75	µs
	t_{PDLH_OC}		NPN mode		1		
C/Q Driver High-to-Low Propagation Delay	t_{PDHL_PP}	CQSLEW[1:0] = 00, Figure 1	Push-pull or NPN mode		0.45	0.75	µs
	t_{PDHL_OC}		PNP mode		1		
C/Q Driver Skew	t_{SKEW}	$\lvert t_{PDLH} - t_{PDHL} \rvert$, CQSLEW[1:0] = 00		-0.25	0.05	+0.25	µs
C/Q Driver Rise Time	t_{RISE}	Push-pull or PNP mode, V_{24}(max) = 30V, Figure 1	CQSLEW[1:0] = 00	0.05	0.15	0.3	µs
			CQSLEW[1:0] = 01 (I^2C mode) or when in pin mode	0	0.3	0.84	
			CQSLEW[1:0] = 10	0.45	0.9	1.4	
			CQSLEW[1:0] = 11	1.5	3.3	6	
C/Q Driver Fall Time	t_{FALL}	Push-pull or NPN mode, V_{24}(max) = 30V, Figure 1	CQSLEW[1:0] = 00	0.05	0.16	0.3	µs
			CQSLEW[1:0] = 01 (I^2C mode) or when in pin mode	0.15	0.33	0.5	
			CQSLEW[1:0] = 10	0.45	0.8	1.3	
			CQSLEW[1:0] = 11	1.5	3.3	6	
Difference in C/Q Rise and Fall Time		$\lvert t_{RISE} - t_{FALL} \rvert$, Push-pull mode, V_{24}(max) = 30V	CQSLEW[1:0] = 00		0.01		µs
			CQSLEW[1:0] = 01 (I^2C mode) or when in pin mode		0.03		
			CQSLEW[1:0] = 10		0.1		
			CQSLEW[1:0] = 11		0		
C/Q Driver Enable Time High	t_{ENH}	Push-pull or NPN configuration, Figure 2			0.5	0.75	µs
C/Q Driver Enable Time Low	t_{ENL}	Push-pull or PNP configuration, Figure 3			0.2	0.4	µs
C/Q Driver Disable Time High	t_{DISH}	Push-pull or NPN configuration, Figure 2			1.8		µs
C/Q Driver Disable Time Low	t_{DISL}	Push-pull or PNP configuration, Figure 3			1.8		µs
AC ELECTRICAL CHARACTERISTICS / C/Q, DI RECEIVER							
C/Q Receiver Low-to-High Propagation Delay	t_{PRLH_CQ}	Figure 4	RXFILTER = 1	0.85	1.35	1.8	µs
			RXFILTER = 0	0.25	0.38	0.55	
C/Q Receiver High-to-Low Propagation Delay	t_{PRHL_CQ}	Figure 4	RXFILTER = 1	0.85	1.28	1.8	µs
			RXFILTER = 0	0.2	0.3	0.5	
C/Q Receiver Skew		RXFILTER = 1			70		ns
		RXFILTER = 0			70		

Electrical Characteristics—AC (continued)

(V_{24} = 8V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, All logic inputs at V_L or GND, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DI Receiver Low-to-High Propagation Delay	t_{PRLH_DI}	Figure 4	DIFILTER = 1	1.2	1.8	2.4	µs
			DIFILTER = 0	0.6	0.9	1.2	
DI Receiver High-to-Low Propagation Delay	t_{PRHL_DI}	Figure 4	DIFILTER = 1	1.2	1.7	2.4	µs
			DIFILTER = 0	0.5	0.75	1.1	
AC ELECTRICAL CHARACTERISTICS / WAKE-UP DETECTION (Figure 5)							
Wake-Up Input Minimum Pulse Width	t_{WUMIN}	C_{LOAD} = 3nF		60	66	70	µs
Wake-Up Input Maximum Pulse Width	t_{WUMAX}	C_{LOAD} = 3nF		85	95	110	µs
SDA/$\overline{WU}$ (Pin mode), $\overline{WU}$/IRQ (I^2C Mode) Output Low Time	t_{WUL}	Valid wake-up condition on C/Q (Note 6)		150	200	250	µs
AC ELECTRICAL CHARACTERISTICS / WAKE-UP GENERATION (I^2C mode only, Figure 6)							
Setup Time before Wake-Up	t_{SU_WU}				80		µs
Wake-Up Pulse Duration	t_{WU}	Wake-up pulse has opposite polarity of the existing C/Q level		75	80	85	µs
On-Time after Wake-Up	t_{ON_WU}	C/Q driver enabled with original polarity after t_{WU}			2		µs
High Impedance Time after Wake-Up	t_{DIS_WU}	C/Q driver is high impedance after t_{ON_WU}			418		µs
C/Q Driver Current Limit During Wake-Up Pulse	I_{WU}	WURQ = 1, CLDIS = 0 or 1		500			mA
AC ELECTRICAL CHARACTERISTICS / MCLK CLOCK TIMING							
MCLK Frequency	f_{MCLK}	CLKDIV[2:0] = 000		3.612	3.686	3.761	MHz
		CLKDIV[2:0] = 001		7.225	7.373	7.523	
		CLKDIV[2:0] = 010		14.45	14.74	15.05	
		CLKDIV[2:0] = 011		28.90	29.49	30.09	
		CLKDIV[2:0] = 100		1.806	1.843	1.881	
MCLK Duty Cycle	D_{MCLK}				50		%
AC ELECTRICAL CHARACTERISTICS / I^2C TIMING SPECIFICATIONS (Figure 7)							
Maximum I^2C Clock Frequency	f_{I2CCLK}					2	MHz
Maximum Clock Period	t_{SCLMAX}			100			µs
Bus Free Time Between STOP and START Condi- tions	t_{I2CBUF}			0.16			µs
START Condition Setup Time	$t_{I2CSUSTA}$			0.05			µs
Repeat START Condition Setup Time	$t_{I2CSUSTA}$	90% to 90%		0.05			µs
START Condition Hold Time	$t_{I2CHDSTA}$	10% of SDA/WU to 90% of SCL/100MA		0.09			µs

Electrical Characteristics—AC (continued)

(V_{24} = 8V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, All logic inputs at V_L or GND, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STOP Condition Setup Time	$t_{I2CSUSTO}$	90% of SCL/100MA to 10% of SDA/WU	0.05			µs
Clock Low Period	t_{I2CLOW}	10% to 10%	0.12			µs
Clock High Period	$t_{I2CHIGH}$	90% to 90%	0.18			µs
Data Valid to SCL/ 100MA Rise Time	$t_{I2CSUDAT}$	Write Setup Time	50			ns
Data Hold Time	$t_{I2CHDDAT}$	Write Hold Time			0	ns
Maximum SDA/$\overline{WU}$ Drive Low Time	t_{DATLOW}		1.0	1.1	1.2	ms
ESD AND EMC TOLERANCE						
ESD Protection (V_{24}, C/Q, DI Pins)		IEC 61000-4-2 Contact Discharge, 500pF load on C/Q, 1.5kΩ in series with DI		±4		kV
ESD Protection (All Other Pins)		Human Body Model		±2		kV
Surge Protection (V_{24}, C/Q, DI, GND Pins)	V_{SRG}	IEC 61000-4-5, 500Ω, 8/20µs surge		±1.2		kV

Note 1: All devices 100% production tested at T_A = +25ºC. Limits over operating temperature range are guaranteed by design.

Note 2: Currents out of the device are negative. Currents into the device are positive.

Note 3: Not production tested. Guaranteed by design.

Note 4: V_{DROP} is measured as the voltage from the driver output to GND (V_{DRIVER} - V_{GND}) when measuring the low-side drivercurrent limit and as (V_{24} - V_{DRIVER}) when measuring the high-side current limit.

Note 5: When CQ_PD or CQ_PU are set to 1, the weak pullups and weak pulldowns are enabled in all C/Q operating modes: transceiver in receive mode and driver in push-pull, NPN, or PNP modes

Note 6: SDA/$\overline{WU}$ always asserts when a valid wake-up condition is received when operating in pin mode. When operating the device in I^2C mode, $\overline{WU}$/IRQ asserts for t_{WUL} only when no interrupts have been registered (INTERRUPT register) and the WUM = 1 in the IRQMASK register. If WUM = 0, WUINT is set when a valid wake-up event is detected and $\overline{WU}$/IRQ asserts until the INTERRUPT register is read.

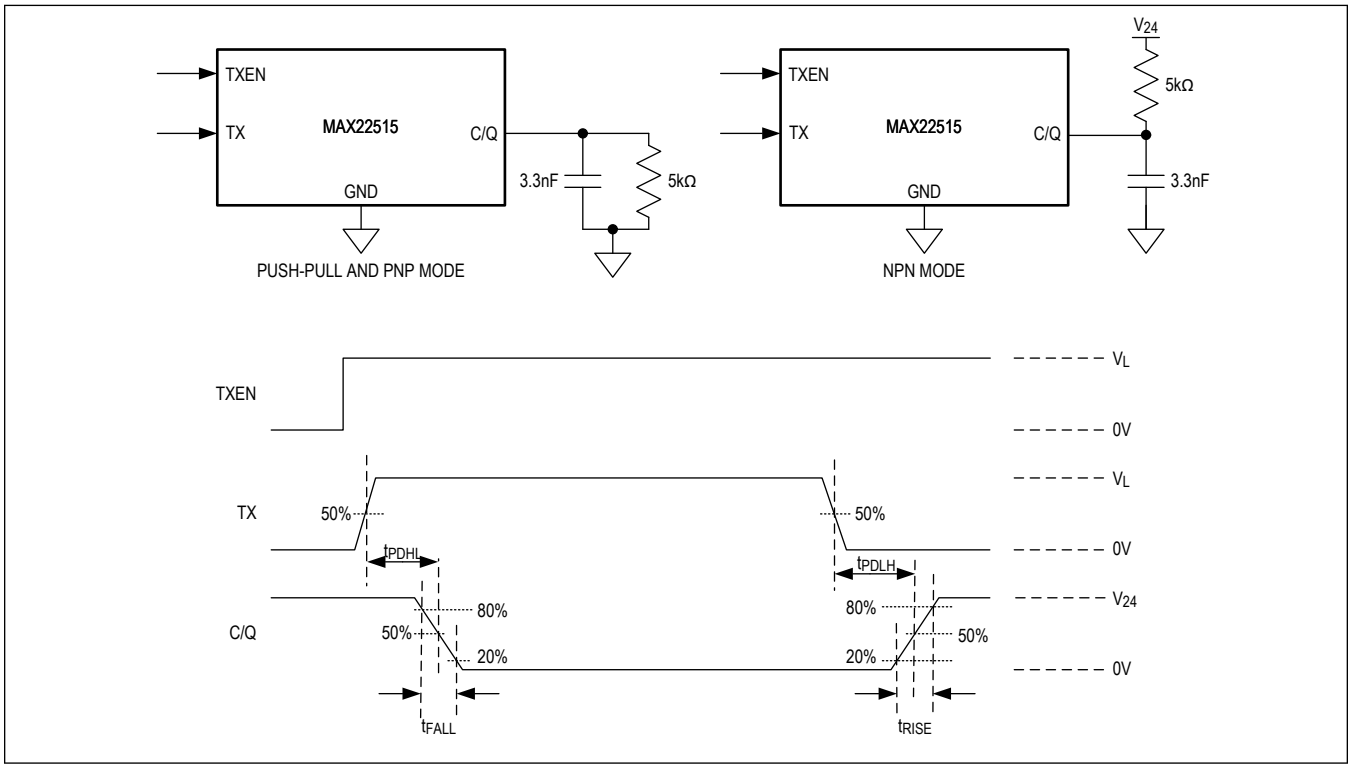


Figure 1. C/Q Driver Propagation Delays

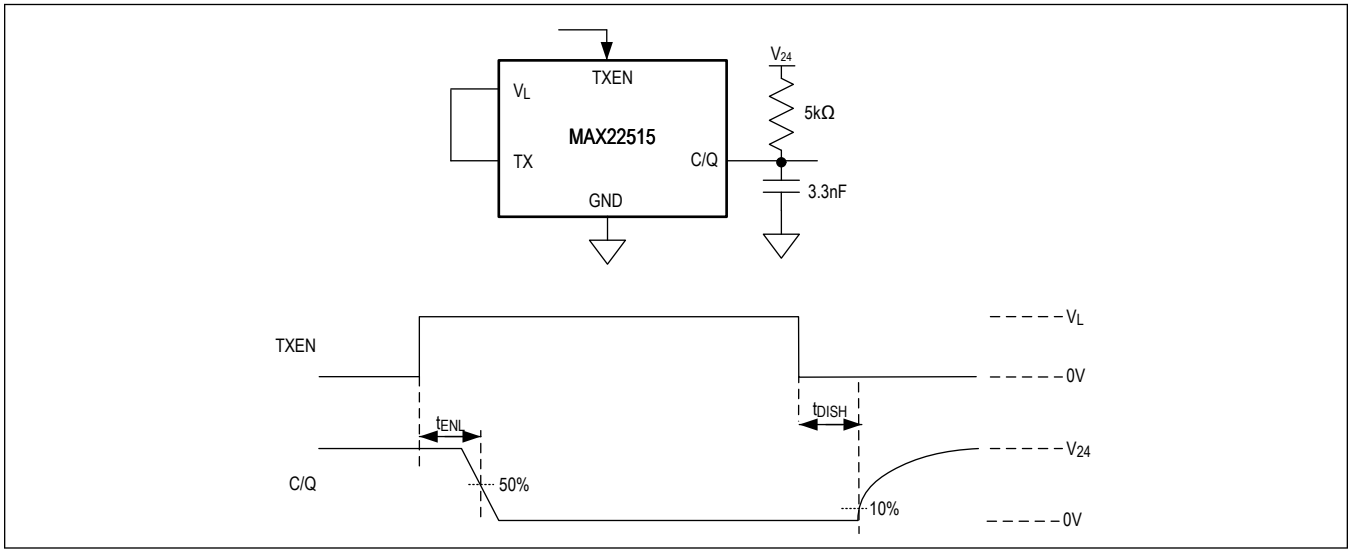


Figure 2. C/Q Driver Enable Low and Disable High Timing

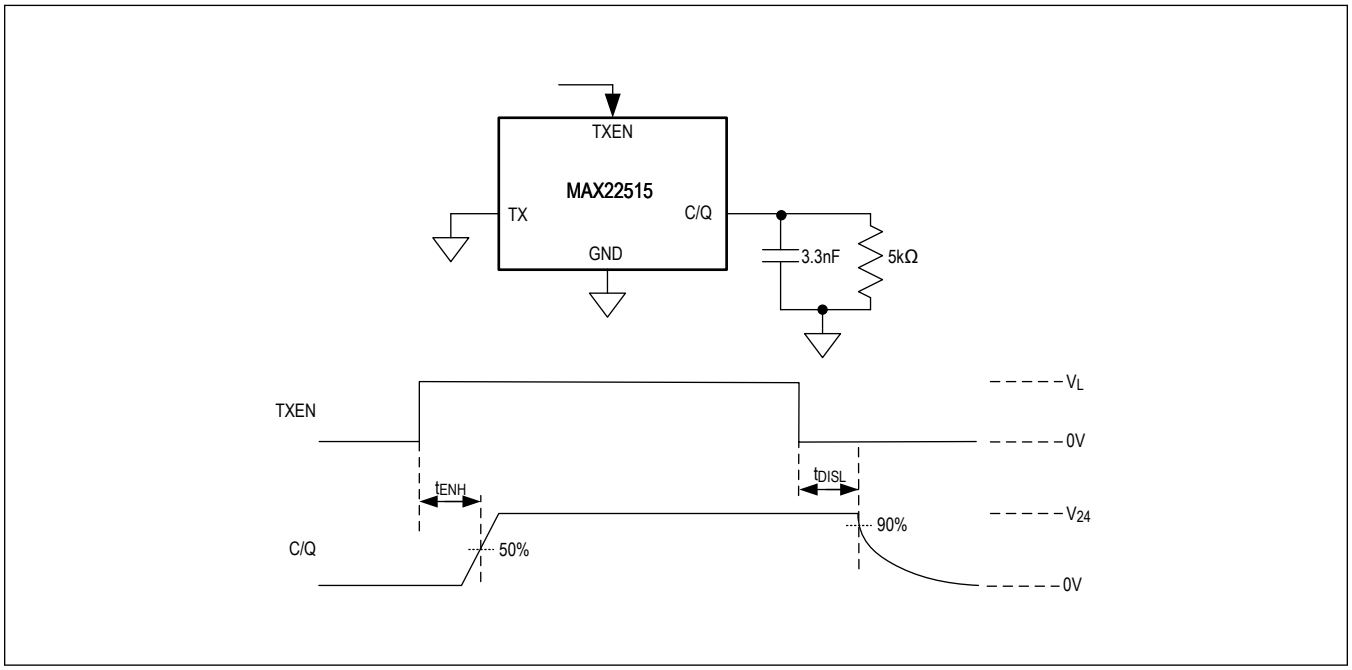


Figure 3. C/Q Driver Enable Time High and Disable Time Low

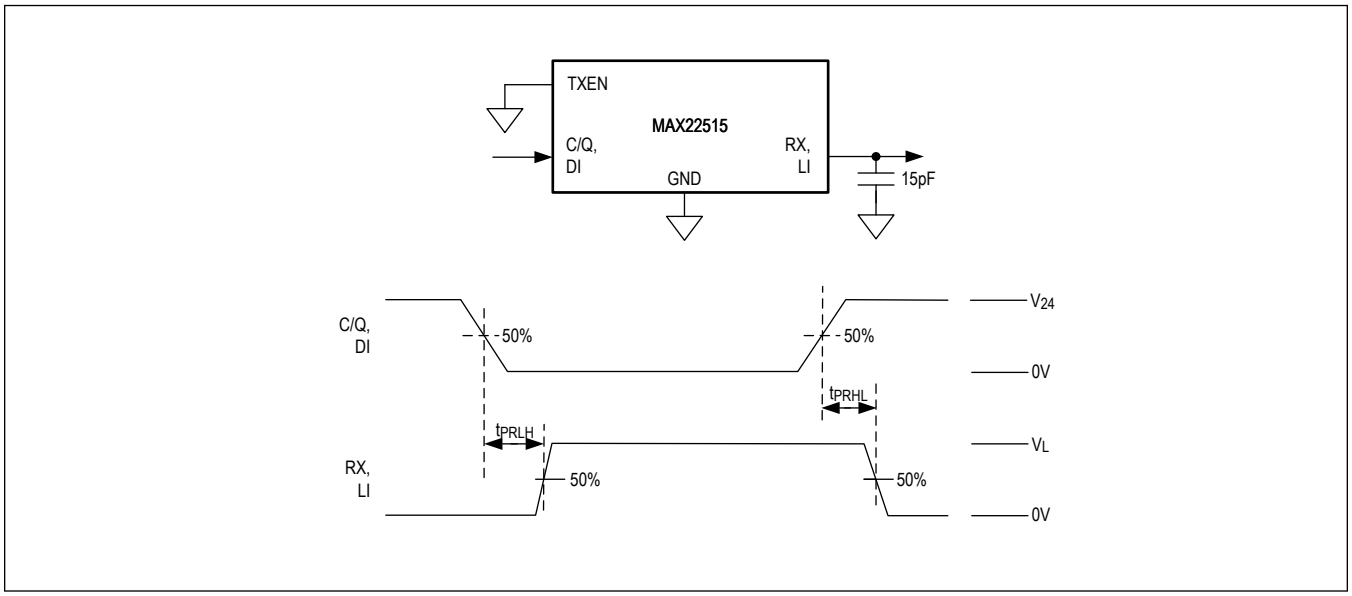


Figure 4. C/Q and DI Receiver Timing

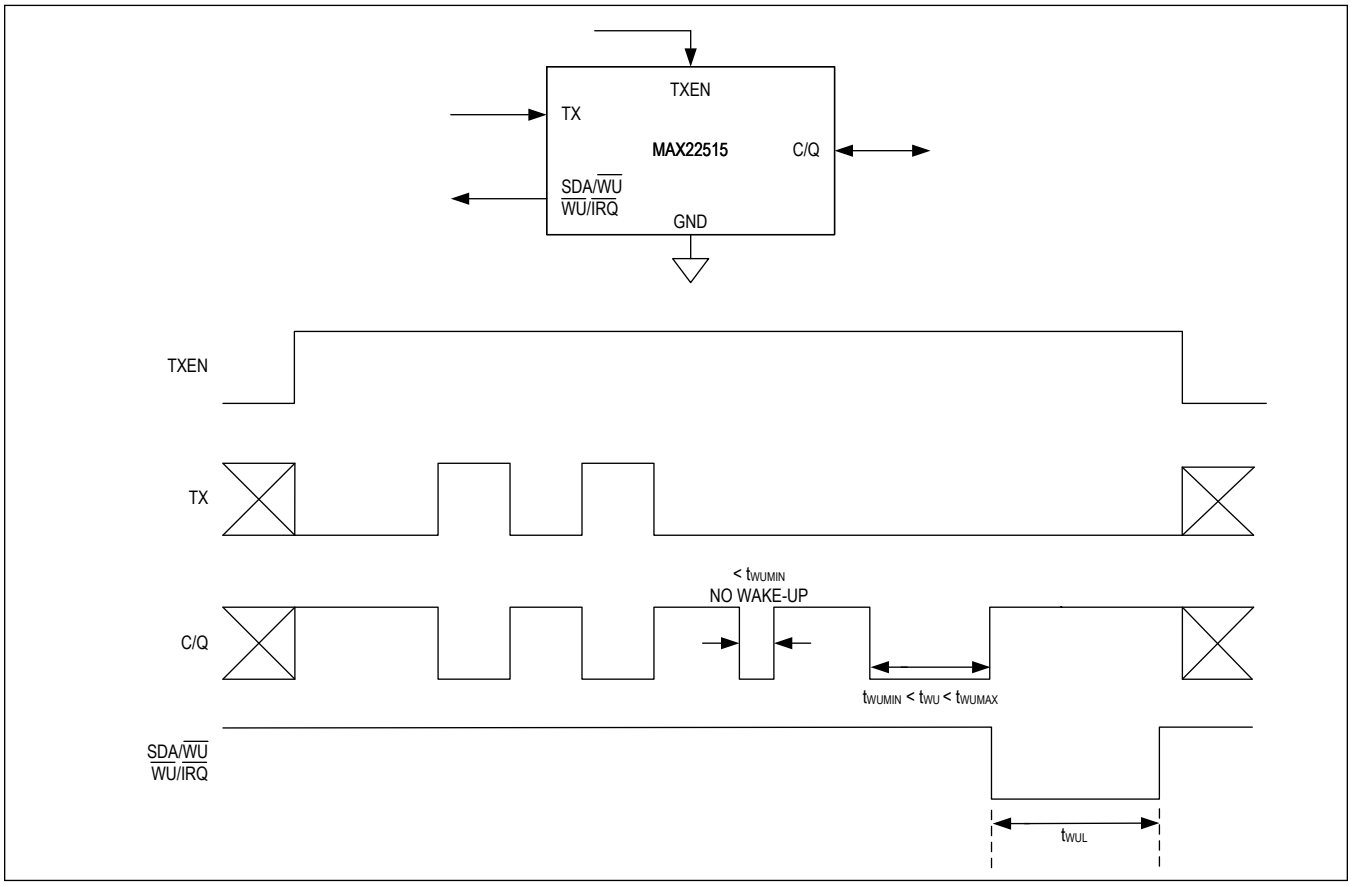


Figure 5. Wake-Up Detection Timing

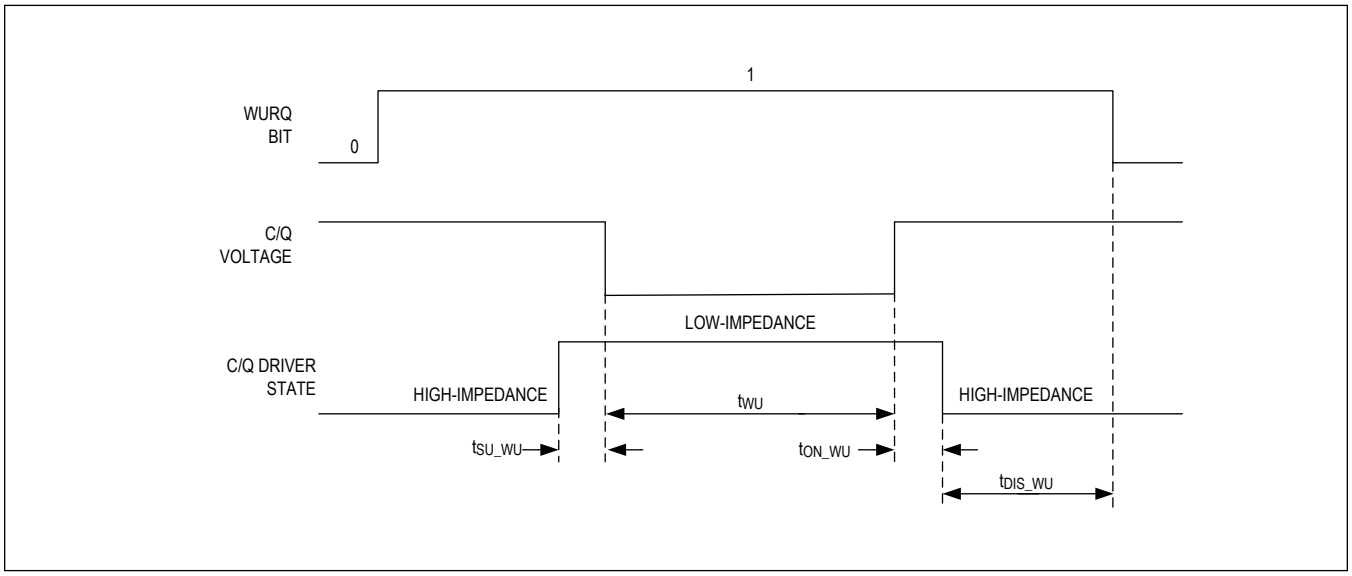


Figure 6. Wake-Up Generation Timing

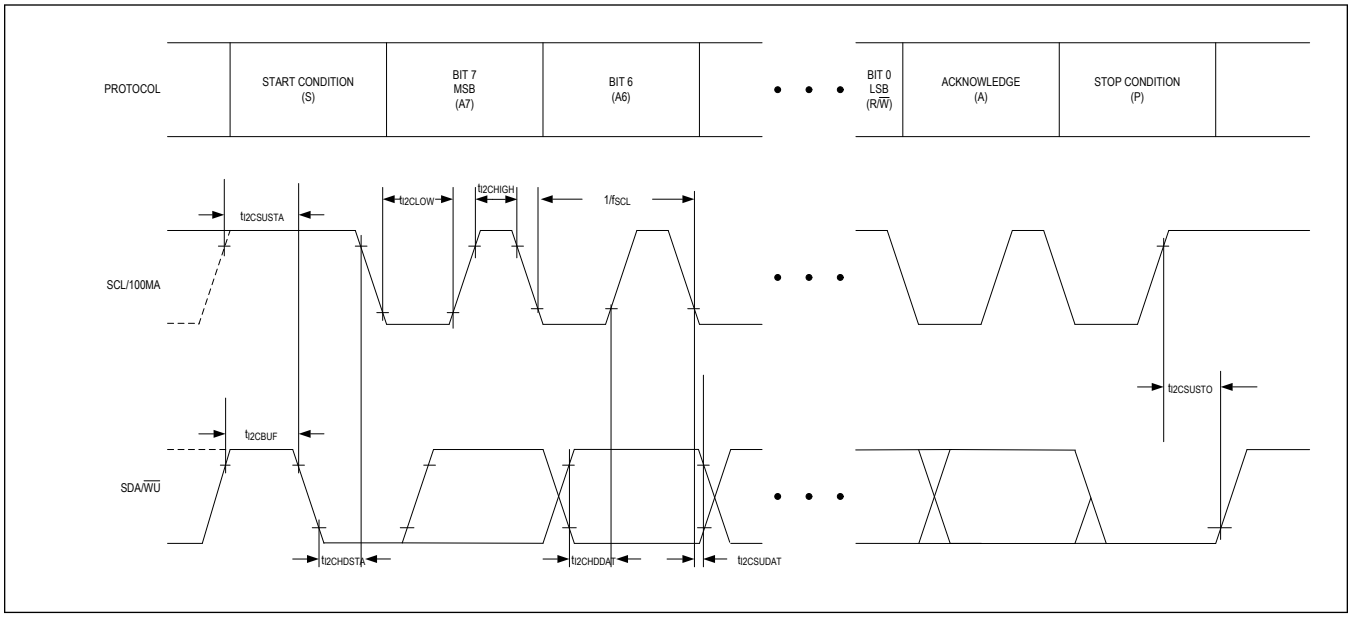
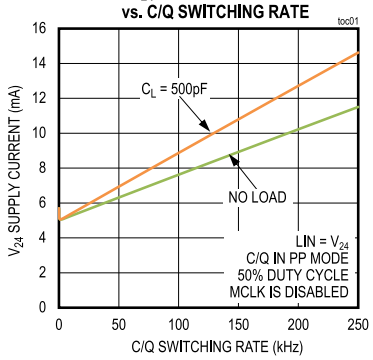


Figure 7. I^2C Timing

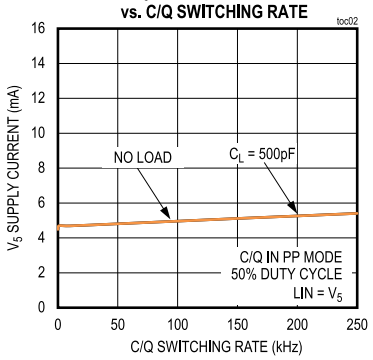
Typical Operating Characteristics

(V_{24} = 24V, LIN is connected to V_{24}, V_L = V_{33}, T_A = 25°C, unless otherwise noted.)

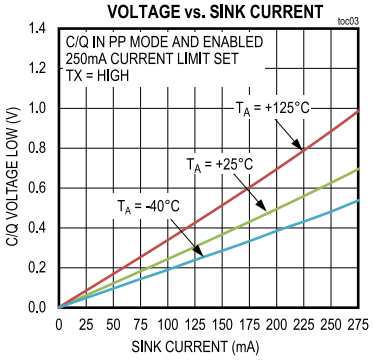
V_{24} SUPPLY CURRENT vs. C/Q SWITCHING RATE



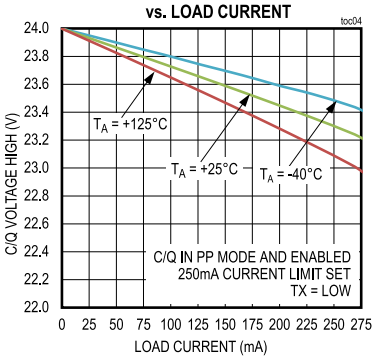
V_5 SUPPLY CURRENT vs. C/Q SWITCHING RATE



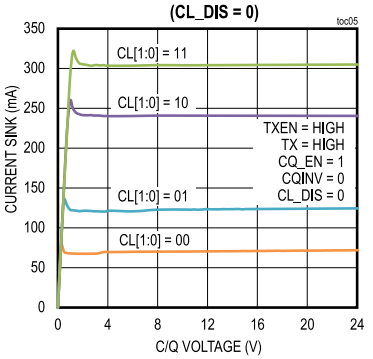
C/Q DRIVER OUTPUT LOW VOLTAGE vs. SINK CURRENT



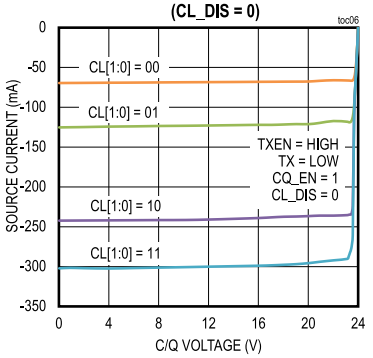
C/Q DRIVER OUTPUT HIGH vs. LOAD CURRENT



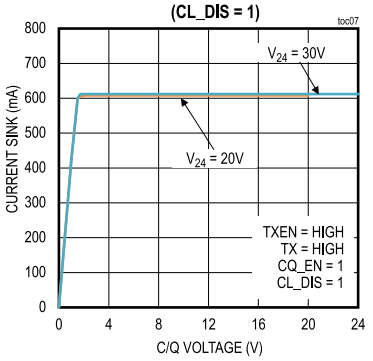
C/Q DRIVER LOW CURRENT LIMIT vs. C/Q VOLTAGE (CL_DIS = 0)



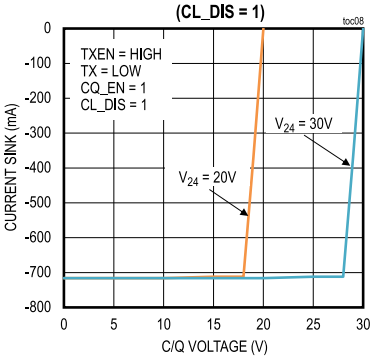
C/Q DRIVER HIGH CURRENT LIMIT vs. C/Q VOLTAGE (CL_DIS = 0)



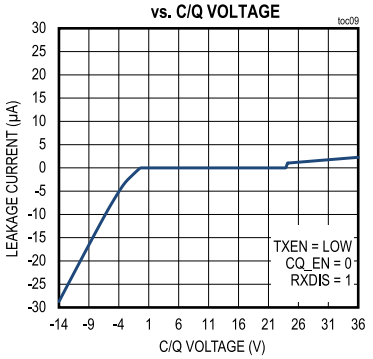
C/Q DRIVER LOW CURRENT LIMIT vs. C/Q VOLTAGE (CL_DIS = 1)



C/Q DRIVER HIGH CURRENT LIMIT vs. C/Q VOLTAGE (CL_DIS = 1)



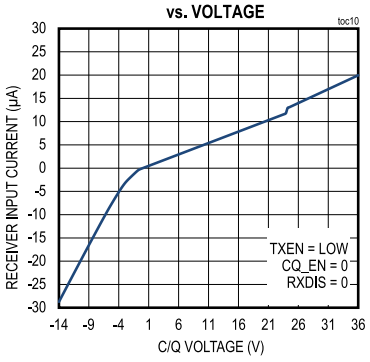
C/Q DRIVER LEAKAGE CURRENT vs. C/Q VOLTAGE



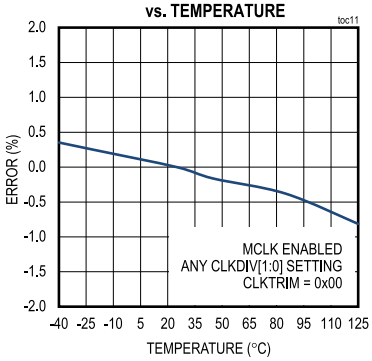
Typical Operating Characteristics (continued)

(V_{24} = 24V, LIN is connected to V_{24}, V_L = V_{33}, T_A = 25°C, unless otherwise noted.)

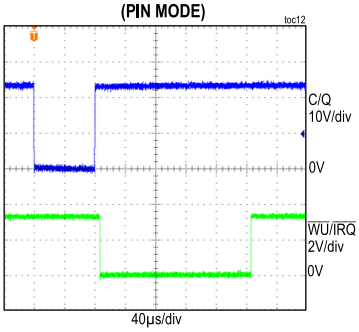
C/Q RECEIVER INPUT CURRENT vs. VOLTAGE



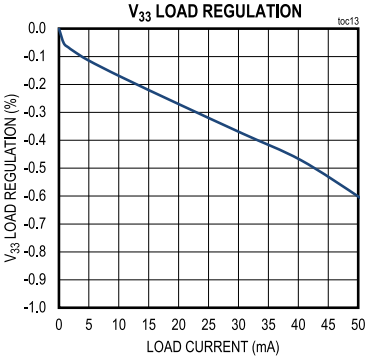
MCLK FREQUENCY ACCURACY vs. TEMPERATURE



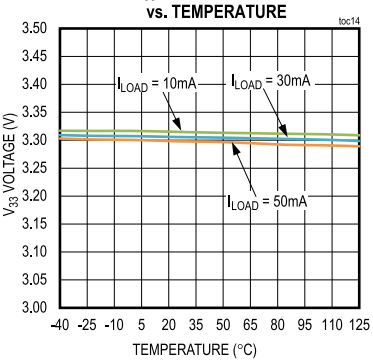
WAKE-UP DETECT (PIN MODE)



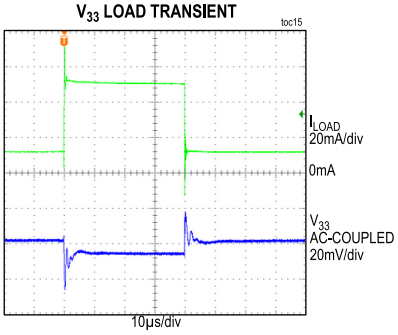
V_{33} LOAD REGULATION



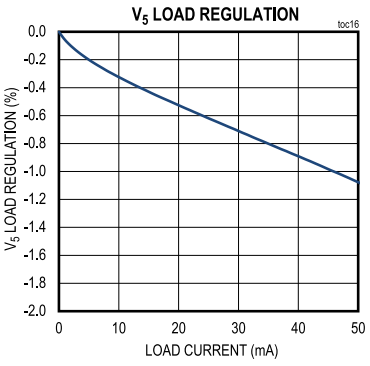
V_{33} OUTPUT VOLTAGE vs. TEMPERATURE



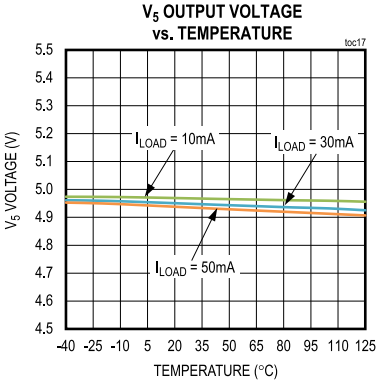
V_{33} LOAD TRANSIENT



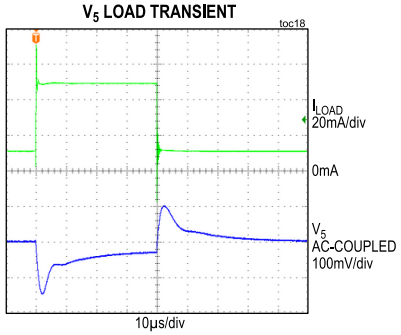
V_5 LOAD REGULATION



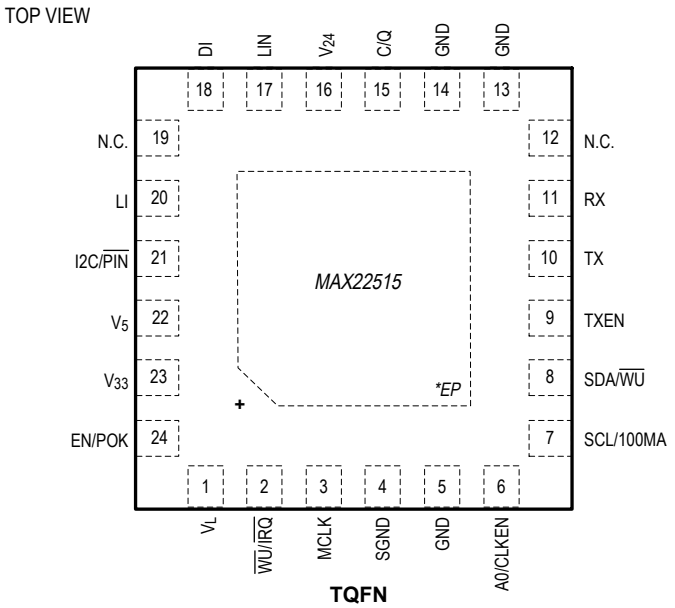
V_5 OUTPUT VOLTAGE vs. TEMPERATURE



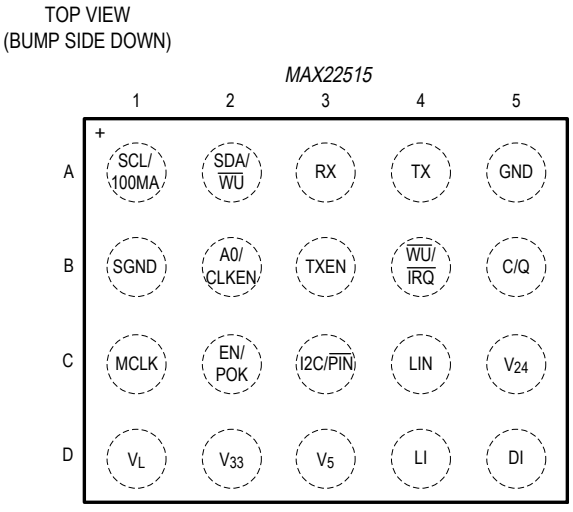
V_5 LOAD TRANSIENT



Pin Configurations



TQFN
4mm x 4mm



WLP

Pin Description

PIN		NAME	FUNCTION
TQFN	WLP		
POWER			
1	D1	V_L	Logic Supply Input. Bypass V_L to GND with a 0.1µF capacitor as close to the device as possible. V_L sets the logic level for all logic signals. Connect V_L to V_{33}, V_5, or to an external voltage between 2.5V and 5V.
4	B1	SGND	Signal Ground. Connect SGND to GND.

Pin Description (continued)

PIN		NAME	FUNCTION
TQFN	WLP		
5, 13, 14	A5	GND	Ground
16	C5	V_{24}	Supply Voltage Input. Apply a 24V (typ) supply to V_{24}. Bypass V_{24} to GND with a 10nF capacitor as close to the device as possible.
17	C4	LIN	5V Linear Regulator Input. Bypass LIN to GND with a 10nF capacitor as close to the device as possible. Connect LIN to V_{24} or to an external supply between 8V and 36V. Short LIN to V_5 to disable the internal regulator. Connect 5V to LIN and V_5 when the internal regulator is disabled.
22	D3	V_5	5V Linear Regulator Output/Supply Input. Bypass V_5 to GND with a 1µF capacitor as close to the device as possible. V_5 is the output of the internal 5V linear regulator. To disable the internal regulator, connect LIN to V_5. 5V is required on V_5 for normal operation. If the 5V regulator is disabled, apply an external 5V power supply to V_5.
23	D2	V_{33}	3.3V Linear Regulator Output. Bypass V_{33} to GND with a 1µF capacitor as close to the device as possible. V_{33} is not required for normal operation.
EP	-	EP	Exposed Pad (TQFN Only). Connect EP to GND.
24V LINE INTERFACE			
15	B5	C/Q	IO-Link Transceiver Input/Output. I²C Mode: C/Q is disabled at startup. Set CQ_EN = 1 and drive TXEN high to enable the C/Q driver. Pin mode: Drive TXEN high to enable the C/Q driver.
18	D5	DI	Auxiliary Digital Input. I²C Mode: DI is enabled at power-up. Disable DI by setting the DIDIS bit in the CONTROL register. Pin mode: DI is enabled and cannot be disabled.
CONTROL INTERFACE			
2	B4	$\overline{WU}/\overline{IRQ}$	IO-Link Wake-Up Detection/Interrupt Open-Drain Output. I²C Mode: $\overline{WU}/\overline{IRQ}$ asserts low when a valid IO-Link wake-up is detected on the C/Q line or when a bit in the INTERRUPT register is set. Pin mode: $\overline{WU}/\overline{IRQ}$ asserts low when a thermal or overcurrent fault occurs. $\overline{WU}/\overline{IRQ}$ deasserts when the fault is no longer present.
6	B2	A0/CLKEN	I²C Address Select/MCLK Enable Input. I²C Mode: Connect A0/CLKEN high or low to set the I²C address for the MAX22515. See the *I²C Controller Interface* section for more information. Pin mode: Drive A0/CLKEN high to enable the clock output on MCLK. Drive A0/CLKEN low to disable the clock output. MCLK is 14.74MHz (typ) in pin mode. MCLK is high impedance when disabled.
7	A1	SCL/100MA	I²C Serial Clock/C/Q Driver Current Limit Setting Input. I²C Mode: I²C interface clock input. Pin mode: Drive SCL/100MA high to set the C/Q driver current limit to 100mA (min). Drive SCL/100MA low to set the driver current limit to 200mA (min).

Pin Description (continued)

PIN		NAME	FUNCTION
TQFN	WLP		
8	A2	SDA/$\overline{WU}$	I^2C Serial Data Input/Ouput/Wake-Up Detection Output. I^2C Mode: I^2C serial data input/output. Pin mode: SDA/$\overline{WU}$ asserts when a valid IO-Link wake-up is detected on the C/Q line.
20	D4	LI	DI Receiver Logic Output. The DI receiver is enabled by default. I^2C Mode: LI is inverted relative to the logic state of DI by default. Set the LIDIS bit in the CONTROL register to disable the LI output. LI is high impedance when LIDIS = 1. Pin mode: LI is inverted relative to the logic state of DI by default. LI cannot be disabled.
21	C3	I^2C/$\overline{PIN}$	I^2C or Pin Mode Control Interface Selection Input. Connect I^2C/$\overline{PIN}$ high to configure and monitor the MAX22515 with the I2C interface. Connect I^2C/$\overline{PIN}$ low to configure the MAX22515 for pin mode control.
24	C2	EN/POK	Dual Function Enable Input and Open-Drain Power-OK (POK) Output. Connect EN/POK to V_L with a 10kΩ resistor. Enable Input: Drive EN/POK high to enable the MAX22515 for normal operation. Drive EN/POK low to disable the device. The C/Q driver is disabled and registers are reset (when using I^2C mode) when EN/POK is low. POK Output: The MAX22515 drives EN/POK low when the V_5 voltage falls below 3V. The C/Q driver is disabled and registers are reset (when using I^2C mode) when EN/POK is low. The MAX22515 releases EN/POK when the V_5 voltage rises above the 3.5V threshold.
UART INTERFACE			
9	B3	TXEN	C/Q Driver Enable Logic Input. Connect TXEN to the RTS output of a microcontroller for IO-Link communication. I^2C Mode: Set CQ_EN = 1 and drive TXEN high to enable the C/Q driver. Pin mode: Drive TXEN high to enable the C/Q driver. Drive TXEN low to disable the driver.
10	A4	TX	C/Q Driver Logic Input. Connect TX to the TX output of a UART for IO-Link communication. I^2C Mode: TX is inverted relative to the logic state of C/Q by default. Pin mode: TX is inverted relative to the logic state of C/Q.
11	A3	RX	C/Q Receiver Logic Output. Connect RX to the RX input of a UART for IO-Link communication. I^2C Mode: RX is inverted relative to the logic state of C/Q by default. Set the RXDIS bit in the CONTROL register to disable RX. RX is high impedance when RXDIS = 1. Pin mode: RX is inverted relative to the logic state of C/Q. RX cannot be disabled.

Pin Description (continued)

PIN		NAME	FUNCTION
TQFN	WLP		
CLOCK OUTPUT			
3	C1	MCLK	Microcontroller Clock Output. I²C Mode: Set the MCLK frequency by setting the CLKDIV bits in the CLKCONFIG register. Connect MCLK to an external microcontroller for comparison and trimming. The MCLK frequency is 14.74MHz (typ) by default, but can be disabled or programmed to 3.686MHz, 7.373MHz, 14.74MHz, 29.49MHz, or 1.843MHz. Pin mode: The MCLK frequency is fixed at 14.74MHz (typ). Drive A0/CLKEN high to enable the MCLK output. Drive A0/CLKEN low to disable the MCLK output. MCLK is high impedance when A0/CLKEN is low.
NOT CONNECTED			
12, 19	-	N.C.	Not connected. Not internally connected.

Detailed Description

The MAX22515 low-power industrial transceiver with integrated surge protection can be configured to operate as either an IO-Link device or in a non-IO-Link industrial sensor. The transceiver includes one IO-Link C/Q bidirectional channel and one digital input (DI) channel.

The MAX22515 features a flexible control interface. Set the device in pin mode control for operation with switching sensors that do not use a microcontroller. For sensors with microcontrollers set the device to operate in I^2C mode allowing extensive configuration and monitoring. Additionally, an integrated oscillator (MCLK) output simplifies clock generation for IO-Link devices.

All 24V line interface pins (V_{24}, C/Q, DI, and GND) are reverse voltage protected, short circuit protected, hot-plug protected, and feature integrated ±1.2kV/500Ω surge protection.

Control Interface (I^2C or Pin Mode)

Overview

The MAX22515 features a selectable control interface: I^2C or pin mode control. Drive the $I^2C/\overline{PIN}$ input high to set the device to operate in I^2C mode. In this mode, connect SCL/100MA to the I^2C clock generator of the microcontroller and connect SDA/$\overline{WU}$ to the SDA I/O on the microcontroller. Set the A0/CLKEN input high or low to set the I^2C address of the device. See the *I^2C Controller Interface* section for more information. Drive the $I^2C/\overline{PIN}$ input low to set the device to operate in pin mode.

I^2C Mode

Set the $I^2C/\overline{PIN}$ input high to configure the MAX22515 to operate in I2C mode control.

The MAX22515 I^2C interface is available for extensive monitoring and configuration of the device. The C/Q driver configuration, driver current limit, and fault behaviors are all configurable in I^2C mode. Additionally, extensive fault detection (driver overcurrent fault, thermal warning and thermal shutdown faults), and wake-up event detection allow the microcontroller to quickly determine the state of the device and react accordingly.

The MAX22515 can generate a wake-up pulse in I^2C mode only.

Pin Mode

Set the $I^2C/\overline{PIN}$ input low to operate the MAX22515 in pin mode. The MAX22515 has limited configurability in pin mode and includes the following nonconfigurable functionality:

- V_{33} cannot be disabled.
- The C/Q rise time is 0.3µs and the fall time is 0.33µs.
- The C/Q driver current limit cannot be disabled.
  - Drive SCL/100MA high to enable the 100mA (typ) driver current limit.
  - Drive SCL/100MA low to enable the 200mA (typ) driver current limit.
- Autoretry functionality is enabled with a 500µs blanking time 50ms fixed off-time during overcurrent events.
- C/Q is the logic inverse of TX.
- RX is the logic inverse of C/Q.
- LI is the logic inverse of DI.
- Glitch filters on C/Q and DI receivers are disabled.
- Weak pullup and pulldown currents on C/Q are disabled.
- SDA/$\overline{WU}$ asserts low when a wake-up is detected on C/Q.
  - $\overline{WU}/\overline{IRQ}$ does not assert when a wake-up is detected.
- $\overline{WU}/\overline{IRQ}$ asserts during a driver fault condition or thermal overload condition, or when V_{24} is below the warning threshold voltage (V_{24}_W).
  - $\overline{WU}/\overline{IRQ}$ deasserts when the fault condition is removed and when V_{24} is above the warning threshold voltage.
- The MAX22515 cannot generate a wake-up pulse.
- The MCLK switching frequency is 14.74MHz (typ).

24V Interface

C/Q Driver Overcurrent Limiting

When a load attempts to draw more current than the current limit threshold that has been set, the C/Q driver actively limits the load current so a higher current does not flow. The MAX22515 features a selectable C/Q driver current limit in both I^2C mode and in pin mode.

In I^2C mode, select the C/Q driver current limit by setting the CL[1:0] bits in the CURRLIM register. Current limit thresholds can be set to 50mA (min), 100mA (min), 200mA (min), or 250mA (min).

In pin mode, select the C/Q driver current limit by setting the SCL/100MA input high or low. Drive SCL/100MA high to set the driver current limit to 100mA (min). Drive SCL/100MA low to set the current limit to 200mA (min).

C/Q Driver Continuous Current Limiting with Blanking Time and Autoretry

The MAX22515 features two overcurrent management functions to allow the C/Q driver to drive large loads without triggering a fault: blanking time and autoretry.

When the C/Q driver current exceeds the current limit threshold for a duration longer than the blanking time, a fault is generated. Loads that require large currents are often capacitive, incandescent lamps, or can be short circuits. When driving capacitive or lamp loads, ensure that the blanking time is long enough to charge up the required load.

- In I^2C mode, the CQFAULT bit in the INTERRUPT register is set and, if the interrupt is not masked, the $\overline{WU}/\overline{IRQ}$ output asserts.
- In pin mode, $\overline{WU}/\overline{IRQ}$ asserts and deasserts when the fault condition is removed.

Select the blanking time in I^2C mode by setting the CL_BL[1:0] bits in the CURRLIM register. Available blanking times are 128µs (typ), 500µs (typ), 1ms (typ), or 5ms (typ). The blanking time is fixed at 500µs (typ) when operating in pin mode.

When autoretry is enabled, the driver is automatically disabled after the blanking time and remains off for a set off-time. The driver is reenabled after the off-time. If the overcurrent condition is still present, the driver is disabled again after the blanking time and the cycle continues.

- In I^2C mode, enable autoretry functionality by setting the AUTORETRYEN bit in the CURRLIM register. Select the driver off-time during autoretry by setting the TAROFF[1:0] bits in the CURRLIM register.
- In pin mode, autoretry functionality is enabled and the driver off-time is fixed as 50ms.

C/Q Driver Thermal Shutdown

The C/Q driver is automatically disabled when the driver junction temperature exceeds the +150°C (typ) driver thermal shutdown temperature. A fault condition is signaled after the set blanking time (and the auto-retry off period if enabled).

- In I^2C mode, the CQFAULT bit in the INTERRUPT register is set and, if the fault is not masked (CQFAULTM = 0), $\overline{WU}/\overline{IRQ}$ asserts.
- In pin mode, $\overline{WU}/\overline{IRQ}$ asserts until the driver temperature falls below the thermal shutdown hysteresis.

If autoretry is disabled (I^2C mode only) the driver is automatically reenabled when the driver temperature falls below 140°C (typ). If autoretry is enabled (AUTORETRYEN = 1), or the device is in pin mode, the MAX22515 waits for the autoretry delay and reenables the driver.

Receiver Threshold

Although the IO-Link standard defines device/sensor operation for a supply ranging between 18V and 30V, industrial sensors in the field commonly operate with supply voltages as low as 9V. The MAX22515 operates with a supply voltage between 8V and 36V. When the V_{24} supply voltage is above 18V, the C/Q and DI receiver thresholds fall within the IO-Link required values. When V_{24} is less than 18V, the MAX22515 scales the C/Q and DI receiver thresholds with respect to V_{24}, allowing receiver functionality down to the lowest supply voltage.

Wake-Up Detection

The MAX22515 detects a wake-up condition as a combination of current and a voltage event on the C/Q line when the driver is enabled in PNP, NPN, or push-pull mode. A wake-up event occurs when an IO-Link master forces a level on the C/Q line to the opposite logic-level and a current is sourced (or sinked) for 80µs (typ).

In I^2C mode, the WUINT bit in the INTERRUPT register is set and, unless masked (WUIM = 1 in the IRQMASK register), $\overline{WU}/\overline{IRQ}$ asserts to indicate that a wake-up has been detected. Wake-up detection is enabled by default. Set the WUDIS bit in the CONTROL register to disable wake-up detection.

In pin mode, a wake-up event is only detected when TXEN is high (driver enabled) and a wake-up event (voltage or current) occurs. Wake-up events are not detected in emulated PNP and/or NPN modes where TXEN is low. Wake-up detection is always enabled in pin mode and cannot be disabled. SDA/$\overline{WU}$ asserts low when a valid wake-up has been detected in pin mode. $\overline{WU}/\overline{IRQ}$ does not assert when a wake-up has been detected in pin mode.

The MAX22515 automatically ignores false wake-up events that can sometimes occur as a consequence of driving large capacitive or lamp loads where the time constant of charge-up is in the range of 80µs. No wake-up event is detected for the duration of the set blanking time after the C/Q driver changes logic state.

Using the MAX22515 as a Master Transceiver (I^2C Mode Only)

In I^2C mode, the MAX22515 can be configured to operate as an IO-Link master transceiver. An IO-Link master must be able to generate a wake-up pulse on the C/Q line.

To prepare the transceiver to generate a wake-up pulse, set the C/Q driver in receive mode (CQ_EN = 1 and TXEN = low) and set the TX input high. Set the WURQ bit in the WAKEUP register to generate the wake-up pulse.

When WURQ = 1, the MAX22515 samples the voltage level on the C/Q receiver. The device then enables the C/Q driver and pulls the C/Q line to the opposite polarity of the sampled voltage for 80µs (typ). The driver remains enabled and the line is driven back to the original polarity after the wake-up pulse duration. Following the on-time after wake-up delay (t_{ON_WU}), the driver is set to high impedance. The MAX22515 continues to ignore signals on TX and TXEN and holds the driver in a high impedance state for the high-impedance time after wake-up delay (t_{DIS_WU}), after which the microcontroller can initiate the normal IO-Link communication sequence. See Figure 6.

The CURRLIM register contents do not have to be changed before initiating a wake-up pulse. When WURQ = 1, the MAX22515 automatically changes the current limit to ensure that the 500mA (min) wake-up current can flow for the duration of the wake-up pulse.

Ensure that the CQSLEW[1:0] bits in the CQCONFIG register are set to 00 to ensure that driver rise and fall times are as short as possible.

An IO-Link master transceiver must also include a 5mA pullup/pulldown on the C/Q line. The MAX22515 requires this functionality to be added with external components. See Maxim's application note 7330, *Configuring an IO-Link Device Transceiver for use in an IO-Link Master*, for more information.

EN Input/Power OK (POK) Output

The EN/POK input is a dual function open-drain logic input/output, functioning as an active-high enable input and a power-OK (POK) output. Connect EN/POK to V_L with a 10kΩ resistor. To avoid contention, drive EN/POK with an open-drain output.

Drive EN/POK low to set the MAX22515 in reset mode. The C/Q driver is disabled and the registers are reset (if using I^2C mode) when EN/POK is low. I^2C communication is available while EN/POK is low if V_L is present.

The MAX22515 asserts EN/POK low when the V_5 voltage falls below the V_5 POK threshold. The C/Q driver is disabled

and the registers are reset (if using I²C mode) when EN/POK is low. The MAX22515 deasserts EN/POK 4ms (typ) after the V_5 voltage rises above the POK threshold.

Protection

Reverse Polarity Protection

The MAX22515 is protected against reverse polarity connections on the C/Q, DI, V_{24}, and GND pins. Any combination of these pins can be connected to a voltage in the range of -36V to +36V. This results in a current flow of less than 500µA. Note that the maximum voltage between any pins should not exceed *Absolute Maximum Ratings*.

Thermal Shutdown

The MAX22515 enters thermal shutdown when the average die temperature exceeds the +160°C (typ) thermal shutdown threshold. The C/Q driver is switched off during thermal shutdown. The V_5 and V_{33} regulators remain on during thermal shutdown and I²C communication is available, if enabled. When the average die temperature falls below the 145°C (typ) thermal shutdown hysteresis, the device exits thermal shutdown.

In I²C mode, the THSHUTD bit in the STATUS register and the THSHUTINT bit in the INTERRUPT register are set, and if not masked (THSHUTM = 0 in the IRQMASK register), $\overline{WU}/\overline{IRQ}$ asserts. THSHUTD is cleared when the MAX22515 exits thermal shutdown. Read the INTERRUPT register to clear the THSHUTINT bit and deassert $\overline{WU}/\overline{IRQ}$.

In pin mode, $\overline{WU}/\overline{IRQ}$ asserts when the MAX22515 enters thermal shutdown and deasserts when it exits thermal shutdown.

POR and Register Corruption Check (I²C Mode Only)

The MAX22515 performs on-going checks of all register bits. A register is corrupted when the value is changed by an external event (for example, an ESD discharge, etc.). When a corrupt register bit is detected, the CORR_REG bit in the STATUS2 register is set, the NOTREADY bit in the INTERRUPT register is set, and the $\overline{WU}/\overline{IRQ}$ output is asserted. The C/Q driver is disabled when the NOTREADY bit is set.

The microcontroller must rewrite correct values to all of the registers after the COR_REG bit has been set. The COR_REG bit is automatically cleared when the registers have been rewritten to their preevent cycle values. Once the CORR_REG bit is cleared, read the INTERRUPT register to clear the NOTREADY bit and deassert $\overline{WU}/\overline{IRQ}$.

I²C Controller Interface

Overview

Drive the I²C/$\overline{PIN}$ pin high to set the MAX22515 to operate with the I²C control interface. The I²C interface supports fast mode plus with a clock frequency up to 1MHz and features SDA stuck protection. SCL/100MA and SDA/WU require pullup resistors to V_L or an external voltage for I²C communication.

The MAX22515 supports both burst and single-byte read and write functionality.

I²C Slave Address

Set the A0/CLKEN pin to set the 7-bit slave address for I²C communication. The first 6 bits (MSBs) of the slave address are factory-programmed and is always 011010. Connect A0/CLKEN to V_L or GND to set the LSB of the address. The address is defined as the 7 MSBs followed by a read/write bit. Set the read/write bit to 1 to configure the MAX22515 to read mode. Set the read/write bit to 0 to configure the device for write mode. The address is the first byte of information sent to the device after the START condition.

I²C Address Map

I²C Byte Write

With this operation the master sends an address and 1 or 2 data bytes to the slave device (Figure 8). The write byte procedure is as follows:

1. The master sends a START condition.
2. The master sends the 7-bit slave ID plus a write bit (low).
3. The addressed slave asserts an ACK on the data line.
4. The master sends the 8-bit register address.
5. The active slave asserts an ACK on the data line only if the address is valid (NACK if not).
6. The master sends the 8-bit data byte.
7. The slave asserts an ACK on the data line.
8. The master generates a STOP condition.

Table 1. I²C Address Map

A0/CLKEN	READ/WRITE	I²C ADDRESS
0	W	0x68
	R	0x69
1	W	0x6A
	R	0x6B

I²C Byte Read

With this operation the master sends an address and receives 1 or 2 data bytes from the slave device (Figure 9). The read byte procedure is as follows:

1. The master sends a START condition.
2. The master sends the 7-bit slave ID plus a write bit (low).
3. The addressed slave asserts an ACK on the data line.
4. The master sends the 8-bit register address.
5. The active slave asserts an ACK on the data line only if the address is valid (NACK if not).
6. The master sends a repeated START (Sr).
7. The master sends the 7-bit slave ID plus a read bit (high).
8. The slave asserts an ACK on the data line.
9. The slave sends 8 data bits.
10. The master asserts a NACK on the data line.
11. The master generates a STOP condition.

SDA Stuck Protection

A stuck bus occurs in I²C communication when a slave receives some communication but does not receive a stop (P) or repeated start (Sr) that signals to the slave to release the bus. When this happens, the data line (SDA/$\overline{WU}$) is held low by the slave and no further communication can occur on the bus until it is released. The MAX22515 features an internal timer that monitors the data line to protect against this situation. If SDA/$\overline{WU}$ is held low for more than 1.1ms (typ), the MAX22515 releases the data line high, resuming normal communication. This bus protection limits the minimum I²C clock frequency to 10kHz.

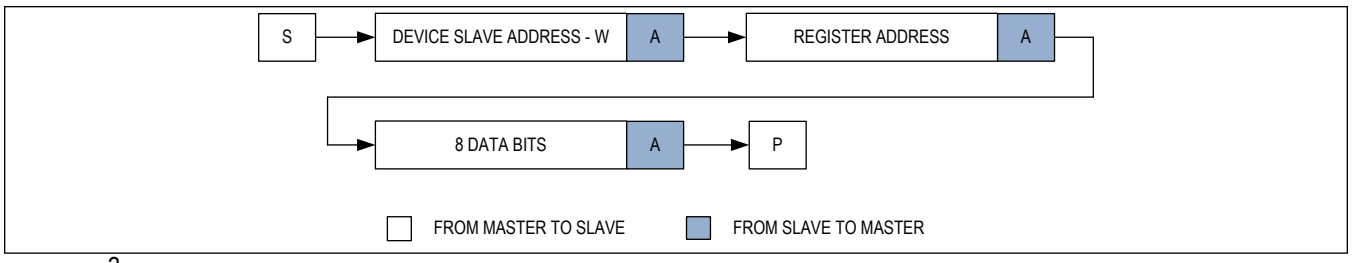


Figure 8. I^2C Byte Write

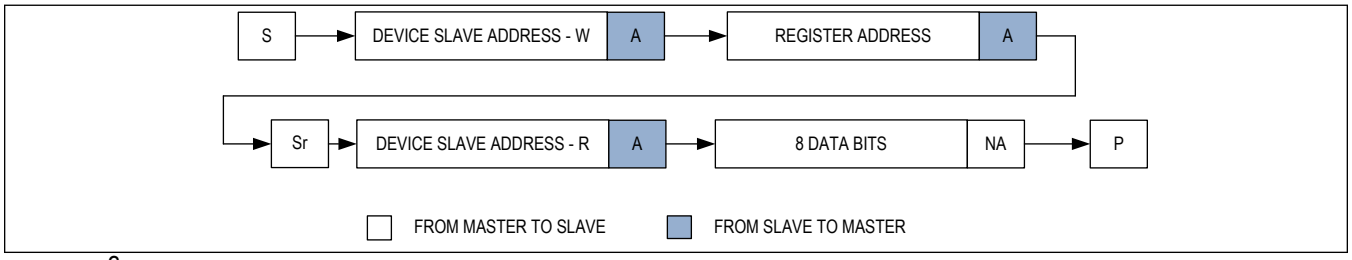


Figure 9. I^2C Byte Read

Register Map

MAX22515

– Reserved. Do not use.

ADDRESS	NAME	MSB							LSB
Functional									
0x00	INTERRUPT[7:0]	NOTREADY	WUINT	–	CQFAULTINT	V24WINT	UV24INT	THSHUTINT	THERMWINT
0x01	IRQMASK[7:0]	–	WUM	–	CQFAULTM	V24WM	UV24M	THSHUTM	THERMWM
0x02	STATUS1[7:0]	CQLVL	DILVL	–	CQFAULT	V24WARN	UV24	THSHUTD	THERMW
0x03	STATUS2[7:0]	CORR_REG	–	–	–	–	–	–	–
0x04	MODE[7:0]	RST	–	–	–	–	–	–	–
0x05	CURRLIM[7:0]	CL[1:0]		CLDIS	CL_BL[1:0]		TAR[1:0]		AUTORETRYEN
0x06	CONTROL[7:0]	LDO33DIS	WUDIS	DIDIS	DIFILTER	RXDIS	RXFILTER	–	CQ_Q
0x07	CQCONFIG[7:0]	CQSLEW[1:0]		CQ_PD	CQ_PU	CQ_NPN	CQ_PP	INVCQ	CQ_EN
0x08	DICONFIG[7:0]	–	–	–	–	–	–	INVDI	LIDIS
0x09	CLKCONFIG[7:0]	ENCLKTRIM	–	–	–	CLKDIV[2:0]			MCLKDIS
0x0A	CLKTRIM[7:0]	CKTRIM[7:0]							
0x0B	WAKEUP[7:0]	WURQ	–	–	–	–	–	–	–
0x0C	CHIPID[7:0]	CHIPID[7:0]							

Register Details

INTERRUPT (0x00)

BIT	7	6	5	4	3	2	1	0
Field	NOTREADY	WUINT	–	CQFAULTINT	V24WINT	UV24INT	THSHUTINT	THERMWINT
Reset	0	0	–	0	0	0	0	0
Access Type	Read Clears All	Read Clears All	–	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION
NOTREADY	7	0 = The MAX22515 is operating normally. 1 = Any of the following conditions has occurred since the last INTERRUPT register read: * The V_5 supply voltage dropped below its UVLO threshold and the registers were reset. * A power-up occurred and the registers have been reset. * At least one register has been corrupted due to an external event (not POR). The NOTREADY interrupt cannot be masked.

BITFIELD	BITS	DESCRIPTION
WUINT	6	0 = No wake-up event has been detected. 1 = An IO-Link wake-up event has been detected on the C/Q line since the last INTERRUPT register read.
CQFAULTINT	4	0 = C/Q driver operating normally. 1 = Overcurrent/overload condition or driver thermal shutdown event has occurred on the C/Q driver since the last INTERRUPT register read.
V24WINT	3	0 = V_{24} is above 16V (typ). 1 = V_{24} voltage has fallen below 16V (typ) since the last INTERRUPT register read.
UV24INT	2	0 = V_{24} is above the 7V (typ) undervoltage threshold (UVLO). 1 = The V_{24} voltage has fallen below the 6V (typ) undervoltage threshold since the last INTERRUPT register read.
THSHUTINT	1	0 = The MAX22515 has not entered thermal shutdown. 1 = The MAX22515 has entered thermal shutdown since the last INTERRUPT register read.
THERMWINT	0	0 = The MAX22515 temperature has not risen above the thermal warning temperature threshold. 1 = The MAX22515 temperature has risen above the thermal warning temperature threshold since the last INTERRUPT register read.

IRQMASK (0x01)

BIT	7	6	5	4	3	2	1	0
Field	–	WUM	–	CQFAULTM	V24WM	UV24M	THSHUTM	THERMWM
Reset	–	0	–	0	0	0	0	0
Access Type	–	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
WUM	6	0 = $\overline{WU}/\overline{IRQ}$ asserts when the WUINT bit in the INTERRUPT register is set. 1 = $\overline{WU}/\overline{IRQ}$ asserts for 200µs (typ) and then deasserts after a valid wake-up condition is detected.
CQFAULTM	4	0 = $\overline{WU}/\overline{IRQ}$ asserts when the CQFAULT bit in the INTERRUPT register is set. 1 = $\overline{WU}/\overline{IRQ}$ does not assert when the CQFAULT bit in the INTERRUPT register is set.
V24WM	3	0 = $\overline{WU}/\overline{IRQ}$ asserts when the V24WINT bit in the INTERRUPT register is set. 1 = $\overline{WU}/\overline{IRQ}$ does not assert when the V24WINT bit in the INTERRUPT register is set.
UV24M	2	0 = $\overline{WU}/\overline{IRQ}$ asserts when the UV24INT bit in the INTERRUPT register is set. 1 = $\overline{WU}/\overline{IRQ}$ does not assert when the UV24INT bit in the INTERRUPT register is set.
THSHUTM	1	0 = $\overline{WU}/\overline{IRQ}$ asserts when the THSHUTINT bit in the INTERRUPT register is set. 1 = $\overline{WU}/\overline{IRQ}$ does not assert when the THSHUTINT bit in the INTERRUPT register is set.
THERMWM	0	0 = $\overline{WU}/\overline{IRQ}$ asserts when the THERMWINT bit in the INTERRUPT register is set. 1 = $\overline{WU}/\overline{IRQ}$ does not assert when the THERMWINT bit in the INTERRUPT register is set.

STATUS1 (0x02)

BIT	7	6	5	4	3	2	1	0
Field	CQLVL	DILVL	–	CQFAULT	V24WARN	UV24	THSHUTD	THERMW
Reset		0	–	0	0	0	0	0
Access Type	Read Only	Read Only	–	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
CQLVL	7	0 = C/Q is high. 1 = C/Q is low.
DILVL	6	0 = DI is high. 1 = DI is low.
CQFAULT	4	0 = No fault on the C/Q driver. 1 = Overcurrent or thermal overload fault on the C/Q driver.
V24WARN	3	0 = V_{24} is above the 16V (typ) warning threshold. 1 = V_{24} is below the 16V (typ) warning threshold.
UV24	2	0 = V_{24} is above the 7V (typ) rising undervoltage lockout (UVLO) threshold. 1 = V_{24} is below the 6V (typ) falling UVLO threshold.
THSHUTD	1	0 = The die temperature is below the thermal shutdown threshold. 1 = The die temperature is above the thermal shutdown threshold. The MAX22515 is in thermal shutdown.
THERMW	0	0 = The die temperature is below the 125ºC (typ,falling) warning threshold. 1 = The die temperature is above the 140ºC (typ, rising) warning threshold.

STATUS2 (0x03)

BIT	7	6	5	4	3	2	1	0
Field	CORR_REG	–	–	–	–	–	–	–
Reset	0	–	–	–	–	–	–	–
Access Type	Read Only	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
CORR_REG	7	0 = All register values are correct. 1 = Register values are corrupted. C/Q is disabled and RX and LI are high impedance when CORR_REG = 1. V_{33} is forced on and MCLK is enabled at switching at 14.74MHz (typ).

MODE (0x04)

BIT	7	6	5	4	3	2	1	0
Field	RST	–	–	–	–	–	–	–
Reset	0	–	–	–	–	–	–	–
Access Type	Write Only Clears All	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
RST	7	0 = Registers are not in reset state. 1 = Set all registers to their default state. RST clears automatically.

CURRLIM (0x05)

BIT	7	6	5	4	3	2	1	0
Field	CL[1:0]		CLDIS	CL_BL[1:0]		TAR[1:0]		AUTORETRYEN
Reset	00		0	00		00		0
Access Type	Write, Read		Write, Read	Write, Read		Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION
CL	7:6	CL[1:0] bits set the active current limit levels for the C/Q driver when CLDIS = 0. 00 = 50mA (min) current limit 01 = 100mA (min) current limit 10 = 200mA (min) current limit 11 = 250mA (min) current limit
CLDIS	5	0 = The C/Q driver current limit is enabled. The current limit is set by the CL[1:0] bits. 1 = The C/Q driver current limit is disabled. The C/Q driver current will exceed 500mA (min).
CL_BL	4:3	CL_BL1:0] set the blanking time for the C/Q driver. 00 = 128µs(typ) 01 = 500µs (typ) 10 = 1ms (typ) 11 = 5ms (typ)
TAR	2:1	The TAR[1:0] bits set the fixed off-time for the C/Q driver after an overcurrent or driver thermal shutdown fault has been generated and autoretry functionality is enabled (AUTOETRYEN = 1). The driver is automatically reenabled after the fixed off-time delay. 00 = 50ms (typ) 01 = 100ms (typ) 10 = 200ms (typ) 11 = 500ms (typ)
AUTORETRYEN	0	Enable/disable autoretry for overcurrent and overtemperature events. 0 = Autoretry is disabled on the C/Q driver. When AUTORETRYEN = 0, the C/Q driver is only turned-off due to thermal overload. 1 = Autoretry is enabled on the C/Q driver. When a fault is signaled on the driver, the driver is disabled for the selected off-time and then automatically reenabled.

CONTROL (0x06)

BIT	7	6	5	4	3	2	1	0
Field	LDO33DIS	WUDIS	DIDIS	DIFILTER	RXDIS	RXFILTER	–	CQ_Q
Reset	0	0	0	0	0	0	–	0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	Write, Read

BITFIELD	BITS	DESCRIPTION
LDO33DIS	7	0 = V_{33} linear regulator is enabled. 1 = V_{33} linear regulator is disabled.

BITFIELD	BITS	DESCRIPTION
WUDIS	6	0 = IO-Link wake-up detection is enabled. 1 = IO-Link wake-up detection is disabled.
DIDIS	5	0 = DI receiver is enabled. 1 = DI receiver is disabled. DI input current is reduced when DIDIS = 1.
DIFILTER	4	0 = The 1µs (typ) glitch filter on the DI receiver is disabled. 1 = The 1µs (typ) glitch filter on the DI receiver is enabled.
RXDIS	3	0 = RX logic output is enabled. 1 = RX logic output is disabled. C/Q input current is reduced when RXDIS = 1. RX is high impedance when RXDIS = 1.
RXFILTER	2	0 = The 1µs (typ) glitch filter on the C/Q receiver is disabled. 1 = The 1µs (typ) glitch filter on the C/Q receiver is enabled.
CQ_Q	0	Use the CQ_Q bit to control the C/Q driver output. See Table 3 for more information.

CQCONFIG (0x07)

BIT	7	6	5	4	3	2	1	0
Field	CQSLEW[1:0]		CQ_PD	CQ_PU	CQ_NPN	CQ_PP	INVCQ	CQ_EN
Reset	00		0	0	0	0	0	0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
CQSLEW	7:6	The CQSLEW[1:0] bits set the typical rising and falling times on the C/Q driver. 00 = 0.15µs (typ, rising), 0.16µs (typ, falling) 01 = 0.3µs (typ, rising), 0.33µs (typ, falling) 10 = 0.9µs (typ, rising), 0.8µs (typ, falling) 11 = 3.3µs (typ, rising), 3.3µs (typ, falling)
CQ_PD	5	0 = The 300µA (typ) weak pulldown current sink on the C/Q driver is disabled. 1 = The 300µA (typ) weak pulldown current sink on the C/Q driver is enabled. When configured as PNP or NPN, the weak pulldown current sink on C/Q is enabled when the driver is enabled and CQ_PD is 1.
CQ_PU	4	0 = The 300µA (typ) weak pullup current source on the C/Q driver is disabled. 1 = The 300µA (typ) weak pullup current source on the C/Q driver is enabled.
CQ_NPN	3	0 = The C/Q driver is in PNP mode (CQ_PP = 0) or push-pull mode (CQ_PP = 1). 1 = The C/Q driver is in NPN mode (CQ_PP = 0) or push-pull mode (CQ_PP = 1).
CQ_PP	2	0 = The C/Q driver is in PNP mode (CQ_NPN = 0) or NPN mode (CQ_NPN = 1). 1 = The C/Q driver is in push-pull mode.
INVCQ	1	0 = The C/Q logic is inverted compared to TX and RX. 1 = The C/Q logic is the same as TX and RX.
CQ_EN	0	0 = The C/Q driver is disabled. The C/Q receiver remains enabled when CQ_EN = 0 if RXDIS = 0. 1 = The C/Q driver is enabled.

DICONFIG (0x08)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	INVDI	LIDIS
Reset	–	–	–	–	–	–	0	0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
INVDI	1	0 = The DI logic is inverted compared to LI. 1 = The DI logic is the same as LI.
LIDIS	0	0 = LI is enabled. 1 = LI is disabled. LI is high impedance when disabled.

CLKCONFIG (0x09)

BIT	7	6	5	4	3	2	1	0
Field	ENCLKTRIM	–	–	–	CLKDIV[2:0]			MCLKDIS
Reset	0	–	–	–	010			0
Access Type	Write, Read	–	–	–	Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION
ENCLKTRIM	7	0 = Fine trimming of the MCLK frequency is disabled. 1 = Fine trimming of the MCLK frequency is enabled. Set the bits in the CLKTRIM register to trim the MCLK frequency.
CLKDIV	3:1	The CLKDIV[2:0] bits set the internal clock divider ratio. 000 = MCLK frequency is 3.686MHz (typ). 001 = MCLK frequency is 7.373MHz (typ). 010 = MCLK frequency is 14.74MHz (typ). 011 = MCLK frequency is 29.49MHz (typ). 100 = MCLK frequency is 1.843MHz (typ).
MCLKDIS	0	0 = MCLK is enabled. 1 = MCLK is disabled. MCLK is high impedance when disabled.

CLKTRIM (0x0A)

BIT	7	6	5	4	3	2	1	0
Field	CKTRIM[7:0]							
Reset	0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
CKTRIM	7:0	The CKTRIM[7:0] bits are used to trim the internally generated MCLK frequency when ENCLKTRIM = 1. The bits are binary coded, centered to 0 from 0x80 for -3% to 0xF0 for +3%.

WAKEUP (0x0B)

BIT	7	6	5	4	3	2	1	0
Field	WURQ	–	–	–	–	–	–	–
Reset	0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION
WURQ	7	0 = No wake-up pulse is generated by the MAX22515. 1 = Generate wake-up pulse on the C/Q line.

CHIPID (0x0C)

BIT	7	6	5	4	3	2	1	0
Field	CHIPID[7:0]							
Reset	0b00000011							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CHIPID	7:0	The CHIPID[7:0] bits identify the revision of the MAX22515.

Applications Information

MCLK Microcontroller Clocking

The MCLK output produces a clock that can be used for UART clocking.

Select the frequency of the MCLK output (in I^2C mode) by setting the CLKDIV[2:0] bits in the CLKCONFIG register. Available MCLK frequencies are 1.843MHz (typ), 3.686MHz (typ), 7.373MHz (typ), 14.74MHz (typ), and 29.49MHz (typ). The MCLK frequency can be further adjusted by setting the ENCKTRIM bit in the CLKCONFIG register to 1 and writing the CKTRIM bits in the CLKTRIM register.

Jitter on the MCLK output signal depends on the selected frequency. Typical jitter values range from 0.08% at a frequency of 1.843MHz to 0.33% at the 29.49MHz frequency. See Table 2.

MCLK is enabled by default and the switching frequency is 14.74MHz (typ).

In pin mode, the MCLK output frequency cannot be changed.

MCLK voltage output levels are referenced to the V_L logic supply.

Table 2. MCLK Jitter and Programmable Frequencies

MCLK PROGRAMMED FREQUENCY (MHz)	MCLK CALCULATED PERIOD (ns)	MCLK MEASURED JITTER, RMS (ps)	MCLK JITTER, RMS (% OF PERIOD)
29.49	33.91	110.6	0.33
14.74	67.84	187.9	0.28
7.373	135.63	316.6	0.23
3.686	271.30	561	0.21
1.843	542.59	433.8	0.08

Maxim calibrates the MCLK frequency for lowest error at T_A = +25°C.

EMC Protection

The MAX22515 features integrated surge protection of ±1.2kV/500Ω for 8µs/20µs surge line-to-line and line-to-ground on the C/Q, DI, V_{24}, and GND pins.

External TVS diodes are required to meet higher levels of surge protection. Ensure that the TVS diode peak clamping voltage is within the *Absolute Maximum Ratings* voltage.

Power Dissipation and Thermal Considerations

Ensure that the total power dissipation in the MAX22515 is less than the limit in the *Absolute Maximum Ratings*. Total power dissipation for the MAX22515 is calculated using the following equation:

$$P_{TOTAL} = P_Q + P_{V5} + P_{V33} + P_{C/Q}$$

where:

P_Q = Quiescent power dissipated in MAX22515

$P_{C/Q}$ = Power dissipated in the C/Q driver

P_{V33} and P_{V5} = Power dissipated by the internal linear regulators

Quiescent power dissipated in the MAX22515 is calculated as:

$$P_Q = [I_{24} \times V_{24}(max)] + [I_5 \times V_5]$$

Power dissipated in the C/Q driver is calculated as:

$$P_{C/Q} = I_{C/Q}(max)^2 x R_{ON}$$

$I_{C/Q}$ is the load current driven by the C/Q driver and R_{ON} is the driver on-resistance.

Power dissipated in the 5V linear regulator (V_5) is calculated as:

$P_{V5} = (V_{LIN} - V_5)xI_{5LOAD}$

I_{5LOAD} includes both the load current on the V_5 regulator and the 3.3V regulator.

Power dissipated in the 3.3V linear regulator (V_{33}) is calculated as:

$P_{V33} = 1.7V \times I_{33LOAD}$

I_{33LOAD} is the load on the 3.3V regulator.

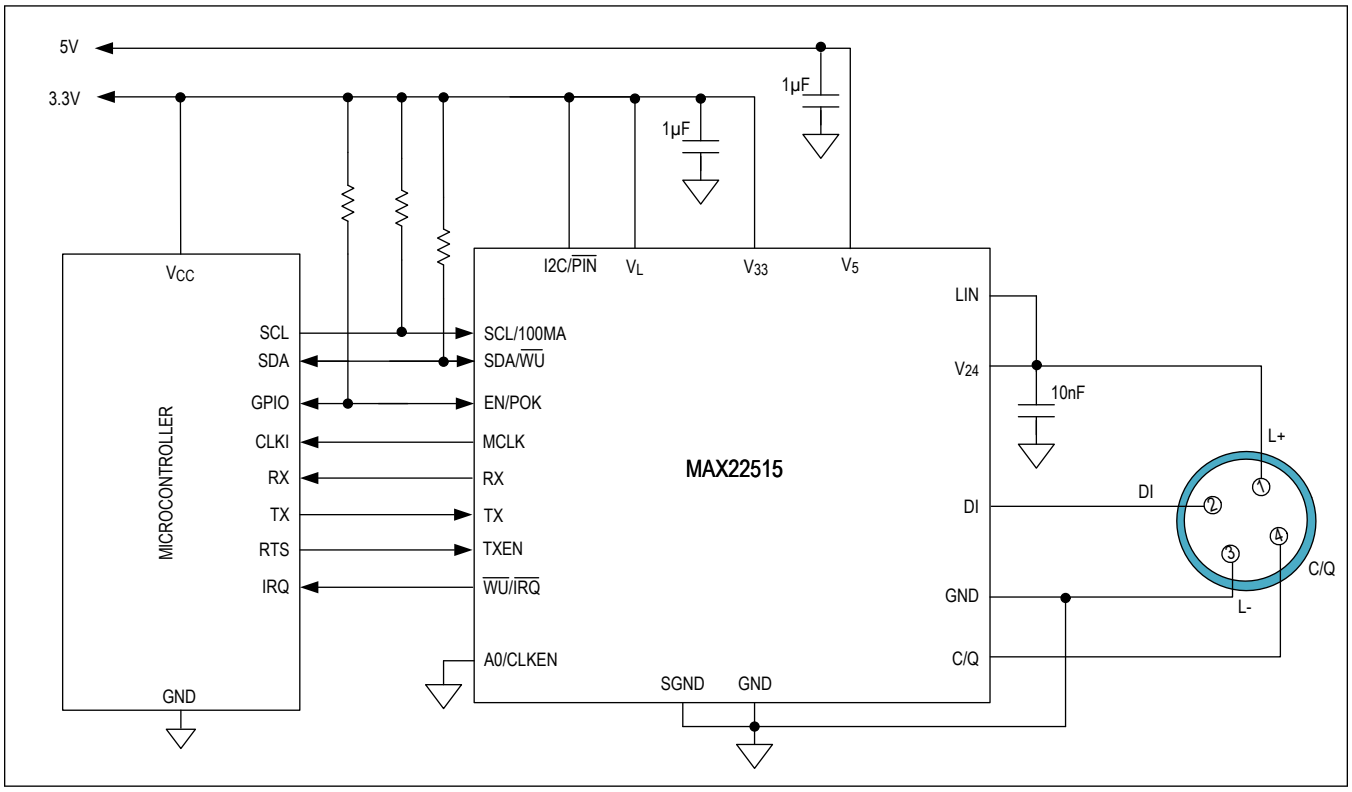
Table 3. C/Q Control

CQ_EN	TXEN	TX	CQ_Q	CQ		
				NPN	PNP	PP
0	X	X	X	Z	Z	Z
1	L	L	0	Z	Z	Z
			1	Z	H	H
		H	0	Z	Z	Z
			1	Z	H	H
	H	L	0	Z	H	H
			1	Z	H	H
		H	0	L	Z	L
			1	Z	H	H

X = Don't Care, Z = High Impedance

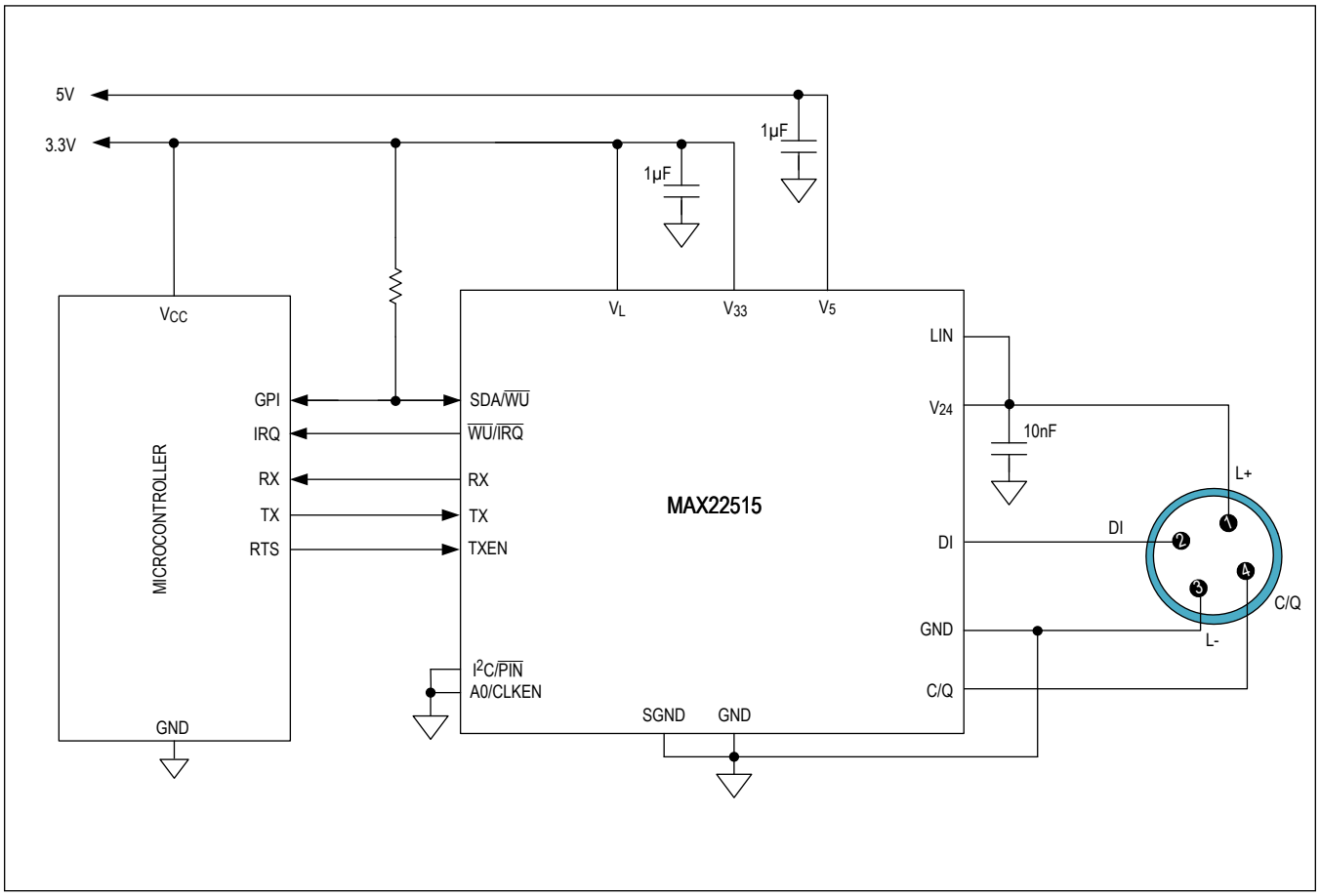
Typical Application Circuits

I²C Application



Typical Application Circuits (continued)

Pin Mode Application



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	BALL PITCH
MAX22515ATG+	-40°C to +125°C	24 TQFN-EP	—
MAX22515ATG+T	-40°C to +125°C	24 TQFN-EP	—
MAX22515AWP+	-40°C to +125°C	20 WLP	0.5mm
MAX22515AWP+T	-40°C to +125°C	20 WLP	0.5mm

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/19	Initial release	—
1	7/19	Marked MAX22515ATG+ and MAX22515ATG+T as future parts in the *Ordering Information* table	34
2	9/19	Updated *Outline Number*, Figure 5; corrected typo	1, 3, 12
3	9/19	Removed future product designation from MAX22515ATG+ and MAX22515ATG+T in the *Ordering Information* table	34
4	10/19	Updated the *Electrical Characteristics* section	5
5	7/20	Updated the *Electrical Characteristics*, *Wake-up Detection, Wake-Up Generation (I^2C Mode Only)* and *MCLK Microcontroller Clocking* sections, and the CLKCONFIG and CHIPID registers	8, 21, 31–33
6	1/21	Update *Table 3;* corrected typo	35
7	4/21	Updated the *General Description, Benefits and Features, Electrical Characteristics*, *Pin Mode, Using the MAX22515 as a Master Transceiver (I^2C Mode Only),* and *MCLK Microcontroller Clocking*, and the *Typical Application Circuits* section; updated the CQCONFIG(0x07) register and the CLDIS bit in the CURRLIM(0x05), Table 3, and added new TOC16 and renumbered remaining TOCs	1, 5, 10, 15–16, 23, 31, 34, 35–36

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MAX22515ATG+ MAX22515AWP+T MAX22515ATG+T