19-1639; Rev 1; 10/06

Octal SMBus-to-Parallel I/O Expanders

General Description

The MAX1608/MAX1609 provide remote input/output (I/O) expansion through an SMBus™ 2-wire serial interface. Each device has eight high-voltage open-drain outputs that double as TTL-level logic inputs, providing continuous bidirectional capabilities. The open-drain outputs tailor the MAX1608/MAX1609 for use in load-switching and other level-shifting applications as well as general-purpose I/O applications.

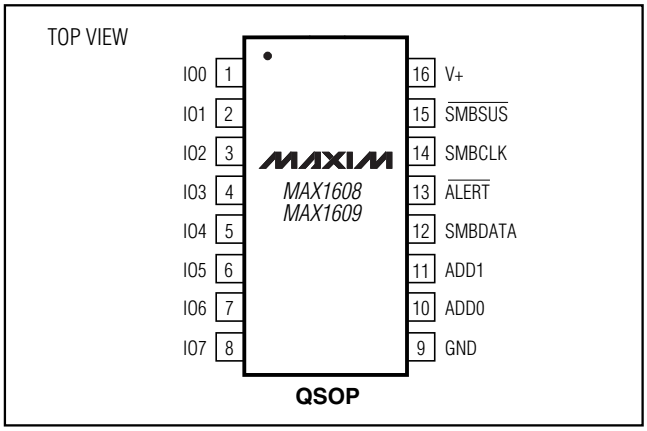
Two complete sets of registers allow the device and its outputs to be toggled between two states using the $\overline{SMBSUS}$ input, without the inherent latency of reprogramming outputs over the serial bus. The eight I/O lines are continuously monitored and can be used as inputs. Each line can generate asynchronous maskable interrupts on the falling edge, the rising edge, or both edges.

For load-switching applications, the MAX1608 is designed to drive n-channel MOSFETs, and its outputs are low upon power-up; the MAX1609 is designed to drive p-channel MOSFETs, and its I/Os are high impedance upon power-up. Other features of both devices include thermal-overload and output-overcurrent protection, ultra-low supply current, and a wide +2.7V to +5.5V supply range. The MAX1608/MAX1609 are available in space-saving 16-pin QSOP packages.

Applications

Parallel I/O Expansion
Power-Plane Switching
Notebook and Desktop Computers
Servers and Workstations
Notebook Docking Stations
Industrial Equipment

Pin Configuration



SMBus is a trademark of Intel Corp.

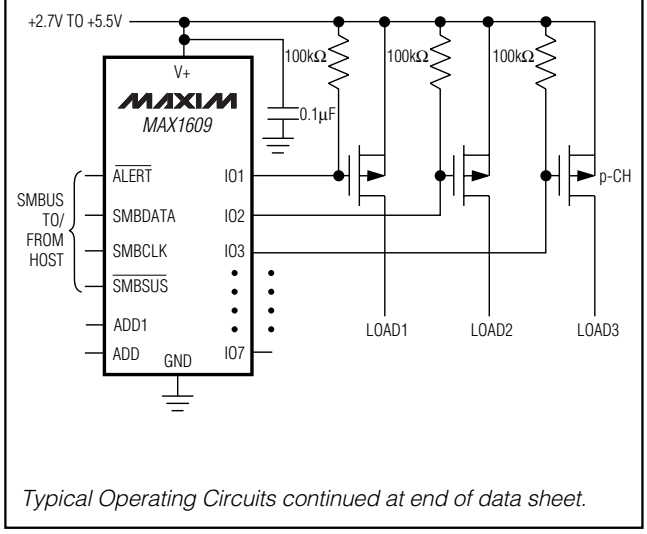
Features

- **Serial-to-Parallel or Parallel-to-Serial Conversions**
- **8 General-Purpose Digital I/O Pins (Withstand +28V)**
- **SMBus 2-Wire Serial Interface**
- **Supports $\overline{SMBSUS}$ Asynchronous Suspend**
- **9 Pin-Selectable Slave Addresses**
- **Outputs High Impedance on Power-Up (MAX1609)**
- **Outputs Low on Power-Up (MAX1608)**
- **2.5µA Supply Current**
- **+2.7V to +5.5V Supply Range**
- **16-Pin QSOP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1608EEE	-40°C to +85°C	16 QSOP
MAX1609EEE	-40°C to +85°C	16 QSOP

Typical Operating Circuits



Typical Operating Circuits continued at end of data sheet.

Octal SMBus-to-Parallel I/O Expanders

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +6V
IO_ to GND .....-0.3V to +30V
IO_ Sink Current .....-1mA to +50mA
SMBCLK, SMBDATA, $\overline{SMBSUS}$ and $\overline{ALERT}$ to GND .....-0.3V to +6V
ADD_ to GND .....-0.3V to (V+ + 0.3V)
SMBDATA and $\overline{ALERT}$ Sink Current .....-1mA to +50mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate 8.3mW/°C above +70°C).....667mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +2.7V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range		2.7		5.5	V
Supply Current (Note 2)	Static, outputs in any combination of on or off states up to 28V		7	18	µA
	Static, all IOs low or pulled to 0		3.5	9	
	SMBus interface operating, clock frequency = 100kHz		7		
POR Threshold Voltage	Falling edge of V+	1.2	1.8	2.5	V
I/O Sink Current	IO_ forced to 0.4V	2			mA
	IO_ forced to 1.0V, V+ = 4.5V	8	13		
I/O Current Limit	IO_, V+ = 4.5V	15	25	50	mA
I/O Leakage Current	IO_ forced to 28V		0.5	2	µA
Propagation Delay	SMBCLK to IO_			2.5	µs
	$\overline{SMBSUS}$ to IO_			1	
	IO_ to $\overline{ALERT}$			10	
IO_ Data Set-Up Time	10% or 90% of I/O to 10% of SMBCLK (Note 3)	10			µs
IO_ Data Hold Time	(Note 3)	3			µs
SMBus Logic Input Voltage Range	$\overline{SMBSUS}$, SMBCLK, SMBDATA (Note 2)	0		5.5	V
Logic Input High Voltage	IO_, $\overline{SMBSUS}$, SMBCLK, SMBDATA	2.1			V
Logic Input Low Voltage	IO_, $\overline{SMBSUS}$, SMBCLK, SMBDATA			0.8	V
SMBus Output Low Sink Current	SMBDATA forced to 0.6V	6			mA
$\overline{ALERT}$ Output Low Sink Current	$\overline{ALERT}$ forced to 0.4V	1			mA
$\overline{ALERT}$ Output High Leakage Current	$\overline{ALERT}$ forced to 5.5V			1	µA
Thermal Shutdown	10°C typical hysteresis		140		°C
Sample Address Input Impedance	ADD_ during address sampling (POR, SPOR, and RAP) to V+ and GND (Note 4)		20		kΩ
Logic Input Current	SMBDATA, SMBCLK, $\overline{SMBUS}$, ADD_	-1		1	µA
SMBus Input Capacitance	SMBCLK, SMBDATA		5		pF

TIMING CHARACTERISTICS

(V+ = +2.7V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

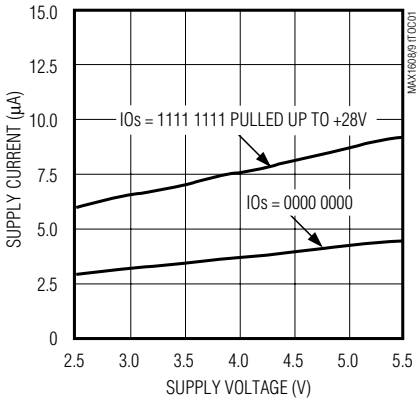
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SMBus Clock Frequency		(Note 5)	DC		100	kHz
SMBCLK Clock Low Time	t_{LOW}	10% to 10% points	4.7			µs
SMBCLK Clock High Time	t_{HIGH}	90% to 90% points	4			µs
SMBus Rise Time		SMBCLK, SMBDATA; 10% to 90% points			1	µs
SMBus Fall Time		SMBCLK, SMBDATA; 90% to 10% points			300	ns
SMBus START Condition Setup Time			4.7			µs
SMBus Repeated START Condition Setup Time	$t_{SU:STA}$	90% to 90% points	500			ns
SMBus START Condition Hold Time	$t_{HD:STA}$	10% of SMBDATA to 90% of SMBCLK	4			µs
SMBus STOP Condition Setup Time	$t_{SU:STO}$	90% of SMBCLK to 10% of SMBDATA	4			µs
SMBus Data Valid to SMBCLK Rising Edge Time	$t_{SU:DAT}$	10% or 90% of SMBDATA to 10% of SMBCLK	250			ns
SMBus Data Hold Time	$t_{HD:DAT}$		300			ns
SMBCLK Falling Edge to SMBDATA Valid Time		Master clocking in data			3	µs

Note 1: Specifications from 0°C to -40°C are guaranteed by design, not production tested.
Note 2: For supply current, SMBus logic inputs driven to 0 or V+.
Note 3: Data hold and set-up times measured from falling edge of 9th clock.
Note 4: Must be driven to GND, V+, or floating. See *SMBus Addressing* section.
Note 5: The SMBus logic block is a static design and will work with clock frequencies down to DC. While slow operation is possible, it violates the 10kHz minimum clock frequency and SMBus specifications and may use excessive space on the bus.

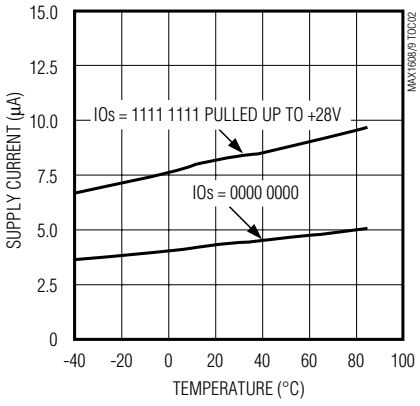
Typical Operating Characteristics

(V+ = +5V, T_A = +25°C, unless otherwise noted.)

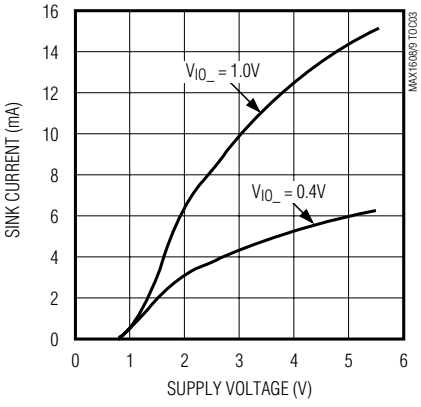
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



IO_ SINK CURRENT vs. SUPPLY VOLTAGE



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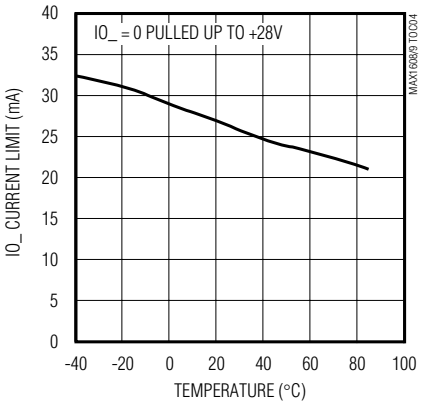
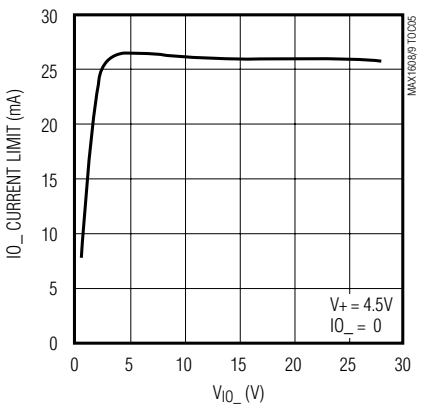
Typical Operating Characteristics (continued)

(V+ = +5V, T_A = +25°C, unless otherwise noted.)

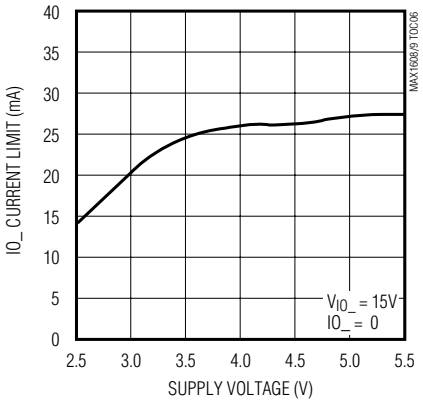
IO_ CURRENT LIMIT vs. TEMPERATURE



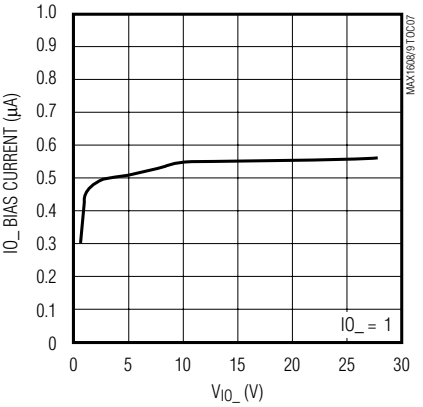
IO_ CURRENT LIMIT vs. IO_ VOLTAGE



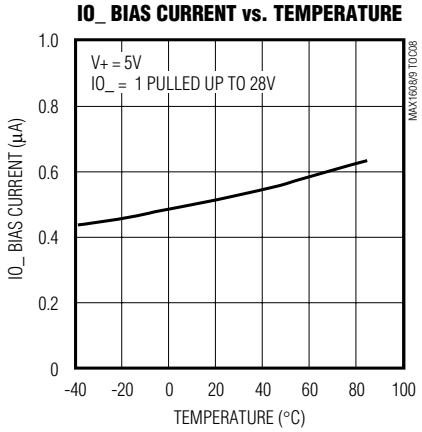
IO_ CURRENT LIMIT vs. SUPPLY VOLTAGE



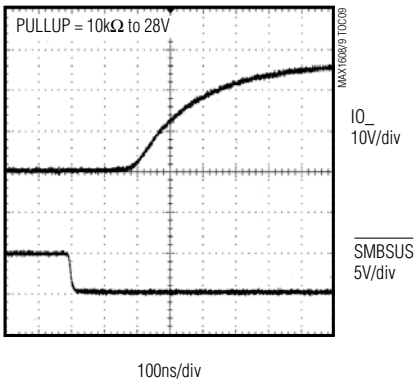
IO_ BIAS CURRENT vs. IO_ VOLTAGE



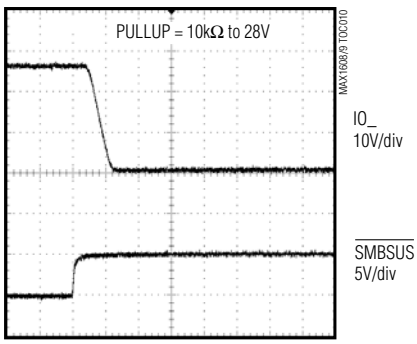
IO_ BIAS CURRENT vs. TEMPERATURE



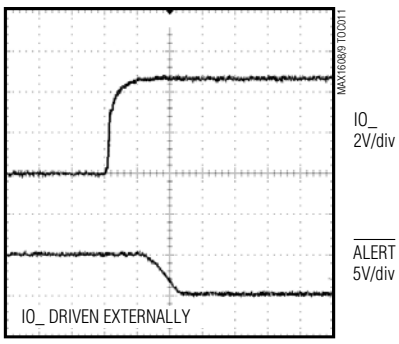
SUSPEND-STATE DELAY (IO_ RISING)



SUSPEND-STATE DELAY (IO_ FALLING)



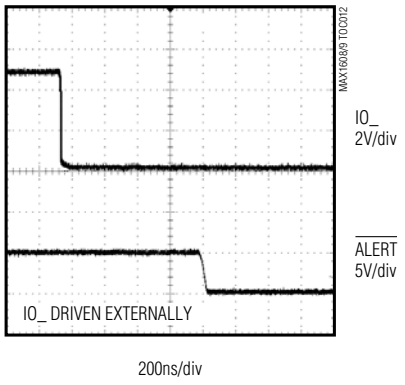
ALERT DELAY (IO_ RISING)



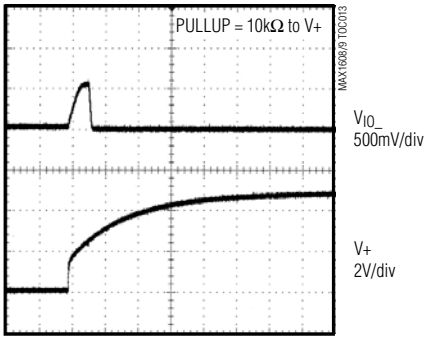
Typical Operating Characteristics (continued)

(V+ = +5V, T_A = +25°C, unless otherwise noted.)

$\overline{\text{ALERT}}$ DELAY (IO_ FALLING)



MAX1608 IO_ POWER-UP RESPONSE



Pin Description

PIN	NAME	FUNCTION
1–8	IO0–IO7	Combined Input/Output. Open-drain output. Can withstand +28V.
9	GND	Ground
10, 11	ADD0, ADD1	SMBus Address Select. See Table 1.
12	SMBDATA	SMBus Serial-Data Input/Output. Open-drain output. Requires external pullup resistor.
13	$\overline{\text{ALERT}}$	Active-Low Interrupt Output. Open-drain output. Requires external pullup resistor.
14	SMBCLK	SMBus Serial Clock Input
15	$\overline{\text{SMBSUS}}$	SMBus Suspend-Mode Control Input. The device enters the state previously stored in the suspend-mode registers if low, or enter the state previously stored in the normal-mode registers if high.
16	V+	Supply Voltage Input, +2.7V to +5.5V. Bypass to GND with a 0.1µF capacitor.

Detailed Description

The MAX1608/MAX1609 convert 2-wire SMBus serial data into eight latched parallel outputs (IO0–IO7). These devices are intended for general-purpose remote I/O expansion. Each device has eight high-voltage open-drain outputs that double as TTL-level logic inputs. Typical applications range from high-side MOSFET load-switch drivers in power-management systems, to push-button switch monitors, to general-purpose digital I/Os.

The MAX1608/MAX1609 include two complete sets of registers, each consisting of one output data register to set the output states and two interrupt mask registers. The $\overline{\text{SMBSUS}}$ line selects which set of registers control the device state. The input register is used to perform readback of the actual IO states.

The MAX1608/MAX1609 operate from a single +2.7V to +5.5V supply with a typical quiescent current of 2.5µA, making them ideal for portable applications. Additionally, the devices include an $\overline{\text{ALERT}}$ function to alert the master of change of condition (Figure 1).

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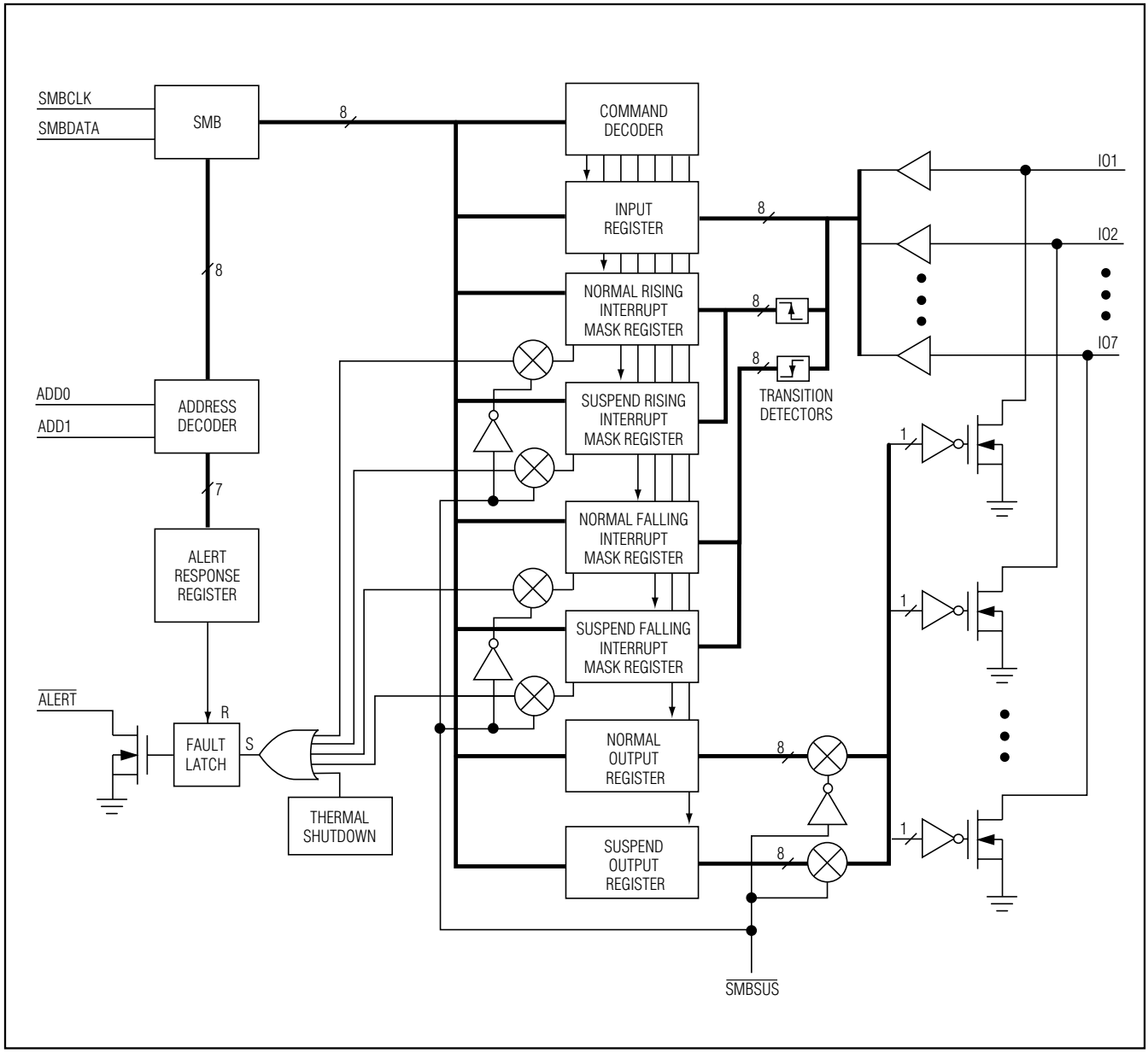

Figure 1. Functional Diagram

SMBus Interface Operation

The SMBus serial interface is a 2-wire interface with multimastering capability. The MAX1608/MAX1609 are 2-wire slave-only devices and employ standard SMBus write-byte, send-byte, read-byte, and receive-byte protocols (Figure 2) as documented in System Management Bus Specification v1.08 (available at www.sbs-forum.org). SMBDATA and SMBCLK are Schmitt-triggered inputs that can accommodate slower edges; however, the rising and falling edges should still be faster than 1µs and 300ns, respectively.

Communication starts with the master signaling the beginning of a transmission with a START condition, which is a high-to-low transition on SMBDATA while SMBCLK is high. When the master has finished communicating with the slave, it issues a STOP condition, which is a low-to-high transition on SMBDATA while SMBCLK is high (Figures 3 and 4). The bus is then free for another transmission from any master on the bus.

The address byte, command byte, and data byte are transmitted between the START and STOP conditions. Figures 3 and 4 show the timing diagrams for signals on the 2-wire interface. The SMBDATA state is allowed to change only while SMBCLK is low, except for the START and STOP conditions. Data is transmitted in 8-bit words and is sampled on the rising edge of SMBCLK. Nine clock cycles are required to transfer each byte in or out of the MAX1608/MAX1609 (Figure 2), since either the master or the slave acknowledges receipt of the correct byte during the ninth clock. The IC responds to the address selected by the ADD0 and ADD1 pins (Table 1).

If the MAX1608/MAX1609 receive the correct slave address followed by $R\overline{W}$ = 0, the selected device expects to receive 1 or 2 bytes of information. If the device detects a START or STOP condition prior to clocking in a full additional byte of data, it considers this an error condition and disregards all of the data. If no error occurs, the registers are updated immediately after the falling edge of the acknowledge clock pulse (Figure 5). If the MAX1608/MAX1609 receive the correct slave address followed by $R\overline{W}$ = 1, the selected device expects to clock out the contents of the previously accessed register during the next byte transfer.

A third interface line ($\overline{SMBSUS}$) is used to execute commands asynchronously from previously stored registers (see *$\overline{SMBSUS}$ (Suspend-Mode) Input* section).

SMBus Addressing

After the START condition, the master transmits a 7-bit address followed by the $R\overline{W}$ bit (Figure 2). If the MAX1608/MAX1609 recognize their own address, it sends an acknowledgment pulse by pulling SMBDATA low.

Table 1. Slave Addresses

ADD0	ADD1	ADDRESS (A6–A0)	
		MAX1608	MAX1609
GND	GND	0010 100	0100 100
GND	High-Z	0010 101	0100 101
GND	V+	0010 110	0100 110
High-Z	GND	1100 100	1101 100
High-Z	High-Z	1100 101	1101 101
High-Z	V+	1100 110	1101 110
V+	GND	0111 000	0110 000
V+	High-Z	0111 001	0110 001
V+	V+	0111 010	0110 010

Each slave responds to only two addresses: its own unique address (set by ADD1 and ADD0, Table 1), and the alert response address (0x19). The device's unique address is determined at power-up, with a software sample-address-pin command (SAP), or a software power-on-reset command (SPOR). The MAX1608/MAX1609 address pins (ADD1–ADD0) are high impedance except when ADD1–ADD0 are sampled, which occurs during power-up and when requested (SPOR, RAP). During sampling, the equivalent input circuit can be described as a resistor-divider from V+ to GND (20kΩ each), which momentarily bias the pins to mid-supply if they are left floating. To set the ADD_ pins high or low, connect or drive the pins to the rails (V+ or GND) to guarantee a correct level detection. During sampling, the pins draw a momentary input bias current (V+ / 20kΩ). Also, stray capacitance in excess of 50pF on the ADD_ pins when floating may cause address recognition problems.

SMBus Commands

The 8-bit command byte (Table 2) is the master index that points to the registers within the MAX1608/MAX1609. The devices include 10 registers: the data registers (NDR1–NDR3, SDR1–SDR3) are accessed through both the read-byte and write-byte protocols (Figure 2), the RSB and MDIF registers are accessed with the read-byte protocols, and the RAP and SPOR registers

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use the send-byte protocol. The shorter receive-byte protocol can be used instead of the read-byte protocol, provided the correct data register was previously selected by a read-byte or write-byte instruction. Use caution with the shorter protocols in multimaster systems, since a second master could overwrite the command byte without informing the first master. The register selected at POR is 0b0000 0000 so that a receive-byte transmission that occurs immediately after initial power-up returns the setting of NDR1. SPOR does not reset the register pointer.

Data Registers

The MAX1608/MAX1609 each have seven data registers, three normal registers, three suspend registers, and one readback register. The $\overline{SMBUS}$ line determines which registers controls the output states and the interrupt mask states (normal registers if $\overline{SUSBUS}$ = 1, suspend registers if $\overline{SMBSUS}$ = 0).

Register 1 (NDR1 and SDR1) sets the state of each of the eight outputs to either low or high impedance. When using an external pullup, high impedance corresponds to an output high. To use the IO_ pins as TTL inputs only, set the corresponding bit high. The MAX1608 powers up with all IO_ pins set low; the MAX1609 powers up with all IO_ pins set to high impedance (Table 3).

Register 2 (NDR2 and SDR2) is used to mask rising-edge triggered interrupts, while register 3 is used to mask falling-edge triggered interrupts. On power-up, all interrupts are masked (Tables 4 and 5).

The IO_ Status Data Register (RSB, Table 6) reads the actual TTL-logic level of the IO_ pins. The IO_ pins are sampled on the falling edge of the third byte's acknowledge (ACK) for a read-byte format, or on the falling edge of the first byte's ACK for a receive-byte protocol (Figure 5). There is a 15µs data-set-up time requirement, due to the slow level translators needed for high-voltage (28V) operation. Data-hold time is 300ns. Do not write to the RSB register because writes to read-only registers are redirected to NDR1. SMBus sends

Write-Byte Format

S	ADDRESS	WR	ACK	COMMAND	ACK	DATA	ACK	P
	7 bits	1b	1b	8 bits	1b	8 bits	1b	

Slave Address

Command Byte: selects which register you are writing to

Data Byte: data goes into the register set by the command byte

Read-Byte Format

S	ADDRESS	WR	ACK	COMMAND	ACK	S	ADDRESS	RD	ACK	DATA	///	P
	7 bits	1b	1b	8 bits	1b		7 bits	1b	1b	8 bits	1b	

Slave Address

Command Byte: selects which register you are reading from

Slave Address: repeated due to change in data-flow direction

Data Byte: reads from the register set by the command byte

Send-Byte Format

S	ADDRESS	WR	ACK	COMMAND	ACK	P
	7 bits	1b	1b	8 bits	1b	

Command Byte: sends command with no data; usually used for one-shot command

Receive-Byte Format

S	ADDRESS	RD	ACK	DATA	///	P
	7 bits	1b	1b	8 bits	1b	

Slave Address

Data Byte: reads data from the register commanded by the last read-byte or write-byte transmission; also used for SMBus Alert Response return address

S = Start condition
P = Stop condition
Shaded = Slave transmission
Ack= Acknowledged = 0
/// = Not acknowledged = 1
WR = Write = 0
RD = Read =1

Figure 2. SMBus Protocols

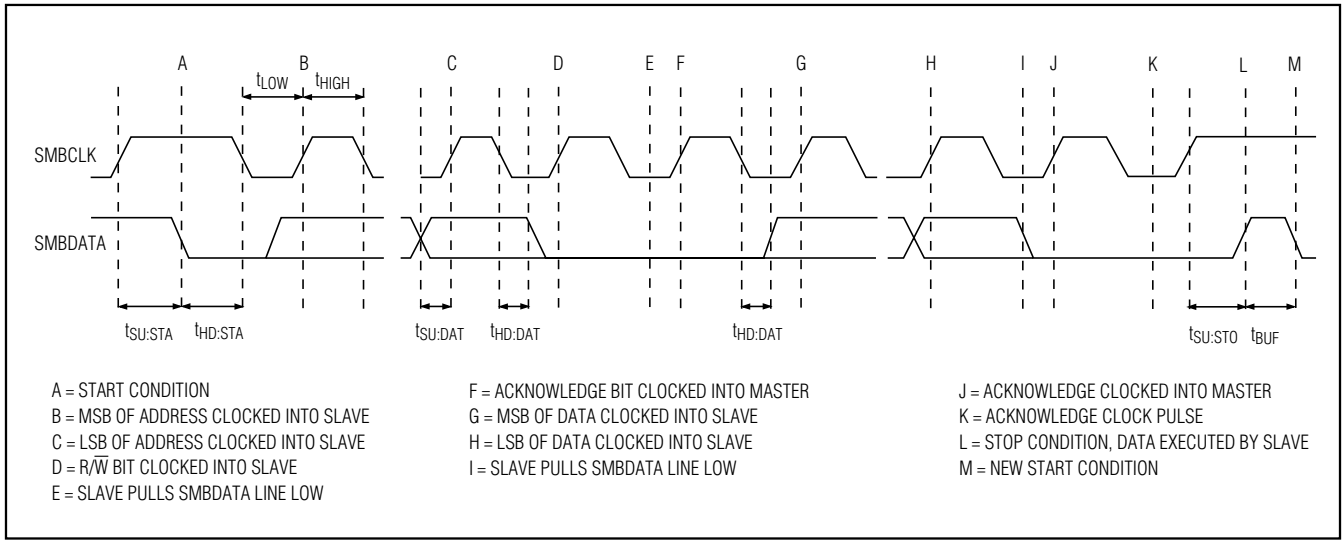

Figure 3. SMBus Write Timing

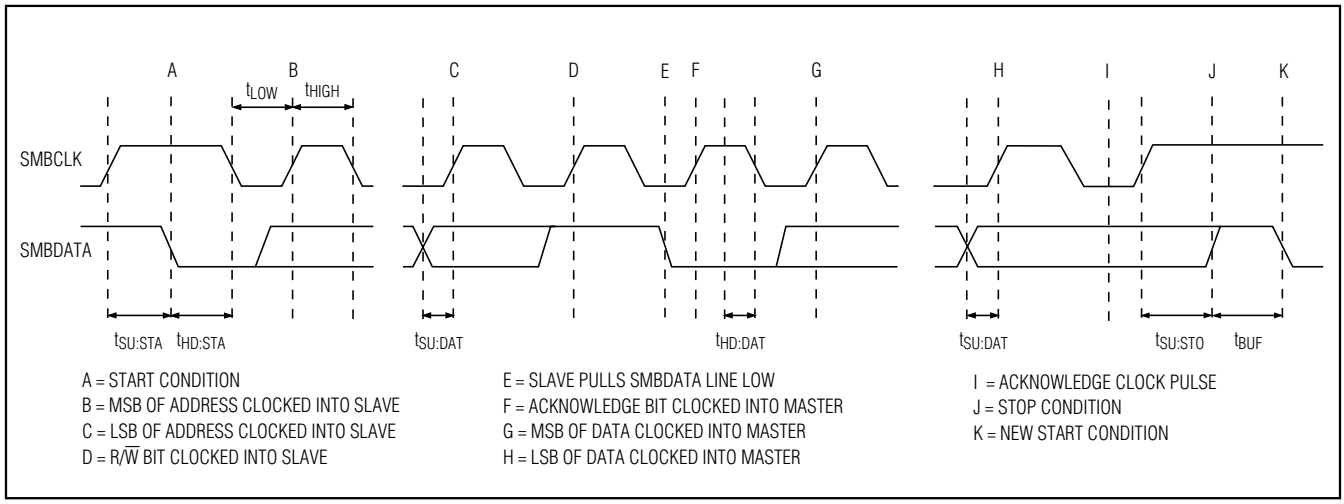

Figure 4. SMBus Read Timing

data MSB first; therefore, IO7, MASK7, and data 7 bit correspond to the MSB (first bit of the data byte).

Other Registers

RAP uses the send-byte protocol to resample the address pins. Do not use read- and write-byte protocols to RAP because data is redirected to NDR1 although the ADD_ pins will be sampled.

SPOR uses the send-byte protocol to resample the address pins and reset the registers to the POR state. Do not use read- and write-byte protocols to SPOR because data is redirected to NDR1 although the function will be performed.

MFID uses the read-byte protocol to access the ID register. Do not use write-byte protocol to MFID because data is redirected to NDR1.

$\overline{\text{SMBSUS}}$ (Suspend-Mode) Input

The state of the $\overline{\text{SMBSUS}}$ input selects which register contents (NDR1 or SDR1) are applied to the IO_ pins and which set of registers are used to mask the interrupts (NDR2, NDR3 or NDR2, SDR3). Driving $\overline{\text{SMBSUS}}$ low selects the suspend-mode registers, while driving $\overline{\text{SMBSUS}}$ high selects the normal registers. This feature allows the system to select between two different I/O configurations asynchronously, eliminating latencies introduced by the serial bus.

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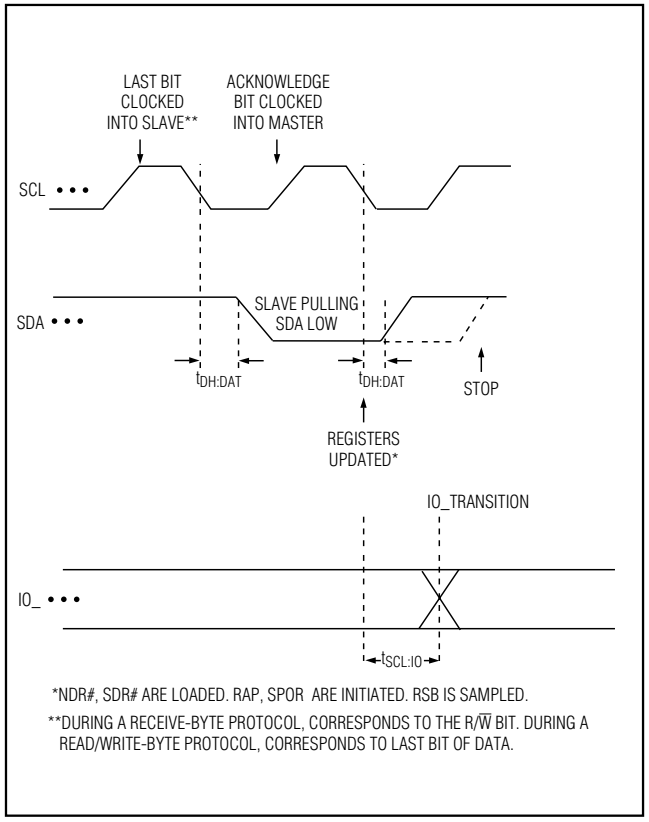


Figure 5. Registers/IO_ Update Timing Diagram

ALERT

The MAX1608/MAX1609 can generate hardware interrupts whenever the logic states of the IO_ pins change or when thermal shutdown occurs. Interrupts are signaled on the $\overline{ALERT}$ pin. The IO_ interrupts can be masked individually through the mask registers. Registers NDR2 and SDR2 mask the IO_ rising-edge interrupts, while NDR3 and SDR3 mask the IO_ falling-edge interrupts. The power-on-reset state masks all interrupts (Tables 4 and 5).

The thermal-shutdown protection also generates an interrupt. This interrupt cannot be masked (see *Thermal Shutdown* section). An interrupt can be cleared with a SPOR or an Alert Response. However, after an interrupt has occurred, masking will not clear it.

Alert Response Address (0b00011001)

The alert response (interrupt pointer) address provides quick fault identification for simple slave devices that cannot initiate communication as a bus master. When a slave device generates an interrupt, the host (bus master) interrogates the bus slave devices through a special receive-byte operation that includes the alert response address (0x19). The offending slave device returns its own address during this receive-byte operation.

The interrupt pointer address can activate several different slave devices simultaneously. If more than one slave attempts to respond, bus arbitration rules apply, with the lowest address code going first. The other device(s) will not generate an acknowledge and will

Table 2. Command-Byte/Register Assignment

REGISTER	COMMAND	POR STATE		FUNCTION
		MAX1608	MAX1609	
NDR1	00h	0000 0000	1111 1111	Normal Data Register 1. Sets the IO_ states.
NDR2	01h	1111 1111	1111 1111	Normal Data Register 2. Masks the L/H interrupt.
NDR3	02h	1111 1111	1111 1111	Normal Data Register 3. Masks the H/L interrupt.
SDR1	03h	0000 0000	1111 1111	Suspend Data Register 1. Sets the IO_ states.
SDR2	04h	1111 1111	1111 1111	Suspend Data Register 2. Masks the L/H interrupt.
SDR3	05h	1111 1111	1111 1111	Suspend Data Register 3. Masks the H/L interrupt.
RSB	06h	—	—	IO_ Status Data Register. Read pin state.
RAP	07h	—	—	Sample the address pins.
SPOR	08h	—	—	Execute software POR and samples address pins.
MFID	FEh	4Dh	4Dh	Read manufacturer ID (ASCII code for "M"axim).

Table 3. Data Register 1 (NDR1 and SDR1) Bit Assignments (Read or Write)

BIT	NAME	POR STATE		FUNCTION
		MAX1608	MAX1609	
7	IO7	0	1	Sets IO7 state. 0 = on (low state), 1 = off (high-impedance).
6	IO6	0	1	Sets IO6 state. 0 = on (low state), 1 = off (high-impedance).
5	IO5	0	1	Sets IO5 state. 0 = on (low state), 1 = off (high-impedance).
4	IO4	0	1	Sets IO4 state. 0 = on (low state), 1 = off (high-impedance).
3	IO3	0	1	Sets IO3 state. 0 = on (low state), 1 = off (high-impedance).
2	IO2	0	1	Sets IO2 state. 0 = on (low state), 1 = off (high-impedance).
1	IO1	0	1	Sets IO1 state. 0 = on (low state), 1 = off (high-impedance).
0	IO0	0	1	Sets IO0 state. 0 = on (low state), 1 = off (high-impedance).

Table 4. Data Register 2 (NDR2 and SDR2) Bit Assignments (Read or Write)

BIT	NAME	POR STATE	FUNCTION
7	MASKH7	1	Masks IO7 low-to-high interrupt. 0 = interrupts, 1 = masked.
6	MASKH6	1	Masks IO6 low-to-high interrupt. 0 = interrupts, 1 = masked.
5	MASKH5	1	Masks IO5 low-to-high interrupt. 0 = interrupts, 1 = masked.
4	MASKH4	1	Masks IO4 low-to-high interrupt. 0 = interrupts, 1 = masked.
3	MASKH3	1	Masks IO3 low-to-high interrupt. 0 = interrupts, 1 = masked.
2	MASKH2	1	Masks IO2 low-to-high interrupt. 0 = interrupts, 1 = masked.
1	MASKH1	1	Masks IO1 low-to-high interrupt. 0 = interrupts, 1 = masked.
0	MASKH0	1	Masks IO0 low-to-high interrupt. 0 = interrupts, 1 = masked.

continue to hold the $\overline{ALERT}$ pin low until it is allowed to clear its own interrupt.

Clearing the interrupt has no effect on the state of the status registers.

Input/Output Pins

Each IO_ pin is protected by an internal 20mA (typical) current-limit circuit. Typical pulldown on-resistance at V_{CC} = +2.7V and +5.5V is 100Ω and 66Ω, respectively. When the IO_ is high impedance, it actually has a 0.5µA pulldown current source included as part of the read-back functionality.

External pullup resistors and IO_ sink capability can affect the outputs' rise and fall times. When using the MAX1608/MAX1609 to control an external MOSFET in power-switching applications, pullup and/or series resistance can be used together with the MOSFET's gate capacitance or additional external capacitance (Figure 6) to control the transition time of the switched source.

The input logic levels are TTL compatible and are sampled during a readback SMBus transmission (see RSB register in *Data Registers* section).

Power-On Reset

The MAX1608/MAX1609s' power-on-reset circuit ensures that the IO_ states are defined when V+ is first applied or when the supply dips below the UVLO threshold. The power-on states can also be reset with the SPOR command through the SMBus.

Table 5. Data Register 3 (NDR3 and SDR3) Bit Assignments (Read or Write)

BIT	NAME	POR STATE	FUNCTION
7	MASKL7	1	Masks IO7 high-to-low interrupt. 0 = interrupts, 1 = masked.
6	MASKL6	1	Masks IO6 high-to-low interrupt. 0 = interrupts, 1 = masked.
5	MASKL5	1	Masks IO5 high-to-low interrupt. 0 = interrupts, 1 = masked.
4	MASKL4	1	Masks IO4 high-to-low interrupt. 0 = interrupts, 1 = masked.
3	MASKL3	1	Masks IO3 high-to-low interrupt. 0 = interrupts, 1 = masked.
2	MASKL2	1	Masks IO2 high-to-low interrupt. 0 = interrupts, 1 = masked.
1	MASKL1	1	Masks IO1 high-to-low interrupt. 0 = interrupts, 1 = masked.
0	MASKL0	1	Masks IO0 high-to-low interrupt. 0 = interrupts, 1 = masked.

Table 6. IO_ Status Data Register (RSB) Bit Assignments (Read Only)

BIT	NAME	FUNCTION
7	DATA7	Indicates the current state of IO7. 1 = high, 0 = low.
6	DATA6	Indicates the current state of IO6. 1 = high, 0 = low.
5	DATA5	Indicates the current state of IO5. 1 = high, 0 = low.
4	DATA4	Indicates the current state of IO4. 1 = high, 0 = low.
3	DATA3	Indicates the current state of IO3. 1 = high, 0 = low.
2	DATA2	Indicates the current state of IO2. 1 = high, 0 = low.
1	DATA1	Indicates the current state of IO1. 1 = high, 0 = low.
0	DATA0	Indicates the current state of IO0. 1 = high, 0 = low.

The MAX1608's outputs reset to a low state, while the MAX1609's outputs reset to a high-impedance state. Below V+ = 0.8V (typical), the POR states cannot be enforced, and the I/O pins of both devices exhibit increasingly weak pulldown current capability, eventually becoming high impedance.

The MAX1608 is designed for applications that control n-channel MOSFETs, while the MAX1609 is designed to control p-channel MOSFETs. The power-on state keeps the external MOSFETs off at power-up. Both devices are suited for applications that use the parallel input for serial functionality, although IO_s serving as inputs must first be programmed to high impedance when using the MAX1608.

Thermal Shutdown

These devices have internal thermal-shutdown circuitry that sets all outputs to a high-impedance state (IO_ pins) when the junction temperature exceeds +140°C typical. Thermal shutdown only occurs during an overload condition on the IO_ pins. The device cycles between thermal shutdown and the overcurrent condition (with 10°C hysteresis) until the overload condition is removed. The device asserts $\overline{\text{ALERT}}$ low while it is in thermal shutdown, indicating this fault status. $\overline{\text{ALERT}}$ will be reasserted immediately after it is cleared if the device is still hot. $\overline{\text{ALERT}}$ can only be completely cleared once the fault condition is removed and the device has cooled. Alternatively, forcing the IO_ to high impedance will allow the junction to cool down.

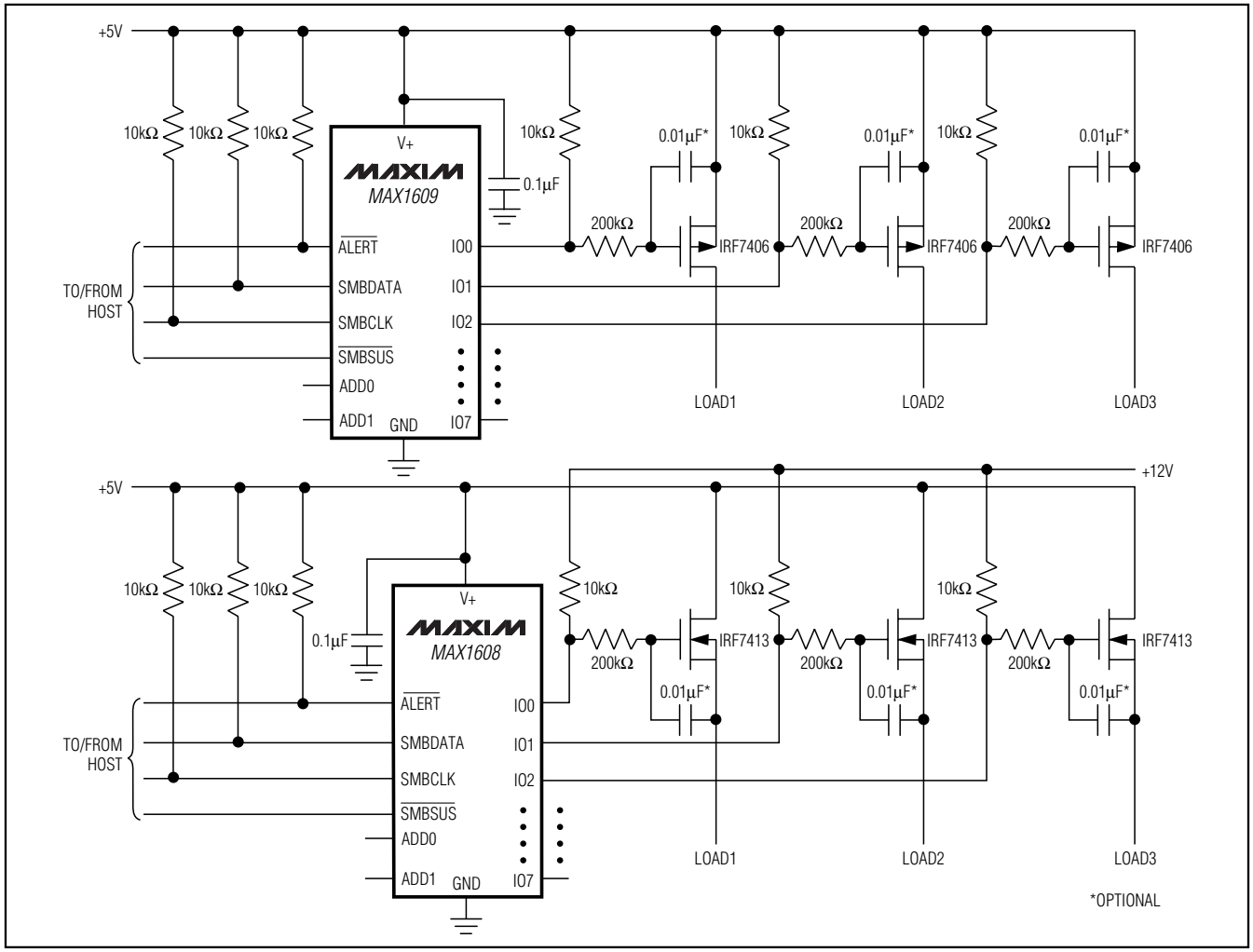


Figure 6. Load Switch with Controlled Turn-On

Application Examples

p-Channel/n-Channel High-Side Load Switch with Controlled Turn-On

In load-switching applications, when a controlled voltage ramp or inrush current limiting is required, add a series resistor to slow the switch turn-on and turn-off times. The external MOSFET gate has a typical capacitance of 150pF to 2000pF, but an optional external capacitance can be added to further slow the switching time (Figure 6). If a slow turn-on time is required, use an n-channel MOSFET with a high-value pullup resistor and no series resistor. Similarly, if a fast turn-on and a slow turn-off are desired, use a p-channel MOSFET with a high-value pullup resistor and no series resistor.

Battery Switch with Back-to-Back MOSFETs

Many battery-operated applications use back-to-back MOSFETs to prevent reverse currents from the load to the supply (Figure 7). This protects the battery from potential damage and isolates the load from the power source.

LED Driver

The MAX1608/MAX1609 can be used as programmable LED drivers (Figure 8). With their low quiescent current, these devices are ideal for use as indicator light drivers on the front panel of a notebook computer.

Octal SMBus-to-Parallel I/O Expanders

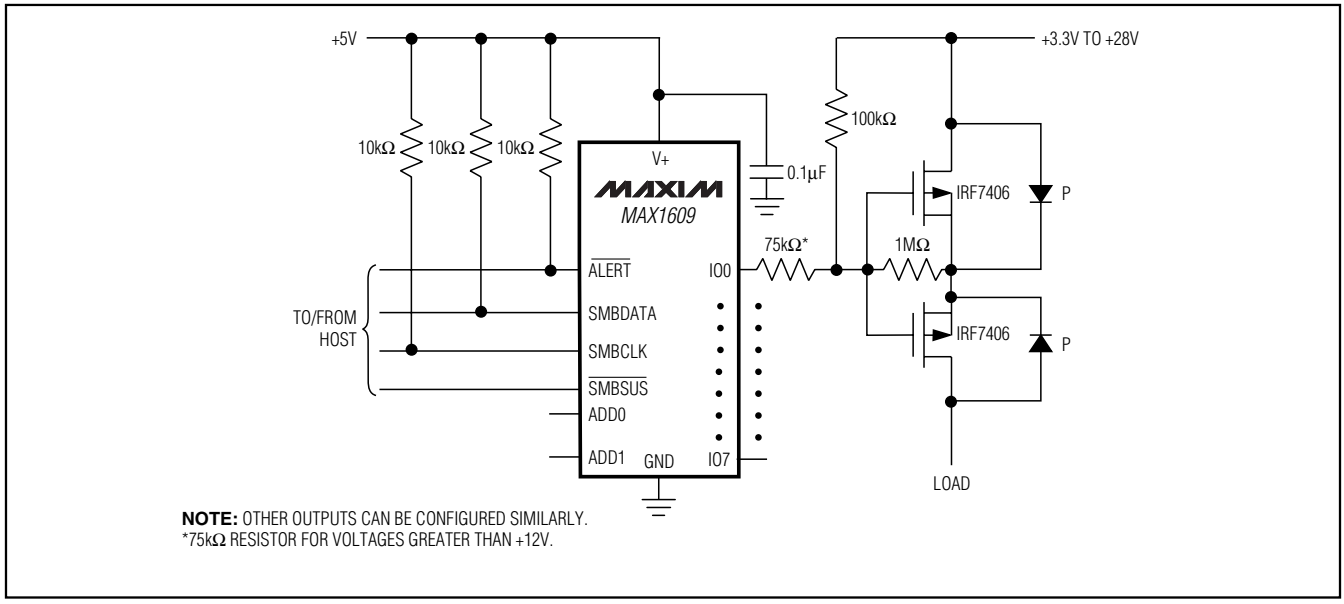


Figure 7. Battery Switch with Back-to-Back MOSFETs

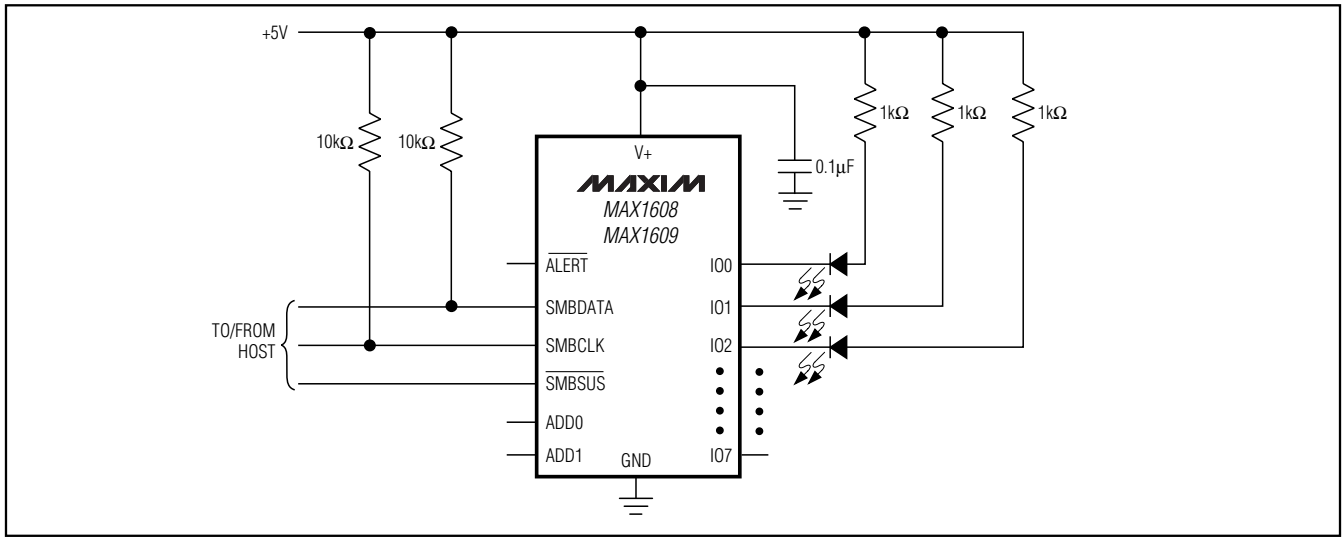


Figure 8. LED Driver

Mechanical Switch Monitor

The MAX1608/MAX1609s' ability to perform IO_ logic-state readback makes them suitable for checking system status. They can be used as an "open-lid indicator," sensing a change in the IO_ and sending an interrupt to the master to indicate a change in status (Figure 9). The same can be done to detect a chassis intrusion, a reset switch, or a card insertion.

Simple High-Voltage Switch

For applications requiring a higher voltage, use a simple resistive divider to protect the gate from breakdown yet allow the MOSFETs to handle higher voltage applications (Figure 10).

Chip Information

TRANSISTOR COUNT: 5762

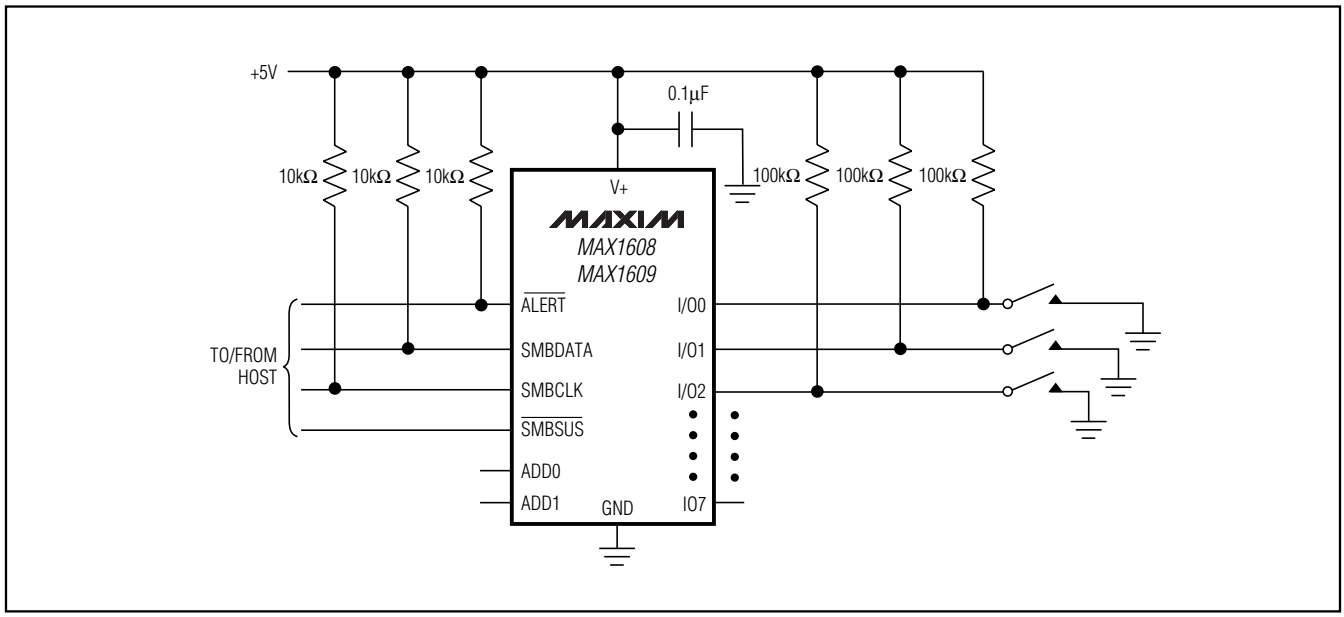


Figure 9. Mechanical Switch Monitor

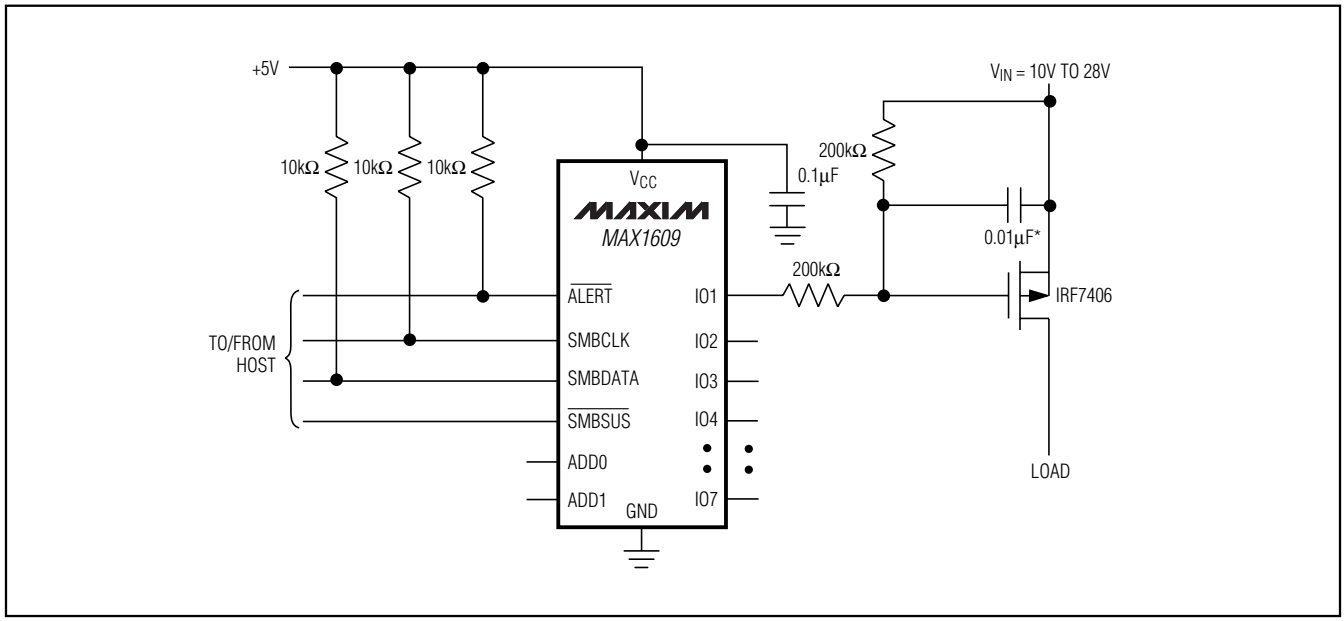
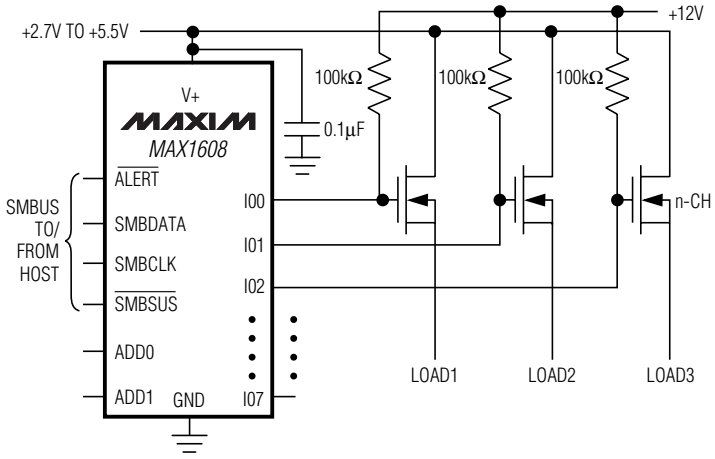


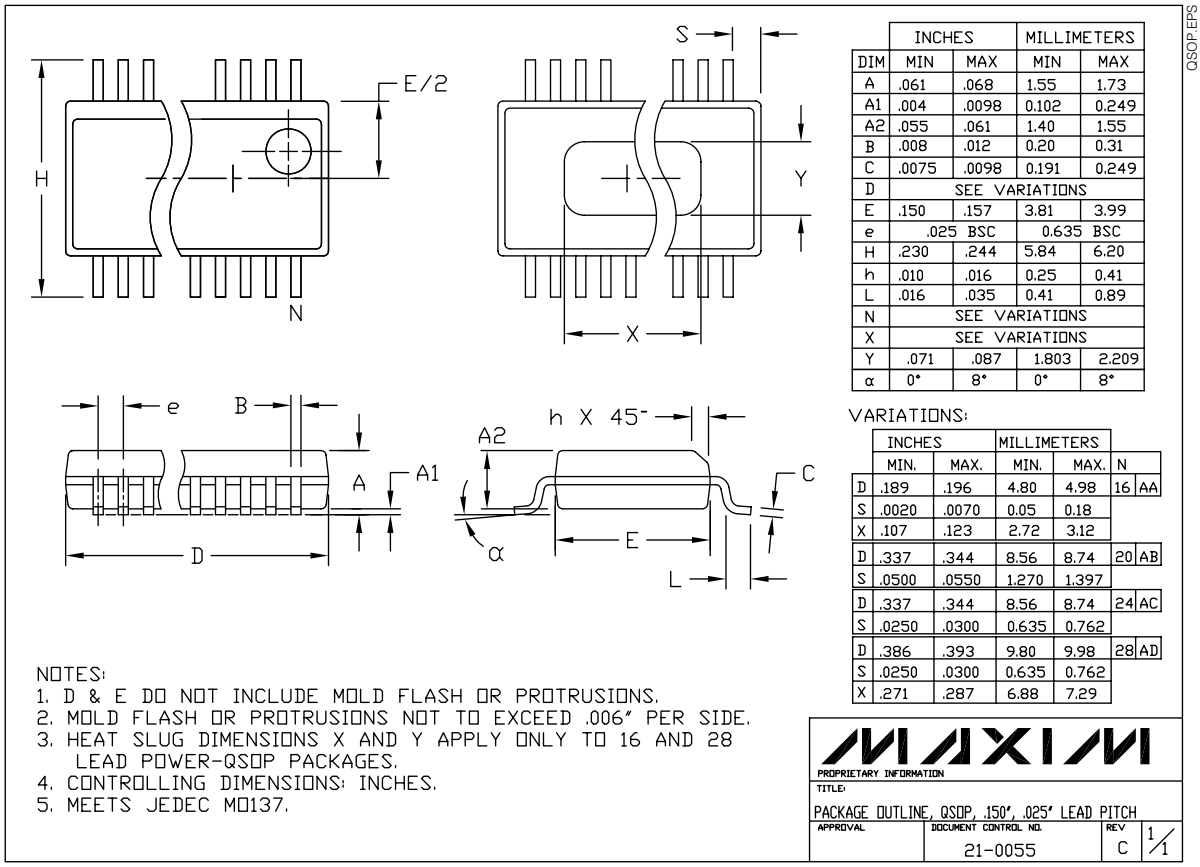
Figure 10. Simple High-Voltage Switch

Typical Operating Circuits (continued)



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

Note: *MAX1608/MAX1609 do not have a heat slug.*

Revision History

Pages changed at Rev 1: 1, 12, 17

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