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## 42V, 300mA, Ultra-Small, High-Efficiency, Synchronous Step-Down DC-DC Converters

# MAX15462

### General Description

The MAX15462 high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operates over a 4.5V to 42V input voltage range. The converter delivers output current up to 300mA at 3.3V (MAX15462A), 5V (MAX15462B), and adjustable output voltages (MAX15462C). The device operates over the -40°C to +125°C temperature range and is available in a compact 8-pin (2mm x 2mm) TDFN package. Simulation models are available.

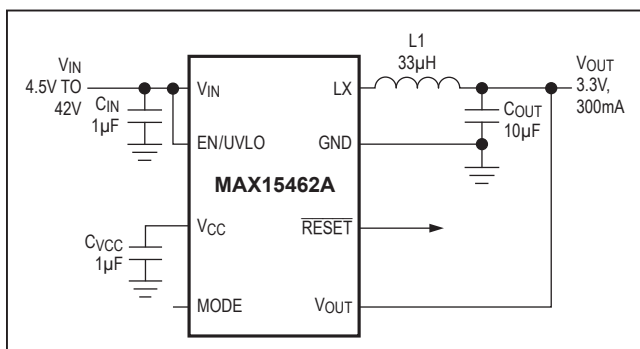
The device employs a peak-current-mode control architecture with a MODE pin that can be used to operate the device in the pulse-width modulation (PWM) or pulse-frequency modulation (PFM) control schemes. PWM operation provides constant frequency operation at all loads and is useful in applications sensitive to variable switching frequency. PFM operation disables negative inductor current and additionally skips pulses at light loads for high efficiency. The low-resistance on-chip MOSFETs ensure high efficiency at full load and simplify the PCB layout.

To reduce input inrush current, the device offers an internal soft-start. The device also incorporates an EN/UVLO pin that allows the user to turn on the part at the desired input-voltage level. An open-drain RESET pin can be used for output-voltage monitoring.

### Applications

- Process Control
- Industrial Sensors
- 4–20mA Current Loops
- HVAC and Building Control
- High-Voltage LDO Replacement
- General-Purpose Point of Load

### Typical Operating Circuit



### Benefits and Features

- Eliminates External Components and Reduces Total Cost
  - No Schottky—Synchronous Operation for High Efficiency and Reduced Cost
  - Internal Compensation
  - Internal Feedback Divider for Fixed 3.3V, 5V Output Voltages
  - Internal Soft-Start
  - All-Ceramic Capacitors, Ultra-Compact Layout
- Reduces Number of DC-DC Regulators to Stock
  - Wide 4.5V to 42V Input Voltage Range
  - Fixed 3.3V and 5V Output Voltage Options
  - Adjustable 0.9V to 0.89 x VIN Output Voltage Option
  - Delivers Up to 300mA Load Current
  - Configurable Between PFM and Forced-PWM Modes
- Reduces Power Dissipation
  - Peak Efficiency = 92%
  - PFM Feature for High Light-Load Efficiency
  - Shutdown Current = 2.2µA (typ)
- Operates Reliably in Adverse Industrial Environments
  - Hiccup-Mode Current Limit and Autoretry Startup
  - Built-In Output Voltage Monitoring with Open-Drain RESET Pin
  - Programmable EN/UVLO Threshold
  - Monotonic Startup into Prebiased Output
  - Overtemperature Protection
  - High Industrial -40°C to +125°C Ambient Operating Temperature Range/-40°C to +150°C Junction Temperature Range

[Ordering Information](#) appears at end of data sheet.

19-7552; Rev 2; 12/23

**Absolute Maximum Ratings**

V <sub>IN</sub> to GND.....	-0.3V to +48V	Continuous Power Dissipation (T <sub>A</sub> = +70°C)
EN/UVLO to GND.....	-0.3V to +48V	8-Pin TDFN (derate 6.2mW/°C above +70°C) .....
LX to GND.....	-0.3V to V <sub>IN</sub> + 0.3V	496mW
V <sub>CC</sub> , FB/V <sub>OUT</sub> , RESET to GND .....	-0.3V to +6V	Junction Temperature.....
MODE to GND.....	-0.3V to V <sub>CC</sub> + 0.3V	+150°C
LX total RMS Current.....	±800mA	Storage Temperature Range .....
Output Short-Circuit Duration .....	Continuous	-65°C to +150°C
		Soldering Temperature (reflow).....
		+260°C
		Lead Temperature (soldering, 10s) .....
		+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Junction temperature greater than +125°C degrades operating lifetimes.

**Package Thermal Characteristics (Note 1)**

TDFN

Junction-to-Ambient Thermal Resistance (θ <sub>JA</sub> ) .....	+162°C/W
Junction-to-Case Thermal Resistance (θ <sub>JC</sub> ).....	+20°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to <https://www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages.html>.

**Electrical Characteristics**

(V<sub>IN</sub> = 24V, V<sub>GND</sub> = 0V, C<sub>IN</sub> = C<sub>VCC</sub> = 1µF, V<sub>EN/UVLO</sub> = 1.5V, LX = MODE = RESET = unconnected; T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>INPUT SUPPLY (V<sub>IN</sub>)</b>						
Input Voltage Range	V <sub>IN</sub>		4.5		42	V
Input Shutdown Current	I <sub>IN-SH</sub>	V <sub>EN/UVLO</sub> = 0V, shutdown mode		2.2	4	µA
Input Supply Current	I <sub>Q-PFM</sub>	MODE = unconnected, FB/V <sub>OUT</sub> = 1.03 x FB/V <sub>OUT-REG</sub>		95	160	µA
	I <sub>Q-PWM</sub>	Normal switching mode, V <sub>IN</sub> = 24V		2.5	4	mA
<b>ENABLE/UVLO (EN/UVLO)</b>						
EN/UVLO Threshold	V <sub>ENR</sub>	V <sub>EN/UVLO</sub> rising	1.19	1.215	1.24	V
	V <sub>ENF</sub>	V <sub>EN/UVLO</sub> falling	1.06	1.09	1.15	
	V <sub>EN-TRUESD</sub>	V <sub>EN/UVLO</sub> falling, true shutdown		0.75		
EN/UVLO Input Leakage Current	I <sub>EN/UVLO</sub>	V <sub>EN/UVLO</sub> = 42V, T <sub>A</sub> = +25°C	-100		+100	nA
<b>LDO (V<sub>CC</sub>)</b>						
V <sub>CC</sub> Output Voltage Range	V <sub>CC</sub>	6V < V <sub>IN</sub> < 42V, 0mA < I <sub>VCC</sub> < 10mA	4.75	5	5.25	V
V <sub>CC</sub> Current Limit	I <sub>VCC-MAX</sub>	V <sub>CC</sub> = 4.3V, V <sub>IN</sub> = 12V	13	30	50	mA
V <sub>CC</sub> Dropout	V <sub>CC-DO</sub>	V <sub>IN</sub> = 4.5V, I <sub>VCC</sub> = 5mA		0.15	0.3	V
V <sub>CC</sub> UVLO	V <sub>CC-UVR</sub>	V <sub>CC</sub> rising	4.05	4.18	4.3	V
	V <sub>CC-UVF</sub>	V <sub>CC</sub> falling	3.7	3.8	3.95	

## Electrical Characteristics (continued)

( $V_{IN} = 24V$ ,  $V_{GND} = 0V$ ,  $C_{IN} = C_{VCC} = 1\mu F$ ,  $V_{EN/UVLO} = 1.5V$ , LX = MODE =  $\overline{RESET}$  = unconnected;  $T_A = -40^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ . All voltages are referenced to GND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER MOSFETs</b>						
High-Side pMOS On-Resistance	$R_{DS-ONH}$	$I_{LX} = 0.3A$ (sourcing)	$T_A = +25^\circ C$	1.35	1.75	$\Omega$
			$T_A = T_J = +125^\circ C$	2.7		
Low-Side nMOS On-Resistance	$R_{DS-ONL}$	$I_{LX} = 0.3A$ (sinking)	$T_A = +25^\circ C$	0.45	0.55	$\Omega$
			$T_A = T_J = +125^\circ C$	0.9		
LX Leakage Current	$I_{LX-LKG}$	$V_{EN/UVLO} = 0V$ , $V_{IN} = 42V$ , $T_A = +25^\circ C$ , $V_{LX} = (V_{GND} + 1V)$ to $(V_{IN} - 1V)$	-1		+1	$\mu A$
<b>SOFT-START (SS)</b>						
Soft-Start Time	$t_{SS}$		3.8	4.1	4.4	ms
<b>FEEDBACK (FB)</b>						
FB Regulation Voltage	$V_{FB-REG}$	MODE = GND, MAX15462C	0.887	0.9	0.913	V
		MODE = unconnected, MAX15462C	0.887	0.915	0.936	
FB Leakage Current	$I_{FB}$	MAX15462C	-100	-25		nA
<b>OUTPUT VOLTAGE (<math>V_{OUT}</math>)</b>						
$V_{OUT}$ Regulation Voltage	$V_{OUT-REG}$	MODE = GND, MAX15462A	3.25	3.3	3.35	V
		MODE = unconnected, MAX15462A	3.25	3.35	3.42	
		MODE = GND, MAX15462B	4.93	5	5.07	
		MODE = unconnected, MAX15462B	4.93	5.08	5.18	
<b>CURRENT LIMIT</b>						
Peak Current-Limit Threshold	$I_{PEAK-LIMIT}$		0.49	0.56	0.62	A
Runaway Current-Limit Threshold	$I_{RUNAWAY-LIMIT}$		0.58	0.66	0.73	A
Negative Current-Limit Threshold	$I_{SINK-LIMIT}$	MODE = GND	0.25	0.3	0.35	A
					0.01	
PFM Current Level	$I_{PFM}$			0.13		A
<b>TIMING</b>						
Switching Frequency	$f_{SW}$		465	500	535	kHz
Events to Hiccup After Crossing Runaway Current Limit				1		Cycles
FB/ $V_{OUT}$ Undervoltage Trip Level to Cause Hiccup			62.5	64.5	66.5	%
Hiccup Timeout				131		ms
Minimum On-Time	$t_{ON-MIN}$			90	130	ns
Maximum Duty Cycle	$D_{MAX}$	FB/ $V_{OUT} = 0.98 \times$ FB/ $V_{OUT-REG}$	89	91.5	94	%

**Electrical Characteristics (continued)**

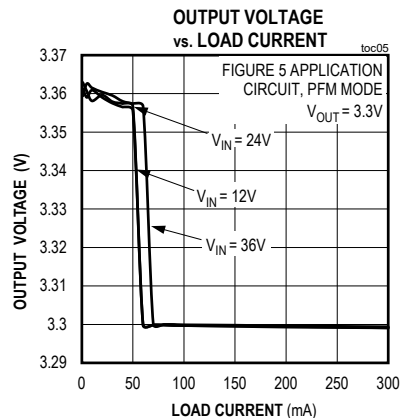
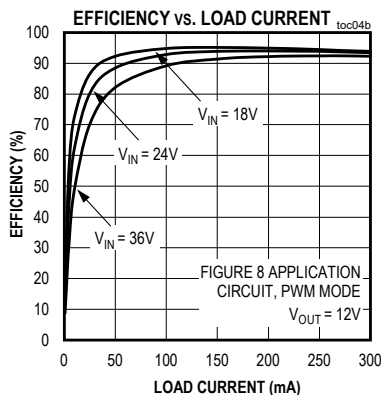
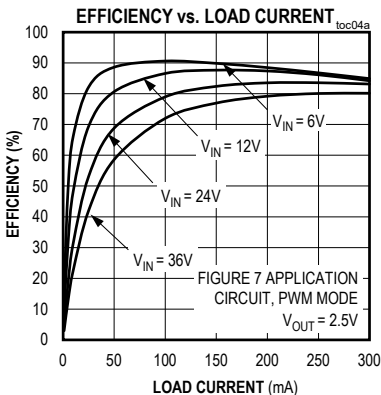
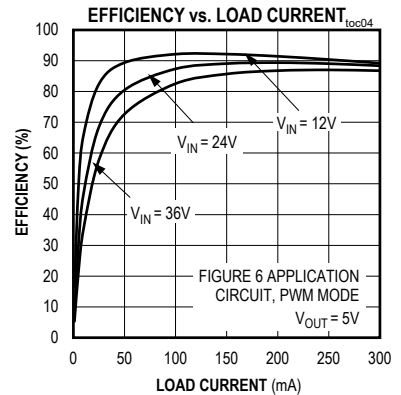
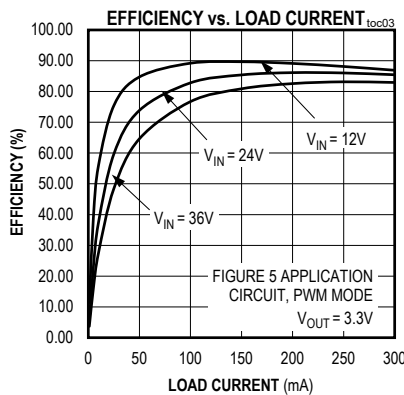
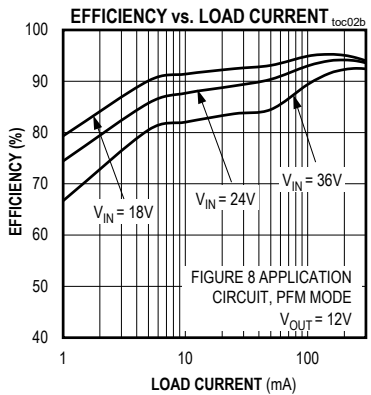
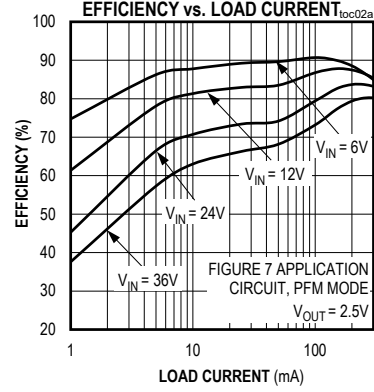
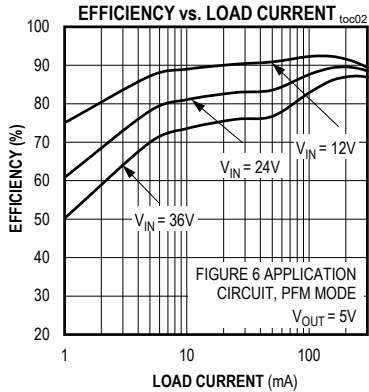
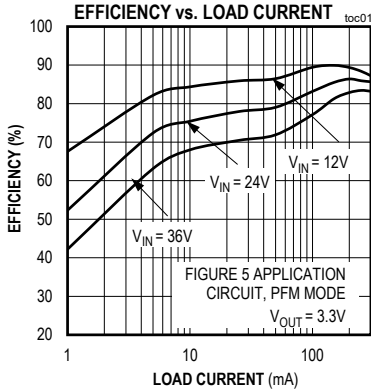
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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LX Dead Time				5		ns
<b><math>\overline{RESET}</math></b>						
FB/ $V_{OUT}$ Threshold for $\overline{RESET}$ Rising		FB/ $V_{OUT}$ rising	93.5	95.5	97.5	%
FB/ $V_{OUT}$ Threshold for $\overline{RESET}$ Falling		FB/ $V_{OUT}$ falling	90	92	94	%
$\overline{RESET}$ Delay After FB/ $V_{OUT}$ Reaches 95% Regulation				2		ms
$\overline{RESET}$ Output Level Low		$I_{\overline{RESET}} = 5mA$			0.2	V
$\overline{RESET}$ Output Leakage Current		$V_{\overline{RESET}} = 5.5V$ , $T_A = +25^\circ C$			0.1	$\mu A$
<b>MODE</b>						
MODE Internal Pullup Resistor				500		k $\Omega$
<b>THERMAL SHUTDOWN</b>						
Thermal-Shutdown Threshold		Temperature rising		166		$^\circ C$
Thermal-Shutdown Hysteresis				10		$^\circ C$

**Note 2:** Limits are 100% tested at  $T_A = +25^\circ C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

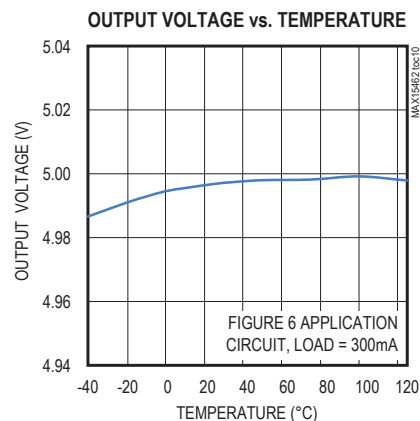
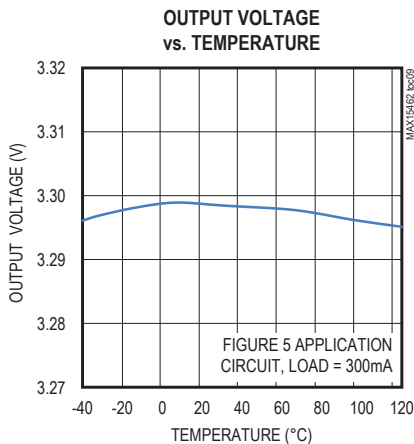
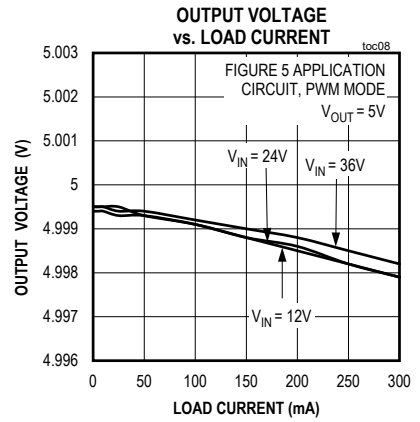
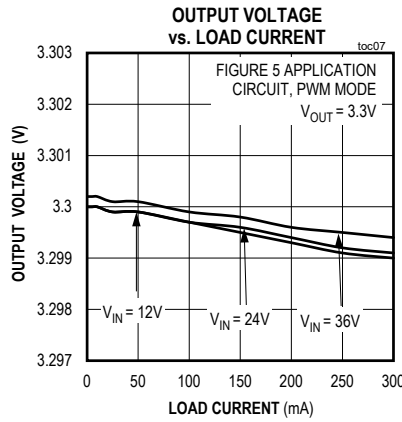
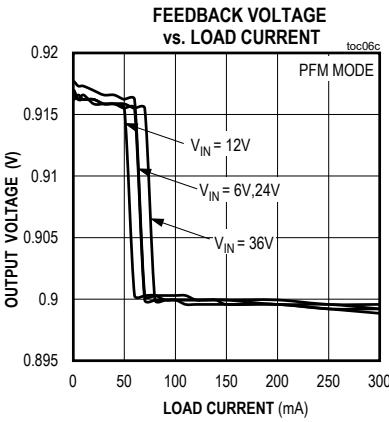
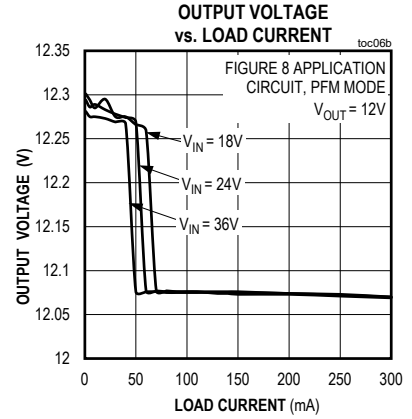
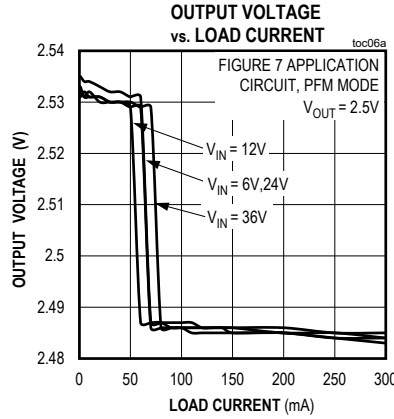
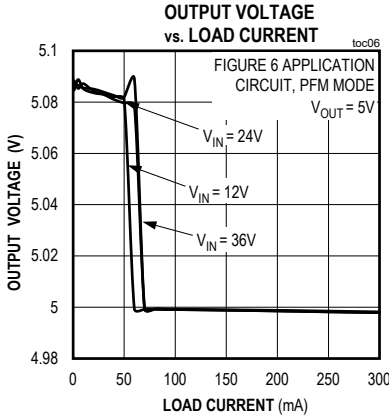
Typical Operating Characteristics

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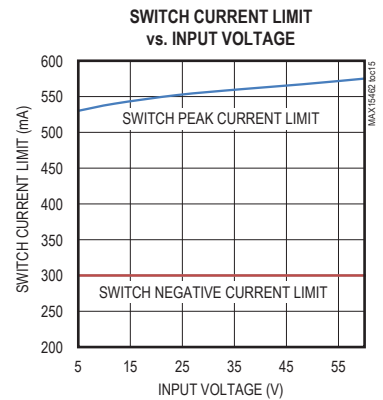
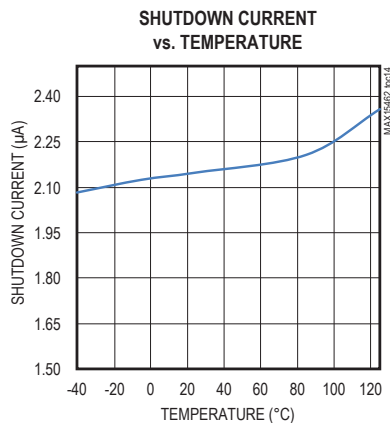
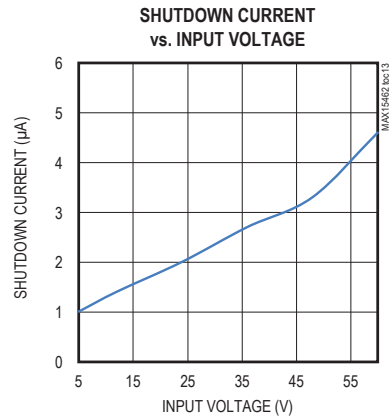
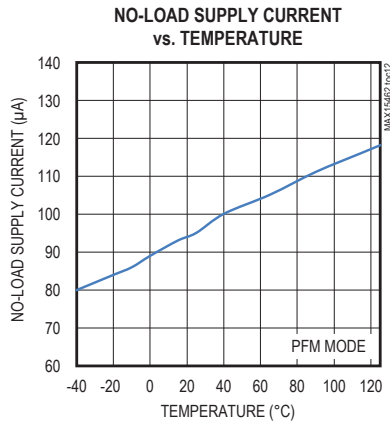
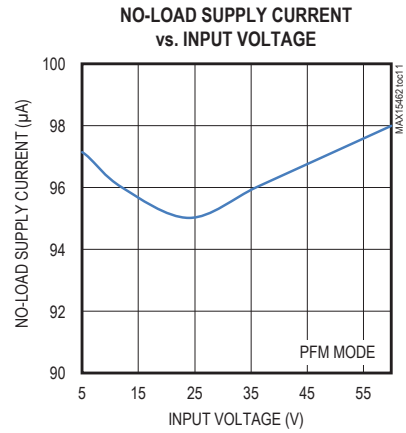
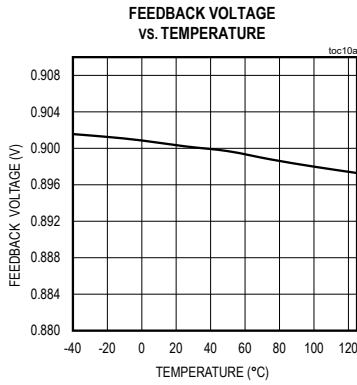
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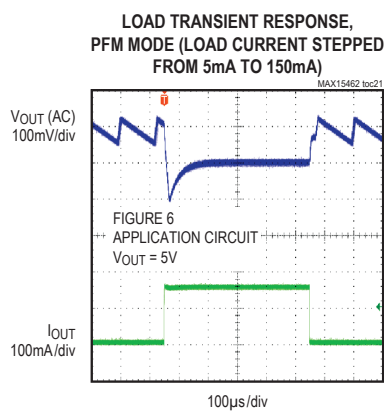
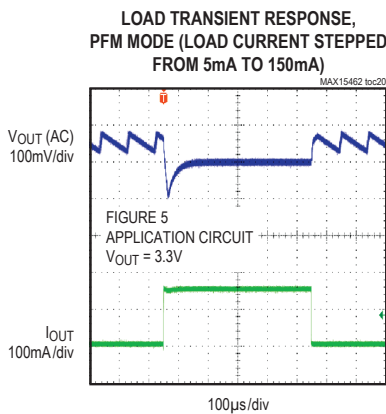
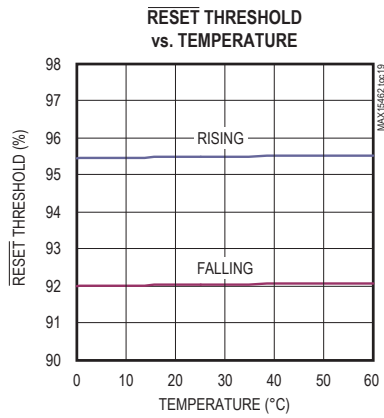
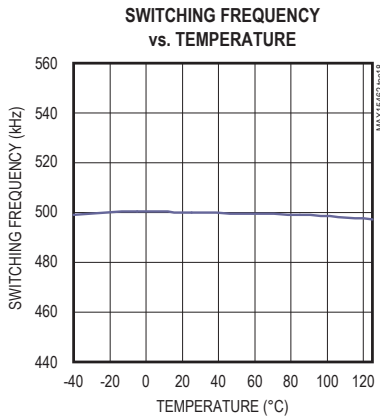
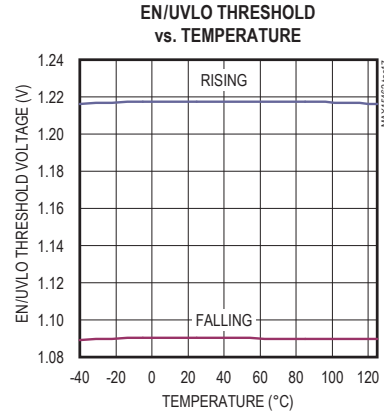
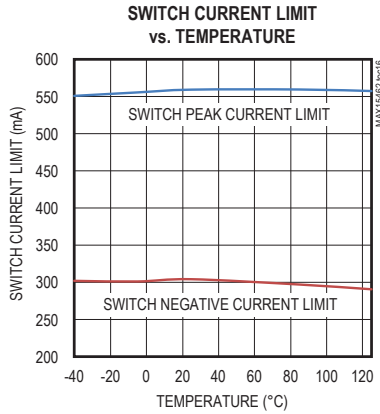
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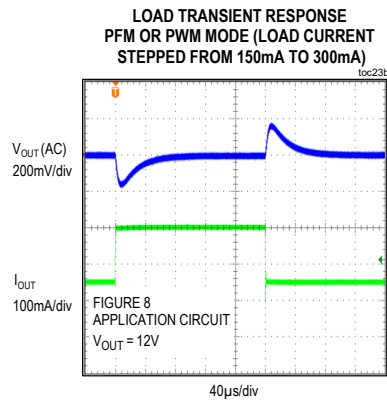
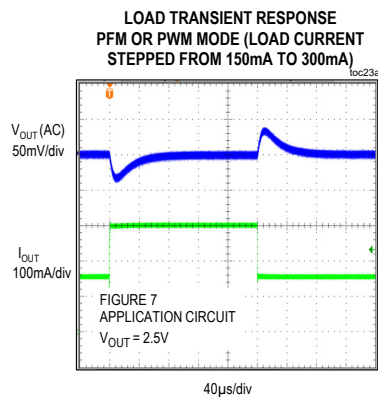
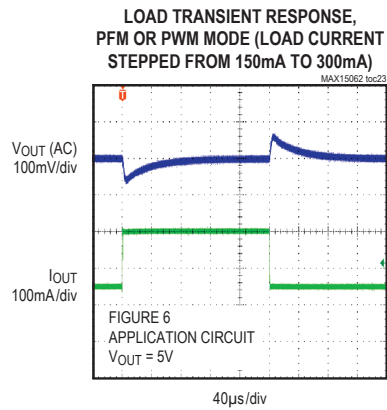
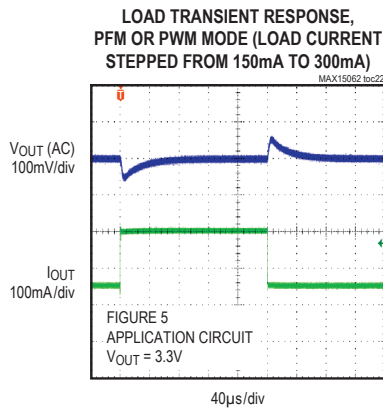
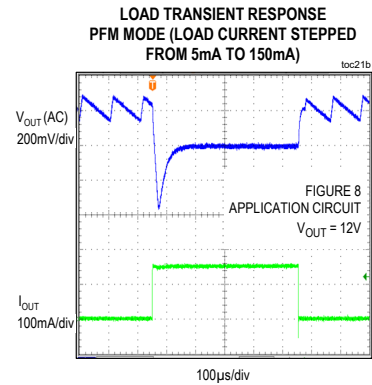
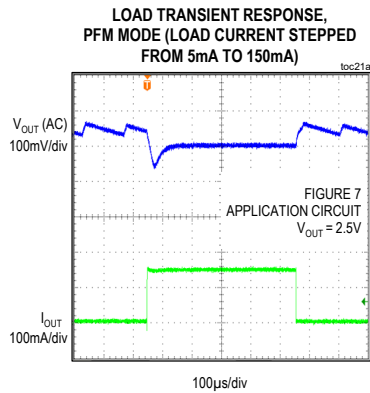
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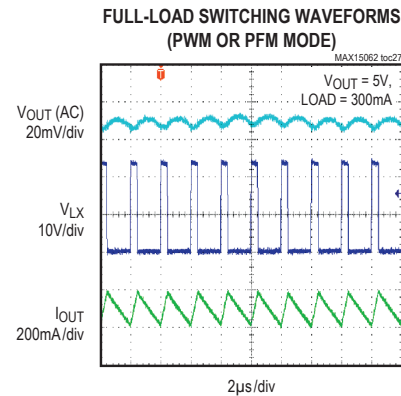
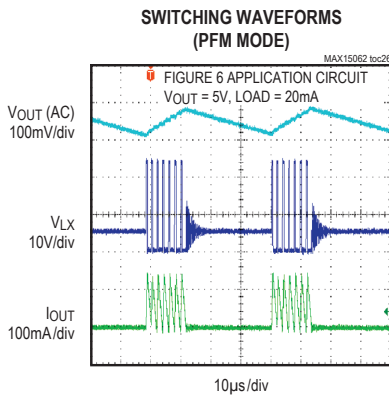
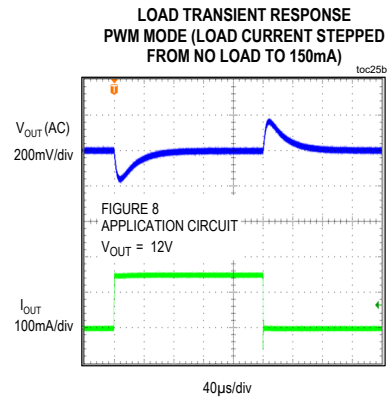
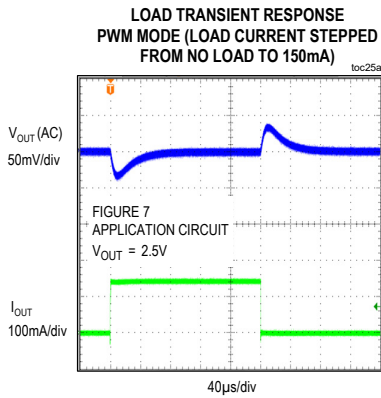
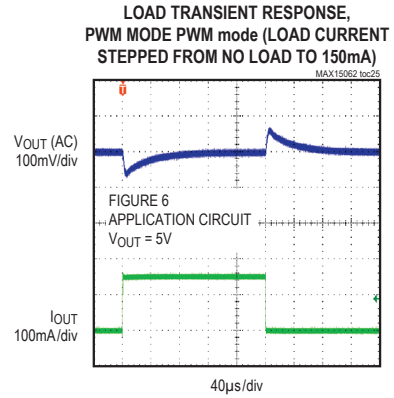
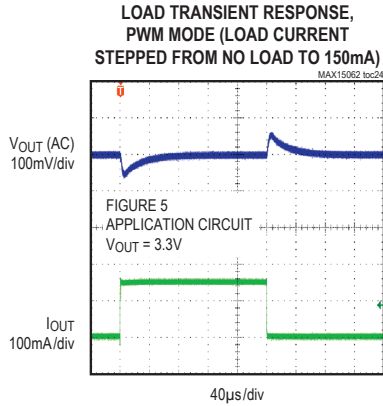
Typical Operating Characteristics (continued)

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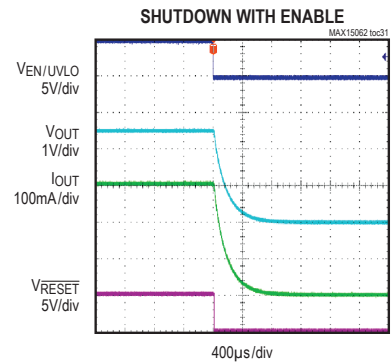
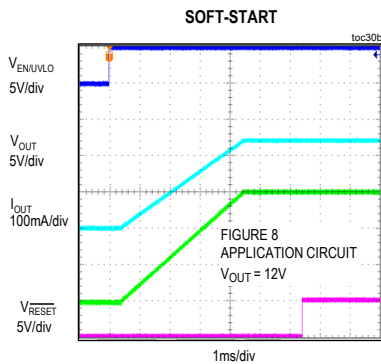
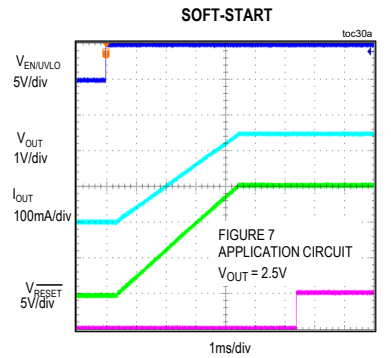
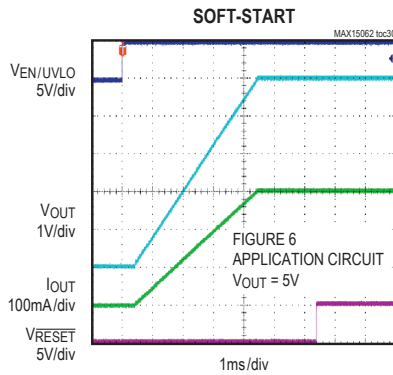
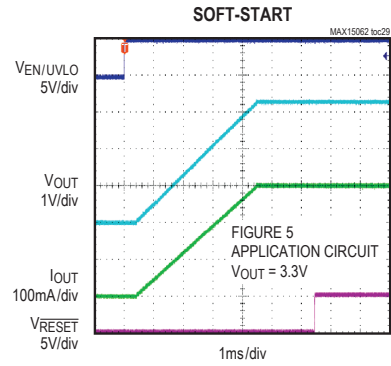
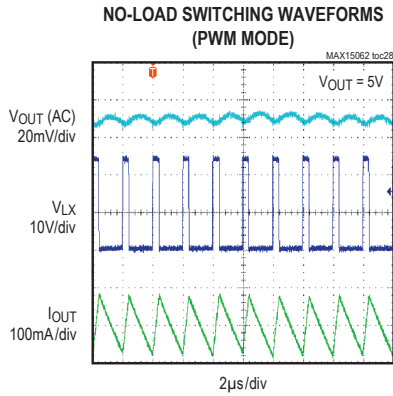
Typical Operating Characteristics (continued)

( $V_{IN} = 24V$ ,  $V_{GND} = 0V$ ,  $C_{IN} = C_{VCC} = 1\mu F$ ,  $V_{EN}/UV_{LO} = 1.5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



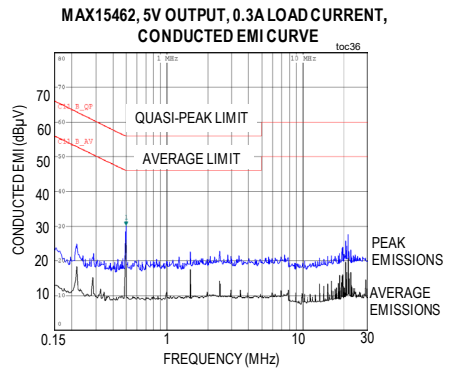
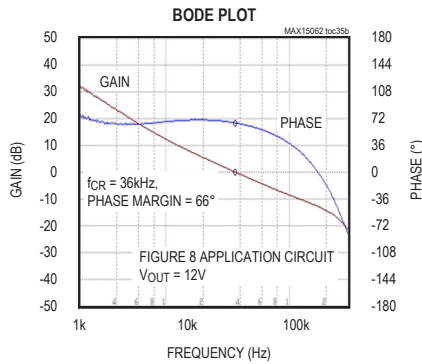
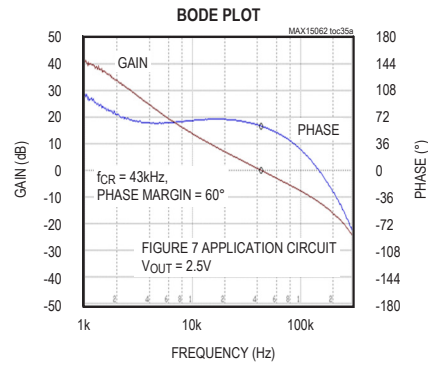
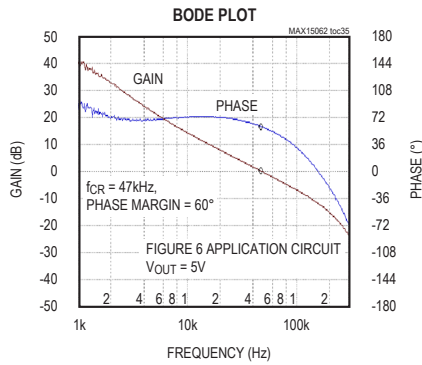
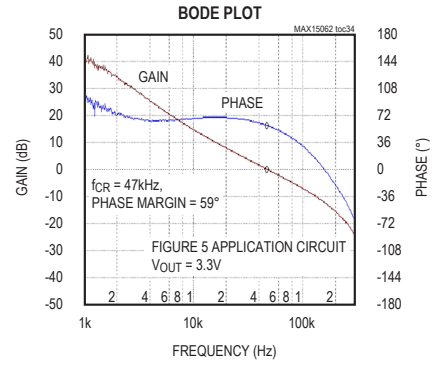
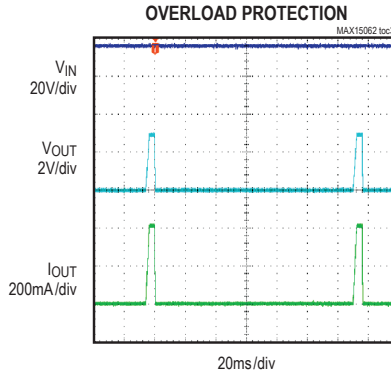
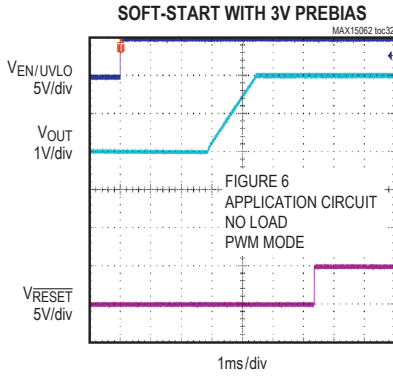
Typical Operating Characteristics (continued)

( $V_{IN} = 24V$ ,  $V_{GND} = 0V$ ,  $C_{IN} = C_{VCC} = 1\mu F$ ,  $V_{EN/UVLO} = 1.5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

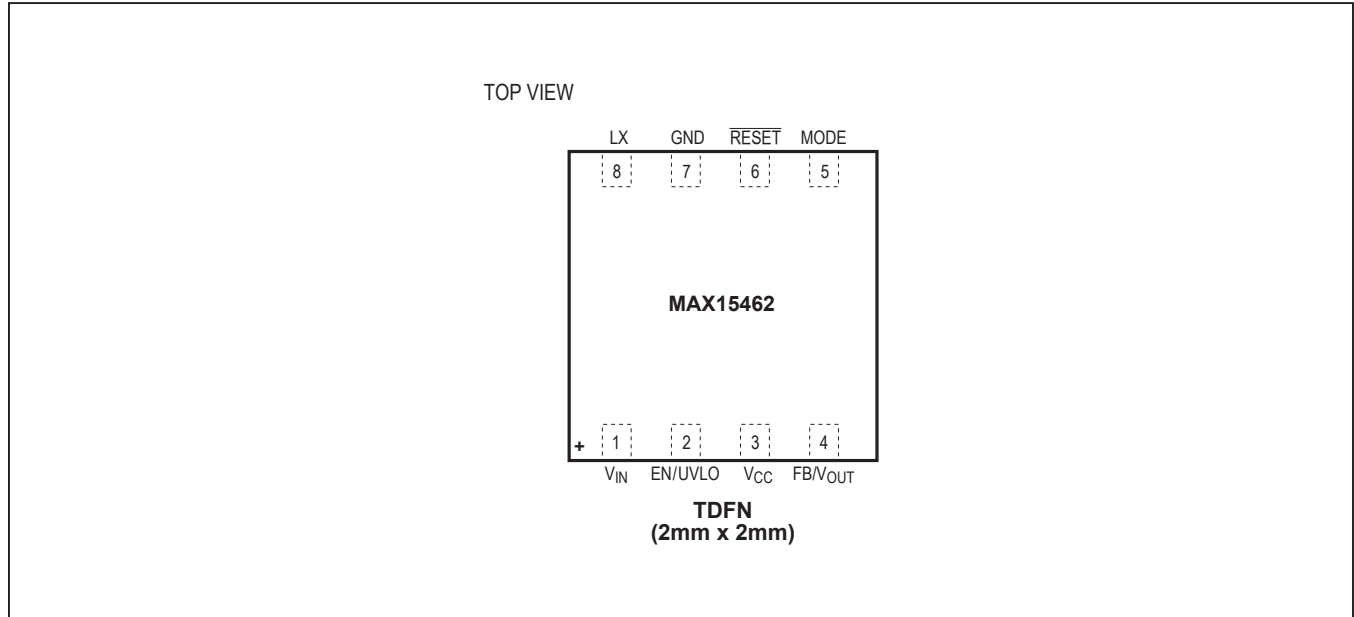


Typical Operating Characteristics (continued)

( $V_{IN} = 24V$ ,  $V_{GND} = 0V$ ,  $C_{IN} = C_{VCC} = 1\mu F$ ,  $V_{EN/UVLO} = 1.5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



Pin Configuration



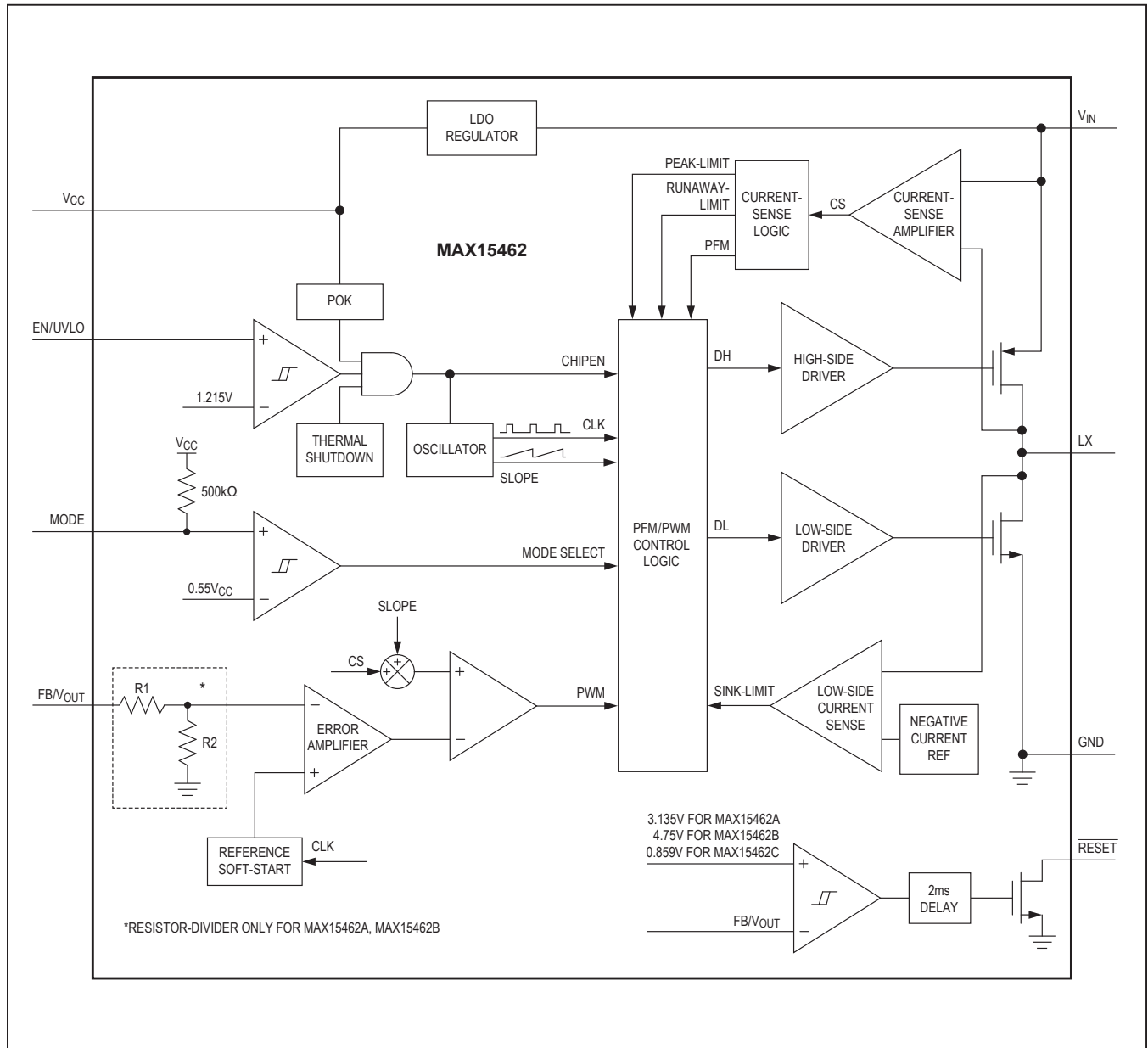
Pin Description

PIN	NAME	FUNCTION
1	$V_{\text{IN}}$	Switching Regulator Power Input. Connect a X7R 1 $\mu\text{F}$ ceramic capacitor from $V_{\text{IN}}$ to GND for bypassing.
2	EN/UVLO	Active-High, Enable/Undervoltage-Detection Input. Pull EN/UVLO to GND to disable the regulator output. Connect EN/UVLO to $V_{\text{IN}}$ for always-on operation. Connect a resistor-divider between $V_{\text{IN}}$ and EN/UVLO to GND to program the input voltage at which the device is enabled and turns on.
3	$V_{\text{CC}}$	Internal LDO Power Output. Bypass $V_{\text{CC}}$ to GND with a minimum 1 $\mu\text{F}$ capacitor.
4	FB/VOU	Feedback Input. For fixed-output voltage versions, connect FB/VOU directly to the output. For the adjustable output voltage version, connect FB/VOU to a resistor-divider between $V_{\text{OUT}}$ and GND to adjust the output voltage from 0.9V to 0.89 x $V_{\text{IN}}$ .
5	MODE	PFM/PWM Mode Selection Input. Connect MODE to GND to enable the fixed-frequency PWM operation. Leave unconnected for light-load PFM operation.
6	$\overline{\text{RESET}}$	Open-Drain Reset Output. Pull up $\overline{\text{RESET}}$ to an external power supply with an external resistor. $\overline{\text{RESET}}$ goes low when the output voltage drops below 92% of the set nominal regulated voltage. $\overline{\text{RESET}}$ goes high impedance 2ms after the output voltage rises above 95% of its regulation value. See the <i>Electrical Characteristics</i> table for threshold values.
7	GND	Ground. Connect GND to the power ground plane. Connect all the circuit ground connections together at a single point. See the <i>PCB Layout Guidelines</i> section.
8	LX	Inductor Connection. Connect LX to the switching-side of the inductor. LX is high impedance when the device is in shutdown.

# MAX15462

## 42V, 300mA, Ultra-Small, High-Efficiency, Synchronous Step-Down DC-DC Converters

### Block Diagram



## Detailed Description

The MAX15462 high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operates over a wide 4.5V to 42V input voltage range. The converter delivers output current up to 300mA at 3.3V (MAX15462A), 5V (MAX15462B), and adjustable output voltages (MAX15462C). When EN/UVLO and  $V_{CC}$  UVLO are satisfied, an internal power-up sequence soft-starts the error-amplifier reference, resulting in a clean monotonic output-voltage soft-start independent of the load current. The FB/ $V_{OUT}$  pin monitors the output voltage through a resistor-divider.  $\overline{RESET}$  transitions to a high-impedance state 2ms after the output voltage reaches 95% of regulation. The device selects either PFM or forced-PWM mode depending on the state of the MODE pin at power-up. By pulling the EN/UVLO pin low, the device enters the shutdown mode and consumes only 2.2 $\mu$ A (typ) of standby current.

## DC-DC Switching Regulator

The device uses an internally compensated, fixed-frequency, current-mode control scheme (see the [Block Diagram](#)). On the rising-edge of an internal clock, the high-side pMOSFET turns on. An internal error amplifier compares the feedback voltage to a fixed internal reference voltage and generates an error voltage. The error voltage is compared to a sum of the current-sense voltage and a slope-compensation voltage by a PWM comparator to set the on-time. During the on-time of the pMOSFET, the inductor current ramps up. For the remainder of the switching period (off-time), the pMOSFET is kept off and the low-side nMOSFET turns on. During the off-time, the inductor releases the stored energy as the inductor current ramps down, providing current to the output. Under overload conditions, the cycle-by-cycle current-limit feature limits the inductor peak current by turning off the high-side pMOSFET and turning on the low-side nMOSFET.

## Mode Selection (MODE)

The logic state of the MODE pin is latched after  $V_{CC}$  and EN/UVLO voltages exceed respective UVLO rising thresholds and all internal voltages are ready to allow LX switching. If the MODE pin is unconnected at power-up, the part operates in PFM mode at light loads. If the MODE pin is grounded at power-up, the part operates in constant-frequency PWM mode at all loads. State changes on the MODE pin are ignored during normal operation.

## PWM Mode Operation

In PWM mode, the inductor current is allowed to go negative. PWM operation is useful in frequency-sensitive applications, providing fixed switching frequency at all

loads. However, the PWM mode of operation gives lower efficiency at light loads compared to PFM mode of operation.

## PFM Mode Operation

PFM mode operation disables negative inductor current and skips pulses at light loads for high efficiency. In PFM mode, the inductor current is forced to a fixed peak of 130mA every clock cycle until the output rises to 102.3% of the nominal voltage. Once the output reaches 102.3% of the nominal voltage, both high-side and low-side FETs are turned off and the part enters hibernate operation until the load discharges the output to 101.1% of the nominal voltage. Most of the internal blocks are turned off in hibernate operation to save quiescent current. After the output falls below 101.1% of the nominal voltage, the device comes out of hibernate operation, turns on all internal blocks, and again commences the process of delivering pulses of energy to the output until it reaches 102.3% of the nominal output voltage. The device naturally exits PFM mode when the load current exceeds 55mA (typ). The advantage of the PFM mode is higher efficiency at light loads because of lower quiescent current drawn from supply.

## Internal 5V Linear Regulator

An internal regulator provides a 5V nominal supply to power the internal functions and to drive the power MOSFETs. The output of the linear regulator ( $V_{CC}$ ) should be bypassed with a 1 $\mu$ F capacitor to GND. The  $V_{CC}$  regulator dropout voltage is typically 150mV. An undervoltage-lockout circuit that disables the regulator when  $V_{CC}$  falls below 3.8V (typ). The 400mV  $V_{CC}$  UVLO hysteresis prevents chattering on power-up and power-down.

## Enable Input (EN/UVLO), Soft-Start

When EN/UVLO voltage is above 1.21V (typ), the device's internal error-amplifier reference voltage starts to ramp up. The duration of the soft-start ramp is 4.1ms, allowing a smooth increase of the output voltage. Driving EN/UVLO low disables both power MOSFETs, as well as other internal circuitry, and reduces  $V_{IN}$  quiescent current to below 2.2 $\mu$ A. EN/UVLO can be used as an input-voltage UVLO adjustment input. An external voltage-divider between  $V_{IN}$  and EN/UVLO to GND adjusts the input voltage at which the device turns on or turns off. If input UVLO programming is not desired, connect EN/UVLO to  $V_{IN}$  (see the [Electrical Characteristics](#) table for EN/UVLO rising and falling threshold voltages).



### Reset Output ( $\overline{\text{RESET}}$ )

The device includes an open-drain  $\overline{\text{RESET}}$  output to monitor the output voltage.  $\overline{\text{RESET}}$  goes high impedance 2ms after the output rises above 95% of its nominal set value and pulls low when the output voltage falls below 92% of the set nominal regulated voltage.  $\overline{\text{RESET}}$  asserts low during the hiccup timeout period.

### Startup into a Prebiased Output

The device is capable of soft-start into a prebiased output, without discharging the output capacitor in both the PFM and forced-PWM modes. Such a feature is useful in applications where digital integrated circuits with multiple rails are powered.

### Operating Input Voltage Range

The maximum operating input voltage is determined by the minimum controllable on-time and the minimum operating input voltage is determined by the maximum duty cycle and circuit voltage drops. The minimum and maximum operating input voltages for a given output voltage should be calculated as follows:

$$V_{\text{INMIN}} = \frac{V_{\text{OUT}} + (I_{\text{OUT}} \times (R_{\text{DCR}} + 0.5))}{D_{\text{MAX}}} + (I_{\text{OUT}} \times 1.0)$$

$$V_{\text{INMAX}} = \frac{V_{\text{OUT}}}{t_{\text{ONMIN}} \times f_{\text{SW}}}$$

where  $V_{\text{OUT}}$  is the steady-state output voltage,  $I_{\text{OUT}}$  is the maximum load current,  $R_{\text{DCR}}$  is the DC resistance of the inductor,  $f_{\text{SW}}$  is the switching frequency (max),  $D_{\text{MAX}}$  is maximum duty cycle (0.9), and  $t_{\text{ONMIN}}$  is the worst-case minimum controllable switch on-time (130ns).

### Overcurrent Protection/Hiccup Mode

The device is provided with a robust overcurrent protection scheme that protects the device under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET whenever the high-side switch current exceeds an internal limit of 0.56A (typ). A runaway current limit on the high-side switch current at 0.66A (typ) protects the device under high input voltage, and short-circuit conditions when there is insufficient output voltage available to restore the inductor current that was built up during the on period of the step-down converter. One occurrence of the runaway current limit triggers a hiccup mode. In addition, if, due to

a fault condition, the output voltage drops to 65% (typ) of its nominal value any time after soft-start is complete, hiccup mode is triggered. In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 131ms. Once the hiccup timeout period expires, soft-start is attempted again. Hiccup mode of operation ensures low power dissipation under output short-circuit conditions.

Care should be taken in board layout and system wiring to prevent violation of the absolute maximum rating of the FB/ $V_{\text{OUT}}$  pin under short-circuit conditions. Under such conditions, it is possible for the ceramic output capacitor to oscillate with the board or wiring inductance between the output capacitor or short-circuited load, thereby causing the absolute maximum rating of FB/ $V_{\text{OUT}}$  (-0.3V) to be exceeded. The parasitic board or wiring inductance should be minimized, and the output voltage waveform under short-circuit operation should be verified, to ensure the absolute maximum rating of FB/ $V_{\text{OUT}}$  is not exceeded.

### Thermal Overload Protection

Thermal overload protection limits the total power dissipation in the device. When the junction temperature exceeds +166°C, an on-chip thermal sensor shuts down the device, turns off the internal power MOSFETs, allowing the device to cool down. The thermal sensor turns the device on after the junction temperature cools by 10°C.

## Applications Information

### Inductor Selection

A low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions should be selected. The saturation current ( $I_{\text{SAT}}$ ) must be high enough to ensure that saturation cannot occur below the maximum current-limit value ( $I_{\text{PEAK-LIMIT}}$ ) of 0.56A (typ). The required inductance for a given application can be determined from the following equation:

$$L = 9.3 \times V_{\text{OUT}}$$

where  $L$  is inductance in  $\mu\text{H}$  and  $V_{\text{OUT}}$  is output voltage. Once the  $L$  value is known, the next step is to select the right core material. Ferrite and powdered iron are commonly available core materials. Ferrite cores have low core losses and are preferred for high-efficiency designs. Powdered iron cores have more core losses and are relatively cheaper than ferrite cores. See [Table 1](#) to select the inductors for typical applications.



**Table 1. Inductor Selection**

INPUT VOLTAGE RANGE $V_{IN}$ (V)	$V_{OUT}$ (V)	$I_{OUT}$ (MA)	L (MH)	RECOMMENDED PART NO.
4.5 to 42	3.3	300	33	Coilcraft LPS4018-333ML
6 to 42	5	300	47	Coilcraft LPS4018-473ML
4.5 to 42	1.8 or 2.5	300	22	Coilcraft LPS4018-223ML
14 to 42	12	300	100	Wurth 74408943101
17 to 42	15	300	150	TDK VLC6045T-151M

**Table 2. Output Capacitor Selection**

INPUT VOLTAGE RANGE $V_{IN}$ (V)	$V_{OUT}$ (V)	$I_{OUT}$ (MA)	$C_{OUT}$ (MF)	RECOMMENDED PART NO.
4.5 to 42	3.3	300	10 $\mu$ F/1206/X7R/6.3V	Murata GRM31CR70J106K
6 to 42	5	300	10 $\mu$ F/1206/X7R/6.3V	Murata GRM31CR70J106K
4.5 to 42	1.8 or 2.5	300	22 $\mu$ F/1206/X7R/6.3V	Murata GRM31CR70J226K
14 to 42	12	300	4.7 $\mu$ F/1206/X7R/16V	Murata GRM31CR71C475K
17 to 42	15	300	4.7 $\mu$ F/1206/X7R/25V	Murata GRM31CR71E475K

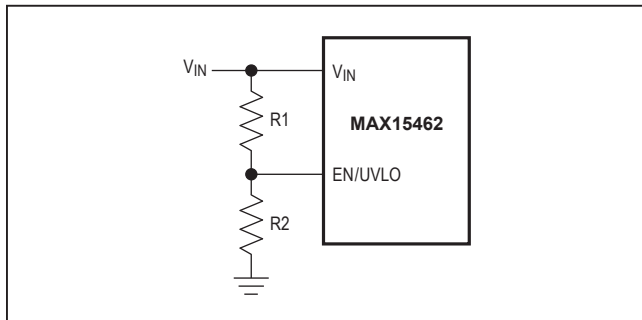


Figure 1. Adjustable EN/UVLO Network

**Input Capacitor**

Small ceramic capacitors are recommended for the device. The input capacitor reduces peak current drawn from the power source and reduces noise and voltage ripple on the input caused by the switching circuitry. A minimum of 1 $\mu$ F, X7R-grade capacitor is recommended for the input capacitor of the device to keep the input voltage ripple under 2% of the minimum input voltage, and to meet the maximum ripple-current requirements.

**Output Capacitor**

Small ceramic X7R-grade capacitors are sufficient and recommended for the device. The output capacitor has two functions. It filters the square wave generated by the device along with the output inductor. It stores sufficient energy to support the output voltage under load transient conditions and stabilizes the device’s internal control loop. Usually, the output capacitor is sized to support a step load of 50% of the maximum output current in the

application, such that the output-voltage deviation is less than 3%. Required output capacitance can be calculated from the following equation:

$$C_{OUT} = \frac{30}{V_{OUT}}$$

where  $C_{OUT}$  is the output capacitance in  $\mu$ F and  $V_{OUT}$  is the output voltage. See Table 2 to select the output capacitor for typical applications. It should be noted that dielectric materials used in ceramic capacitors exhibit capacitance loss due to DC bias levels and should be appropriately derated to ensure the required output capacitance is obtained in the application.

**Setting the Input Undervoltage-Lockout Level**

The devices offer an adjustable input undervoltage-lockout level. Set the voltage at which the device turns on with a resistive voltage-divider connected from  $V_{IN}$  to GND (see Figure 1). Connect the center node of the divider to EN/UVLO.

Choose R1 to be 3.3M $\Omega$  max, and then calculate R2 as follows:

$$R2 = \frac{R1 \times 1.215}{(V_{INU} - 1.215)}$$

where  $V_{INU}$  is the voltage at which the device is required to turn on. If the EN/UVLO pin is driven from an external signal source, a series resistance of minimum 1k $\Omega$  is recommended to be placed between the signal source output and the EN/UVLO pin, to reduce voltage ringing on the line.

**Adjusting the Output Voltage**

The MAX15462C output voltage can be programmed from 0.9V to  $0.89 \times V_{IN}$ . Set the output voltage by connecting a resistor-divider from output to FB to GND (see [Figure 2](#)).

For output voltages less than 6V, choose R2 in the 50kΩ to 150kΩ range. For the output voltages greater than 6V, choose R2 in the 25kΩ to 75kΩ range and calculate R1 with the following equation:

$$R1 = R2 \times \left[ \frac{V_{OUT}}{0.9} - 1 \right]$$

**Power Dissipation**

At a particular operating condition, the power losses that lead to temperature rise of the part are estimated as follows:

$$P_{LOSS} = \left( P_{OUT} \times \left( \frac{1}{\eta} - 1 \right) \right) - (I_{OUT}^2 \times R_{DCR})$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

where  $P_{OUT}$  is the output power,  $\eta$  is the efficiency of power conversion, and  $R_{DCR}$  is the DC resistance of the output inductor. See the [Typical Operating Characteristics](#) for the power-conversion efficiency or measure the efficiency to determine the total power dissipation.

The junction temperature ( $T_J$ ) of the device can be estimated at any ambient temperature ( $T_A$ ) from the following equation:

$$T_J = T_A + (\theta_{JA} \times P_{LOSS})$$

where  $\theta_{JA}$  is the junction-to-ambient thermal impedance of the package. Junction temperature greater than +125°C degrades operating lifetimes.

**PCB Layout Guidelines**

Careful PCB layout is critical to achieve clean and stable operation. The switching power stage requires particular attention. Follow the guidelines below for good PCB layout.

- Place the input ceramic capacitor as close as possible to the  $V_{IN}$  and GND pins.
- Connect the negative terminal of the  $V_{CC}$  bypass capacitor to the GND pin with shortest possible trace or ground plane.
- Minimize the area formed by the LX pin and the inductor connection to reduce the radiated EMI.
- Place the  $V_{CC}$  decoupling capacitor as close as possible to the  $V_{CC}$  pin.
- Ensure that all feedback connections are short and direct.
- Route the high-speed switching node (LX) away from the FB/ $V_{OUT}$ ,  $\overline{RESET}$ , and MODE pins.

For a sample PCB layout that ensures the first-pass success, refer to the MAX15462 evaluation kit layouts available at [www.analog.com](http://www.analog.com).

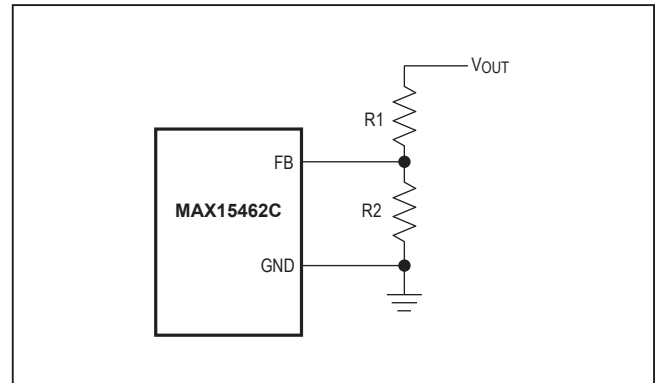


Figure 2. Setting the Output Voltage

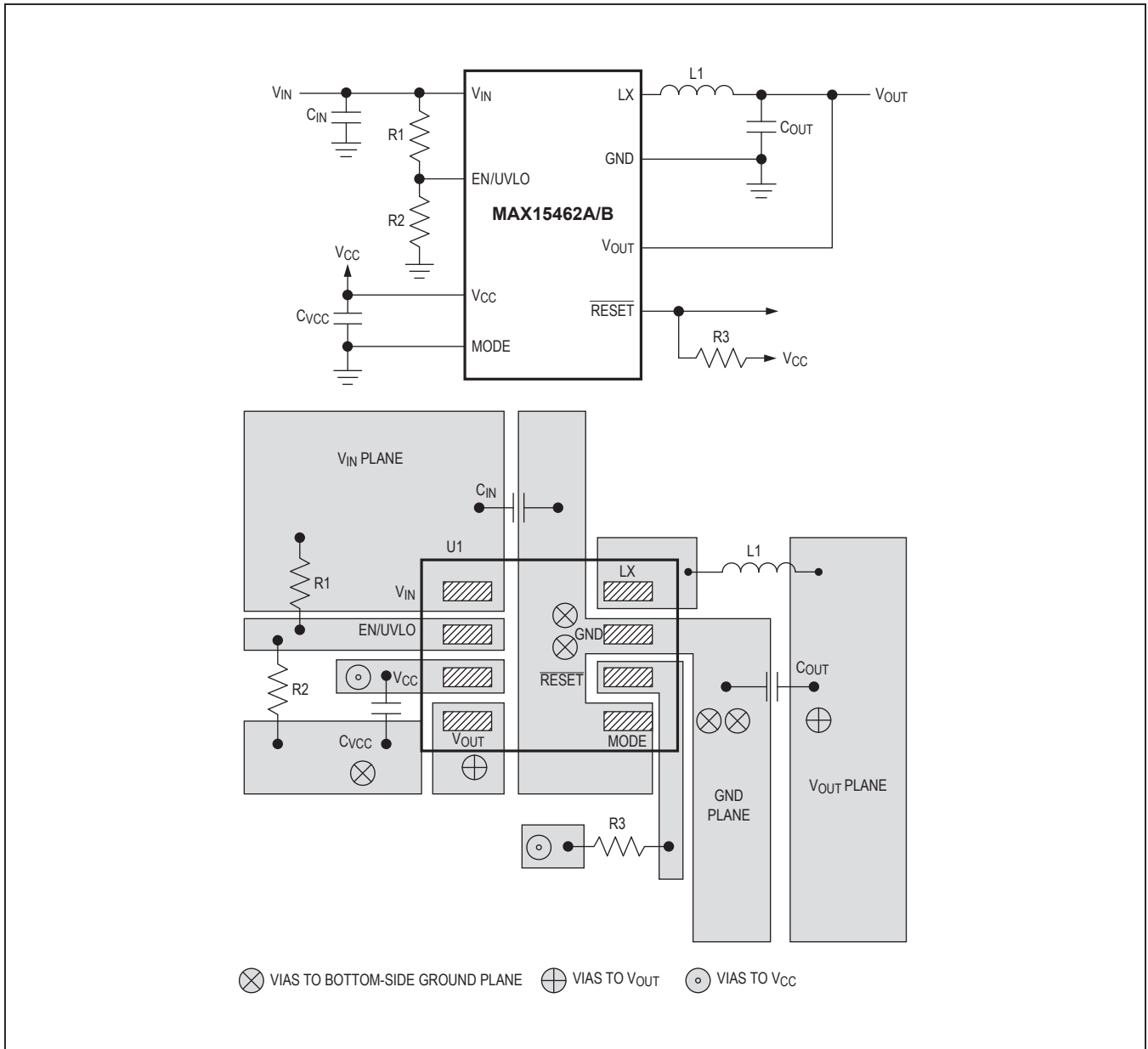


Figure 3. Layout Guidelines for MAX15462A and MAX15462B

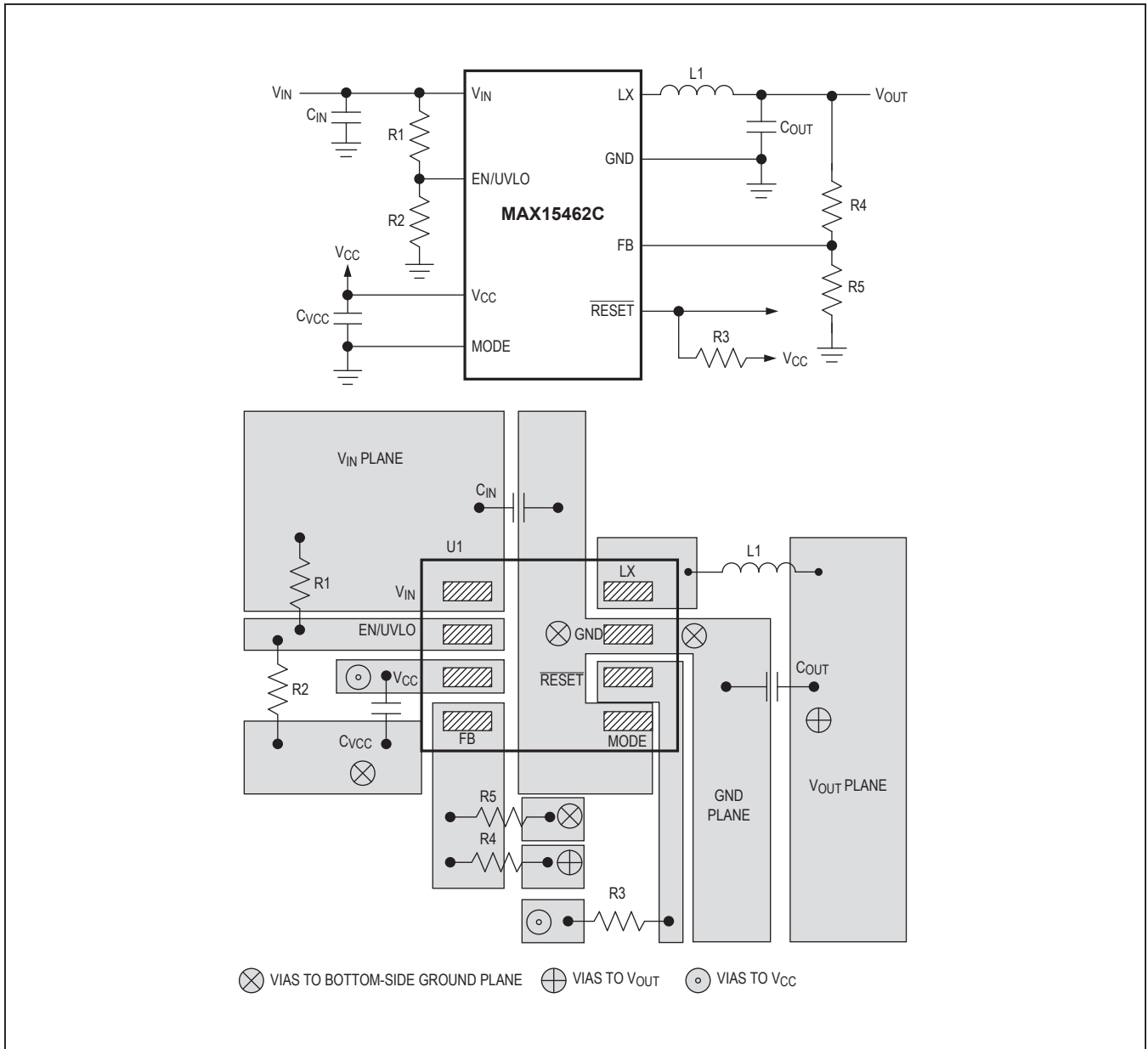


Figure 4. Layout Guidelines for MAX15462C

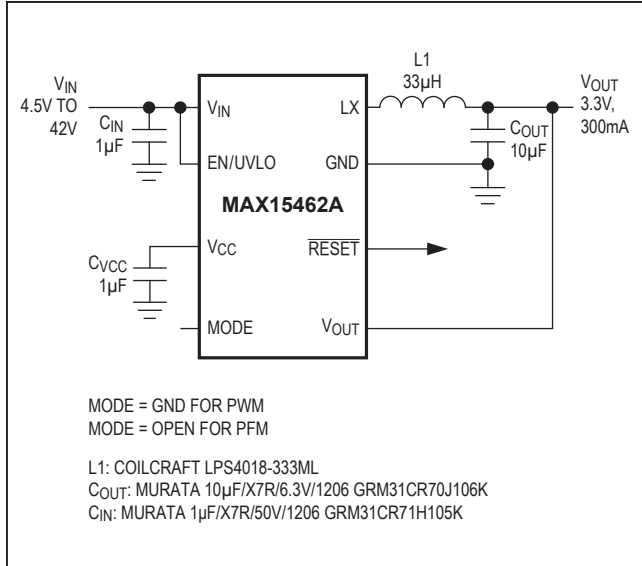


Figure 5. 3.3V, 300mA Step-Down Regulator

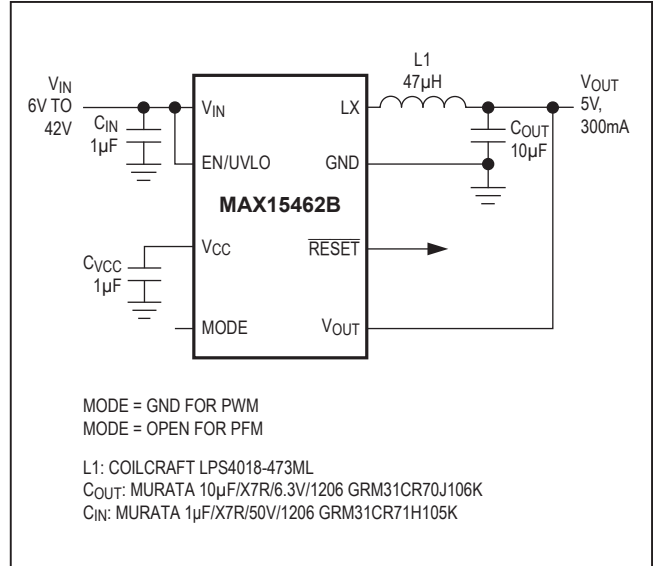


Figure 6. 5V, 300mA Step-Down Regulator

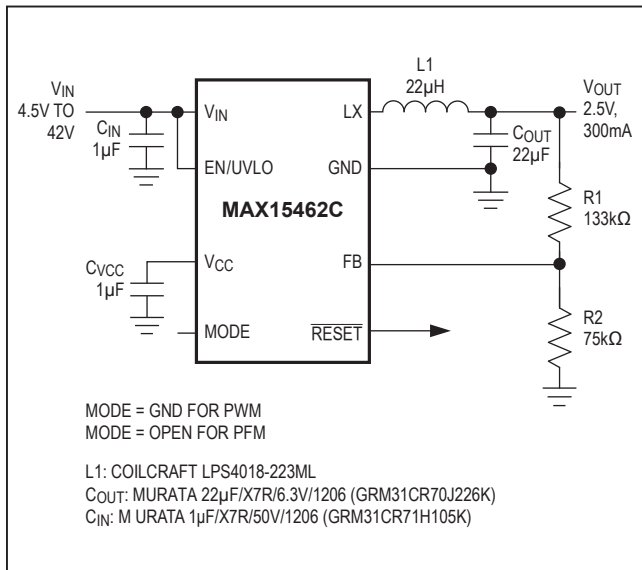


Figure 7. 2.5V, 300mA Step-Down Regulator

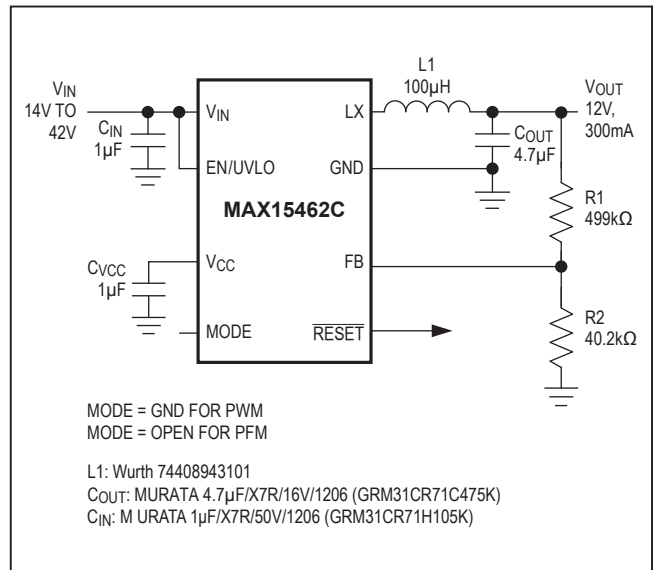


Figure 8. 12V, 300mA Step-Down Regulator

# MAX15462

## 42V, 300mA, Ultra-Small, High-Efficiency, Synchronous Step-Down DC-DC Converters

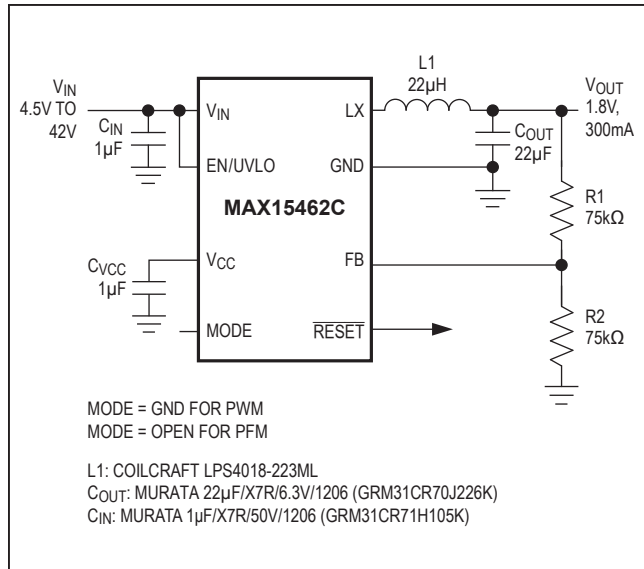


Figure 9. 1.8V, 300mA Step-Down Regulator

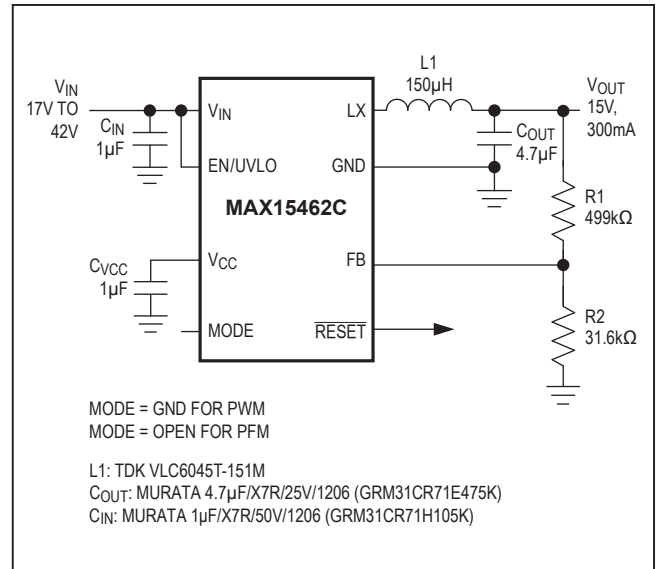


Figure 10. 15V, 300mA Step-Down Regulator

### Ordering Information

PART	TEMP RANGE	PIN-PACK-AGE	V <sub>OUT</sub>
MAX15462AATA+	-40°C to +125°C	8 TDFN	3.3V
MAX15462BATA+	-40°C to +125°C	8 TDFN	5V
MAX15462CATA+	-40°C to +125°C	8 TDFN	Adj

+Denotes a lead(Pb)-free/RoHS-compliant package.

### Chip Information

PROCESS: BiCMOS

### Package Information

For the latest package outline information and land patterns (footprints), go to <https://www.analog.com/en/design-center/package-quality-symbols-footprints/package-index.html>. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PAT-TERN NO.
8 TDFN-CU	T822C+6C	<a href="#">21-100514</a>	<a href="#">90-0349</a>

**Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/15	Initial release	—
1	2/17	Updated junction temperature and added text TOC36	1–4, 12, 17, 18
2	12/23	Updated Package Thermal Characteristics, Package Information sections	2, 22



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