

## MAX14945

## 2.75kV<sub>RMS</sub> Isolated 500kbps Half-Duplex RS-485/RS-422 Transceiver with $\pm 30$ kV ESD Protection

### General Description

The MAX14945 isolated RS-485/RS-422 transceiver provides 2750V<sub>RMS</sub> (60s) of galvanic isolation between the cable side (RS-485/RS-422 driver/receiver side) and the UART side of the device. Isolation improves communication by breaking ground loops and reduces noise when there are large differences in ground potential between ports. Signals are passed across the isolation barrier through integrated high-voltage capacitors. This device allows for robust communication at any speed up to 500kbps.

The device includes one half-duplex drive/receive channel. The receiver is 1/8-unit load, allowing up to 256 transceivers on a common bus.

Integrated true fail-safe circuitry ensures a logic-high on the receiver output when inputs are shorted or open. Undervoltage lockout disables the driver when the cable side or UART side power supplies are below functional levels.

The driver outputs/receiver inputs are protected from  $\pm 30$ kV electrostatic discharge (ESD) to GNDB on the cable side, as specified by the Human Body Model (HBM).

The MAX14945 is available in a wide body 16-pin SO package and operates over the  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  temperature range.

### Benefits and Features

- High-Performance Transceiver Enables Flexible Designs
  - Integrated LDO for Cable-Side Power
  - Compliant with RS-485 EIA/TIA-485 Standard
  - 500kbps Maximum Data Rate
  - Allows Up to 256 Devices on the Bus
- Integrated Protection Ensures Robust Communication
  - $\pm 30$ kV ESD (HBM) on Driver Outputs/Receiver Inputs
  - 2.75kV<sub>RMS</sub> Withstand-Isolation Voltage for 60s ( $V_{\text{ISO}}$ )
  - 630V<sub>PEAK</sub> Maximum Repetitive Peak-Isolation Voltage ( $V_{\text{IORM}}$ )
  - 445V<sub>RMS</sub> Maximum Working-Isolation Voltage ( $V_{\text{IOWM}}$ )
  - > 30 Years Lifetime at Rated Working Voltage
  - Withstands  $\pm 10$ kV Surge per IEC 61000-4-5
  - Thermal Shutdown

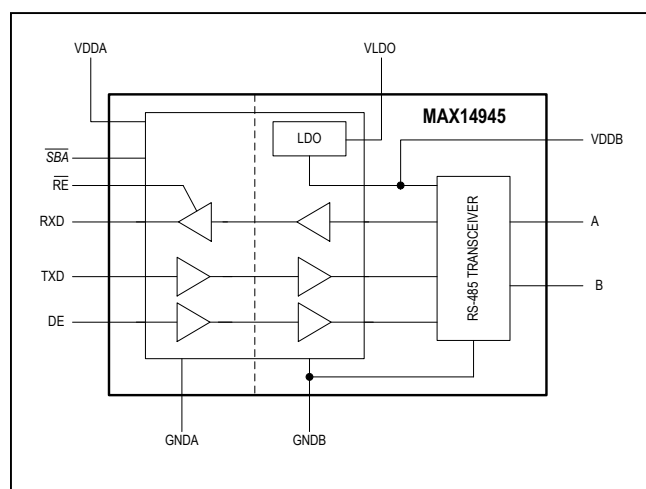
### Safety Regulatory Approvals

- UL According to UL1577
- cUL According to CSA Bulletin 5A

### Applications

- Industrial Automation Equipment
- Programmable Logic Controllers
- HVAC
- Power Meters

### Functional Diagram



[Ordering Information/Selector Guide](#) appears at end of data sheet.

## Absolute Maximum Ratings

V <sub>DDA</sub> to GNDA .....	-0.3V to +6V	Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
V <sub>DDB</sub> to GNDB .....	-0.3V to +6V	16-pin Wide SOIC	
V <sub>LDO</sub> to GNDB .....	-0.3V to +16V	(derate 14.1mW/°C above +70°C).....	1126.8mW
TXD, DE, $\overline{\text{RE}}$ to GNDA .....	-0.3V to +6V	Operating Temperature Range .....	-40°C to +85°C
$\overline{\text{SBA}}$ , RXD to GNDA .....	-0.3V to (V <sub>DDA</sub> + 0.3V)	Junction Temperature .....	+150°C
A, B to GNDB .....	-8V to +13V	Storage Temperature Range .....	-65°C to +150°C
Short Circuit Duration (RXD, $\overline{\text{SBA}}$ to GNDA, A, B, V <sub>DDB</sub> to GNDB).....	Continuous	Lead Temperature (soldering, 10s) .....	+300°C
		Soldering Temperature (reflow) .....	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Package Thermal Characteristics (Note 1)

Junction-to-Ambient Thermal Resistance (θ <sub>JA</sub> ) .....	71°C/W	Junction-to-Case Thermal Resistance (θ <sub>JC</sub> ) .....	23°C/W
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**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

## DC Electrical Characteristics

(V<sub>DDA</sub> – V<sub>GNDA</sub> = 1.71V to 5.5V, V<sub>DDB</sub> – V<sub>GNDB</sub> = 4.5V to 5.5V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at V<sub>DDA</sub> – V<sub>GNDA</sub> = 3.3V, V<sub>DDB</sub> – V<sub>GNDB</sub> = 5V, V<sub>GNDA</sub> = V<sub>GNDB</sub>, and T<sub>A</sub> = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER						
Supply Voltage	V <sub>DDA</sub>		1.71		5.5	V
	V <sub>DDB</sub>		4.5		5.5	
Supply Current	I <sub>DDA</sub>	V <sub>DDA</sub> = 5V, DE = high, $\overline{\text{RE}}$ = TXD = low, RXD unconnected, no load		4	6.6	mA
	I <sub>DDB</sub>	DE = high, $\overline{\text{RE}}$ = TXD = low, RXD unconnected, no load, V <sub>DDB</sub> = 5V		6.3	12.5	
Undervoltage-Lockout Threshold	V <sub>UVLOA</sub>	V <sub>DDA</sub> rising	1.50	1.58	1.65	V
	V <sub>UVLOB</sub>	V <sub>DDB</sub> rising	2.55	2.7	2.85	
Undervoltage-Lockout Threshold Hysteresis	V <sub>UVHYSTA</sub>			50		mV
	V <sub>UVHYSTB</sub>			200		
LDO						
LDO Supply Voltage	V <sub>LDO</sub>	Relative to GNDB, LDO is on (Note 4)	4.68		14	V
LDO Supply Current	I <sub>LDO</sub>	DE = high, $\overline{\text{RE}}$ = TXD = low, no load, V <sub>LDO</sub> = 5.5V		6.5	12.9	mA
LDO Output Voltage	V <sub>DDB</sub>		4.5	5	5.5	V
LDO Current Limit				300		mA
Load Regulation		V <sub>LDO</sub> = 5.68V, I <sub>LOAD</sub> = 20mA to 40mA		0.19	1.7	mV/mA
Line Regulation		V <sub>LDO</sub> = 5.68V to 14V, I <sub>LOAD</sub> = 20mA		0.12	1.8	mV/V

## DC Electrical Characteristics (continued)

( $V_{DDA} - V_{GNDA} = 1.71V$  to  $5.5V$ ,  $V_{DDB} - V_{GNDB} = 4.5V$  to  $5.5V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{DDA} - V_{GNDA} = 3.3V$ ,  $V_{DDB} - V_{GNDB} = 5V$ ,  $V_{GNDA} = V_{GNDB}$ , and  $T_A = +25^{\circ}C$ .) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Dropout Voltage		V <sub>LDO</sub> = 4.68V, I <sub>DDB</sub> = -120mA			100	180	mV
Load Capacitance		Nominal value		1		10	μF
LOGIC INTERFACE (TXD, RXD, DE, $\overline{RE}$ , $\overline{SBA}$ )							
Input High Voltage	V <sub>IH</sub>	$\overline{RE}$ , TXD, DE to GNDA	2.25V ≤ V <sub>DDA</sub> ≤ 5.5V	0.7 x V <sub>DDA</sub>		V	
			1.71V ≤ V <sub>DDA</sub> ≤ 1.89V	0.78 x V <sub>DDA</sub>			
Input Low Voltage	V <sub>IL</sub>	$\overline{RE}$ , TXD, DE to GNDA	2.25V ≤ V <sub>DDA</sub> ≤ 5.5V	0.8		V	
			1.71V ≤ V <sub>DDA</sub> ≤ 1.89V	0.6			
Input Hysteresis	V <sub>HYS</sub>	$\overline{RE}$ , TXD, DE to GNDA		220		mV	
Input Capacitance	C <sub>IN</sub>	$\overline{RE}$ , TXD, DE, f = 1MHz		2		pF	
Input Pullup Current	I <sub>PU</sub>	TXD		-10	-4.5	-1.5	μA
Input Pulldown Current	I <sub>PD</sub>	DE, $\overline{RE}$		1.5	4.5	10	μA
$\overline{SBA}$ Pullup Resistance	R <sub>SBA</sub>			3	5	8	kΩ
Output Voltage High	V <sub>OH</sub>	RXD to GNDA, I <sub>OUT</sub> = -4mA		V <sub>DDA</sub> -0.4		V	
Output Voltage Low	V <sub>OL</sub>	RXD to GNDA, I <sub>OUT</sub> = 4mA		0.40		V	
		$\overline{SBA}$ to GNDA, I <sub>OUT</sub> = 4mA		0.45			
Short-Circuit Output Pullup Current	I <sub>SH_PU</sub>	0V ≤ V <sub>RXD</sub> ≤ V <sub>DDA</sub> , $\overline{RE}$ = low		-42		mA	
Short-Circuit Output Pulldown Current	I <sub>SH_PD</sub>	0V ≤ V <sub>RXD</sub> ≤ V <sub>DDA</sub> , $\overline{RE}$ = low		+40		mA	
		0V ≤ V $\overline{SBA}$ ≤ V <sub>DDA</sub> , side B is powered and working		+60			
Three-State Output Current	I <sub>OZ</sub>	0V ≤ V <sub>RXD</sub> ≤ V <sub>DDA</sub> , $\overline{RE}$ = high		-1		+1	μA
DRIVER							
Differential Driver Output	V <sub>OD</sub>	R <sub>L</sub> = 54Ω, TXD = high or low, Figure 1a		2		V	
		R <sub>L</sub> = 100Ω, TXD = high or low, Figure 1a		3			
		-7V ≤ V <sub>CM</sub> ≤ +12V, Figure 1b		1.5			5
Change in Magnitude of Differential Driver Output Voltage	ΔV <sub>OD</sub>	R <sub>L</sub> = 54Ω (Note 5)		0.2		V	
Driver Common Mode Output Voltage	V <sub>OC</sub>	R <sub>L</sub> = 54Ω		V <sub>DDB</sub> /2		3	V

**DC Electrical Characteristics (continued)**

( $V_{DDA} - V_{GNDA} = 1.71V$  to  $5.5V$ ,  $V_{DDB} - V_{GNDB} = 4.5V$  to  $5.5V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $V_{DDA} - V_{GNDA} = 3.3V$ ,  $V_{DDB} - V_{GNDB} = 5V$ ,  $V_{GNDA} = V_{GNDB}$ , and  $T_A = +25^{\circ}C$ .) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Change in Magnitude of Common-Mode Voltage	$\Delta V_{OC}$	$R_L = 54\Omega$ (Note 5)				0.2	V
Driver Short-Circuit Output Current	$I_{OSD}$	$GNDB \leq V_{OUT} \leq +12V$ , output low (Note 6)		+40		+250	mA
		$-7V \leq V_{OUT} \leq V_{DDB}$ , output high (Note 6)		-250		-40	
Driver Short-Circuit Foldback Output Current	$I_{OSDF}$	$(V_{DDB} - 1V) \leq V_{OUT} \leq +12V$ , output low (Note 6)		+20			mA
		$-7V \leq V_{OUT} \leq +1V$ , output high (Note 6)				-20	
RECEIVER							
Input Current (A and B)	$I_A, I_B$	DE = low, $V_{DDB} = GNDB$ or 5.5V	$V_{IN} = +12V$	+125			$\mu A$
			$V_{IN} = -7V$	-100			
Receiver Differential Threshold Voltage	$V_{TH}$	$-7V \leq V_{CM} \leq +12V$		-200	-125	-50	mV
Receiver Input Hysteresis	$\Delta V_{TH}$	$V_{CM} = 0V$		15			mV
Receiver Input Resistance	$R_{IN}$	$-7V \leq V_{CM} \leq +12V$ , DE = low		96	$k\Omega$		
PROTECTION							
Thermal-Shutdown Threshold	$T_{SHDN}$	Temperature Rising		+160			$^{\circ}C$
Thermal-Shutdown Hysteresis	$T_{HYST}$			15			$^{\circ}C$
ESD Protection (A and B Pins to GNDB)		Human Body Model		$\pm 30$			kV
		IEC 61000-4-2 Air Gap Discharge		$\pm 15$			
		IEC 61000-4-2 Contact Discharge		$\pm 10$			
ESD Protection (All Other Pins)		Human Body Model		$\pm 4$			kV

## Switching Electrical Characteristics

(V<sub>DDA</sub> – V<sub>GNDA</sub> = 1.71V to 5.5V, V<sub>DDB</sub> – V<sub>GNDB</sub> = 4.5V to 5.5V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at V<sub>DDA</sub> – V<sub>GNDA</sub> = 3.3V, V<sub>DDB</sub> – V<sub>GNDB</sub> = 5V, V<sub>GNDA</sub> = V<sub>GNDB</sub>, and T<sub>A</sub> = +25°C.) (Note 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DYNAMIC</b>						
Common Mode Transient Immunity	CMTI	(Note 8)		35		kV/μs
Glitch Rejection		TXD, DE, RXD	10	17	29	ns
<b>DRIVER</b>						
Driver Propagation Delay	t <sub>DPLH</sub> , t <sub>DPHL</sub>	R <sub>L</sub> = 54Ω, C <sub>L</sub> = 50pF, Figure 2 and Figure 3			1040	ns
Differential Driver Output Skew  t <sub>DPLH</sub> – t <sub>DPHL</sub>	t <sub>DSKEW</sub>	R <sub>L</sub> = 54Ω, C <sub>L</sub> = 50pF, Figure 2 and Figure 3			144	ns
Driver Differential Output Rise or Fall Time	t <sub>LH</sub> , t <sub>HL</sub>	R <sub>L</sub> = 54Ω, C <sub>L</sub> = 50pF, Figure 2 and Figure 3			900	ns
Maximum Data Rate	DR <sub>MAX</sub>		500			kbps
Driver Enable to Output High	t <sub>DZH</sub>	R <sub>L</sub> = 500Ω, C <sub>L</sub> = 50pF, Figure 4			2540	ns
Driver Enable to Output Low	t <sub>DZL</sub>	R <sub>L</sub> = 500Ω, C <sub>L</sub> = 50pF, Figure 5			2540	ns
Driver Disable Time from Low	t <sub>DLZ</sub>	R <sub>L</sub> = 500Ω, C <sub>L</sub> = 50pF, Figure 5			140	ns
Driver Disable Time from High	t <sub>DHZ</sub>	R <sub>L</sub> = 500Ω, C <sub>L</sub> = 50pF, Figure 4			140	ns
<b>RECEIVER</b>						
Receiver Propagation Delay	t <sub>RPLH</sub> , t <sub>RPHL</sub>	C <sub>L</sub> = 15pF, Figure 6 and 7 (Note 9)			240	ns
Receiver Output Skew  t <sub>RPLH</sub> – t <sub>RPHL</sub>	t <sub>RSKEW</sub>	C <sub>L</sub> = 15pF, Figure 6 and 7 (Note 9)			34	ns
Maximum Data Rate	DR <sub>MAX</sub>		500			kbps
Receiver Enable to Output High	t <sub>RZH</sub>	R <sub>L</sub> = 1kΩ, C <sub>L</sub> = 15pF, S2 closed, Figure 8			20	ns
Receiver Enable to Output Low	t <sub>RZL</sub>	R <sub>L</sub> = 1kΩ, C <sub>L</sub> = 15pF, S1 closed, Figure 8			30	ns
Receiver Disable Time From Low	t <sub>RLZ</sub>	R <sub>L</sub> = 1kΩ, C <sub>L</sub> = 15pF, S1 closed, Figure 8			20	ns
Receiver Disable Time From High	t <sub>RHZ</sub>	R <sub>L</sub> = 1kΩ, C <sub>L</sub> = 15pF, S2 closed, Figure 8			20	ns

**Note 2:** All devices are 100% production tested at T<sub>A</sub> = +25°C. Specifications over temperature are guaranteed by design.

**Note 3:** All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to their respective ground (GNDA or GNDB), unless otherwise noted.

**Note 4:** V<sub>LDO</sub> max indicates voltage capability of the circuit. Power dissipation requirements may limit V<sub>LDO</sub> max to a lower value.

**Note 5:** ΔV<sub>OD</sub> and ΔV<sub>OC</sub> are the changes in V<sub>OD</sub> and V<sub>OC</sub>, respectively, when the TXD input changes state.

**Note 6:** The short circuit output current applies to the peak current just prior to foldback current limiting.

**Note 7:** Not production tested. Guaranteed by design.

**Note 8:** CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output states. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDA and GNDB.

**Note 9:** Capacitive load includes test probe and fixture capacitance.

## Insulation Characteristics

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	V <sub>PR</sub>	Method B1 = V <sub>IORM</sub> × 1.875 (t = 1s, partial discharge < 5pC)	1182	V <sub>P</sub>
Maximum Repetitive Peak Withstand Voltage	V <sub>IORM</sub>	Peak voltage for 50 yrs, min (Note 7)	630	V <sub>P</sub>
Maximum Working Isolation Voltage	V <sub>IOWM</sub>	(Note 7)	445	V <sub>RMS</sub>
Maximum Transient Isolation Voltage	V <sub>IOTM</sub>	t = 1s	4600	V <sub>P</sub>
Maximum Withstand Isolation Voltage	V <sub>ISO</sub>	t = 60s, f = 60Hz (Note 7, 8)	2750	V <sub>RMS</sub>
Maximum Surge Isolation Voltage	V <sub>ISOM</sub>	IEC 61000-4-5, 1.2/50μs	10	kV
Insulation Resistance	R <sub>S</sub>	T <sub>A</sub> = +150°C, V <sub>IO</sub> = 500V	>10 <sup>9</sup>	Ω
Barrier Capacitance Input to Output	C <sub>IO</sub>		2	pF
Creepage Distance	CPG	Wide SO	8	mm
Clearance Distance	CLR	Wide SO	8	mm
Internal Clearance		Distance through insulation	0.015	mm
Comparitive Tracking Resistance Index	CTI	Material Group II (IEC 60112)	575	
Climatic Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

**Note 10:** V<sub>IORM</sub>, V<sub>IOWM</sub>, and V<sub>ISO</sub> are defined by the IEC 60747-5-5 standard.

**Note 11:** Product is qualified at V<sub>ISO</sub> for 60 seconds. 100% production tested at 120% of V<sub>ISO</sub> for 1 second.

## Safety Regulatory Approvals

<b>UL</b>
The MAX14945 is certified under UL1577. For more details, see File E351759.
Rate up to 2750V <sub>RMS</sub> isolation voltage for basic insulation.
<b>cUL</b>
The MAX14945 is certified under UL1577. For more details, see File E351759. Rate up to 2750V <sub>RMS</sub> isolation voltage for basic insulation.

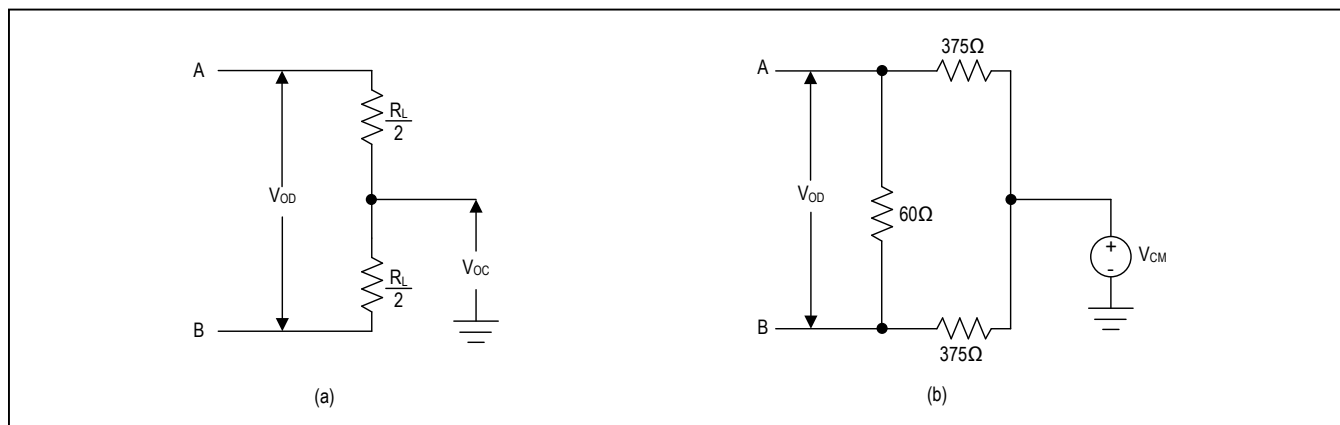


Figure 1. Driver DC Test Load

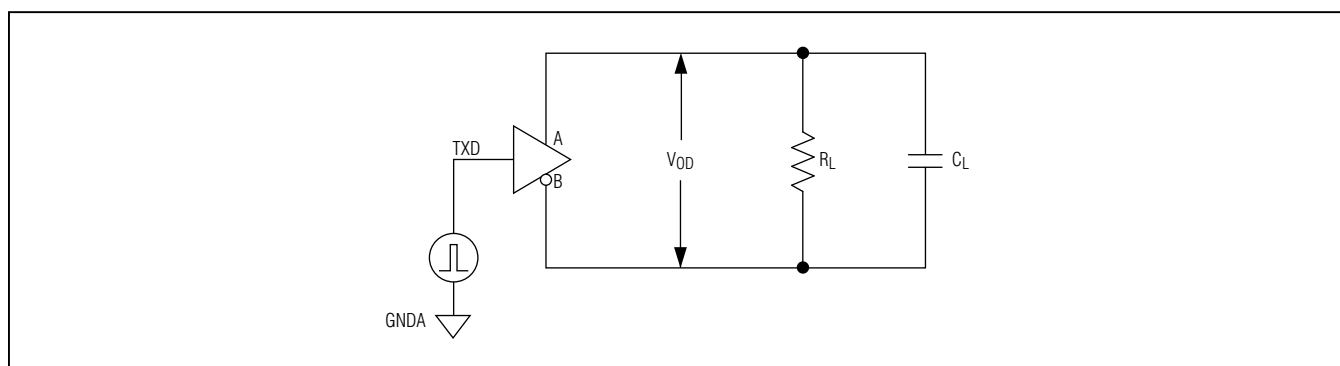


Figure 2. Driver Timing Test Circuit

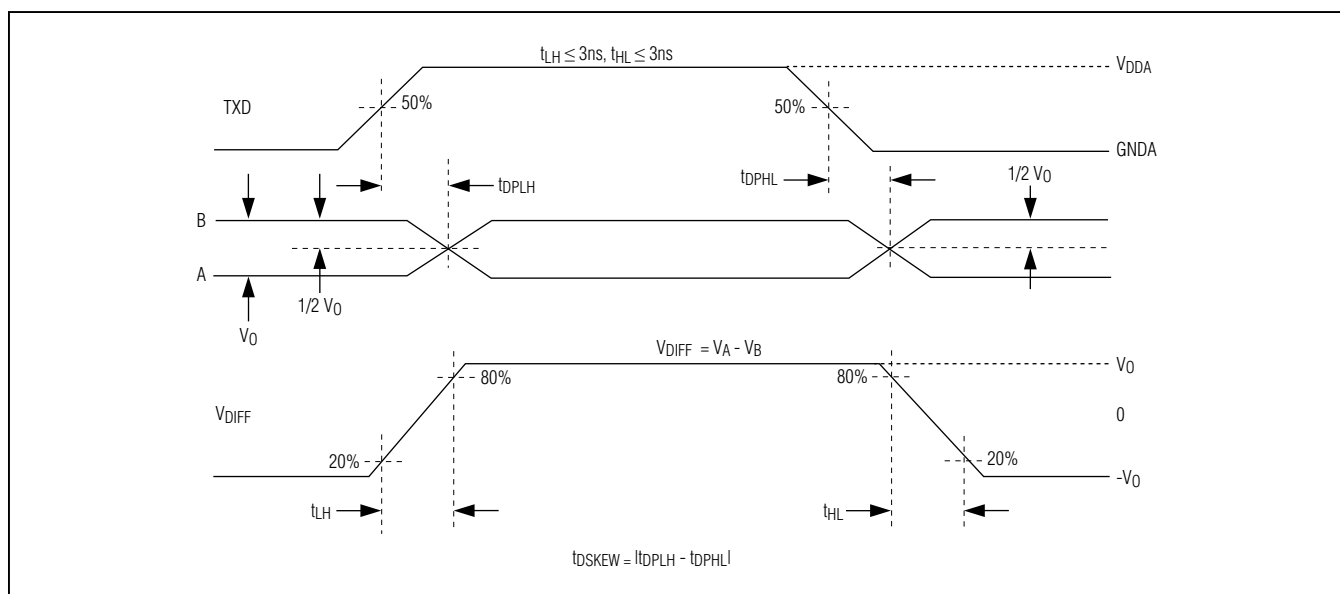


Figure 3. Driver Propagation Delays

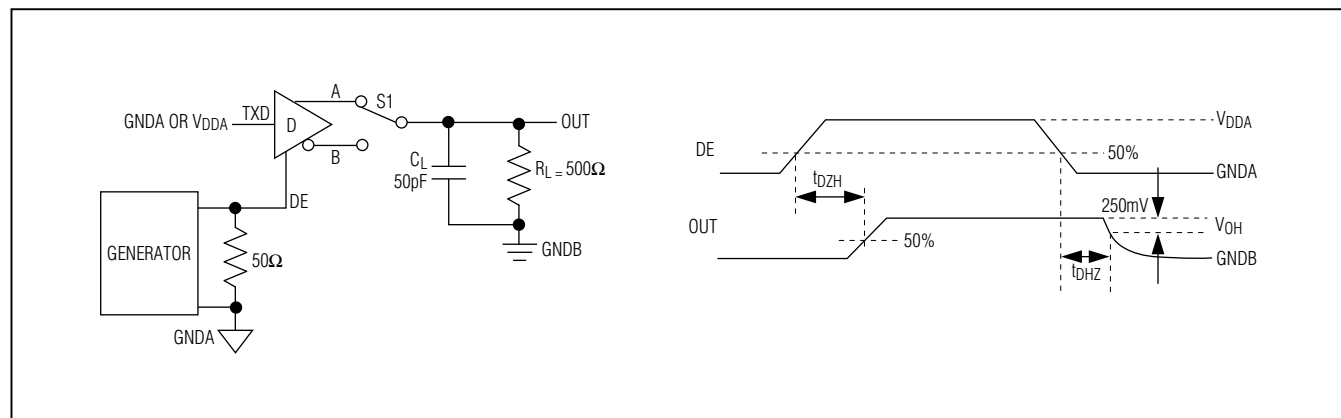
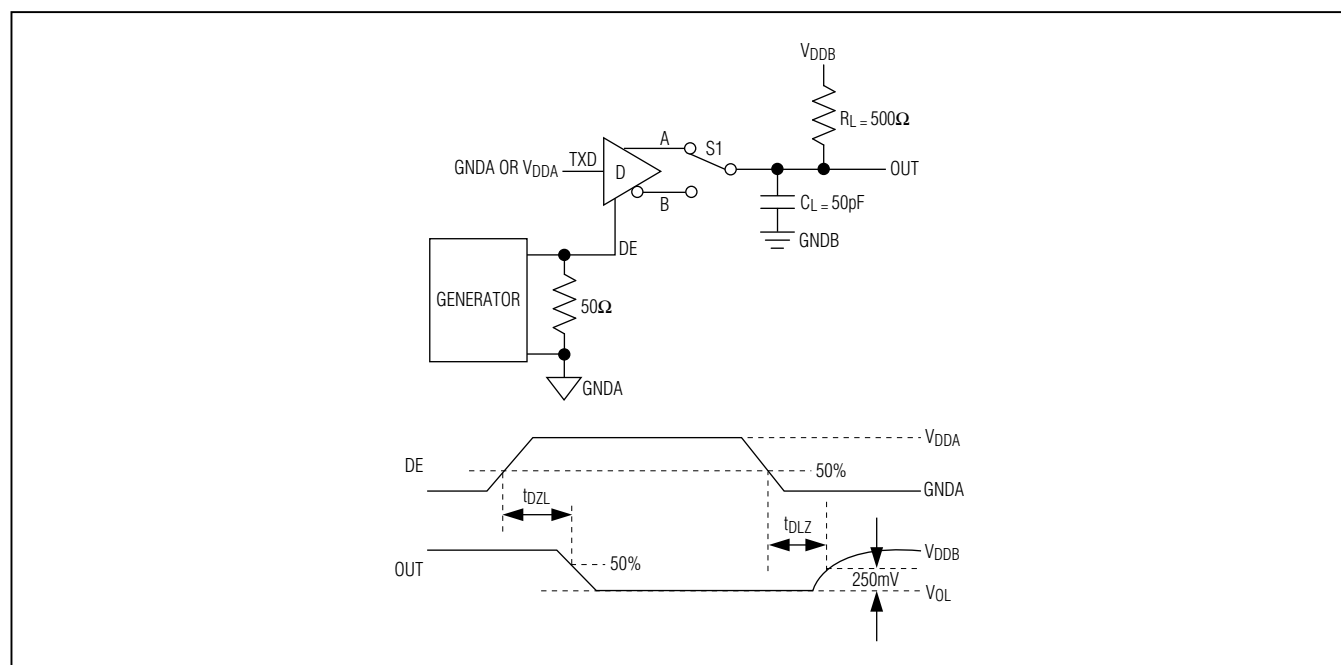
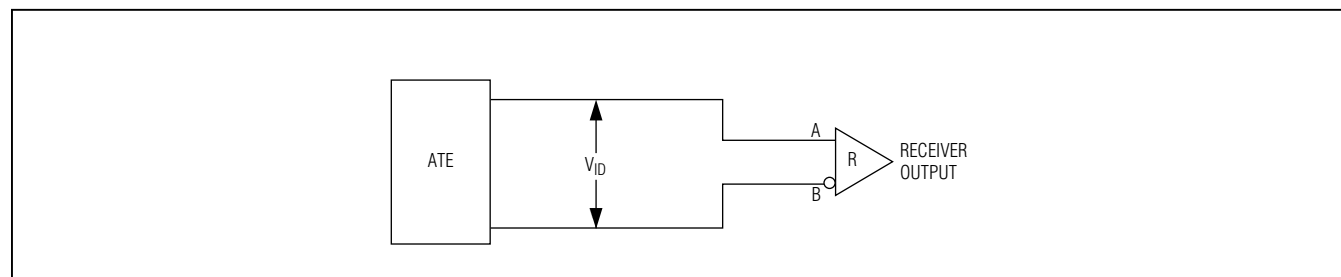
Figure 4. Driver Enable and Disable Times ( $t_{DZH}$ ,  $t_{DZL}$ )Figure 5. Driver Enable and Disable Times ( $t_{DZL}$ ,  $t_{DLZ}$ )

Figure 6. Receiver Propagation Delay Test Circuit



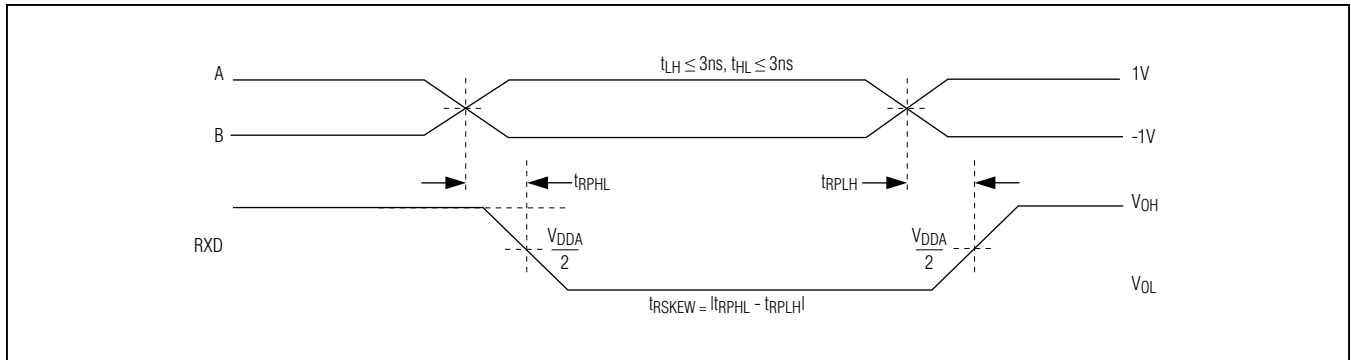


Figure 7. Receiver Propagation Delays

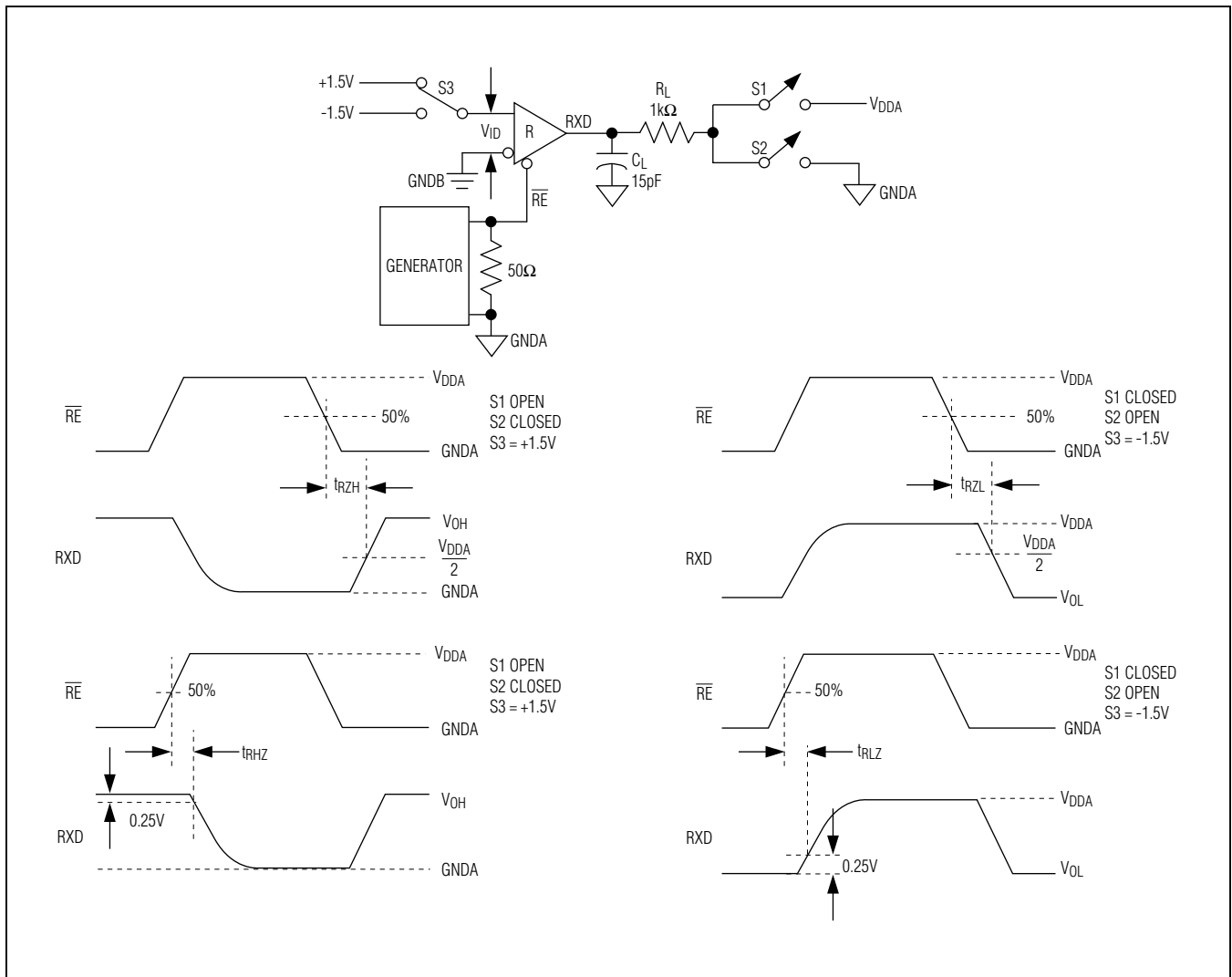
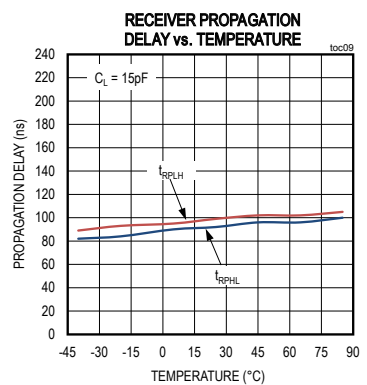
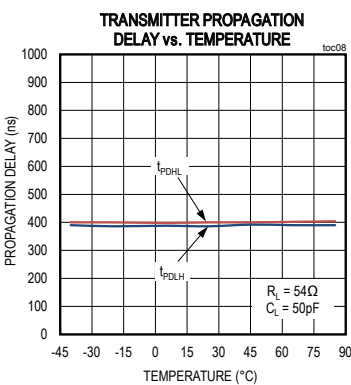
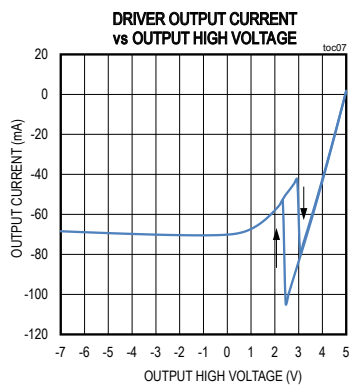
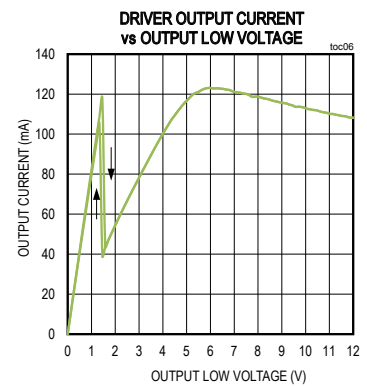
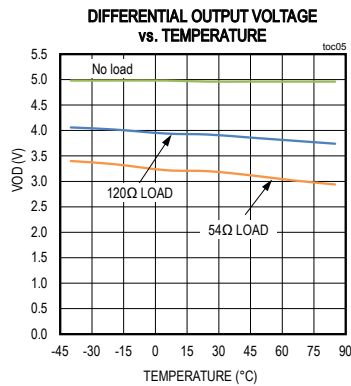
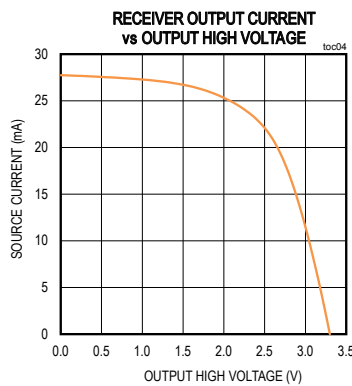
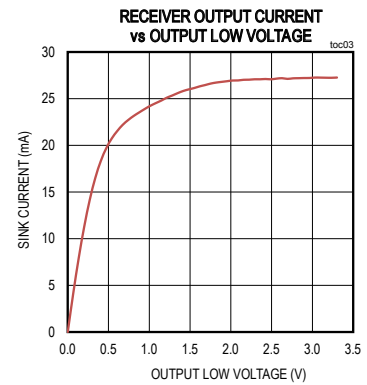
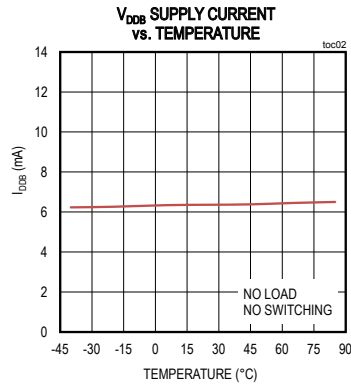
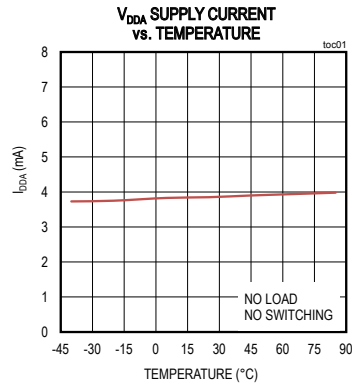


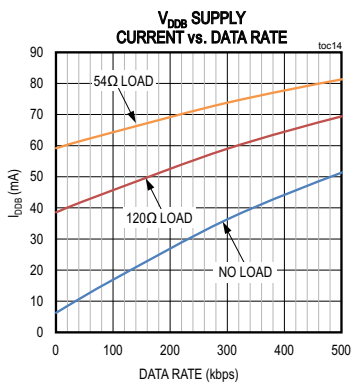
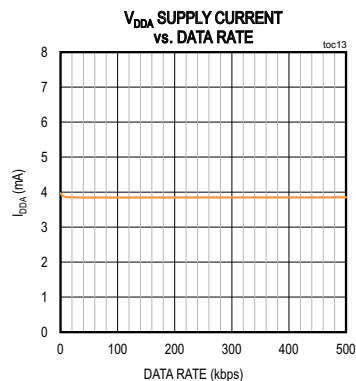
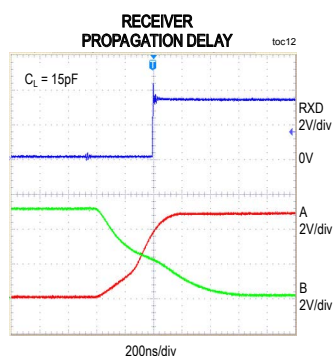
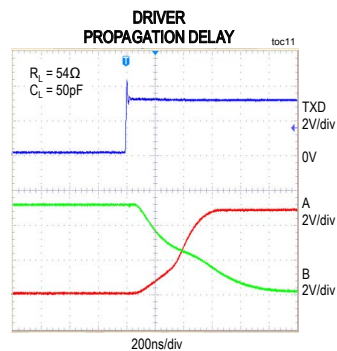
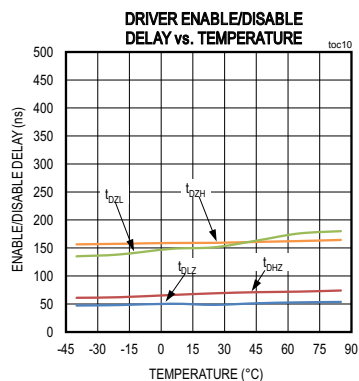
Figure 8. Receiver Enable and Disable Times

## Typical Operating Characteristics

( $V_{DDA} - V_{GNDA} = 3.3\text{V}$ ,  $V_{DDB} - V_{GNDB} = 5\text{V}$ ,  $V_{GNDA} = V_{GNDB}$ , and  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



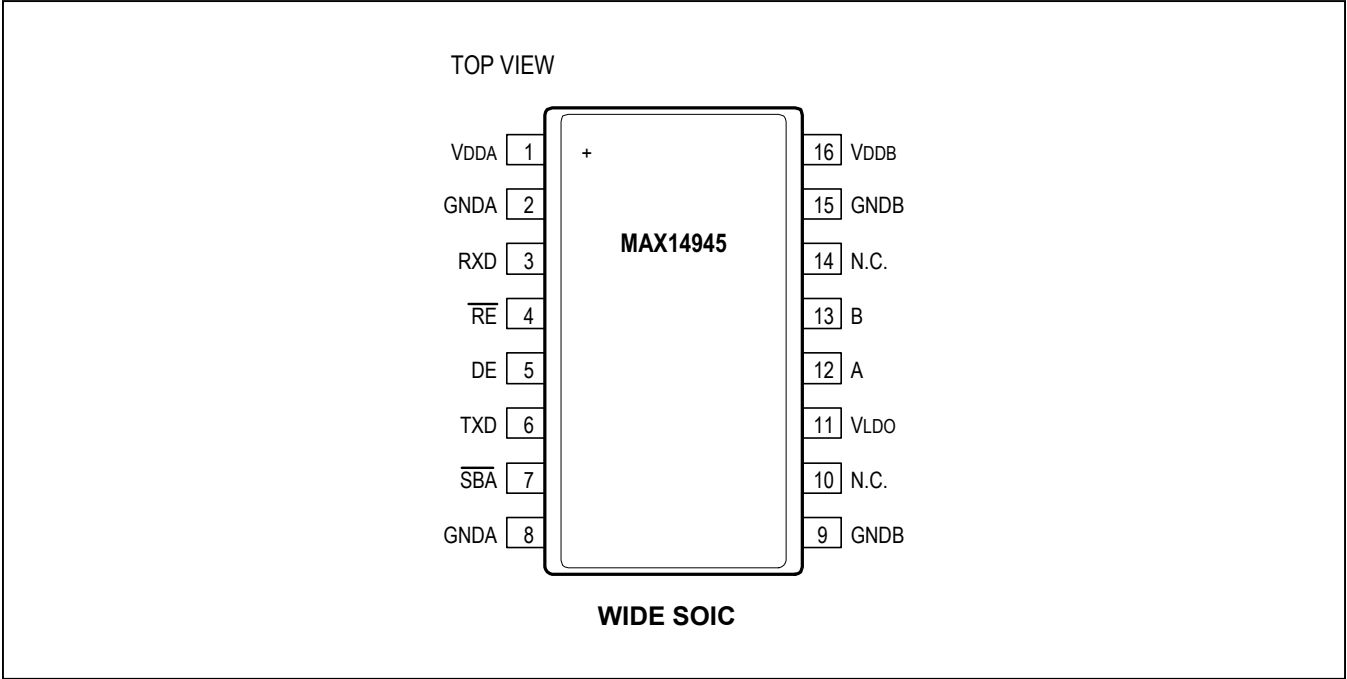
## Typical Operating Characteristics (continued)

(V<sub>DDA</sub> – V<sub>GNDA</sub> = 3.3V, V<sub>DDB</sub> – V<sub>GNDB</sub> = 5V, V<sub>GNDA</sub> = V<sub>GNDB</sub>, and T<sub>A</sub> = +25°C, unless otherwise noted.)

MAX14945

2.75kV<sub>RMS</sub> Isolated 500kbps Half-Duplex RS-485/  
RS-422 Transceiver with ±30kV ESD Protection

Pin Configuration



Pin Description

PIN	NAME	REFERENCE	FUNCTION
1	VDDA	GNDA	UART/Logic-Side Power Input. Bypass VDDA to GNDA with both 0.1μF and 1μF capacitors as close to the device as possible.
2, 8	GNDA	—	UART/Logic-Side Ground. GNDA is the ground reference for digital signals.
3	RXD	GNDA	Receiver Data Output. Drive $\overline{RE}$ low to enable RXD. With $\overline{RE}$ low, RXD is high when $(V_A - V_B) > -50\text{mV}$ and is low when $(V_A - V_B) < -200\text{mV}$ . RXD is high when VDDB is less than VUVLOB. RXD is high impedance when $\overline{RE}$ is high.
4	$\overline{RE}$	GNDA	Receiver Output Enable. Drive $\overline{RE}$ low or connect to GNDA to enable RXD. Drive $\overline{RE}$ high to disable RXD. RXD is high-impedance when $\overline{RE}$ is high. $\overline{RE}$ has an internal 4.5μA pulldown to GNDA.

## Pin Description (continued)

PIN	NAME	REFERENCE	FUNCTION
5	DE	GNDA	Driver Output Enable. Drive DE high to enable bus driver outputs A and B. Drive DE low or connect to GNDA to disable A and B. A and B are high impedance when DE is low. DE has an internal 4.5 $\mu\text{A}$ pulldown to GNDA.
6	TXD	GNDA	Driver Input. With DE high, a low on TXD forces the noninverting output (A) low and the inverting output (B) high. Similarly, a high on TXD forces the noninverting output high and the inverting output low. TXD has an internal 4.5 $\mu\text{A}$ pullup to V <sub>DDA</sub> .
7	$\overline{\text{SBA}}$	GNDA	Side B Active Indicator Output. $\overline{\text{SBA}}$ asserts low when side B is powered and working. $\overline{\text{SBA}}$ has an internal 5k $\Omega$ pullup resistor to V <sub>DDA</sub> .
9, 15	GNDB	—	Cable-Side Ground. GNDB is the ground reference for the internal LDO and the RS-485/RS-422 bus signals.
10, 14	N.C.	—	No Connection. Not internally connected.
11	V <sub>LDO</sub>	GNDB	LDO Power Input. Connect a minimum voltage of 4.68V to V <sub>LDO</sub> to power the cable-side of the transceiver. Bypass V <sub>LDO</sub> to GNDB with both 0.1 $\mu\text{F}$ and 1 $\mu\text{F}$ capacitors as close to the device as possible. To disable the internal LDO, leave V <sub>LDO</sub> unconnected or connect to GNDB.
12	A	GNDB	Noninverting Receiver Input and Noninverting Driver Output
13	B	GNDB	Inverting Receiver Input and Inverting Driver Output
16	V <sub>DDB</sub>	GNDB	Cable-Side Power Input/Isolated LDO Power Output. Bypass V <sub>DDB</sub> to GNDB with both 0.1 $\mu\text{F}$ and 1 $\mu\text{F}$ capacitor as close as possible to the device. V <sub>DDB</sub> is the output of the internal LDO when power is applied to V <sub>LDO</sub> . When the internal LDO is not used (V <sub>LDO</sub> is unconnected or connected to GNDB), V <sub>DDB</sub> is the positive supply input for the cable-side of the IC.

## Function Tables

TRANSMITTING					
INPUTS				OUTPUTS	
V <sub>DDA</sub>	V <sub>DDB</sub>	DE	TXD	A	B
$\geq V_{UVLOA}$	$\geq V_{UVLOB}$	1	1	1	0
$\geq V_{UVLOA}$	$\geq V_{UVLOB}$	1	0	0	1
$\geq V_{UVLOA}$	$\geq V_{UVLOB}$	0	X	High-Z	High-Z
$< V_{UVLOA}$	$\geq V_{UVLOB}$	X	X	High-Z	High-Z
$\geq V_{UVLOA}$	$< V_{UVLOB}$	X	X	High-Z	High-Z
$< V_{UVLOA}$	$< V_{UVLOB}$	X	X	High-Z	High-Z

\*Note: Drive DE low to disable the transmitter outputs. Drive DE high to enable the transmitter outputs. DE has an internal pull-down to G<sub>ND</sub>A.

X = Don't care

RECEIVING				
INPUTS				OUTPUTS
V <sub>DDA</sub>	V <sub>DDB</sub>	$\overline{RE}$	(V <sub>A</sub> - V <sub>B</sub> )	RXD
$\geq V_{UVLOA}$	$\geq V_{UVLOB}$	0	$> -50\text{mV}$	1
$\geq V_{UVLOA}$	$\geq V_{UVLOB}$	0	$< -200\text{mV}$	0
$\geq V_{UVLOA}$	$\geq V_{UVLOB}$	0	Open/Short	1
$\geq V_{UVLOA}$	$\geq V_{UVLOB}$	1	X	High-Z
$< V_{UVLOA}$	$\geq V_{UVLOB}$	X	X	High-Z
$\geq V_{UVLOA}$	$< V_{UVLOB}$	0	X	1
$< V_{UVLOA}$	$< V_{UVLOB}$	X	X	High-Z

\*Note: Drive  $\overline{RE}$  high to disable the receiver output. Drive  $\overline{RE}$  low to enable to receiver output.  $\overline{RE}$  has an internal pull-down to G<sub>ND</sub>A.

X = Don't care

$\overline{SBA}$		
V <sub>DDA</sub>	V <sub>DDB</sub>	$\overline{SBA}$
$< V_{UVLOA}$	$< V_{UVLOB}$	High
$< V_{UVLOA}$	$\geq V_{UVLOB}$	High
$\geq V_{UVLOA}$	$< V_{UVLOB}$	High
$\geq V_{UVLOA}$	$\geq V_{UVLOB}$	Low

## Detailed Description

The MAX14945 isolated RS-485/RS-422 transceiver provides 2750V<sub>RMS</sub> (60s) of galvanic isolation between the RS-485/RS-422 cable side of the transceiver and the UART side. This device allows up to 500kbps communication across an isolation barrier when a large potential exists between grounds on each side of the barrier.

### Isolation

Data isolation is achieved using integrated capacitive isolation that allows data transmission between the UART-side and the cable-side of the transceiver.

### Integrated LDO

The device includes an internal low-dropout regulator with a set 5V (typ) output that is used to power the cable-side of the IC. The output of the LDO is  $V_{DDB}$ . The LDO has a 300mA (typ) current limit. If the LDO is unused, connect  $V_{LDO}$  to GND and apply +5V directly to  $V_{DDB}$ .

### True Fail-Safe

The device guarantees a logic-high on the receiver output when the receiver inputs are shorted or open, or when connected to a terminated transmission line with all drivers disabled. The receiver threshold is fixed between -50mV and -200mV. If the differential receiver input voltage ( $V_A - V_B$ ) is greater than or equal to -50mV, RXD is logic-high. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to zero by the termination resistors. Due to the receiver thresholds of the MAX14945, this results in a logic-high at RXD.

## Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or bus contention. The first, a foldback current limit on the output stage, provides immediate protection against short circuits over the entire common-mode voltage range. The second, a thermal-shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature exceeds +160°C (typ).

### Thermal Shutdown

The device is protected from overtemperature damage by integrated thermal shutdown circuitry. When the junction temperature ( $T_J$ ) exceeds +160°C (typ), the driver outputs go high-impedance. The device resumes normal operation when  $T_J$  falls below +145°C (typ).

## Applications Information

### 256 Transceivers on the Bus

The standard RS-485 receiver input impedance is one unit load. A standard driver can drive up to 32 unit-loads. The MAX14945 transceiver has a 1/8-unit load receiver, which allows up to 256 transceivers, connected in parallel, on one communication line. Connect any combination of these devices, and/or other RS-485 devices, for a maximum of 32 unit-loads to the line.

### Typical Application

The MAX14945 transceiver is designed for bidirectional data communications on multipoint bus transmission lines. [Figure 9](#) shows a typical network application circuit. To minimize reflections, the bus should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible.

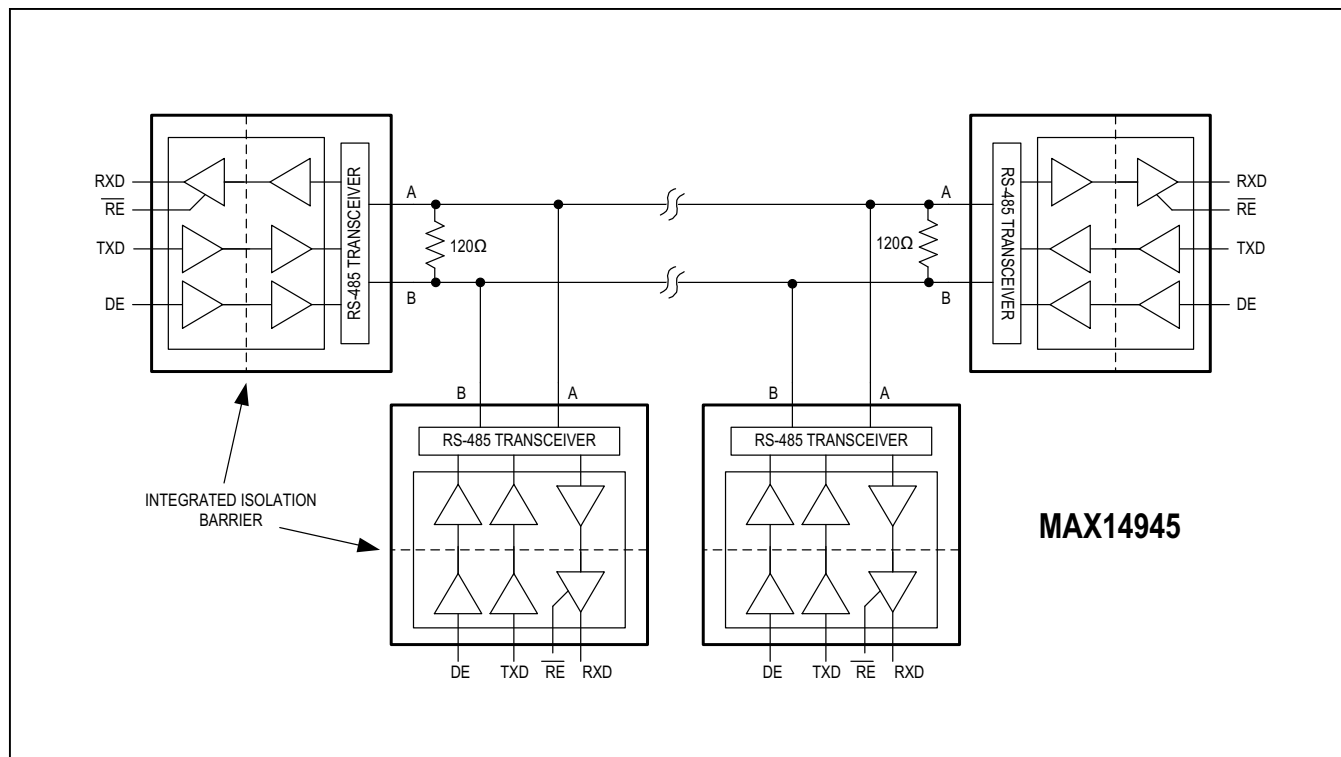


Figure 9. Typical Isolated Half-Duplex RS-485 Application



### Layout Considerations

It is recommended to design an isolation, or keep-out channel underneath the isolator that is free from ground and signal planes. Any galvanic or metallic connection between the cable-side and UART-side defeats the isolation.

Ensure that the decoupling capacitors between  $V_{DDA}$  and  $GNDA$  and between  $V_{LDO}$ ,  $V_{DDB}$ , and  $GNDB$  are located as close as possible to the IC to minimize inductance.

Route important signal lines close to the ground plane to minimize possible external influences. On the cable-side of the device, it is good practice to have the bus connectors and termination resistor as close as possible to the A and B pins.

### Extended ESD Protection

ESD protection structures are incorporated on all pins to protect against electrostatic discharge encountered during handling and assembly. The driver outputs and receiver inputs of the MAX14945 have extra protection against static electricity to both the UART-side and cable-side ground references. The ESD structures withstand high-ESD events during normal operation and when powered down. After an ESD event, the devices keep working without latch-up or damage.

Bypass  $V_{DDA}$  to  $GNDA$  and bypass  $V_{DDB}$  and  $V_{LDO}$  to  $GNDB$  with  $0.1\mu\text{F}$  and  $1\mu\text{F}$  capacitors to ensure maximum ESD protection.

ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the MAX14945 are characterized for protection to the cable-side ground ( $GNDB$ ) to the following limits:

- $\pm 30\text{kV}$  HBM
- $\pm 15\text{kV}$  using the Air-Gap Discharge method specified in IEC 61000-4-2
- $\pm 10\text{kV}$  using the Contact Discharge method specified in IEC 61000-4-2

### ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

### Human Body Model (HBM)

[Figure 10](#) shows the HBM test model, while [Figure 11](#) shows the current waveform it generates when discharged in a low-impedance state. This model consists of a  $100\text{pF}$  capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a  $1.5\text{k}\Omega$  resistor.

### IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The MAX14945 help in designing equipment to meet IEC 61000-4-2 without the need for additional ESD protection components.

The major difference between tests done using the HBM and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the HBM.

[Figure 12](#) shows the IEC 61000-4-2 model and [Figure 13](#) shows the current waveform for IEC 61000-4-2 ESD Contact Discharge Test.

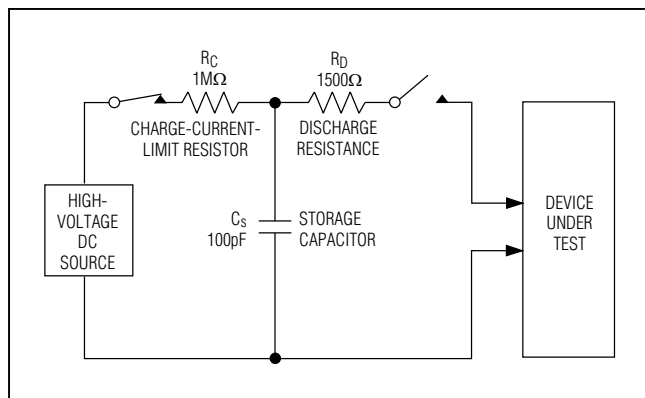


Figure 10. Human Body ESD Test Model

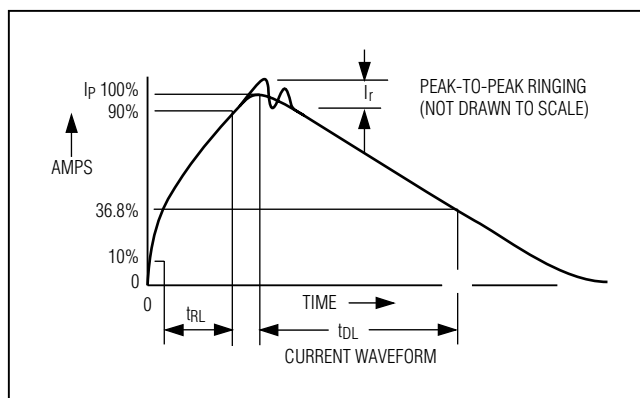


Figure 11. Human Body Current Waveform

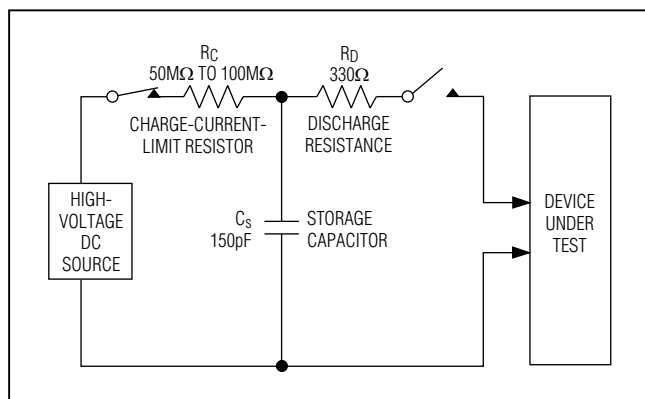


Figure 12. IEC 61000-4-2 ESD Test Model

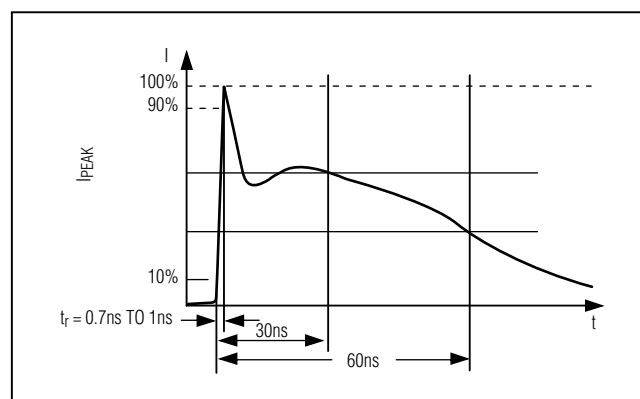
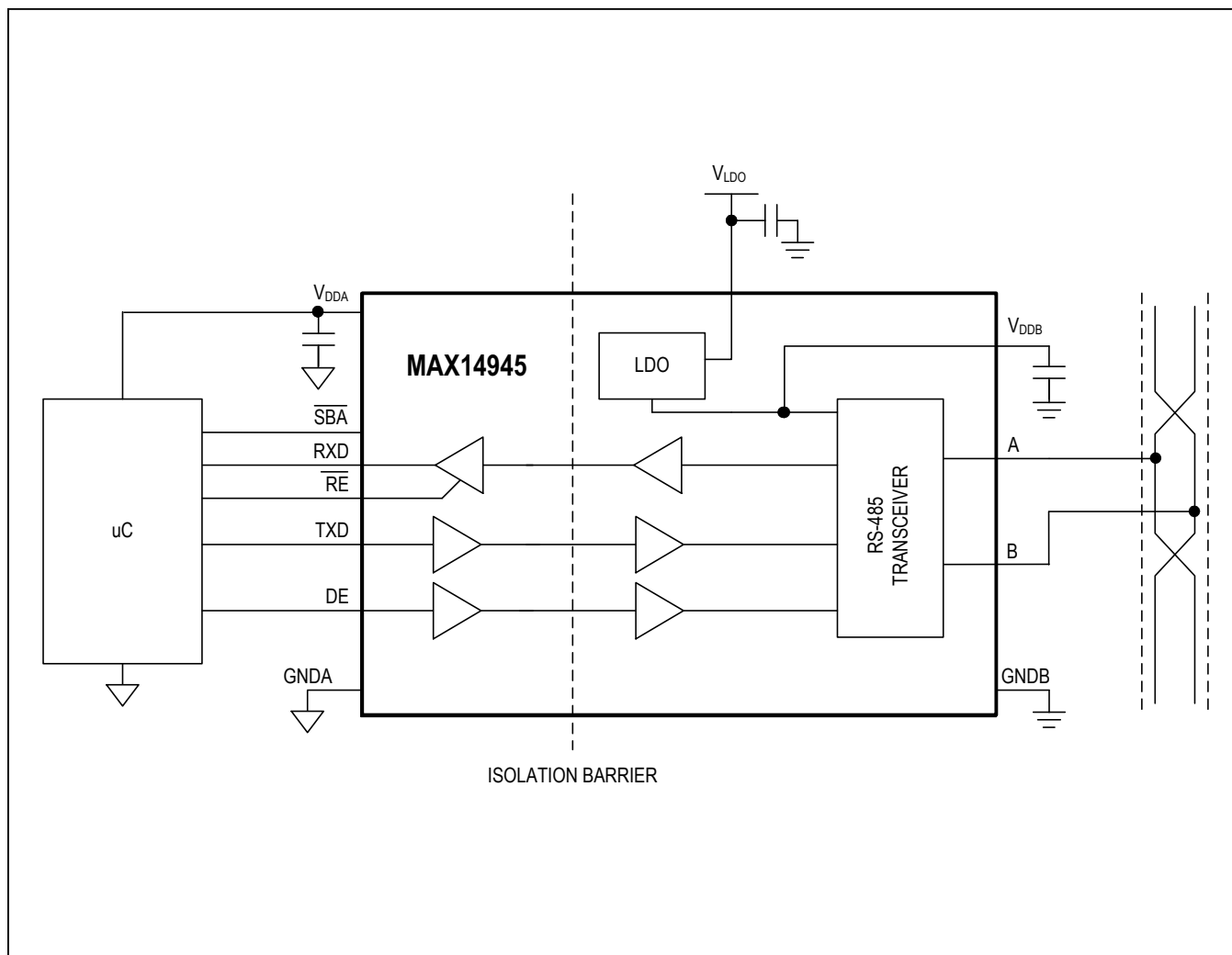


Figure 13. IEC 61000-4-2 ESD Generator Current Waveform

## Typical Application Circuit



MAX14945

2.75kV<sub>RMS</sub> Isolated 500kbps Half-Duplex RS-485/  
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### Ordering Information/Selector Guide

PART	TEMP RANGE	PIN- PACKAGE
MAX14945EWE+	-40°C to +85°C	16 SOIC (W)
MAX14945EWE+T	-40°C to +85°C	16 SOIC (W)

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

### Package Information

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 SOIC	W16M+9	<a href="#">21-0042</a>	<a href="#">91-0107</a>

### Chip Information

PROCESS: BiCMOS

MAX14945

5kV Isolated 500kbps Half-Duplex RS-485/  
RS-422 Transceiver with  $\pm 30\text{kV}$  ESD Protection

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/15	Initial release	—
1	1/17	Updated pending safety approvals	1, 6

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