

+5V, 1Msps, 4 & 8-Channel, 8-Bit ADCs with 1 μ A Power-Down

ABSOLUTE MAXIMUM RATINGS

V _{DD} to GND	-0.3V to +7V	28-Pin Wide Plastic DIP	
Digital Input Voltage to GND	-0.3V to (V _{DD} + 0.3V)	(derate 14.29mW/°C above +70°C)	1.14W
Digital Output Voltage to GND	-0.3V to (V _{DD} + 0.3V)	28-Pin SSOP (derate 9.52mW/°C above +70°C)	762mW
REF+ to GND	-0.3V to (V _{DD} + 0.3V)	28-Pin Wide CERDIP	
REF- to GND	-0.3V to (V _{DD} + 0.3V)	(derate 16.67mW/°C above +70°C)	1.33W
IN ₋ to GND	-0.3V to (V _{DD} + 0.3V)	Operating Temperature Ranges	
Continuous Power Dissipation (T _A = +70°C)		MAX114/MAX118C	0°C to +70°C
24-Pin Narrow Plastic DIP		MAX114/MAX118E	-40°C to +85°C
(derate 13.33mW/°C above +70°C)	1.08W	MAX114/MAX118M	-55°C to +125°C
24-Pin SSOP (derate 8.00mW/°C above +70°C)	640mW	Storage Temperature Range	-65°C to +150°C
24-Pin Narrow CERDIP		Lead Temperature (soldering, 10sec)	+300°C
(derate 12.50mW/°C above +70°C)	1W		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V \pm 5%, REF+ = 5V, REF- = GND, Read Mode (MODE = GND), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY (Note 1)						
Resolution	N		8			Bits
Total Unadjusted Error	TUE				± 1	LSB
Differential Nonlinearity	DNL	No-missing-codes guaranteed			± 1	LSB
Zero-Code Error					± 1	LSB
Full-Scale Error					± 1	LSB
Channel-to-Channel Mismatch					$\pm 1/4$	LSB
DYNAMIC PERFORMANCE						
Signal-to-Noise Plus Distortion Ratio	SINAD	MAX11_C/E, f _{SAMPLE} = 1MHz, f _{IN} = 195.8kHz	45			dB
		MAX11_M, f _{SAMPLE} = 740kHz, f _{IN} = 195.7kHz	45			
Total Harmonic Distortion	THD	MAX11_C/E, f _{SAMPLE} = 1MHz, f _{IN} = 195.8kHz			-50	dB
		MAX11_M, f _{SAMPLE} = 740kHz, f _{IN} = 195.7kHz			-50	
Spurious-Free Dynamic Range	SFDR	MAX11_C/E, f _{SAMPLE} = 1MHz, f _{IN} = 195.8kHz	50			dB
		MAX11_M, f _{SAMPLE} = 740kHz, f _{IN} = 195.7kHz	50			
Input Full-Power Bandwidth		V _{IN} = 5Vp-p		1		MHz
Input Slew Rate, Tracking			3.1	15		V/ μ s
ANALOG INPUT						
Input Voltage Range	V _{IN}		V _{REF-}		V _{REF+}	V
Input Leakage Current	I _{IN}	GND < V _{IN} < V _{DD}			± 3	μ A
Input Capacitance	C _{IN}			32		pF
REFERENCE INPUT						
Reference Resistance	R _{REF}		1	2	4	k Ω
REF+ Input Voltage Range			V _{REF-}		V _{DD}	V
REF- Input Voltage Range			GND		V _{REF+}	V

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MAX114/MAX118

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, REF+ = 5V, REF- = GND, Read Mode (MODE = GND), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS						
Input High Voltage	V _{INH}	\overline{CS} , \overline{WR} , \overline{RD} , \overline{PWRDN} , A0, A1, A2	2.4			V
		MODE	3.5			
Input Low Voltage	V _{INL}	\overline{CS} , \overline{WR} , \overline{RD} , \overline{PWRDN} , A0, A1, A2			0.8	V
		MODE			1.5	
Input High Current	I _{INH}	\overline{CS} , \overline{RD} , \overline{PWRDN} , A0, A1, A2			±1	μA
		\overline{WR}			±3	
		MODE		50	200	
Input Low Current	I _{INL}	\overline{CS} , \overline{WR} , \overline{RD} , \overline{PWRDN} , MODE, A0, A1, A2			±1	μA
Input Capacitance (Note 2)	C _{IN}	\overline{CS} , \overline{WR} , \overline{RD} , \overline{PWRDN} , MODE, A0, A1, A2		5	8	pF
LOGIC OUTPUTS						
Output Low Voltage	V _{OL}	I _{SINK} = 1.6mA, \overline{INT} , D0–D7			0.4	V
		RDY, I _{SINK} = 2.6mA			0.4	
Output High Voltage	V _{OH}	I _{SOURCE} = 360μA, \overline{INT} , D0–D7	4			V
Three-State Current	I _{LKG}	D0–D7, RDY, digital outputs = 0V to V _{DD}			±3	μA
Three-State Capacitance (Note 2)	C _{OUT}	D0–D7, RDY		5	8	pF
POWER REQUIREMENTS						
Supply Voltage	V _{DD}		4.75		5.25	V
V _{DD} Supply Current	I _{DD}	\overline{CS} = \overline{RD} = 0V, \overline{PWRDN} = V _{DD}				mA
		MAX11_C		8	15	
		MAX11_E/M		8	20	
Power-Down V _{DD} Current		\overline{CS} = \overline{RD} = V _{DD} , \overline{PWRDN} = 0V (Note 3)		1	10	μA
Power-Supply Rejection	PSR	V _{DD} = 4.75V to 5.25V, V _{REF} = 4.75V		±1/16	±1/4	LSB

Note 2: Guaranteed by design.

Note 3: Power-down current increases if logic inputs are not driven to GND or V_{DD}.

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TIMING CHARACTERISTICS

(V_{DD} = +4.75V, T_A = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		T _A = +25°C ALL GRADES			T _A = T _{MIN} to T _{MAX}				UNITS
				MIN	TYP	MAX	MAX11_C/E		MAX11_M		
							MIN	MAX	MIN	MAX	
Conversion Time (WR-RD Mode)	t _{CWR}	t _{RD} < t _{INTL} , (Note 5)	C _L = 20pF C _L = 100pF	660 685			865		1125		ns
Conversion Time (RD Mode)	t _{CRD}			700			875		975		
Power-Up Time	t _{UP}			320			370		520		ns
CS to RD, WR Setup Time	t _{CSS}			0			0		0		ns
CS to RD, WR Hold Time	t _{CSH}			0			0		0		ns
CS to RDY Delay	t _{RDY}	C _L = 50pF, R _L = 5.1kΩ to V _{DD}		70			85		100		ns
Data-Access Time (RD Mode)	t _{ACC0}	C _L = 100pF (Note 5)		t _{CRD} + 50			t _{CRD} + 65		t _{CRD} + 75		ns
RD to INT Delay (RD Mode)	t _{INTH}	C _L = 50pF		50 80			85		90		ns
Data Hold Time	t _{DH}	(Note 6)		60			70		80		ns
Minimum Acquisition Time	t _{ACQ}	(Note 7)		160			185		260		ns
WR Pulse Width	t _{WR}			0.25 10			0.28 10		0.4 10		μs
Delay Between WR and RD Pulses	t _{RD}			0.25			0.35		0.45		μs
RD Pulse Width (WR-RD Mode)	t _{READ1}	t _{RD} < t _{INTL} , determined by t _{ACC1}		160			205		240		ns
Data-Access Time (WR-RD Mode)	t _{ACC1}	t _{RD} < t _{INTL} , C _L = 100pF (Note 5)		185			235		275		ns
RD to INT Delay	t _{RI}			150			185		220		ns
WR to INT Delay	t _{INTL}	C _L = 50pF		380 500			610		700		ns
RD Pulse Width (WR-RD Mode)	t _{READ2}	t _{RD} > t _{INTL} , determined by t _{ACC2}		65			75		85		ns
Data-Access Time (WR-RD Mode)	t _{ACC2}	t _{RD} > t _{INTL} , C _L = 100pF (Note 5)		90			110		130		ns
WR to INT Delay	t _{IHWR}	Pipelined mode, C _L = 50pF		80			100		120		ns
Data-Access Time after INT	t _{ID}	Pipelined mode, C _L = 100pF		45			60		70		ns
Multiplexer Address Hold Time	t _{AH}			30			35		40		ns

Note 4: Input control signals are specified with t_r = t_f = 5ns, 10% to 90% of 5V, and timed from a voltage level of 1.6V.

Note 5: See Figure 1 for load circuit. Parameter defined as the time required for the output to cross 0.8V or 2.4V.

Note 6: See Figure 2 for load circuit. Parameter defined as the time required for the data lines to change 0.5V.

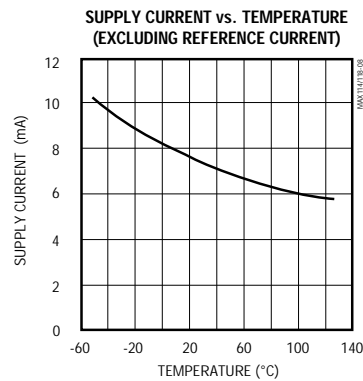
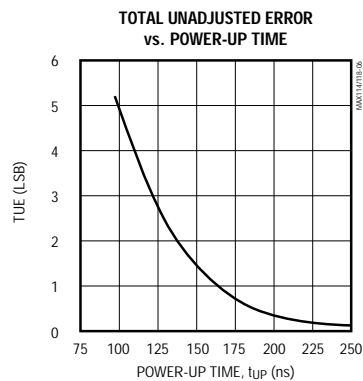
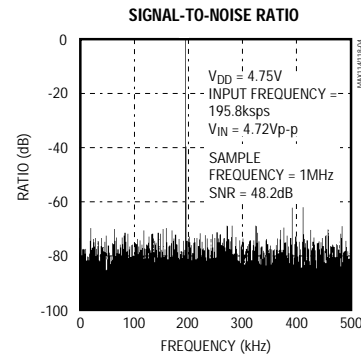
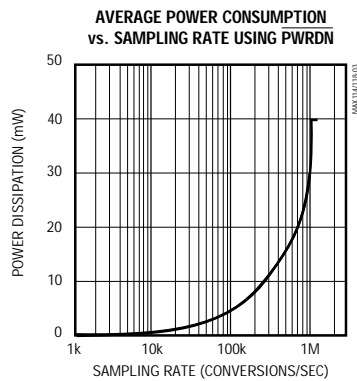
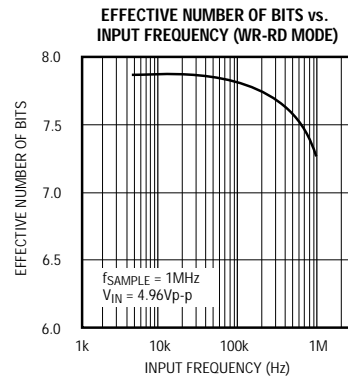
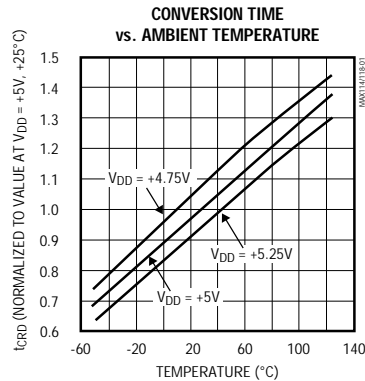
Note 7: Also defined as the Minimum Address-Valid to Convert-Start Time.

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Typical Operating Characteristics

($V_{DD} = +5V$, $T_A = +25^\circ C$, unless otherwise noted.)

MAX1114/MAX1118



+5V, 1Msps, 4 & 8-Channel, 8-Bit ADCs with 1μA Power-Down

MAX1114/MAX1118

Pin Description

PIN		NAME	FUNCTION
MAX114	MAX118		
—	1	IN6	Analog Input Channel 6
—	2	IN5	Analog Input Channel 5
1	3	IN4	Analog Input Channel 4
2	4	IN3	Analog Input Channel 3
3	5	IN2	Analog Input Channel 2
4	6	IN1	Analog Input Channel 1
5	7	MODE	Mode Selection Input. Internally pulled low with a 50μA current source. MODE = 0 activates read mode; MODE = 1 activates write-read mode (see <i>Digital Interface</i> Section).
6	8	D0	Three-State Data Output (LSB)
7, 8, 9	9, 10, 11	D1, D2, D3	Three-State Data Outputs
10	12	\overline{RD}	Read Input. \overline{RD} must be low to access data (see <i>Digital Interface</i> section).
11	13	\overline{INT}	Interrupt Output. \overline{INT} goes low to indicate end of conversion (see <i>Digital Interface</i> section).
12	14	GND	Ground
13	15	REF-	Lower Limit of Reference Span. REF- sets the zero-code voltage. Range is $GND \leq V_{REF-} < V_{REF+}$.
14	16	REF+	Upper Limit of Reference Span. REF+ sets the full-scale input voltage. Range is $V_{REF-} < V_{REF+} \leq V_{DD}$. Internally hard-wired to IN8 (Table 1).
15	17	\overline{WR}/RDY	Write-Control Input/Ready-Status Output (see <i>Digital Interface</i> section)
16	18	\overline{CS}	Chip-Select Input. \overline{CS} must be low for the device to recognize \overline{WR} or \overline{RD} inputs.
17, 18, 19	19, 20, 21	D4, D5, D6	Three-State Data Outputs
20	22	D7	Three-State Data Output (MSB)
—	23	A2	Multiplexer Channel Address Input (MSB)
21	24	A1	Multiplexer Channel Address Input
22	25	A0	Multiplexer Channel Address Input (LSB)
23	26	\overline{PWRDN}	Power-Down Input. \overline{PWRDN} reduces supply current when low.
24	27	VDD	Positive Supply, +5V
—	28	IN7	Analog Input Channel 7

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MAX114/MAX118

Detailed Description

Converter Operation

The MAX114/MAX118 use a half-flash conversion technique (see *Functional Diagram*) in which two 4-bit flash ADC sections achieve an 8-bit result. Using 15 comparators, the flash ADC compares the unknown input voltage to the reference ladder and provides the upper four data bits. An internal digital-to-analog converter (DAC) uses the four most significant bits (MSBs) to generate both the analog result from the first flash conversion and a residue voltage that is the difference between the unknown input and the DAC voltage. The residue is then compared again with the flash comparators to obtain the lower four data bits (LSBs).

An internal analog multiplexer enables the devices to read four (MAX114) or eight (MAX118) different analog voltages under microprocessor (μP) control. One of the MAX118's analog channels, IN8, is internally hard-wired and always reads VREF+ when selected.

Power-Down Mode

In burst-mode or low sample-rate applications, the MAX114/MAX118 can be shut down between conversions, reducing supply current to microamp levels (see *Typical Operating Characteristics*). A logic low on the PWRDN pin shuts the devices down, reducing supply current typically to 1μA when powered from a single +5V supply. A logic high on PWRDN wakes up the MAX114/MAX118, and the selected analog input enters the track mode. The signal is fully acquired after 360ns (this includes both the power-up delay and the track/hold acquisition time), and a new conversion can be started. If the power-down feature is not required, connect PWRDN to VDD. For minimum current consumption, keep digital inputs at the supply rails in power-down mode. Refer to the *Reference* section for information on reducing reference current during power-down.

Digital Interface

The MAX114/MAX118 have two basic interface modes, which are set by the MODE pin. When MODE is low, the converters are in read mode; when MODE is high, the converters are set up for write-read mode. The A0, A1, and A2 inputs control channel selection, as shown in Table 1. The address must be valid for a minimum time, tACQ, before the next conversion starts.

Table 1. Truth Table for Input Channel Selection

MAX114		MAX118			SELECTED CHANNEL
A1	A0	A2	A1	A0	
0	0	0	0	0	IN1
0	1	0	0	1	IN2
1	0	0	1	0	IN3
1	1	0	1	1	IN4
—	—	1	0	0	IN5
—	—	1	0	1	IN6
—	—	1	1	0	IN7
—	—	1	1	1	IN8 (reads VREF+ if selected)

Read Mode (MODE = 0)

In read mode, conversions and data access are controlled by the RD input (Figure 3). The comparator inputs track the analog input voltage for the duration of tACQ. Initiate a conversion by driving CS and RD low. With μPs that can be forced into a wait state, hold RD low until output data appears. The μP starts the conversion, waits, and then reads data with a single read instruction.

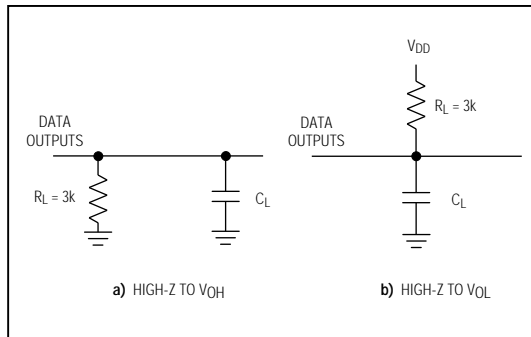


Figure 1. Load Circuits for Data-Access Time Test

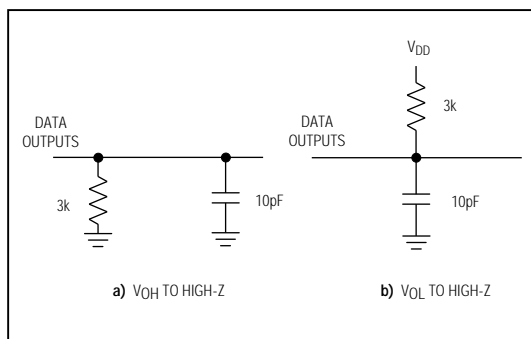


Figure 2. Load Circuits for Data-Hold Time Test

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In read mode, \overline{WR}/RDY is configured as a status output (RDY), so it can drive the ready or wait input of a μP . RDY is an open-collector output (no internal pull-up) that goes low after the falling edge of \overline{CS} and goes high at the end of the conversion. If not used, the \overline{WR}/RDY pin can be left unconnected. The \overline{INT} output goes low at the end of the conversion and returns high on the rising edge of \overline{CS} or \overline{RD} .

Write-Read Mode (MODE = 1)

Figures 4 and 5 show the operating sequence for write-read mode. The comparator inputs track the analog input voltage for the duration of t_{ACQ} . The conversion is initiated by a falling edge of \overline{WR} . When \overline{WR} returns high, the result of the four-MSBs flash is latched into the output buffers and the conversion of the four-LSBs flash starts. \overline{INT} goes low, indicating conversion end, and the lower four data bits are latched into the output buffers. The data is then accessible after \overline{RD} goes low (see *Timing Characteristics*).

A minimum acquisition time (t_{ACQ}) is required from \overline{INT} going low to the start of another conversion (\overline{WR} going low).

Options for reading data from the converter include using internal delay, reading before delay, and pipelined operation (discussed in the following sections).

Using Internal Delay

The μP waits for the \overline{INT} output to go low before reading the data (Figure 4). \overline{INT} goes low after the rising edge of \overline{WR} , indicating that the conversion is complete and the result is available in the output latch. With \overline{CS} low, data outputs D0-D7 can be accessed by pulling \overline{RD} low. \overline{INT} is then reset by the rising edge of \overline{CS} or \overline{RD} .

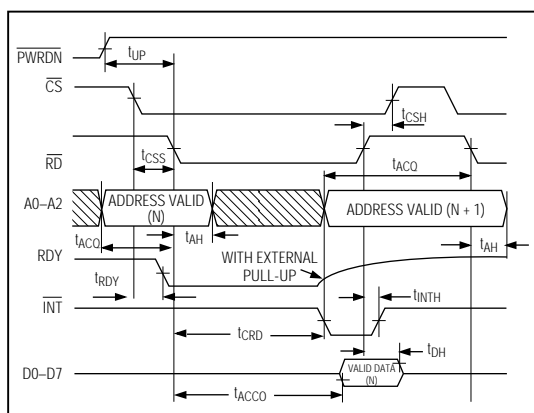


Figure 3. Read Mode Timing (MODE = 0)

Fastest Conversion: Reading Before Delay

Figure 5 shows an external method of controlling the conversion time. The internally generated delay (t_{INTL}) varies slightly with temperature and supply voltage, and can be overridden with \overline{RD} to achieve the fastest conversion time. \overline{RD} is brought low after the rising edge of \overline{WR} , but before \overline{INT} goes low. This completes the conversion and enables the output buffers that contain the conversion result (D0-D7). \overline{INT} also goes low after the falling edge of \overline{RD} and is reset on the rising edge of \overline{RD} or \overline{CS} . The total conversion time is therefore: $t_{WR} + t_{RD} + t_{ACC1} = 660ns$.

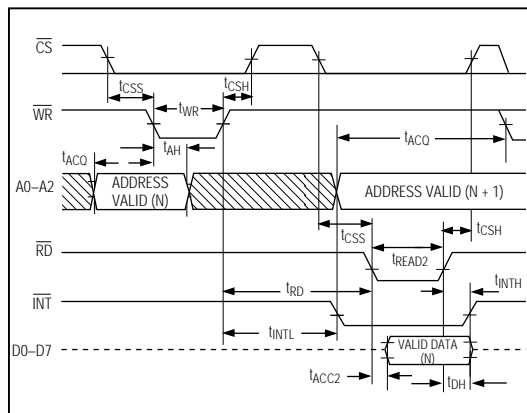


Figure 4. Write-Read Mode Timing ($t_{RD} > t_{INTL}$) (MODE = 1)

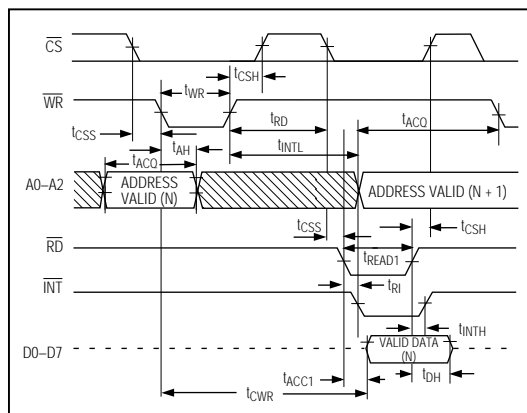


Figure 5. Write-Read Mode Timing ($t_{RD} < t_{INTL}$) (MODE = 1)

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MAX114/MAX118

Pipelined Operation

Besides the two standard write-read-mode options, pipelined operation can be achieved by connecting WR to RD (Figure 6). With CS low, driving WR and RD low initiates a conversion and concurrently reads the result of the previous conversion.

Analog Considerations

Reference

Figures 7a, 7b, and 7c show typical reference connections. The voltages at REF+ and REF- set the ADC's analog input range (see Figure 10). The voltage at REF- defines the input that produces an output code of all zeros, and the voltage at REF+ defines the input that produces an output code of all ones.

The internal resistance from REF+ to REF- can be as low as 1kΩ, and current will flow through it even when the MAX114/MAX118 are shut down. Figure 7d shows how an N-channel MOSFET can be connected to REF-

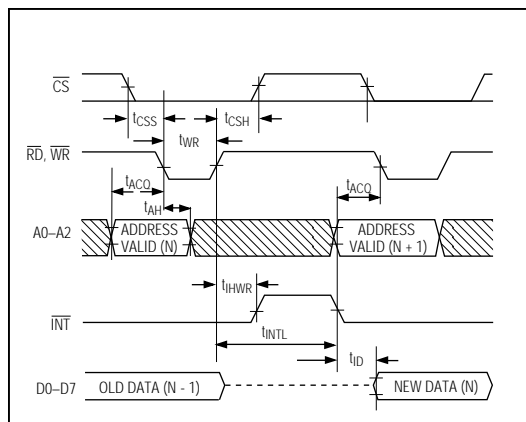


Figure 6. Pipelined Mode Timing ($\overline{WR} = \overline{RD}$) (MODE = 1)

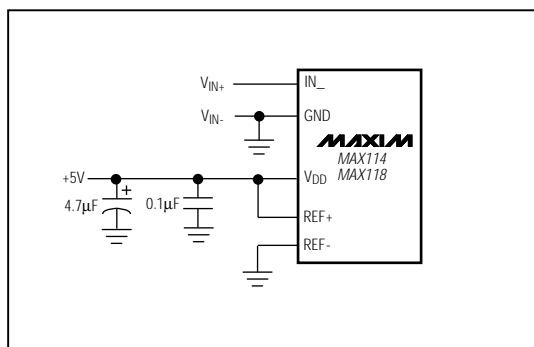


Figure 7a. Power Supply as Reference

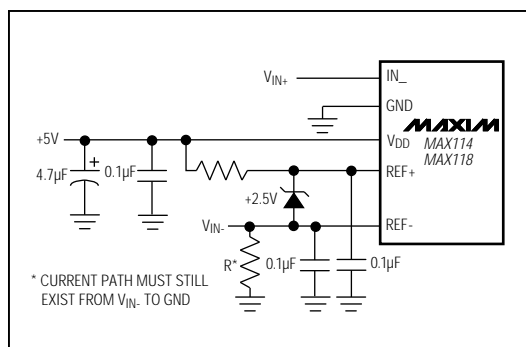


Figure 7c. Input Not Referenced to GND

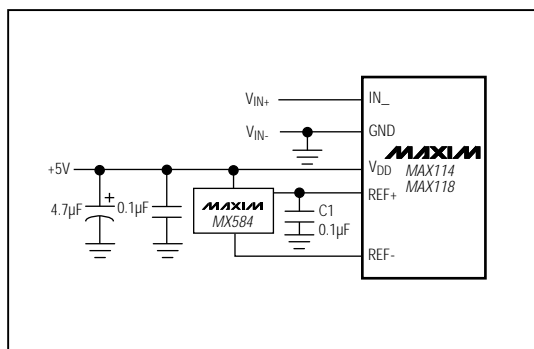


Figure 7b. External Reference, 4.096V Full Scale

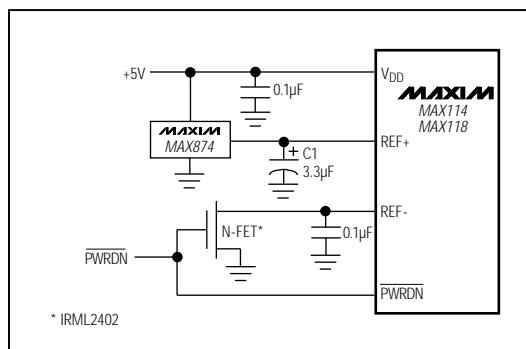


Figure 7d. An N-channel MOSFET switches off the reference load during power-down

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to break this current path during power-down. The FET should have an on-resistance of less than 2Ω with a 5V gate drive. When REF- is switched, as in Figure 7d, a new conversion can be initiated after waiting a period of time equal to the power-up delay (t_{UP}) plus the N-channel FET's turn-on time.

Although REF+ is frequently connected to V_{DD} , the circuit of Figure 7d uses a low-current, low-dropout, 4.096V voltage reference: the MAX874. Since the MAX874 cannot continuously furnish enough current for the reference resistance, this circuit is intended for applications where the MAX114/MAX118 are normally in standby and are turned on in order to make measurements at intervals greater than $65\mu s$. C1 (the capacitor connected to REF+) is slowly charged by the MAX874 during the standby period, and furnishes the reference current during the short measurement period.

C1's 3.3 μF value ensures a voltage drop of less than 1/2LSB when performing four to eight successive conversions. Larger capacitors reduce the error still further. Use ceramic or tantalum capacitors for C1.

Initial Power-Up

When power is first applied, perform a conversion to initialize the MAX114/MAX118. Disregard the output data.

Bypassing

Use a 4.7 μF electrolytic in parallel with a 0.1 μF ceramic capacitor to bypass V_{DD} to GND. Minimize capacitor lead lengths.

Bypass the reference inputs with 0.1 μF capacitors, as shown in Figures 7a, 7b, and 7c.

Analog Inputs

Figure 8 shows the equivalent circuit of the MAX114/MAX118 input. When a conversion starts and \overline{WR} is low, V_{IN-} is connected to sixteen 0.6pF capacitors. During this acquisition phase, the input capacitors charge to the input voltage through the resistance of the internal analog switches. In addition, about 22pF of stray capacitance must be charged. The input can be modeled as an equivalent RC network (Figure 9). As source impedance increases, the capacitors take longer to charge.

The typical 32pF input capacitance allows source resistance as high as 800Ω without setup problems. For larger resistances, the acquisition time (t_{ACQ}) must be increased.

Internal protection diodes, which clamp the analog input to V_{DD} and GND, allow the channel input pins to swing from GND - 0.3V to $V_{DD} + 0.3V$ without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV or be lower than GND by 50mV.

If the analog input exceeds 50mV beyond the supplies, limit the input current to no more than 2mA, as excessive current will degrade the conversion accuracy of the on channel.

Track/Hold

The track/hold enters hold mode when a conversion starts (\overline{RD} low or \overline{WR} low). \overline{INT} goes low at the end of the conversion, at which point the track/hold enters track mode. The next conversion can start after the minimum acquisition time, t_{ACQ} .

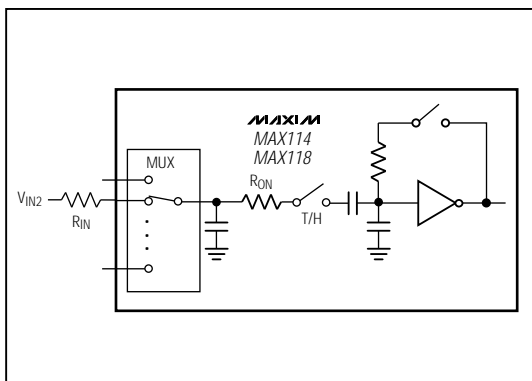


Figure 8. Equivalent Input Circuit

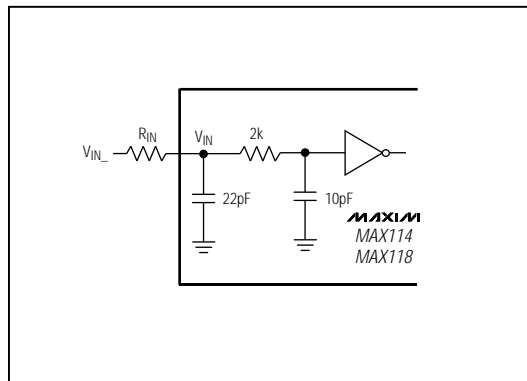


Figure 9. RC Network Equivalent Input Model

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MAX1114/MAX1118

Transfer Function

Figure 10 shows the MAX114/MAX118's nominal transfer function. Code transitions occur halfway between successive-integer LSB values. Output coding is binary with $1\text{LSB} = (V_{\text{REF}+} - V_{\text{REF}-}) / 256$.

Conversion Rate

The maximum sampling rate (f_{MAX}) for the MAX114/MAX118 is achieved in write-read mode ($t_{\text{RD}} < t_{\text{INTL}}$), and is calculated as follows:

$$f_{\text{MAX}} = \frac{1}{t_{\text{WR}} + t_{\text{RD}} + t_{\text{RI}} + t_{\text{ACQ}}}$$

$$f_{\text{MAX}} = \frac{1}{250\text{ns} + 250\text{ns} + 150\text{ns} + 160\text{ns}}$$

$$f_{\text{MAX}} = 1.23\text{MHz}$$

where t_{WR} = the write pulse width, t_{RD} = the delay between write and read pulses, $t_{\text{RI}} = \overline{\text{RD}}$ to $\overline{\text{INT}}$ delay, and t_{ACQ} = minimum acquisition time.

Signal-to-Noise Ratio and Effective Number of Bits

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to all other ADC output signals. The output spectrum is limited to frequencies above DC and below one-half the ADC sample rate.

The theoretical minimum analog-to-digital noise is caused by quantization error, and results directly from the ADC's resolution: $\text{SNR} = (6.02N + 1.76)\text{dB}$, where N is the number of bits of resolution. Therefore, a perfect 8-bit ADC can do no better than 50dB.

The FFT Plot (see *Typical Operating Characteristics*) shows the result of sampling a pure 195.8kHz sinusoid at a 1MHz rate. This FFT plot of the output shows the output level in various spectral bands.

The effective resolution (or "effective number of bits") the ADC provides can be measured by transposing the equation that converts resolution to SNR: $N = (\text{SINAD} - 1.76) / 6.02$ (see *Typical Operating Characteristics*).

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal (in the frequency

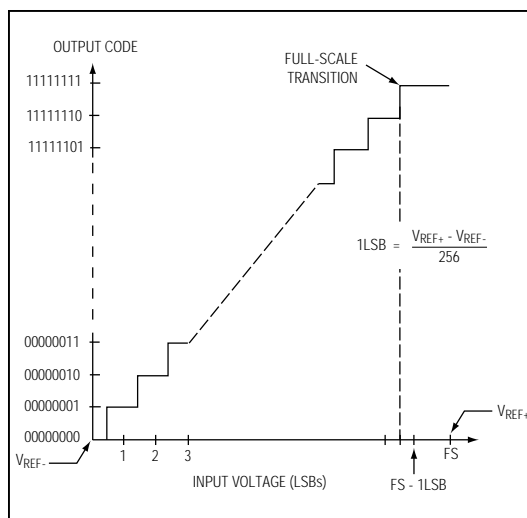


Figure 10. Transfer Function

band above DC and below one-half the sample rate) to the fundamental itself. This is expressed as:

$$\text{THD} = 20\log \left[\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots + V_N^2}}{V_1} \right]$$

where V_1 is the fundamental RMS amplitude, and V_2 through V_N are the amplitudes of the 2nd through Nth harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one-half the sample rate). Usually the next largest spectral component occurs at some harmonic of the input frequency. However, if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor. See the Signal-to-Noise Ratio graph in *Typical Operating Characteristics*.

+5V, 1MSPS, 4 & 8-Channel, 8-Bit ADCs with 1 μ A Power-Down

Ordering Information (continued)

Chip Information

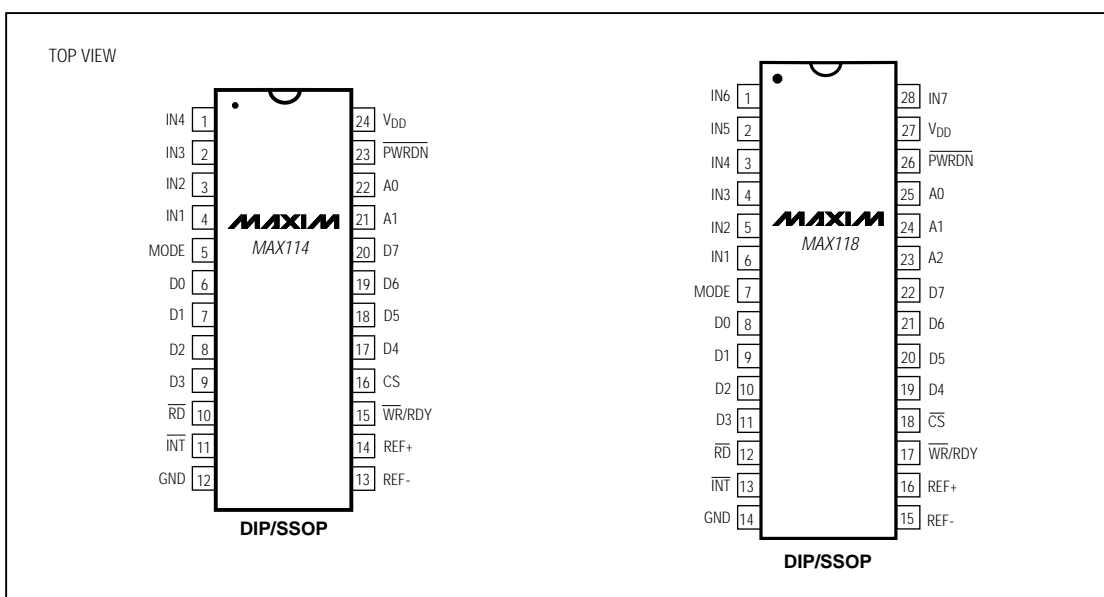
PART	TEMP. RANGE	PIN-PACKAGE
MAX1118CPI	0°C to +70°C	28 Wide Plastic DIP
MAX1118CAI	0°C to +70°C	28 SSOP
MAX1118C/D	0°C to +70°C	Dice*
MAX1118EPI	-40°C to +85°C	28 Wide Plastic DIP
MAX1118EAI	-40°C to +85°C	28 SSOP
MAX1118MJI	-55°C to +125°C	28 Wide CERDIP**

TRANSISTOR COUNT: 2011

*Dice are specified at $T_A = +25^\circ\text{C}$, DC parameters only.

**Contact factory for availability.

Pin Configurations



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