DC1842B and DC1680B
LTC4290B/LTC4271
8-Port PSE with Digital Isolation

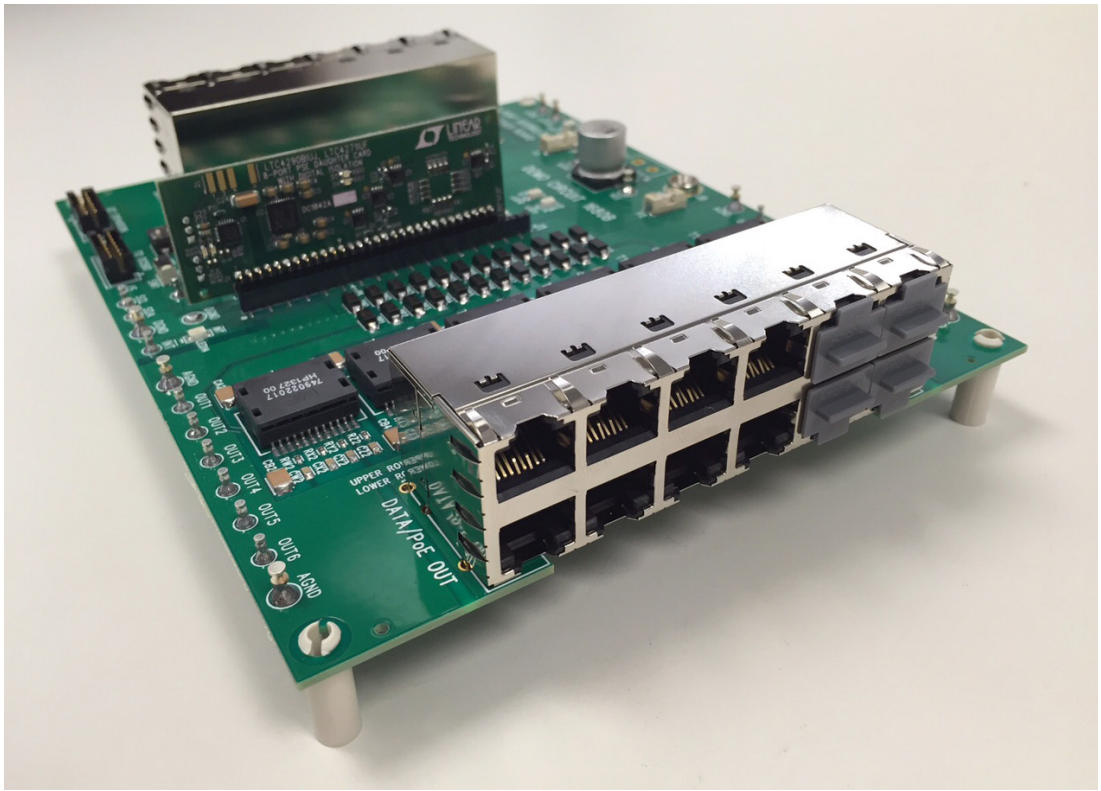
DESCRIPTION

Demonstration kit DC1843B is an 8-port Ethernet Alliance™ certified IEEE 802.3at Type 2 power sourcing equipment (PSE) composed of a DC1842B daughter card and DC1680B motherboard. The kit is used for evaluation of the LTC4290B and LTC4271 PSE chipset. Up to 8 powered devices (PDs) can be connected and powered from this system using a single power supply. A DC590 is connected to the DC1843 for I^2C interfacing with QuikEval™. This demonstration manual provides a Quick Start Procedure, a DC1842B overview, a DC1680B overview, schematics, and layout printouts. Refer to the Layout Guide for Demonstration Circuit 1842B when laying out the LTC4290B/LTC4271 circuit. Contact Analog Devices for this document.

The DC1842B has increased surge protection over the DC1842A. The DC1680B uses discrete Ethernet transformers while the DC1680A has an integrated 12-port RJ45 jack.

Design files for this circuit board are available.

BOARD PHOTO



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QUICK START PROCEDURE

Demonstration kit DC1843B includes the DC1842B daughter card and DC1680B motherboard. The kit is set up for evaluating the LTC4290B/LTC4271. Follow the procedure below and refer to Figures 1 through 4 for proper equipment setup.

NOTE (DC1843B Kit): Connector J1 on the DC1680B has four pegs blocking the unused last four pins to match the 30-pin connector of the DC1842B. Dust caps block the four unused ports at each RJ45 connector on the DC1680B for the 8-Port.

1. On the DC1842B set AUTO jumper JP1 to HI (Figure 1) to enable AUTO pin mode.
2. On the DC1842B set MID jumper JP2 to LO (Figure 1) to disable midspan mode.
3. Align pin 1 of the 30-pin male connector on the DC1842B with pin 1 of the 30-pin female connector on the DC1680B (Figure 2). Pin 12 is polarized to assist with the alignment. Carefully push the DC1842B straight down until the two 30-pin connectors are flush with each other.
4. On the DC1680B, connect a supply with the positive rail to POS and negative rail to NEG (Figure 3). Use a power supply capable of sourcing the maximum load expected (8 ports × 850mA ≥ 6.8A). Ramp the supply up to 51V to 57V.
5. Connect up to 8 PDs to ports 1-8 at the DC1680B, J4 (Figure 3).
6. The DC590 is optionally connected to the DC1680B connector J5 with a 14-pin ribbon cable (Figure 3). A GUI for the LTC4290B/LTC4271 is brought up by QuikEval for I^2C interfacing from a PC (Figure 4).

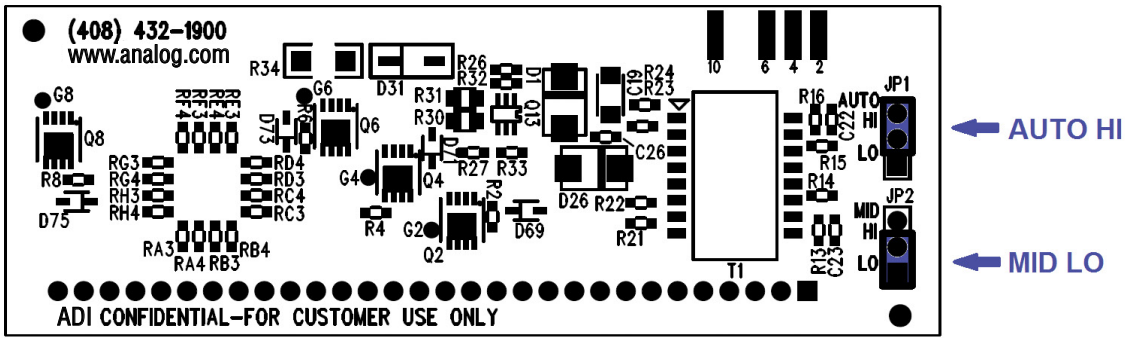


Figure 1. DC1842 Backside. Setting AUTO and MID Jumpers

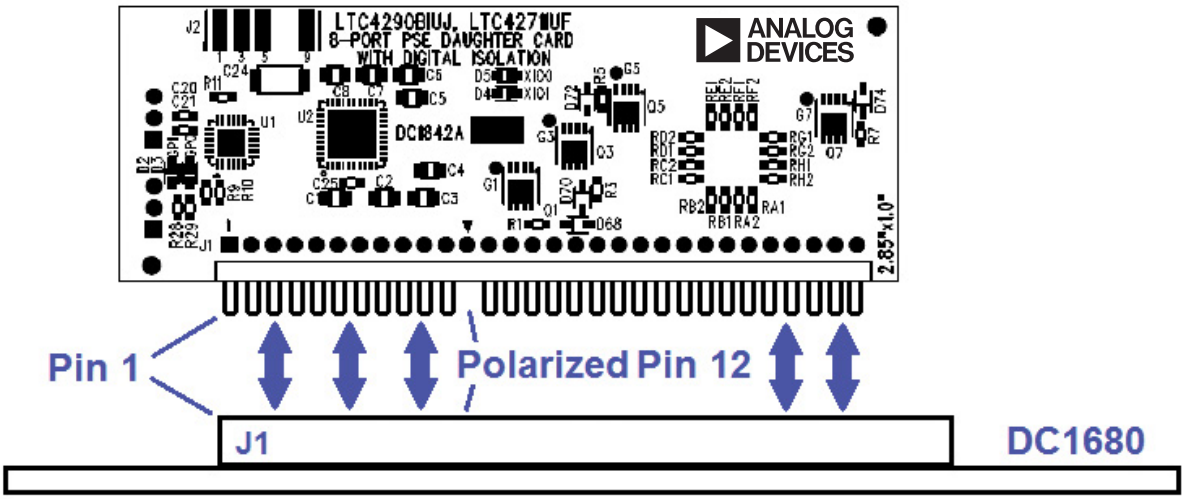


Figure 2. Inserting the DC1842 into J1 of the DC1680

QUICK START PROCEDURE

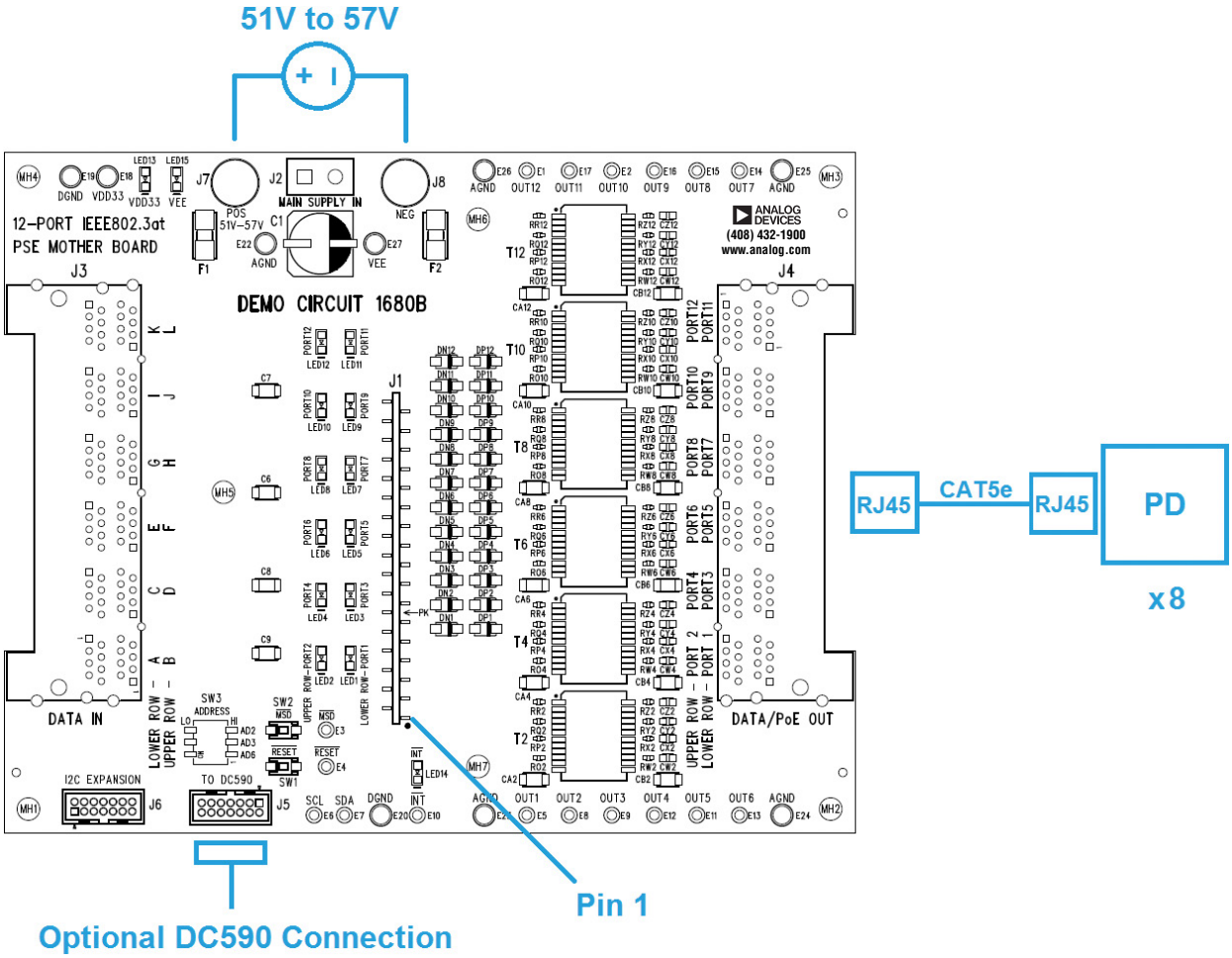


Figure 3. DC1843B Basic Setup

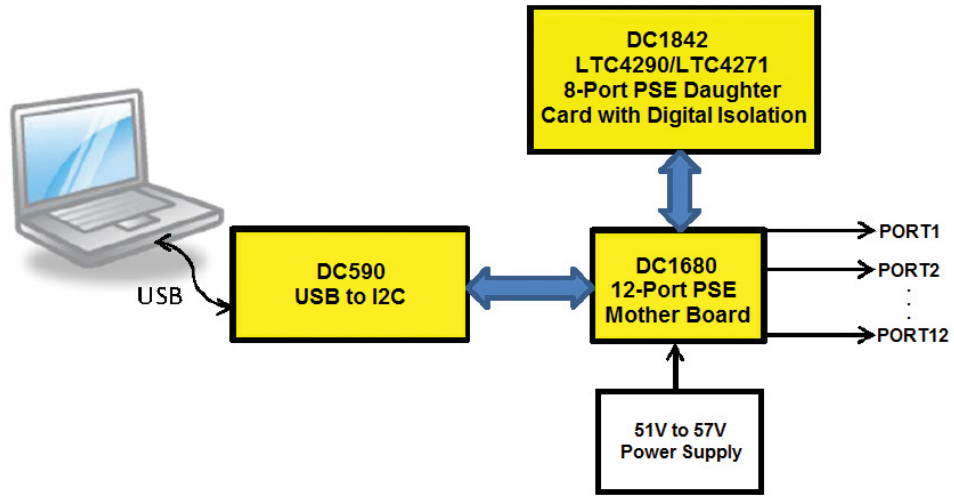


Figure 4. DC1843 System Setup with the DC590, DC1680, DC1842 and 51V to 57V Power Supply

DEMONSTRATION CIRCUIT 1842B OPERATION

8-Port PSE Daughter Card with Digital Isolation

Demonstration circuit 1842B (Figure 5) features the LTC4290B/LTC4271 chipset on a compact daughter card with digital isolation. The LTC4290B/LTC4271 chipset is an 8-port power sourcing equipment (PSE) controller designed for use in IEEE 802.3at Type 1 and Type 2 (high power) compliant Power over Ethernet (PoE) systems. A transformer isolated communication protocol replaces expensive opto-couplers and complex isolated 3.3V supply resulting in significant BOM cost savings. The LTC4290B/LTC4271 chipset delivers lowest-in-industry heat dissipation by utilizing low R_{ON} external MOSFETs and 0.25Ω sense resistors, eliminating the need for expensive heat sinks.

Advanced power management features in the LTC4290B/LTC4271 chipset include: per port 12-bit current monitoring ADCs, DAC programmable current limit, and versatile quick shutdown of preselected ports. PD discovery uses a proprietary dual mode 4-point detection mechanism ensuring excellent immunity from false PD detection. Midspan PSEs are supported with 2-event classification and a two second backoff timer. The LTC4290B/LTC4271 includes an I^2C serial interface operable up to 1MHz.

The DC1842B demonstrates proper LTC4290B/LTC4271 board layout that is approximately the height and width of a 2 × 4 RJ45 connector. The compact layout is made possible by the small package size of key components. The LTC4290B is in a 6mm × 6mm QFN, while the LTC4271 is in a 4mm × 4mm QFN. Each port has a PSMN075-100MSE MOSFET in a 3mm × 3mm LFPAK33 package.

The daughter card inserts in the DC1680B motherboard through J1, a polarized 30-pin connector. Isolated 3.3V and logic control signals are brought in on this connector. Also connected at J1 is the PoE V_{EE} supply from the motherboard and 8 PSE controlled outputs.

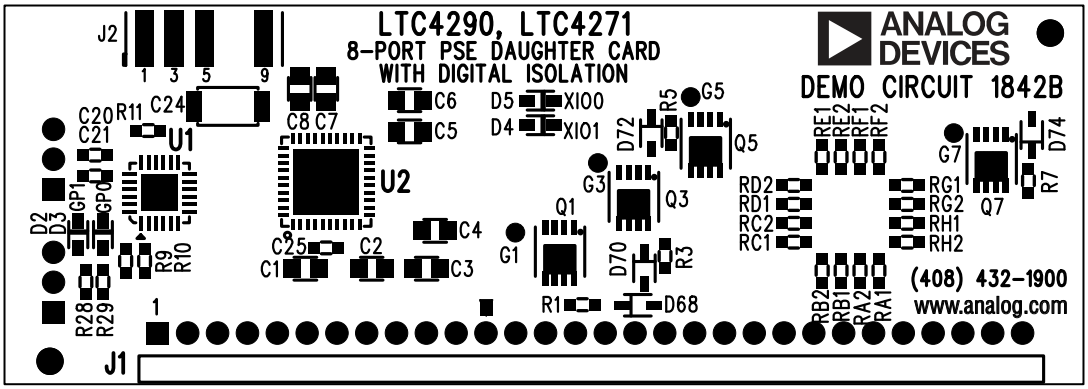


Figure 5. DC1842B 8-Port PSE Daughter Card with Digital Isolation Features the LTC4290B and LTC4271

DEMONSTRATION CIRCUIT 1842B OPERATION

Board Layout

Proper board layout is crucial for proper LTC4290B/LTC4271 chipset operation, robustness, and accuracy. When laying out, pay attention to parts placement, Kelvin sensing, power paths, and copper fill. It is imperative to follow the LTC4290B/LTC4271 Layout Guide document when laying out the board. Contact Analog Devices for this document.

Isolation and Power Supplies

The LTC4290B/LTC4271 chipset provides communication across an isolation barrier through a data transformer (Figure 6). This eliminates the need for expensive optocouplers. All digital pins reside on the digital ground reference and are isolated from the analog PoE supply. A 3.3V supply for V_{DD} and an isolated V_{EE} supply are connected to the DC1842B through the 30-pin connector.

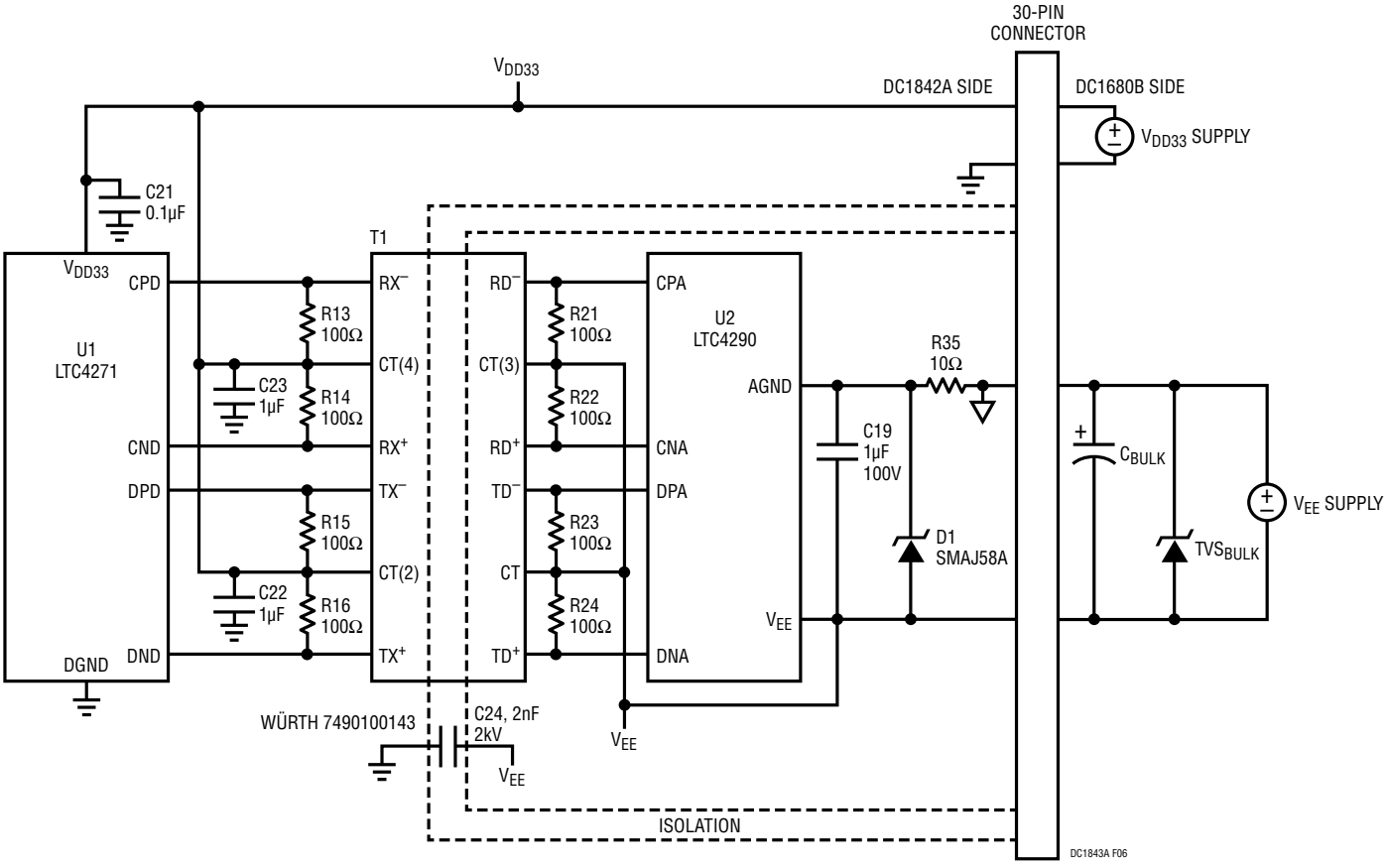


Figure 6. DC1842B Digital and Analog Isolation

DEMONSTRATION CIRCUIT 1842B OPERATION

I²C Communication and Addressing

The LTC4271 internal registers are accessed via I²C to read and/or write configuration, status, and interrupt registers. The I²C lines SDAOUT, SDAIN and SCL connect to the 30-pin connector (Figure 7). Subsequently, the I²C bus is accessed on the DC1680B.

The LTC4290B/LTC4271 chipset has an address of ($A_6$10$A_3A_2A_1A_0$b), where A_6, A_3, A_2, A_1, and A_0 are the logic state of the AD6, AD3, AD2, AD1, and AD0 pins respectively. On the DC1842B, AD0 and AD1 are tied low with pull-down resistors. AD2, AD3 and AD6 are brought out to the 30-pin connector (Figure 7) and set with three switches on the DC1680B.

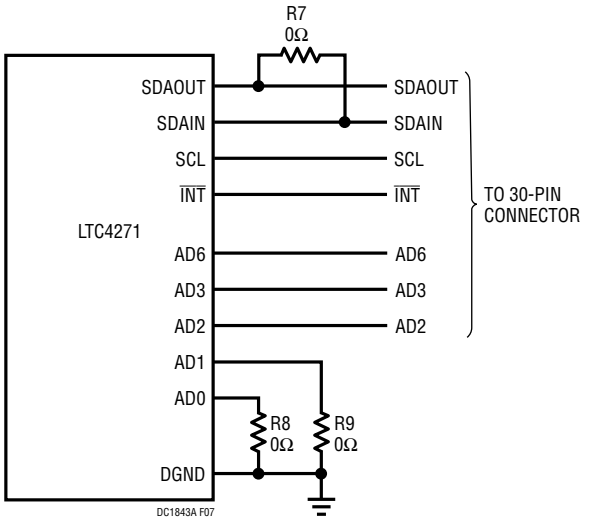


Figure 7. DC1842B, LTC4271 I²C and Address Connections

I/O LED Indicators

The DC1842B features four LEDs to indicate the states of the LTC4290B/LTC4271 chipset general purpose input output pins. These pins are configured as inputs or outputs via I²C. GP1 and GP0 are referenced to DGND and driven by the LTC4271 when set as outputs (Figure 8). XIO0 and XIO1 are referenced to V_{EE} and are driven by the LTC4290B when set as outputs (Figure 9). J2 provides test points for access to these I/Os.

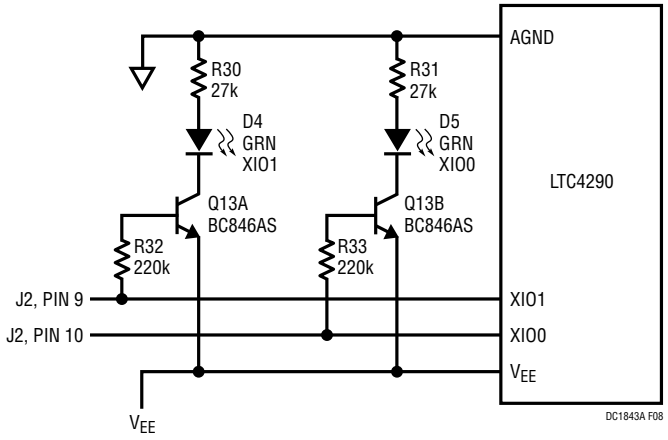


Figure 8. DC1842B, LTC4290B General Purpose I/O LED Indicators

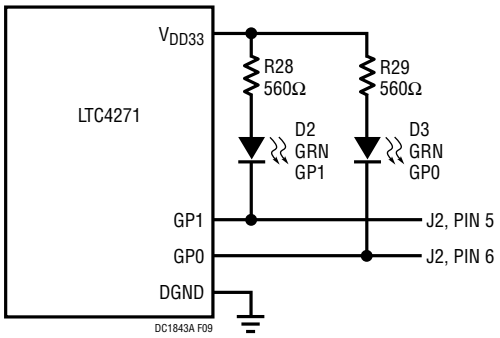


Figure 9. DC1842B, LTC4271 General Purpose I/O LED Indicators

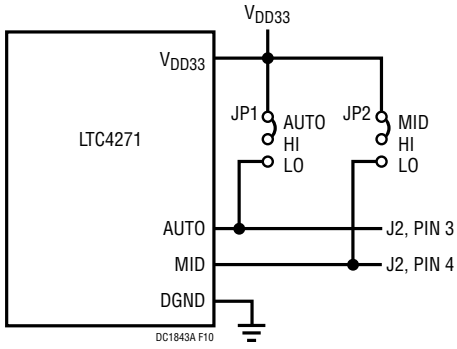


Figure 10. DC1842B AUTO and MID Jumpers

DEMONSTRATION CIRCUIT 1842B OPERATION

AUTO and MID Jumpers

The AUTO and MID pins of the LTC4271 are set by jumpers JP1 and JP2 respectively on the DC1842B (Figure 10). Setting JP1 to HI enables the AUTO pin mode in the LTC4290B/LTC4271 chipset. J2 provides test points for access to AUTO and MID.

In AUTO pin mode (JP1 high), the LTC4290B/LTC4271 chipset internal I^2C registers default to the AUTO pin high state after a software or hardware reset, or system power on. The LTC4290B/LTC4271 chipset autonomously detects, powers on and disconnects power to PDs without the need for I^2C host control.

Setting JP1 to LO disables AUTO pin mode and sets the LTC4290B/LTC4271 chipset to a low current shutdown mode. An I^2C host controller can then be used to configure the LTC4290B/LTC4271 chipset to semi-auto mode for controlled PSE operation or to manual mode for test purposes.

Setting JP2 to HI enables the midspan mode detection backoff timer in the LTC4290B/LTC4271 chipset. For endpoint PSEs, set JP2 to LO to disable midspan mode.

For quick PSE evaluation in AUTO pin mode with MIDSPAN disabled, set JP1 HI and JP2 LO on the DC1842B.

Surge Protection

Ethernet ports can be subject to significant cable surge events. To keep PoE voltages below a safe level and protect the application against damage, protection components, as shown in Figure 11, are required at the main supply, at the LTC4270 supply pins and at each port.

Bulk transient voltage suppression (TVS_{BULK}) and bulk capacitance (C_{BULK}) are required across the main PoE supply and should be sized to accommodate system level surge requirements.

Each LTC4290 requires a 10Ω, 0805 resistor (R1) in series from supply AGND to the LTC4290 AGND pin. Across the LTC4290 AGND pin and V_{EE} pin are an SMAJ58A, 58V TVS (D1) and a 1µF, 100V bypass capacitor (C19). These components must be placed close to the LTC4290 pins.

Finally, each port requires a pair of S1B clamp diodes: one from OUTn to supply AGND and one from OUTn to supply V_{EE}. The diodes at the ports steer harmful surges into the supply rails where they are absorbed by the surge suppressors and the V_{EE} bypass capacitance. The layout of these paths must be low impedance. These S1B diodes are placed on the DC1680 mother board of the DC1843 kit.

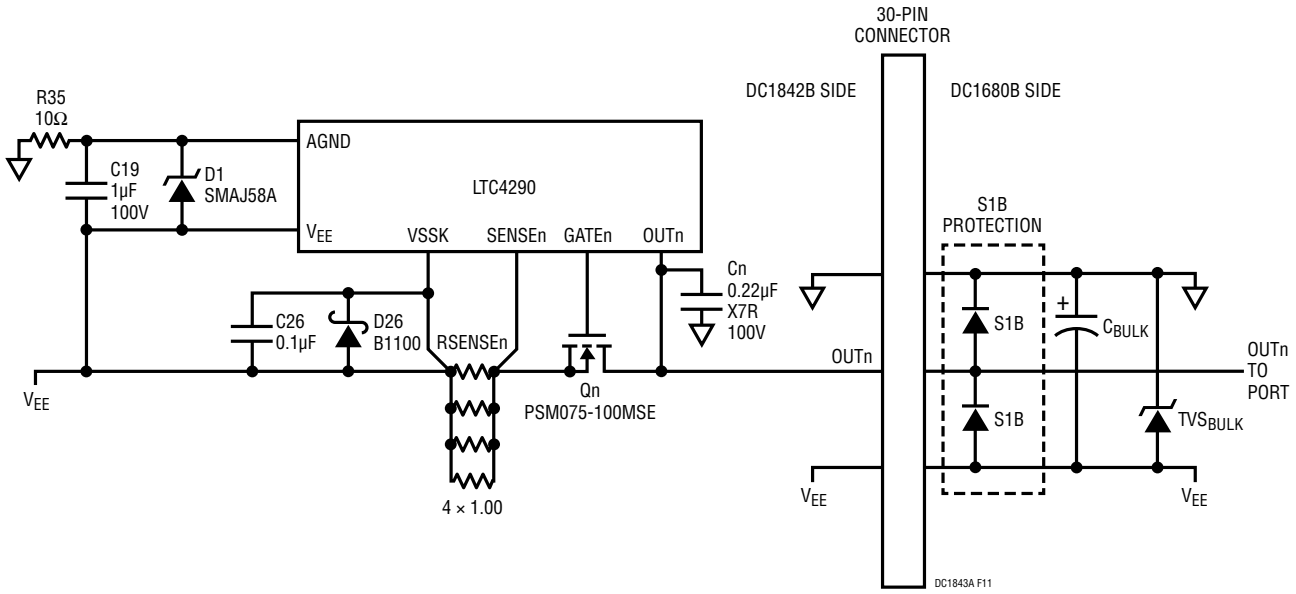


Figure 11. DC1842B, 1 of 8 Port Outputs. Surge Protection

DEMONSTRATION CIRCUIT 1680B OPERATION

Demonstration circuit 1680B is configured as an 8-Port, IEEE802.3at Type 1 and Type 2 PoE PSE motherboard in the DC1843B kit. This board accepts various PSE daughter cards featuring Analog Devices PSE controllers. The DC1680B is capable of powering up to 8 PDs.

Daughter Card Insertion Precautions

When inserting or removing the daughter card into the DC1680B, verify all supplies and LEDs are off. Push the card straight down for insertion or pull straight up for removal to avoid bending the connector pins. Follow the instructions in the Quick Start Procedure for alignment.

V_{EE} Supply

Connect a power supply for V_{EE} with the positive rail to POS and negative rail to NEG as shown in Figure 3 of the Quick Start Procedure. Set the voltage within the range in Table 1 depending on whether the application is a Type 1 or Type 2. Choose a power supply rating and set the current limit high enough to provide power for the maximum number of PDs connected and to meet each PD power requirements.

Table 1. DC1843B V_{EE} Power Range for Type 1 and Type 2 PSEs

PSE TYPE	V_{EE} SUPPLY RANGE	MAX DELIVERED PORT POWER	POWER SUPPLY*
Type 1	45V to 57V	13W	200W
Type 2	51V to 57V	25.5W	400W

*Recommended DC1843B power supply minimum to avoid drooping in a worst-case scenario with I_{LIM} current at all 8 ports.

PD Connection

PDs are connected using an Ethernet cable to any of the 8 ports at the 2×6, RJ45 connector J4 on the DC1680B (Figure 3). Test points for port outputs OUT1 through OUT8 are provided.

8-Port Configuration

The DC1680B is configured for an 8-port PSE motherboard for the DC1843B kit. Four RJ45 dust caps at J3 and four dust caps at J4 are inserted to block off the four unused Ethernet ports. Additional pegs are placed in the last 4 pins of connector J1 to block off the unused pins when the DC1842B daughter card is inserted.

DC1680B USER FEATURES

Refer to Figure 12 and Figure 13 for the following user features.

Onboard 3.3V Supply

The DC1680B has an onboard V_{DD33} digital supply generated from the V_{EE} supply. DGND is a negative voltage referenced to AGND. If an external 3.3V supply is to be used, contact Analog Devices Applications for proper connection.

V_{EE} and V_{DD33} LED Indicators

LEDs for V_{EE} and V_{DD33} indicate if voltage is present at these supplies. Verify these LEDs are off before inserting or removing the daughter card.

Digital Connections

The DC1680B has connections for I^2C control from a host controller. The DC590 is optionally connected to the DC1680B at J5 through a 14-pin ribbon cable. The QuikEval software will automatically detect the DC1680B and open the LTC4271 GUI. A second 14-pin ribbon cable can be connected to J6 for I^2C expansion to another DC1680B board with slight board modifications. Contact Analog Devices Applications for instructions.

Digital test points include SCL, SDA, DGND, $\overline{INT}$, $\overline{MSD}$, and $\overline{RESET}$. I^2C address pin AD6, AD3, and AD2 are set with a 3-bit switch SW3.

Midspan PSE

The DC1843B can be configured as a midspan PSE. Upstream switch data comes in to J3. Data and PoE go out to a PD at J4. Set both MID and AUTO pins logic high.

DEMONSTRATION CIRCUIT 1680B OPERATION

$\overline{\text{MSD}}$ and $\overline{\text{RESET}}$ Pushbuttons

Pushbutton switch SW1, when pressed, pulls the $\overline{\text{RESET}}$ pin of the daughter card logic low. The PSE controller is then held inactive with all ports off and all internal registers reset to their power-up states. When SW1 is released, $\overline{\text{RESET}}$ is pulled high, and the PSE begins normal operation.

Pushbutton switch SW2 when pressed pulls the maskable shutdown input ($\overline{\text{MSD}}$) pin of the daughter card logic low. When pressed, all ports that have their corresponding mask bit set in the mconfig register of the PSE controller will be shutdown. These ports must then be manually re-enabled via I^2C or by resetting the PSE.

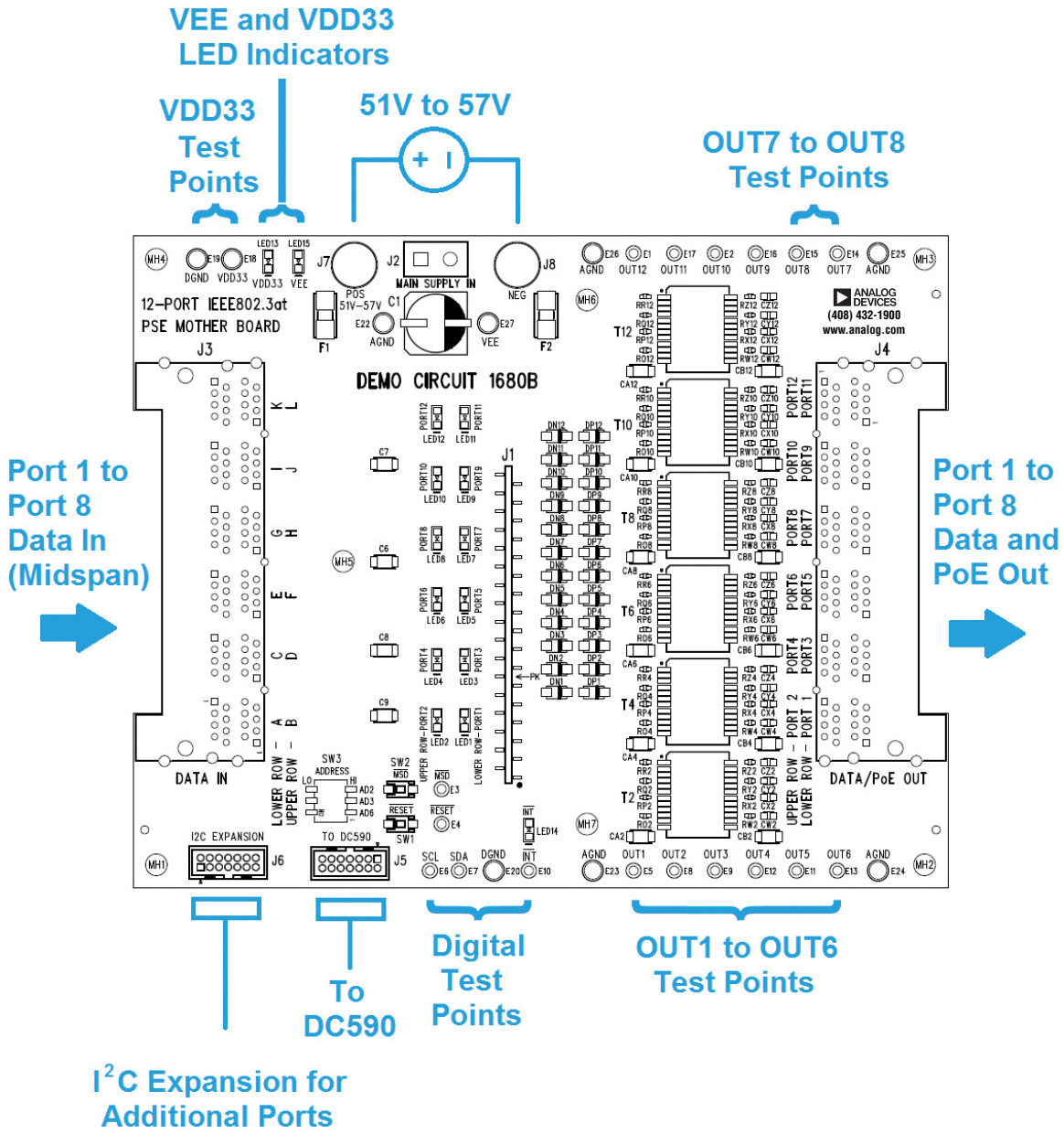


Figure 12. DC1680B Connections and Supply LEDs

DEMONSTRATION CIRCUIT 1680B OPERATION

Interrupt LED

A red LED indicates when the $\overline{INT}$ line is pulled logic low by the daughter card. When the interrupt is cleared (high) via I^2C servicing, the LED is turned off.

Port 1 Through 8 Power LED Indicators

Each PSE port has a green LED indicator to show when PoE power is present at the port. The LEDs are driven by the respective port OUT voltage.

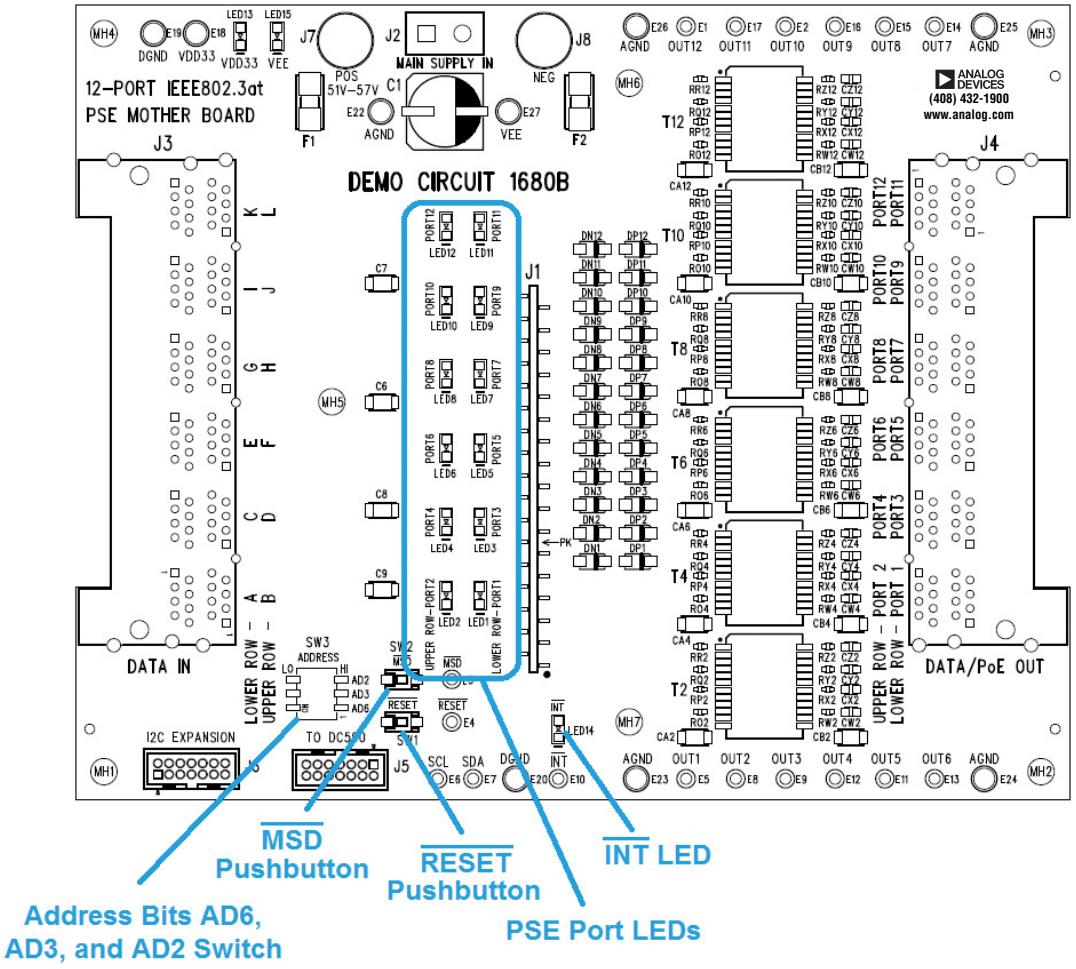


Figure 13. DC1680B Address Switch, Pushbutton Switches, INT LED, and Port Power LEDs

DEMONSTRATION CIRCUIT 1843B SYSTEM

DC1843B System Setup

Figure 14 shows a basic DC1843B system setup. The DC1842B daughter card is inserted in the 30-pin connector J1 on the DC1680B motherboard. A power supply is connected to V_{EE} with banana cables. The DC590 connects with a 14-pin ribbon cable to the DC1680B and to a PC via USB. On the PC, a GUI communicates with the board. At the PSE output, PDs are connected. A sample PD demo board is shown in Figure 14.

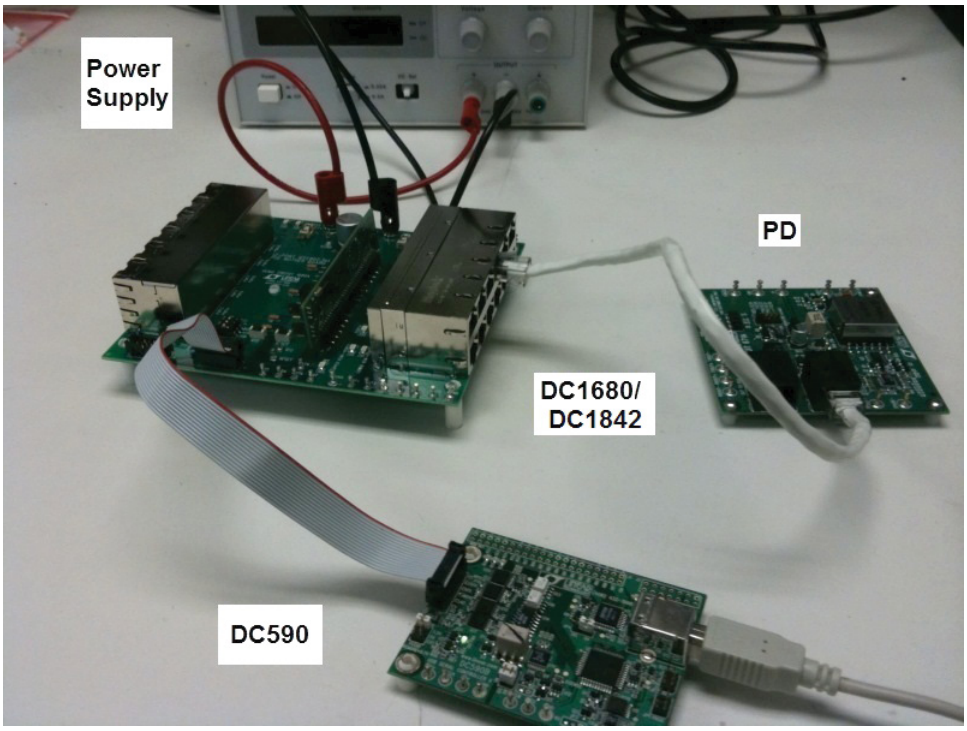


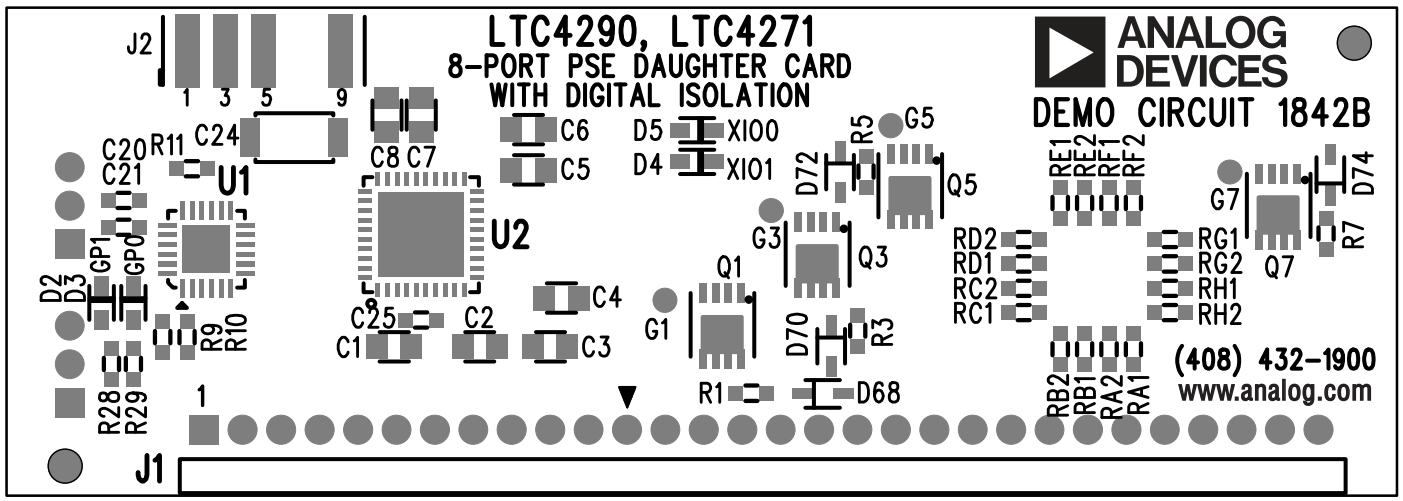
Figure 14. DC1680B and DC1842B System Setup with Power Supply, DC590 and PD Demo Board

Table 2. DC1843 Kit Versions

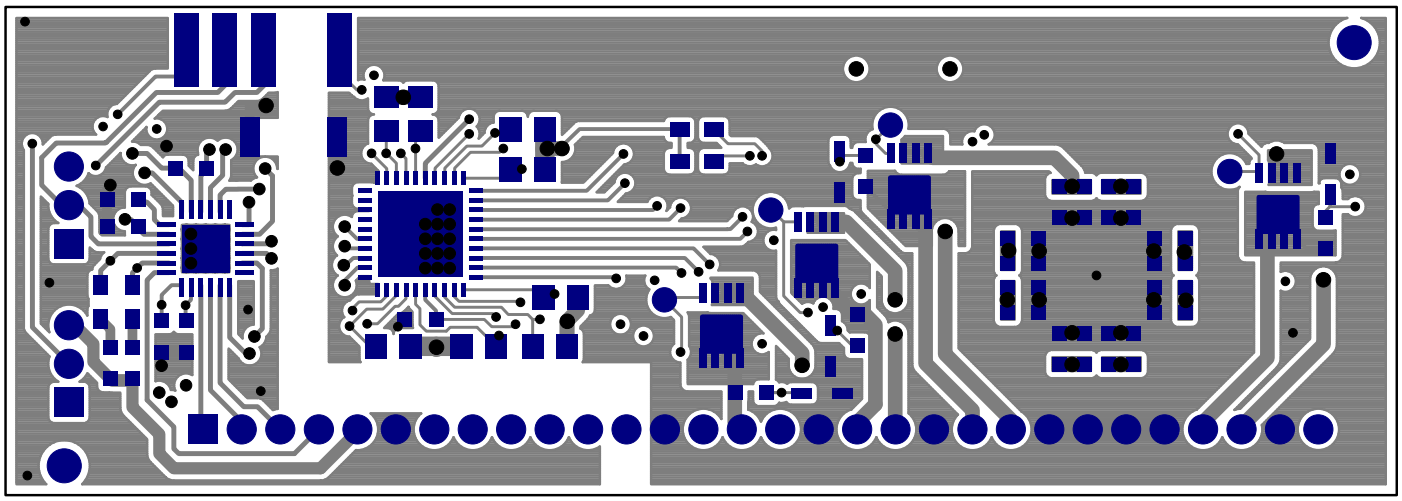
VERSION	FEATURES
DC1843A	DC1680A: Motherboard with Integrated Magjack DC1842A: 8-Port PSE Daughter Card
DC1843B	DC1680B: Motherboard with Discrete Ethernet Transformers DC1842B: 8-Port PSE Daughter Card with Increased Surge Protection

DEMONSTRATION CIRCUIT 1842B LAYOUT

Top Assembly

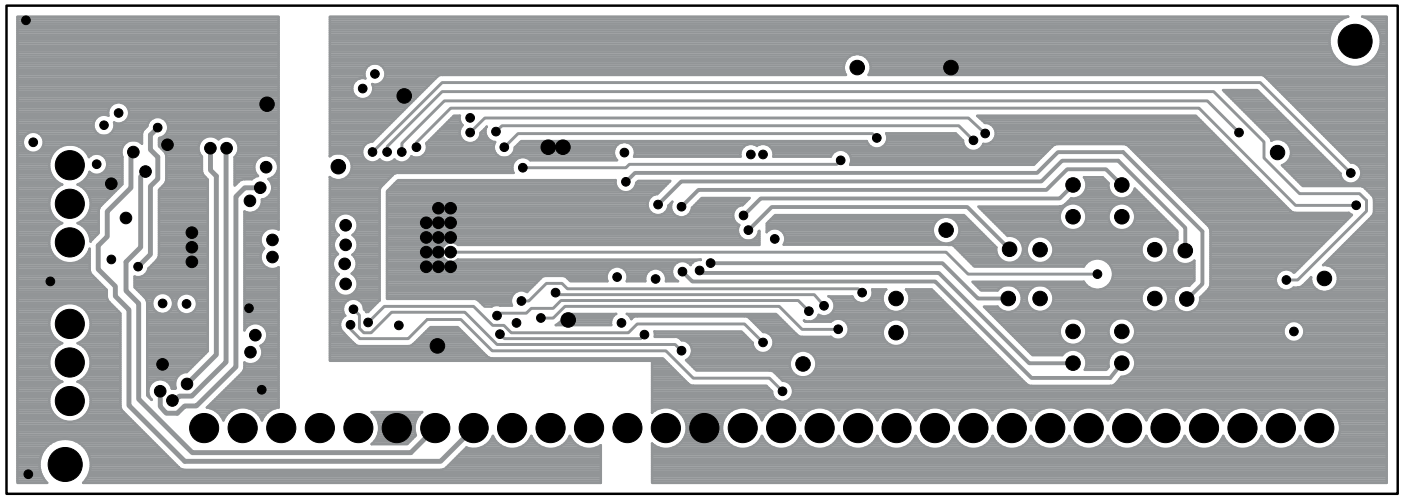


Layer 1: Top Layer

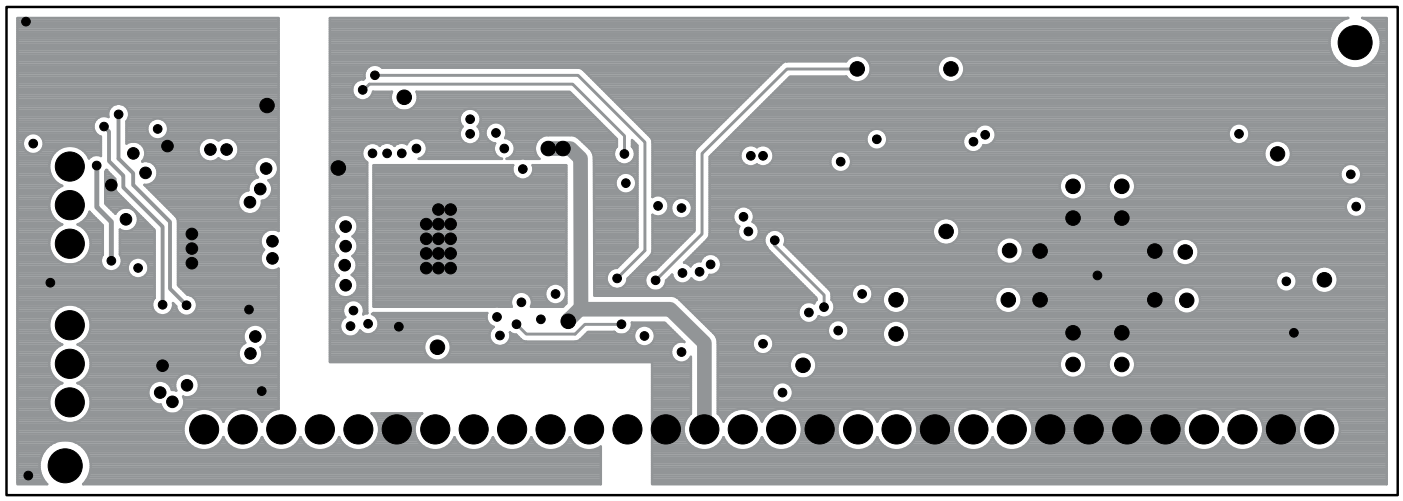


DEMONSTRATION CIRCUIT 1842B LAYOUT

Layer 2: V_{EE} Plane 1

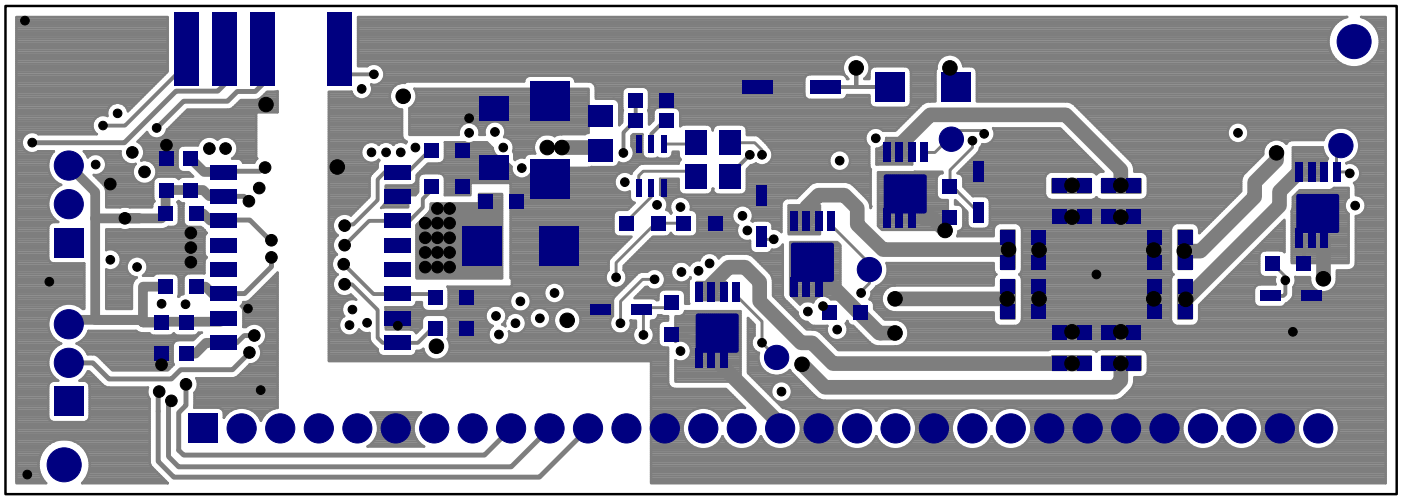


Layer 3: V_{EE} Plane 2

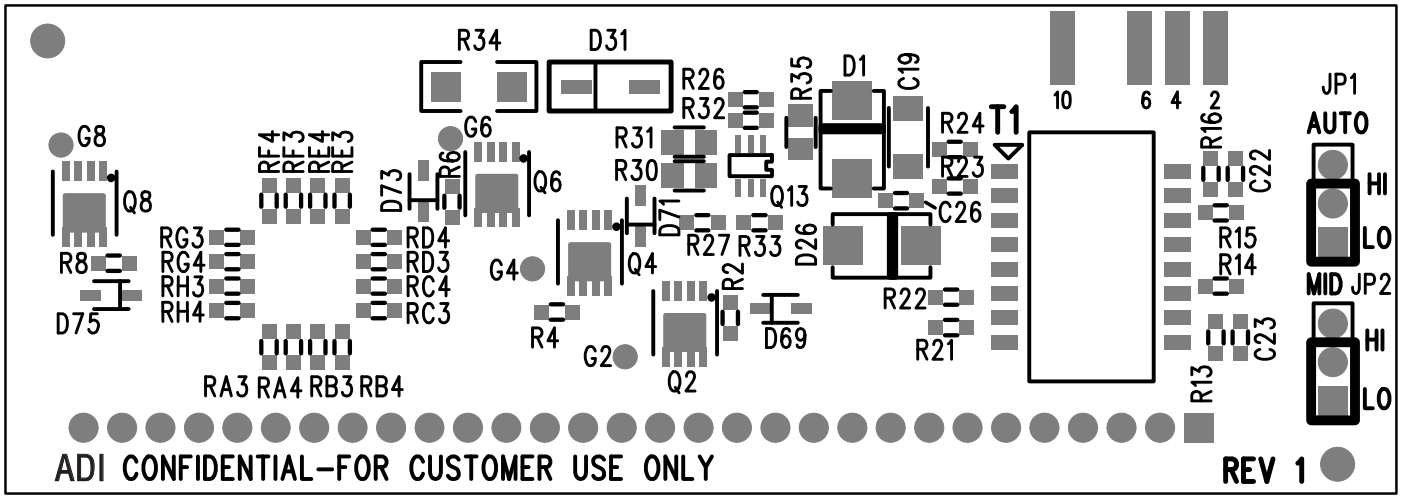


DEMONSTRATION CIRCUIT 1842B LAYOUT

Layer 4: Bottom Layer

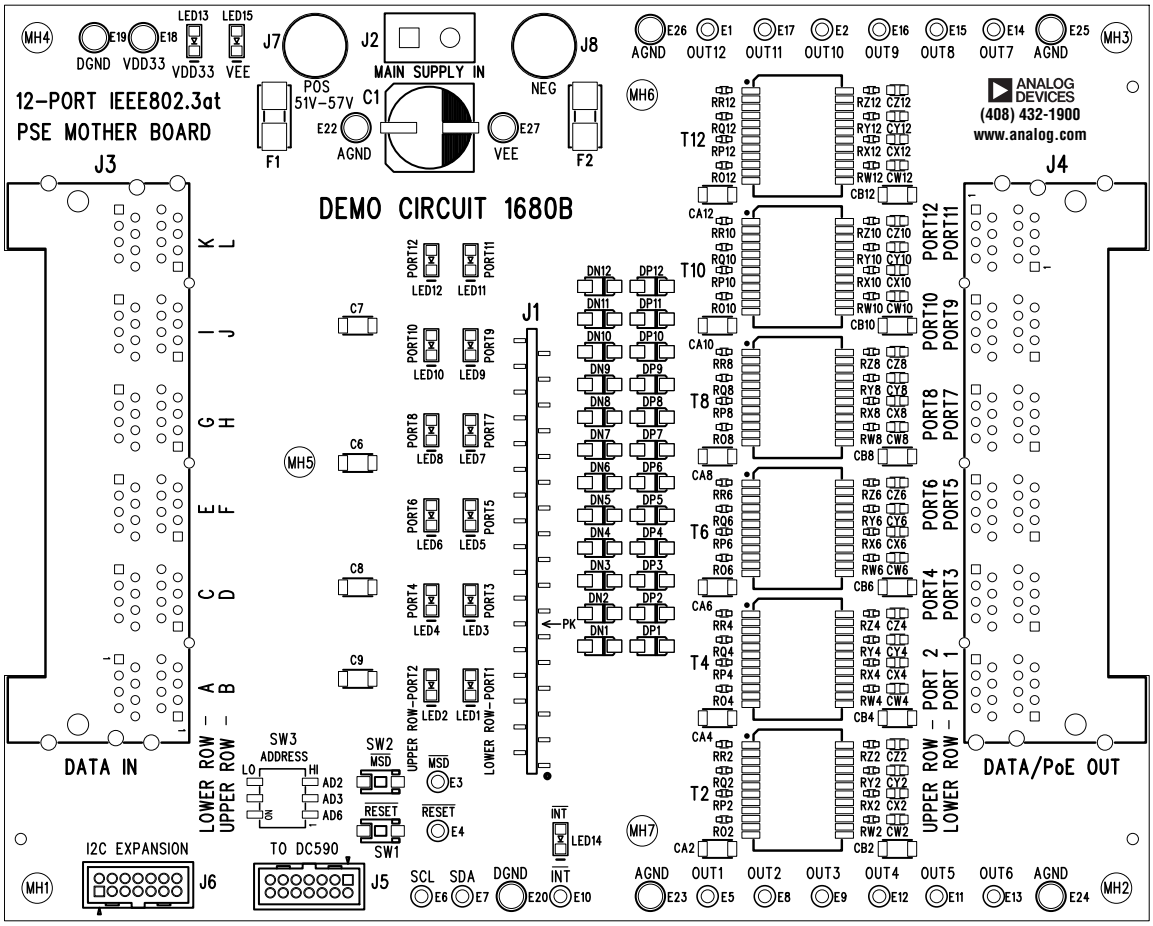


Bottom Assembly



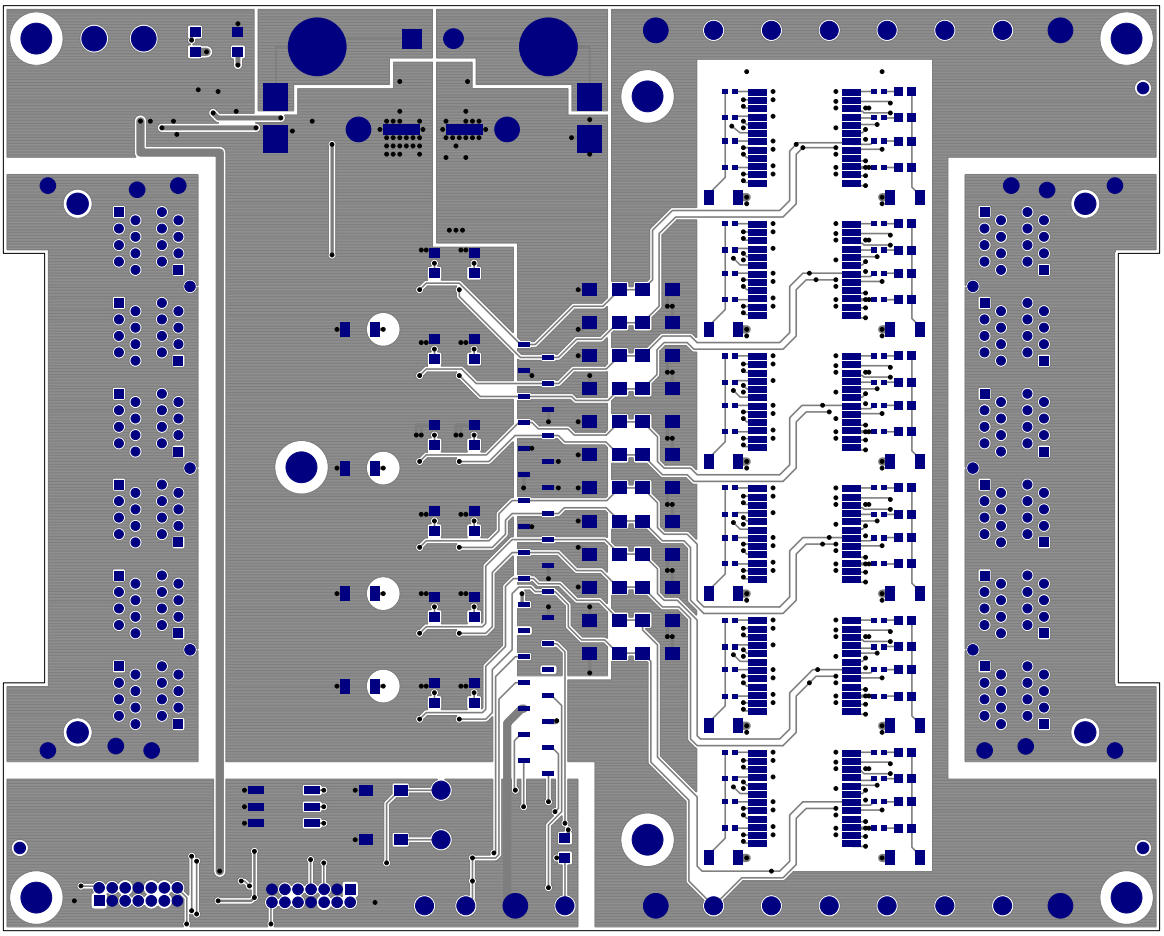
DEMONSTRATION CIRCUIT 1680B LAYOUT

Top Assembly



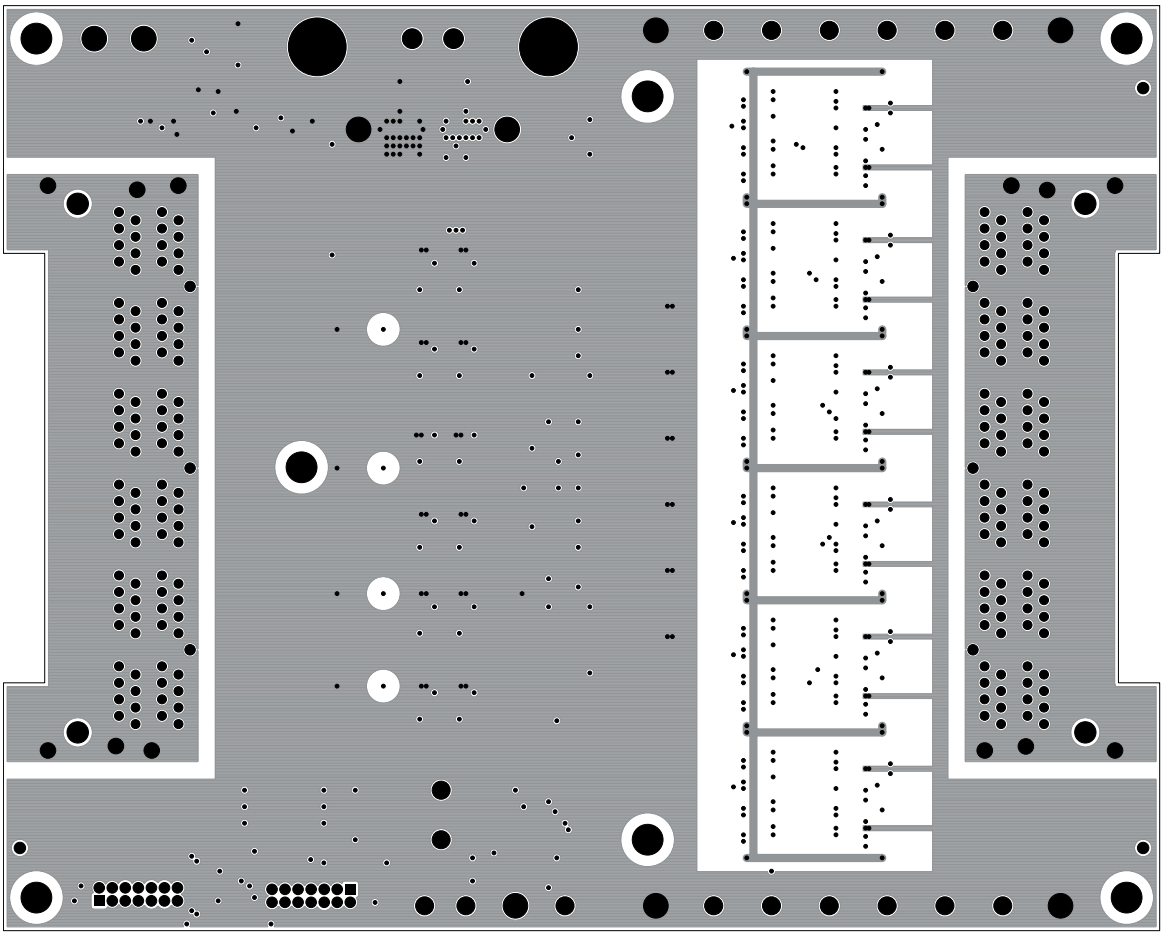
DEMONSTRATION CIRCUIT 1680B LAYOUT

Layer 1: Top Layer



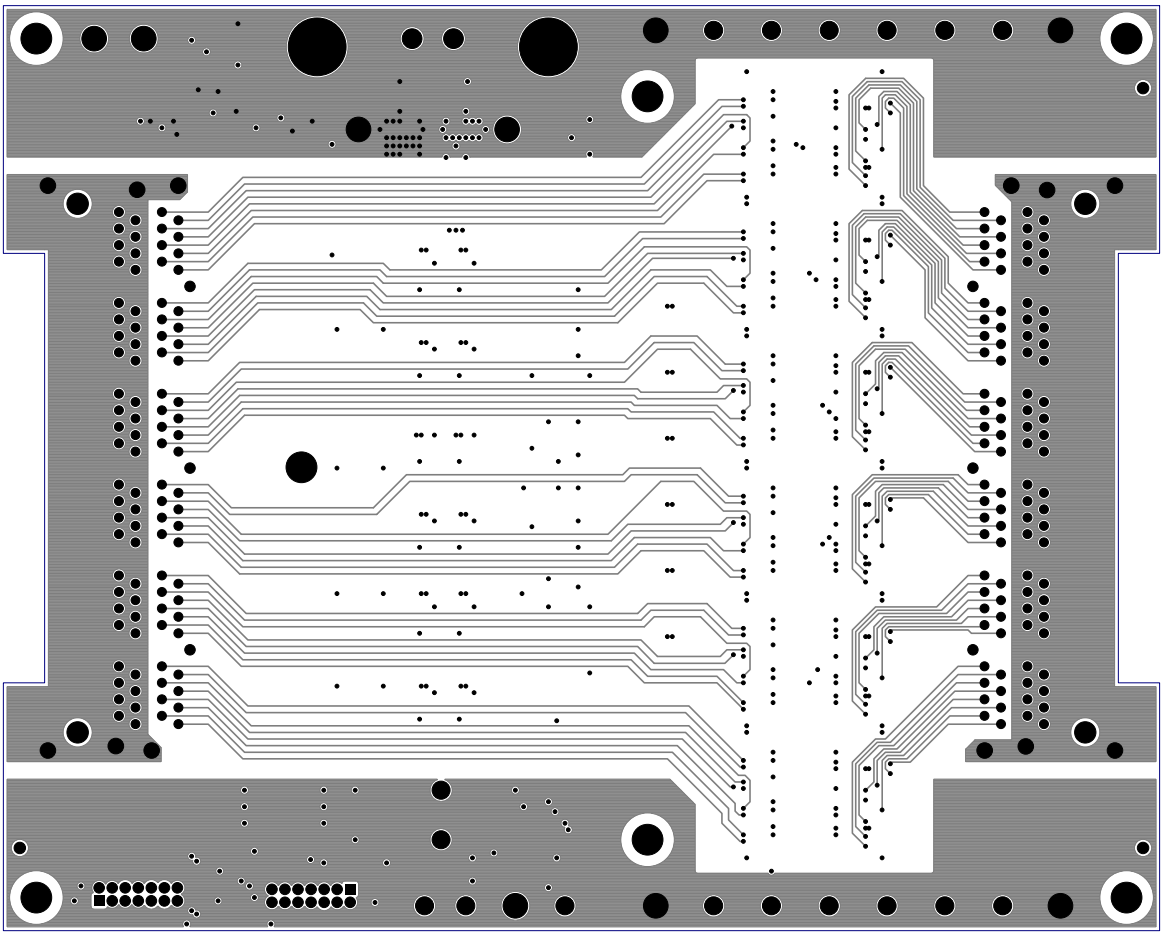
DEMONSTRATION CIRCUIT 1680B LAYOUT

Layer 2: AGND, CGND Plane 1



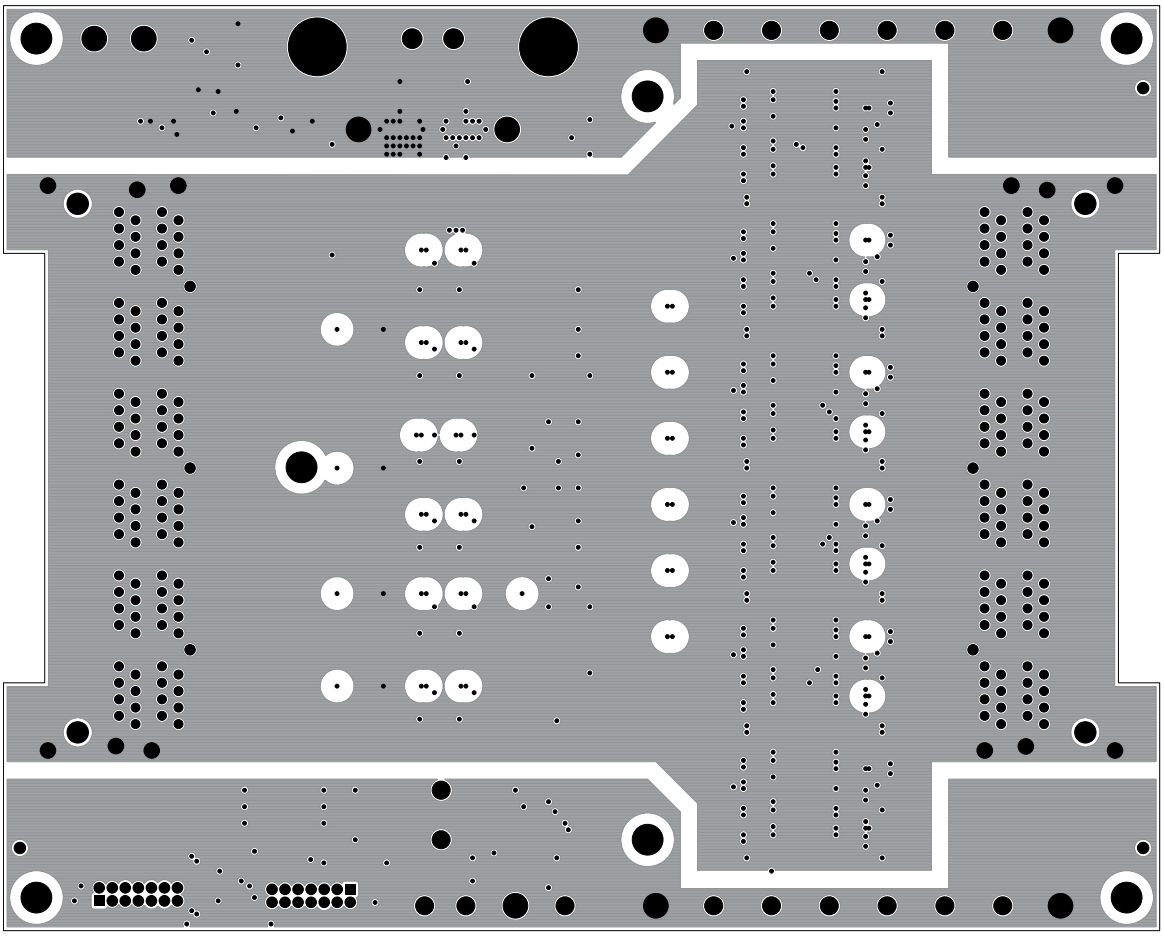
DEMONSTRATION CIRCUIT 1680B LAYOUT

Layer 3: SIG, AGND, CGND Plane 2



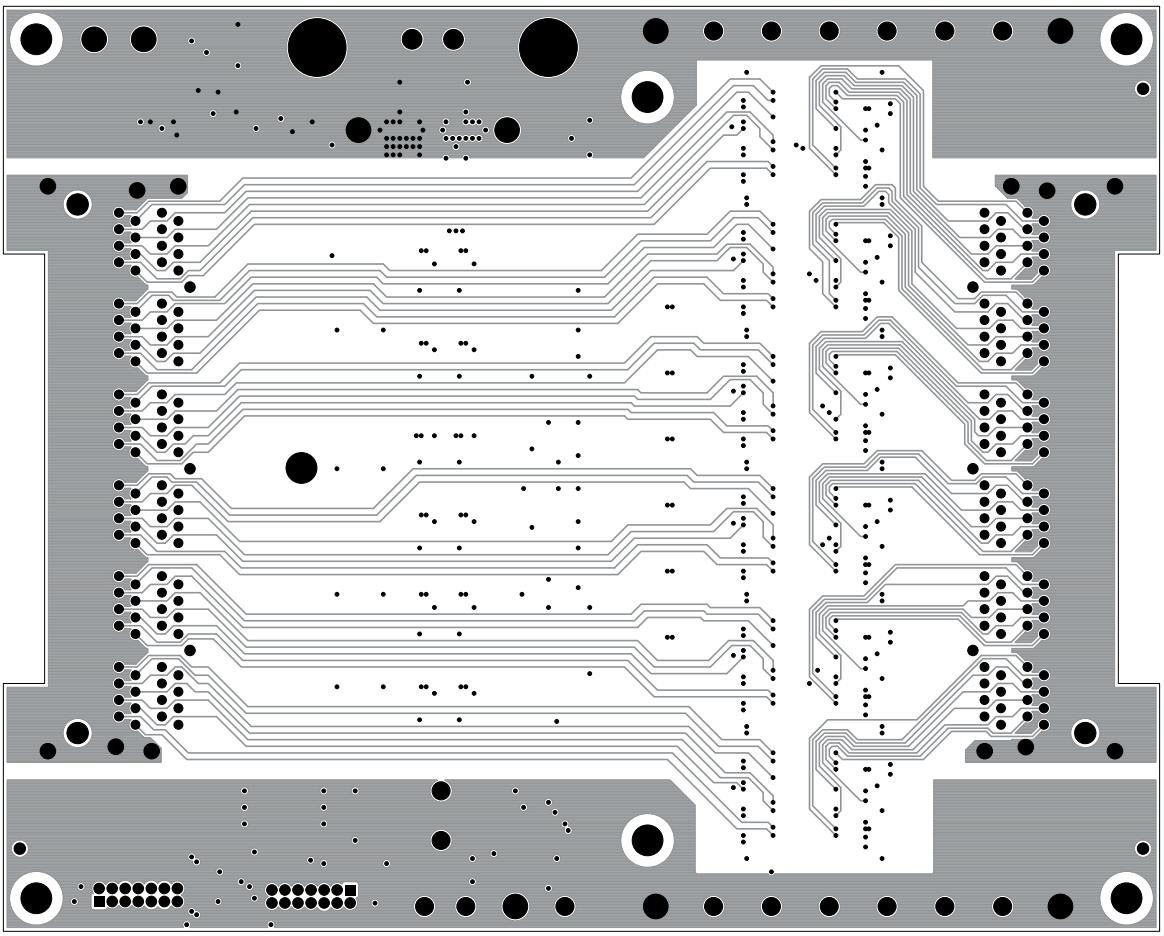
DEMONSTRATION CIRCUIT 1680B LAYOUT

Layer 4: SIG, AGND, CGND Plane 3



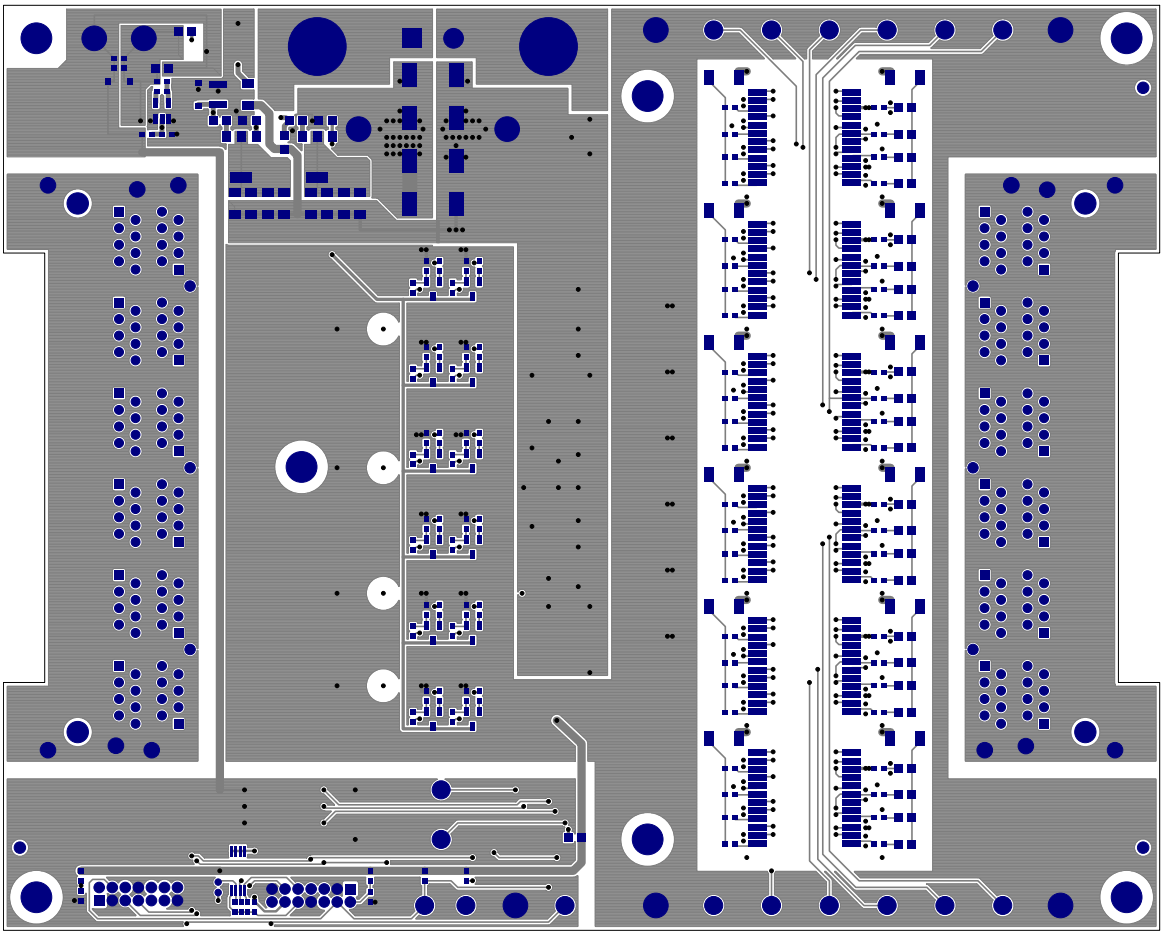
DEMONSTRATION CIRCUIT 1680B LAYOUT

Layer 5: SIG, AGND, CGND Plane 4



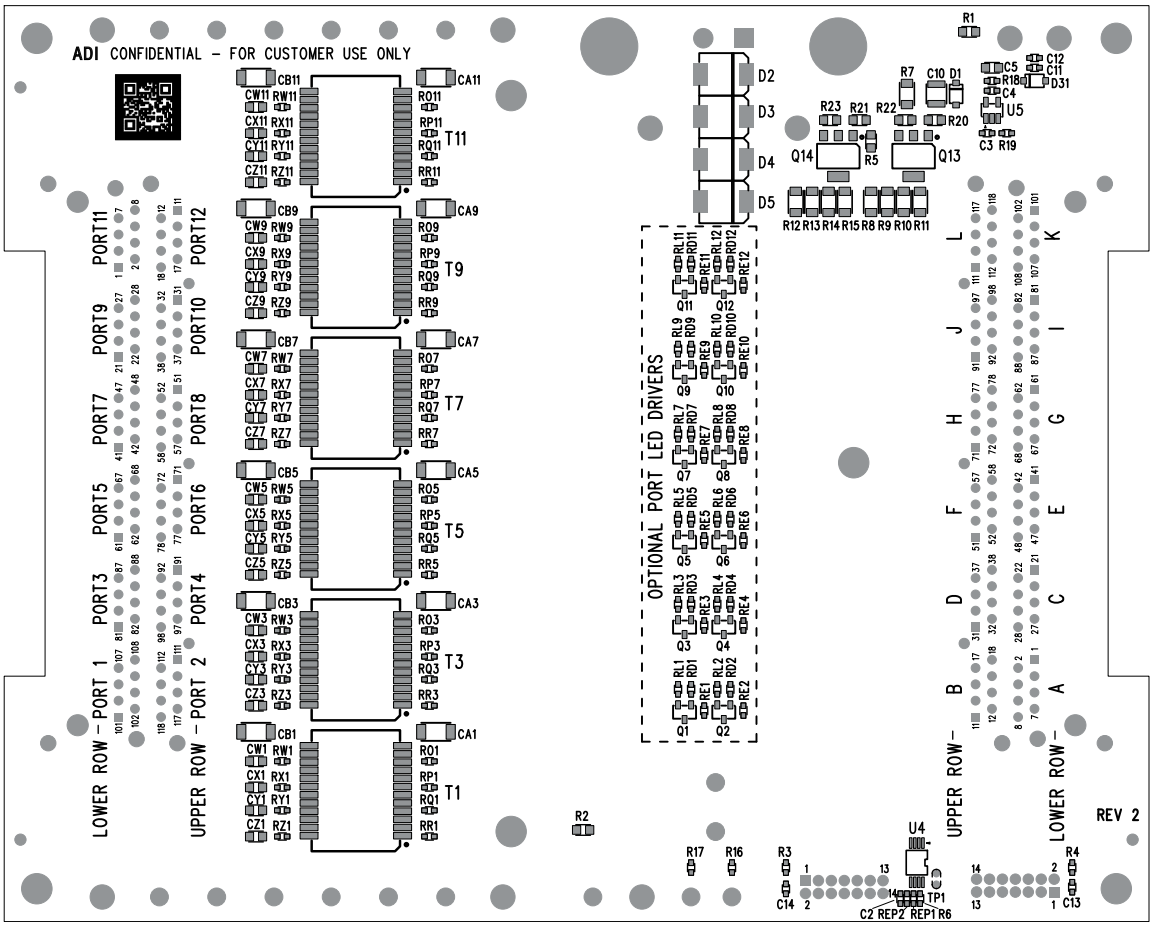
DEMONSTRATION CIRCUIT 1680B LAYOUT

Layer 6: Bottom Layer

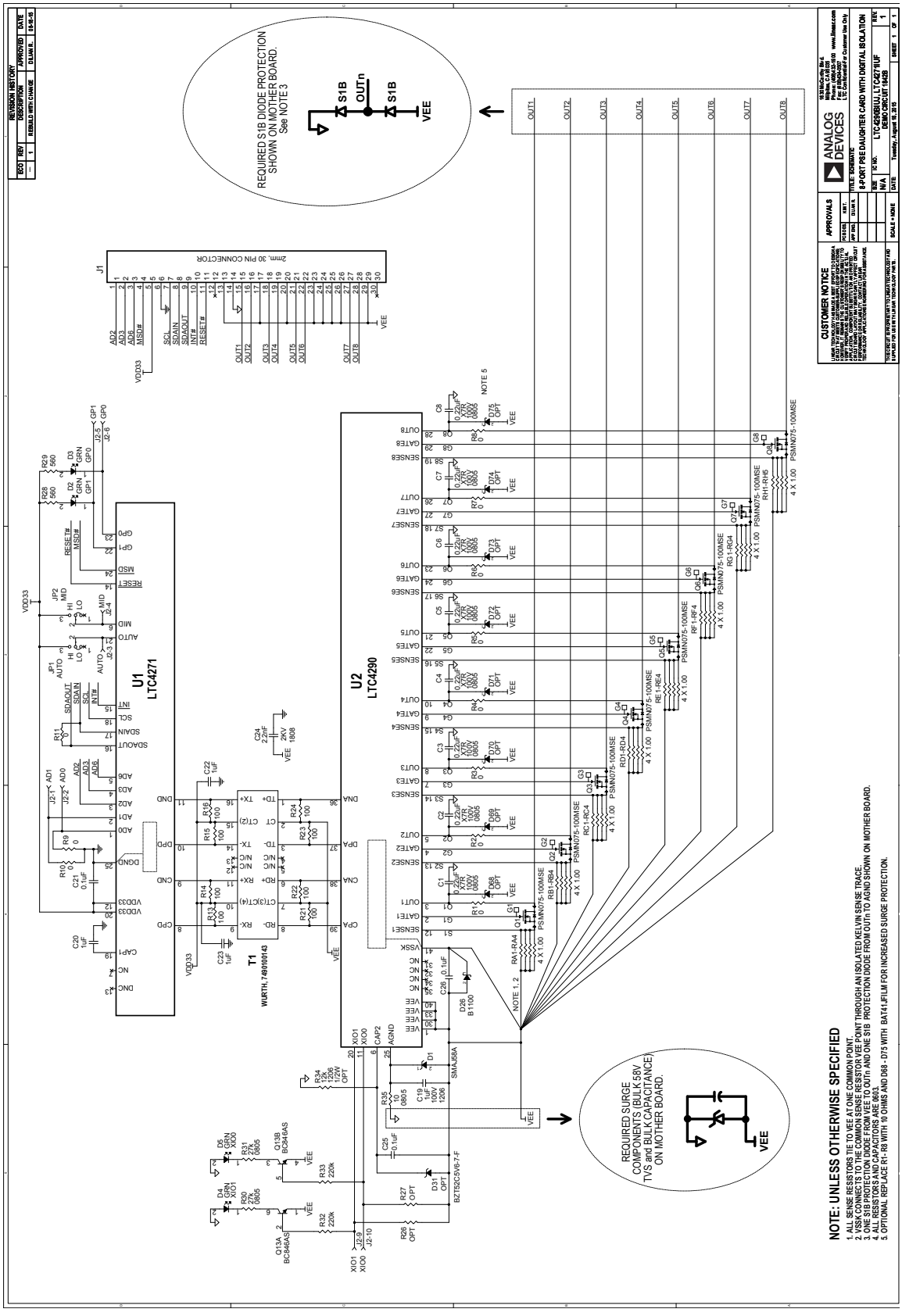


DEMONSTRATION CIRCUIT 1680B LAYOUT

Bottom Assembly



DC1842B SCHEMATIC DIAGRAM



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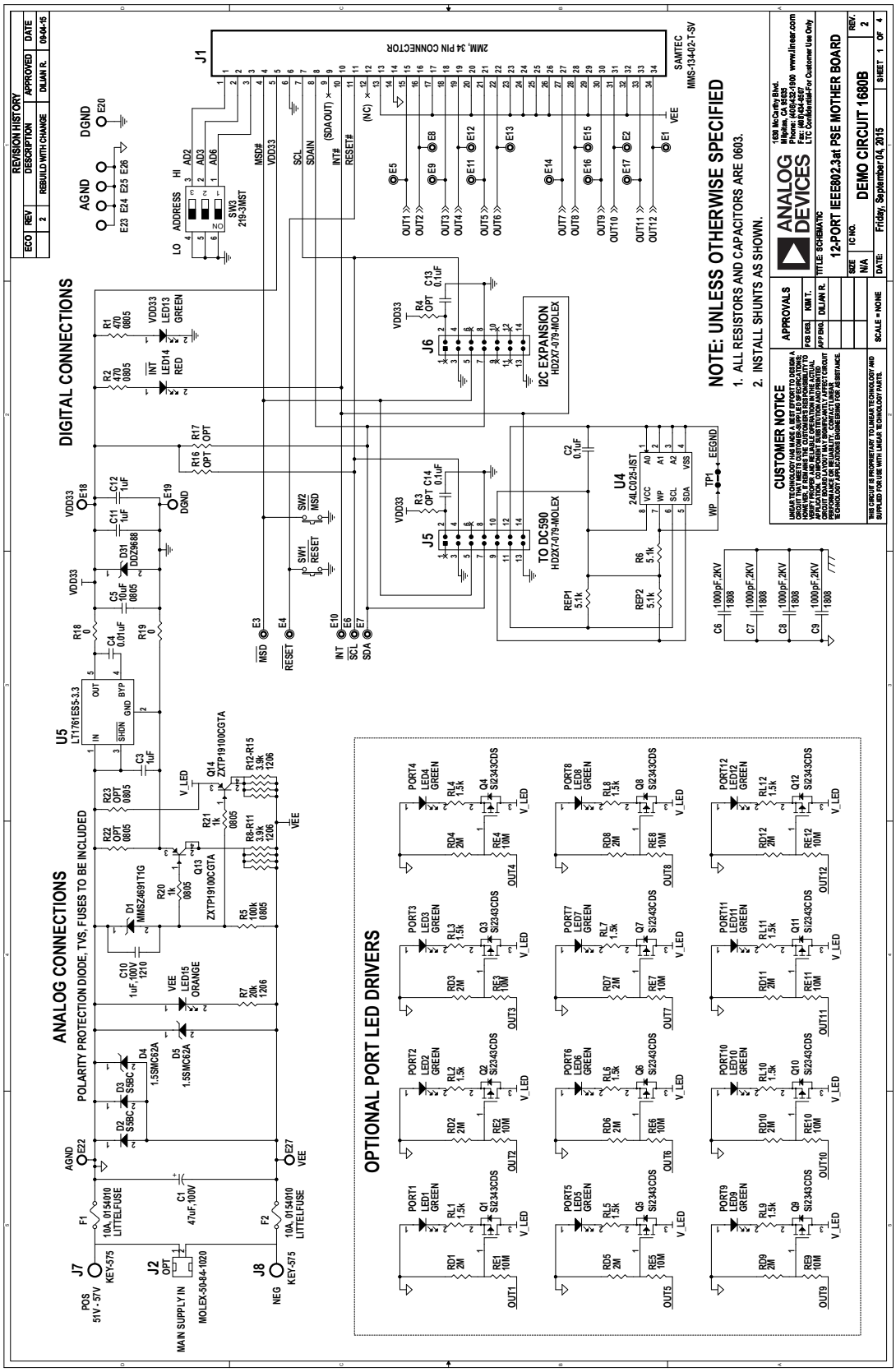

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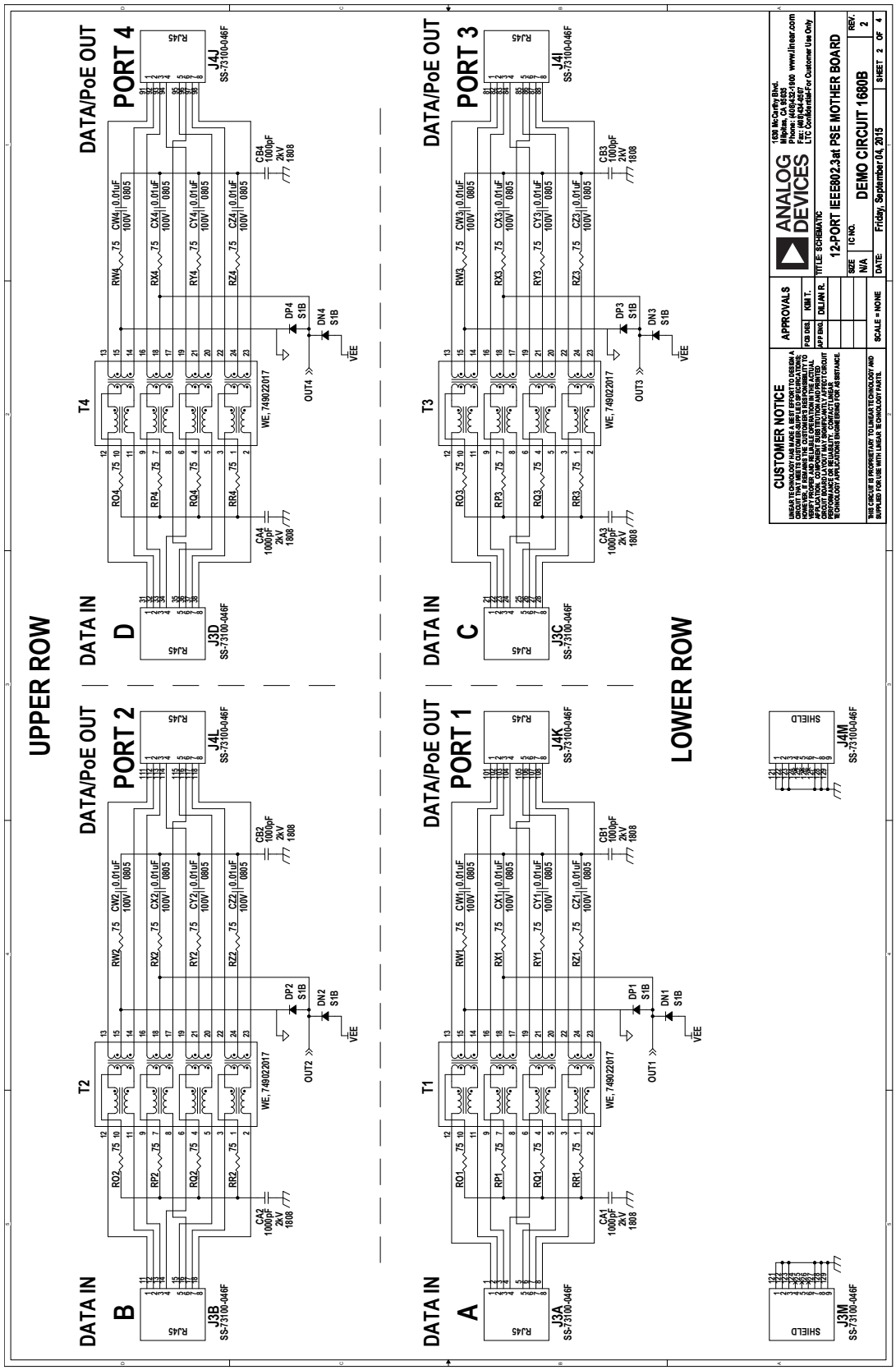

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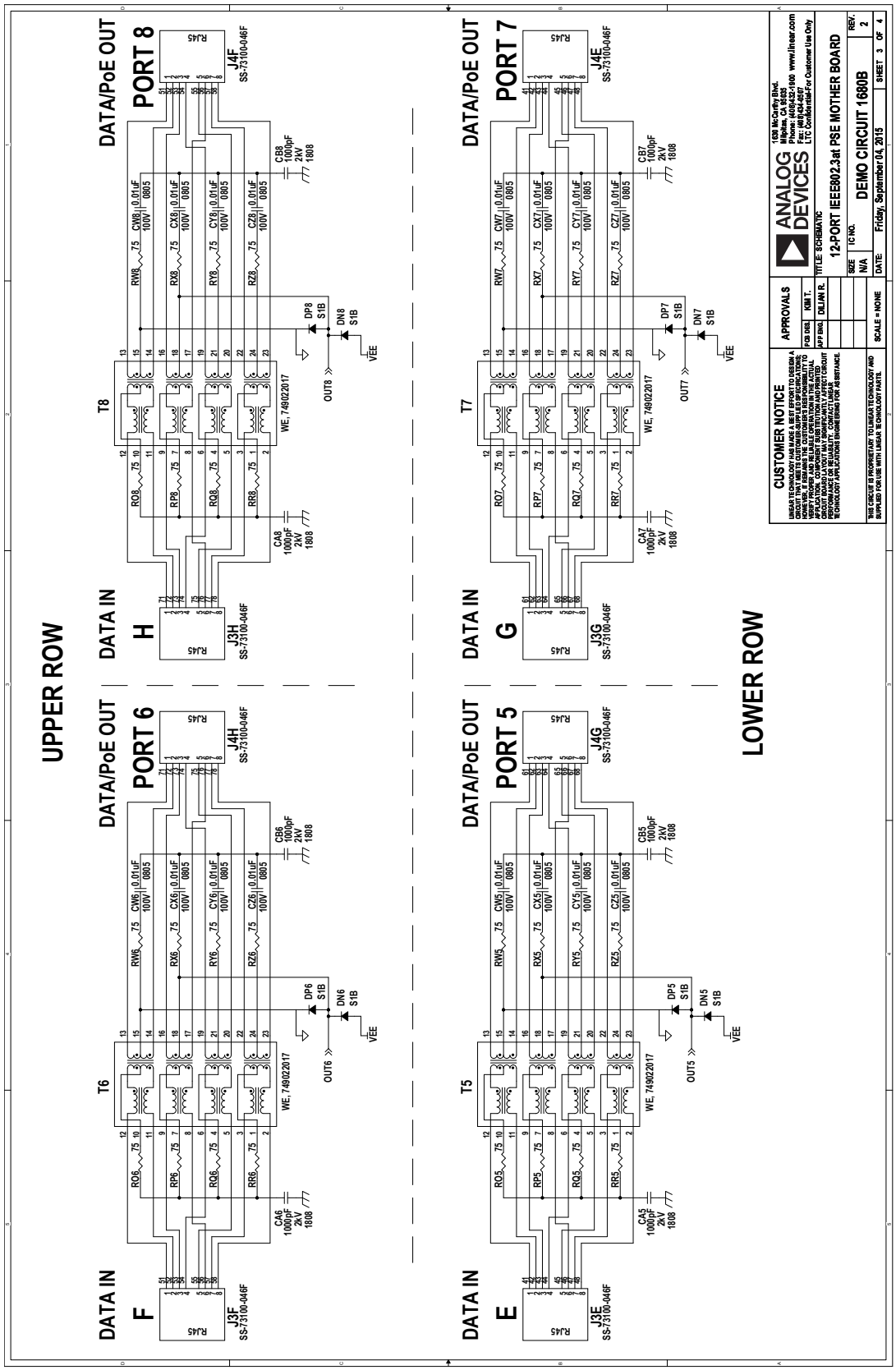

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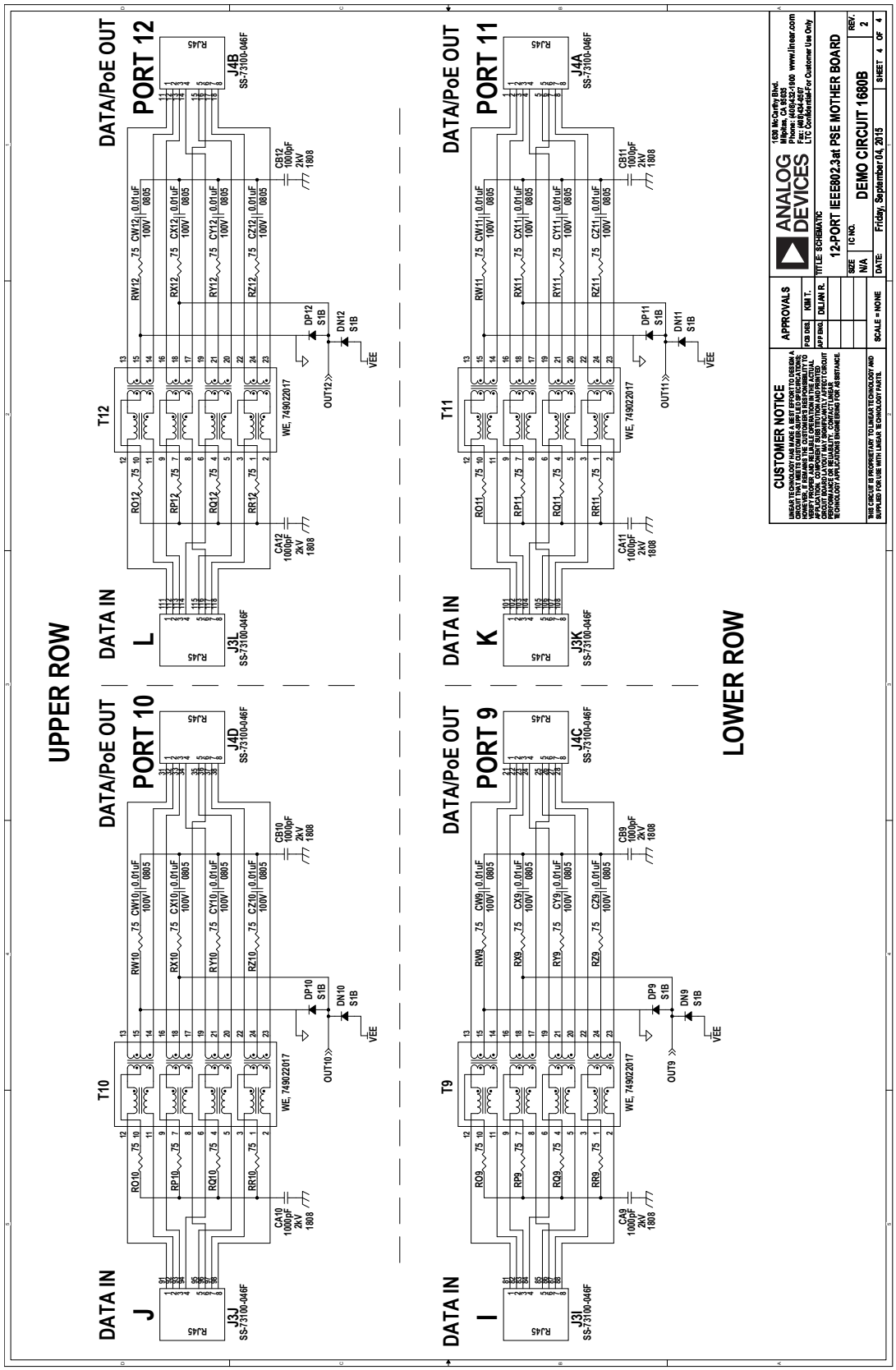

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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