Circuits from the Lab® Reference Designs

Circuits from the Lab® reference designs are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0511.

Devices Connected/Referenced		Devices Connected/Referenced	
AD9166	DC to 9 GHz, Direct RF Transmit (Tx) Sub-system	LT3090	–36 V, 600 mA Negative Linear Regulator with Programmable Current Limit
ADF4372	Microwave Wideband Synthesizer with Integrated VCO	ADP7183	−300 mA, Ultralow Noise, High PSRR, Low Dropout Linear Regulator
LTM8045	DC/DC µMicro Module up to 700 mA Output Current	ADM7150	800 mA Ultralow Noise, High PSRR, RF Linear Regulator
LTC2928	Multichannel Power Supply Sequencer and Supervisor	ADM7154	600 mA, Ultralow Noise, High PSRR, RF Linear Regulator
AD5693R	Tiny 16-Bit I²C *nano*DAC+, with ±2 (16-Bit) LSB INL and 2 ppm/°C Reference	LTM4622	Dual Ultrathin 2.5 A or Single 5 A Step-Down DC/DC µModule Regulator
ADP5073	1.2 A, DC-to-DC Inverting Regulator	ADP1761	1 A, Low VIN, Low Noise, CMOS Linear Regulator

DC to 5.5 GHz Signal Generator with +/-0.5 dB Calibrated Output Power

EVALUATION AND DESIGN SUPPORT

- Circuit Evaluation Boards
  - CN-0511 Reference Design Board (EVAL-CN0511-RPIZ)
- Design and Integration Files
  - Schematics, Layout Files, Bill of Materials, Software

CIRCUIT FUNCTIONS AND BENEFITS

A high frequency, low distortion, low noise signal source is a necessity when testing and debugging communication, radar, and other RF systems. Synthesized RF signal generators are standard equipment in RF test labs, but often require additional filtering when low distortion or low broadband noise is required.

The system shown in Figure 1 is a complete DC to 5.5 GHz sine wave signal generator based on a direct digital synthesis (DDS) architecture. A quad-switch digital-to-analog converter (DAC) core and integrated output amplifier provide exceptionally low-distortion over the entire operating frequency range, with a matched 50 Ω output termination.

A wide bandwidth amplitude calibration ensures that the output power, from 0 dBm to -40 dBm, stays within +/-0.5 dB over the entire operating frequency range.

The onboard clocking solution includes a reference oscillator and phase-locked loop (PLL), eliminating the need for an external clock source. All power is derived from a Raspberry Pi platform board, with ultra high power supply rejection ratio (PSRR) regulators and passive filtering to minimize the impact of the power converters on RF performance.

With this highly integrated solution, wide bandwidth and accurate output power performance comparable to that of commercial benchtop signal generators is now available in a small, low cost, open source reference design.

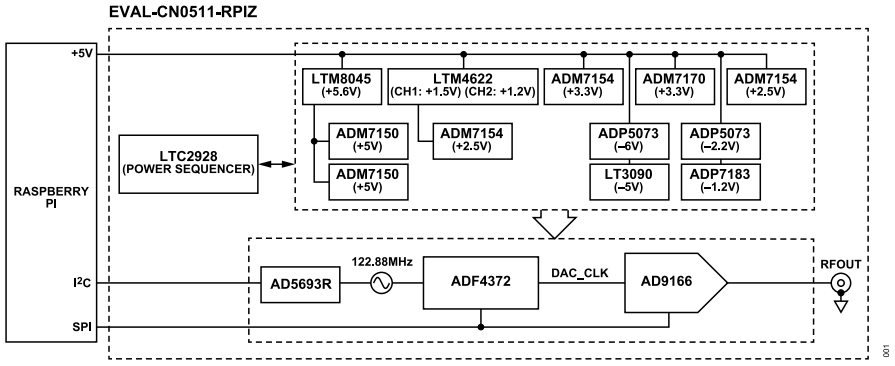

Figure 1. CN0511 Functional Block Diagram

CIRCUIT DESCRIPTION

RF SIGNAL GENERATOR OPERATION

High frequency RF generators, particularly at microwave frequencies, have historically been implemented using phase-locked loop (PLL) based synthesizers. DAC based DDS techniques have several advantages over PLLs: simplicity, low distortion, high-resolution tuning, and nearly instantaneous frequency, phase, and amplitude modulation. A typical DDS based signal generator is shown in Figure 2. A phase accumulator and amplitude to sinusoid converter comprise a numerically controlled oscillator (NCO). A tuning word is applied to a phase accumulator, which determines the slope of the output ramp. The upper bits of the accumulator are passed through an amplitude to sinusoid converter, and finally to a digital to analog converter.

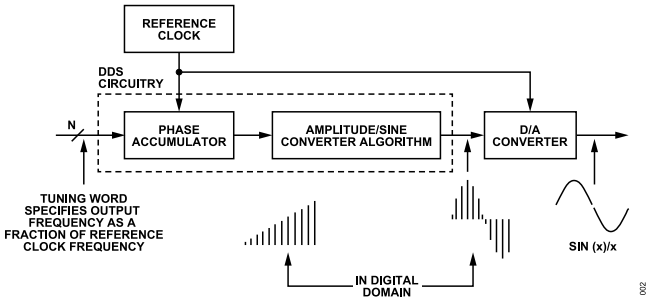

Figure 2. Typical DDS based Signal Generator

DIGITAL-TO-ANALOG CONVERTER

The AD9166 is a DC to 9GHz vector signal generator that incorporates a 6 GSPS (1x, non-return to zero mode) DAC, 8-lane, 12.5Gbps JESD204B data interface, DDS with multiple NCOs, and highly configurable digital data path that includes interpolation filters, wideband FIR85 filter, inverse SINC compensation, and digital mixers to allow flexible spectrum planning.

The AD9166 DAC core is based on a quad-switch architecture, which is configurable to double the effective DAC core update rate to 12 GSPS from a 6 GHz input sampling clock. The DAC has a noise spectral density (NSD) performance of -143 dBc/Hz with a 5 GHz single tone RF output. Spurious free dynamic range is typically 83 dB at 51 MHz, 66 dB at 451 MHz, and 38 dB at 4.051 GHz.

The differential to single-ended buffer eliminates the need for an expensive, wideband balun, and supports the full operating range of the DAC core, from DC to 9 GHz. DC-coupled outputs allow for baseband waveform generation without the need for external bias tees or similar circuitry.

The AD9166 supports return-to-zero and mix-mode operation, extending operation into the second, third, and fourth Nyquist zones. SINC roll-off for these modes are shown in Figure 3. Refer to the AD9166 data sheet for typical performance.

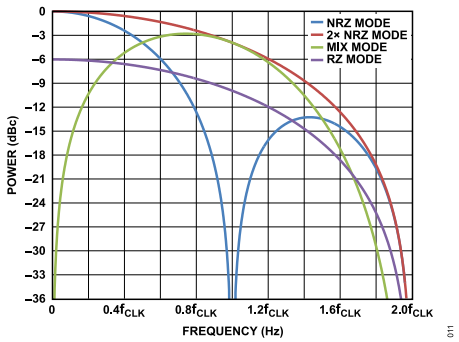

Figure 3. AD9166 Operating Modes

While intended for modulating baseband data via the JESD204B interface, the data inputs can be disabled and a DC value mixed with the NCO output. The AD9166 then functions as a single-chip, DC to 5.5 GHz, low-distortion, ultra-low phase noise RF signal generator.

Output Enable

In typical signal generator applications, it is important to have on/off control over the output so that any connected sensitive RF devices are not damaged. The AD9166 output can be easily configured through the TX_ENABLE pin to enable/disable the DAC output.

The TX_ENABLE pin can also be used for other functionality such as more accurate timing when enabling or disabling the DAC output, resetting the NCO phase accumulator, and even ramp up (or down) the full scale current of the DAC. For complete information on the TX_ENABLE capabilities, please view the AD9166 data sheet.

AMPLITUDE AND FREQUENCY CONTROL

Amplitude Output

The AD9166 output is a single-ended, 50 Ω (at DC), internally terminated output with a bipolar output stage for ease of interface with broadband 50 Ω environments. The equivalent output circuit is shown in Figure 4. The output stage is internally biased and terminated, with no external bias or termination components needed, and can be connected directly to downstream devices that present a 50 Ω ground referenced load.

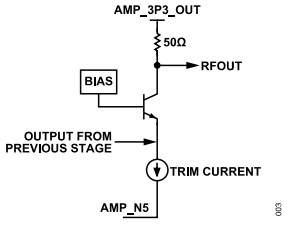

Figure 4. AD9166 Equivalent Output Circuit for RFOUT

In NCO-only mode, there are effectively two parameters that control the amplitude of the sinusoidal output:

- The DAC output current, I_{OUTFS}, is a digitally controlled current reference that determines the DAC full-scale output current.
- The DC Test Data word, DC_TEST_DATA, is a 16-bit digital value that is mixed (multiplied) with the NCO output in place of baseband data when in NCO-only mode.

The I_{OUTFS} value can be adjusted digitally over an 8 mA to 40 mA range by setting the ANA_FULL_SCALE_CURRENT register using Equation 1.

$$I_{OUTFS} = \left(32mA \times \frac{ANA\_FULL\_SCALE\_CURRENT}{1023}\right) + 8mA \quad (1)$$

where:
ANA_FULL_SCALE_CURRENT is the DAC analog full-scale current adjustment value
I_{OUTFS} is the full-scale output current of the AD9166 in mA

Figure 5 shows the uncalibrated output of the AD9166 with various I_{OUTFS} and DC_TEST_DATA settings; the upper trace is with both I_{OUTFS} and DC_TEST_DATA set to their maximum values (40 mA and 32767, respectively). The lower blue trace has I_{OUTFS} set to 40 mA but the DC_TEST_DATA set to 16422, resulting in a 6 dB reduction in output power. The lower red trace has I_{OUTFS} set to 20 mA and DC_TEST_DATA set to the maximum value, 32767, resulting in a 6.02 dB reduction in output power.

Taking both parameters into account, the peak-to-peak output voltage of the AD9166 is then given by Equation 2.

$$VOUT_{PP} = I_{OUTFS} \times 50\Omega \times 0.8 \times \frac{DC\_TEST\_DATA}{32768} \quad (2)$$

where:
$VOUT_{PP}$ is the peak-to-peak output voltage
DC_TEST_DATA is the digital scaling factor
0.8 is the gain of the AD9166 output amplifier.

The output in dBm can then be calculated by equation Equation 3:

$$dBm = 20 \times \log\left(\frac{VOUT_{PP}}{0.63246}\right) \quad (3)$$

The initial tolerance on I_{OUTFS} when set to 40 mA is -10.5% to +3.25%, and -7.9% to +7.1% when set to 8mA. To account for this tolerance, an initial calibration can be performed:

For a desired output amplitude of 0 dBm, set the DC_TEST_DATA to 32767, then reduce I_{OUTFS} until the target amplitude is reached. Typically, this would correspond to an I_{OUTFS} of 16mA.

Band Flatness

Several factors influence the CN0511 band flatness. SINC roll-off effects, as shown in Figure 3, cannot be avoided but are predictable. The output impedance also varies with frequency – it is nominally 50 Ω at DC, 23.91 – j12.44 Ω at 2.24 GHz, and 11.2 + j3.91 Ω at 4.22 GHz.(refer to the AD9166 data sheet for a Smith chart) This change in output impedance, along with any impedance mismatch at the load, causes a frequency dependent change in output amplitude.

The CN0511 frequency response was analyzed to determine the amplitude output flatness over the operating frequency range. During the band flatness test the output frequency was swept from 99 MHz to 5.8 GHz in 2 MHz steps using the AD9166 in NCO only mode.

The plot shown in Figure 5 shows several frequency sweeps using different combinations of I_{OUTFS} and DC_TEST_DATA output power values. Observe that the CN0511 has a relatively flat response below 2 GHz and begins to roll-off at the higher frequencies, ending with a decreased output power of around -6 dB at 5.8 GHz. It should also be noted that the plots shown in Figure 5 did not account for cable losses between the CN0511 and the spectrum analyzer.

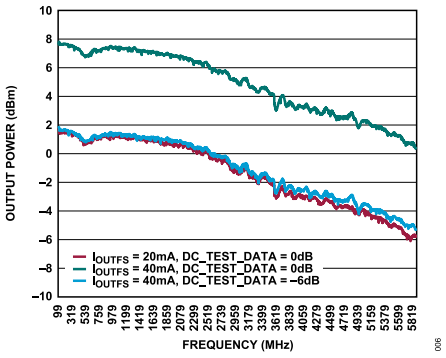

Figure 5. AD9166 Uncalibrated Output Power vs. Frequency

Output Power Calibration

Since band flatness is a critical parameter in signal generator applications, a wideband amplitude calibration was performed to correct the amplitude errors of the CN0511. The CN0511 was swept across the entire operating frequency range in 100 MHz steps and the output power was measured using an RF power meter. This process was repeated for five different output powers, corresponding to 0 dBm, -10 dBm, -20 dBm, -30 dBm, -40 dBm to determine the calibration coefficients required to flatten the CN0511 output power response. At each frequency, the DC_TEST_DATA is set to the desired output power, relative to 32767 = 0 dBm. I_{OUTFS} is then increased until the correct output power is reached. The calibration coefficients are stored in the onboard EEPROM allowing the software to correct for the amplitude errors and provide an overall band flatness better than +/-0.5 dB from 0 dBm to -40 dBm.

Figure 6 shows the wideband compensated band flatness of a typical CN0511 at several different output power levels.

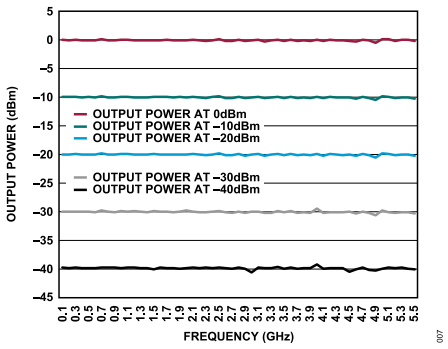

Figure 6. CN0511 Calibrated Output Power vs. Frequency

Frequency Output

The AD9166 has two implementations of the NCO function:

- A 48-bit, dual-modulus NCO for generating single tones
- A fast frequency hopping (FFH) NCO consisting of 32 NCOs, each with its own 32-bit phase accumulator

The main 48-bit NCO of the AD9166 is used in a dual-modulus mode to create fractional frequencies beyond the 48-bit precision. Implementation of the programmable modulus function within the AD9166 is such that the fraction, M/N, is expressed using Equation 4.

$$\frac{f_{CARRIER}}{f_{DAC}} = \frac{M}{N} = \frac{\left(X + \frac{A}{B}\right)}{2^{48}} \quad (4)$$

where:
$f_{CARRIER}$ is the output frequency
f_{DAC} is the DAC sampling frequency
X is the value programmed in the Frequency Tuning Word registers
A is the value programmed in the Accumulator Delta registers
B is the value programmed in the Accumulator Modulus registers
M and N are integers, where
$M < (N/2)$
in order to comply with the Nyquist sampling requirements.

The form of Equation 4 implies a compound frequency tuning word with X representing the integer part and A/B representing the fractional part. X, A, and B are inputs to the modulus control logic in Figure 7. With a 48-bit modulus and a 12 GHz f_{DAC}, the frequency resolution is
$\frac{12\ GHz}{2\text{^}48} = 0.000043\ Hz\ or\ 43\ \mu Hz.$
The dual-modulus mode further increases frequency resolution; for more information on the Modulus NCO Mode, please view the AD9166 data sheet and application note AN-953.

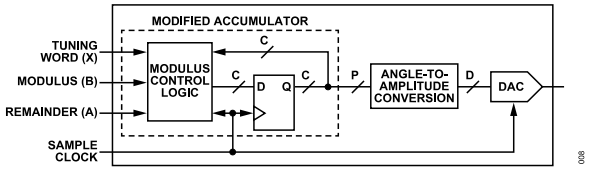

Figure 7. Programmable Modulus DDS Architecture

In FFH NCO mode, the 32 frequency tuning words can be preloaded and any word can be selected by a single register write. Frequency resolution of the 32-bit NCOs is 2.79 Hz with an f_{DAC} of 12 GHz. Phase continuous, phase discontinuous, and phase coherent hopping modes are available. With a 100 MHz serial peripheral interface (SPI), hops and dwell times as fast as 260 ns can be achieved.

Figure 8 illustrates phase coherent frequency hopping. Frequency A is programmed into one NCO tuning word, and Frequency B in another. Upon enabling the phase coherent switching mode, all NCO phase accumulators begin counting simultaneously and all continue counting regardless of which individual NCO output is currently selected. In this way, the frequency of any individual NCO can be selected and is always phase coherent.

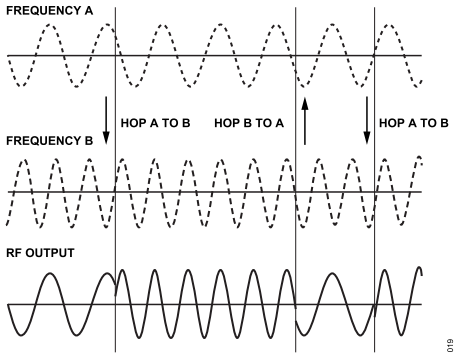

Figure 8. Diagram of Phase Coherent Frequency Hopping

SYSTEM CLOCKING

ADF4372 Synthesizer

The CN0511 uses the ADF4372 PLL that allows implementation of fractional-N or integer-N frequency synthesizers when used with an external loop filter and an external reference frequency. To achieve optimum integer boundary spur and phase noise performance, the ADF4372 uses a single-ended reference input signal, provided at REFP pin. The ADF4372 has an integrated VCO with a fundamental output frequency up to 8000 MHz using the RF8x ports. In addition, the VCO frequency is connected to a divide by 1, 2, 4, 8, 16, 32, or 64 circuit that allows the user to generate RF output frequencies as low as 62.5 MHz at RF8x.

The pair of RF8x output pins from the ADF4372 are collectors of a bipolar (NPN) differential pair driven by buffered outputs of the VCO and it also contains internal 50 Ω resistors, as shown in Figure 9. To optimize the power dissipation vs. the output power requirements, the tail current of the differential pair is programmable. Four current levels can be set. These levels give approximate output power levels from −4 dBm to +5 dBm.

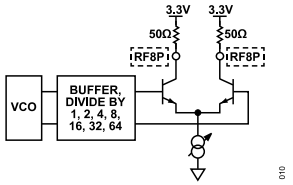

Figure 9. ADF4372 RF8x Output Stage

Equation 5 is used to program the RF output frequency of the ADF4372 synthesizer.

$$f_{RFOUT} = \left(INT + \frac{FRAC1 + \frac{FRAC2}{MOD2}}{MOD1} \right) \times \frac{f_{PFD}}{RF\_Divider} \quad (5)$$

where:
f_{RFOUT} is the RF output frequency
INT is the integer division factor
FRAC1 is the fractionality
FRAC2 is the auxiliary fractionality
MOD1 is the fixed 25-bit modulus
MOD2 is the auxiliary modulus
RF_Divider is the output divider value that divides down the VCO frequency

f_{PFD} is the frequency of the phase frequency detector which can be derived using Equation 6.

$$f_{PFD} = REF_{IN} \times \left(\frac{1 + D}{R \times (1 + T)} \right) \quad (6)$$

where:
REF_{IN} is the reference frequency input
D is the REF_{IN} doubler bit
R is the reference division factor
T is the reference divide by 2 bit (0 or 1)

Reference Input Frequency

The ADF4372 requires a reference input frequency, which is then multiplied to produce the 6 GHz AD9166 clock.

The EVAL-CN0511-RPIZ includes an onboard, ultra-low phase noise, 122.88MHz CMOS voltage-controlled crystal oscillator (VCXO) with phase noise of -166 dBc/Hz at a 1 MHz offset. The onboard VCXO enables fast bring up and evaluation of the CN0511, without the need for additional and expensive equipment.

Initial tolerance of the onboard oscillator is 20 ppm typical, suitable for many test and measurement applications. If greater accuracy is required, the VCXO clock frequency can be adjusted by the AD5693R voltage output DAC, enabling programmable clock trimming for increased accuracy.

Alternatively, the AD9166 output frequency can be trimmed by adding an offset to the frequency tuning word; the 48-bit NCO resolution provides a potential trimming frequency resolution of 42.6 µHz.

If lower system noise, tighter frequency accuracy, or more precise frequency drift is required, or if the CN0511 must be synchronized to external equipment, an external reference frequency can be applied to the clock reference connector. Any external clock source used must not exceed the 500 MHz maximum reference input frequency.

AD9166 Clock Reference Input

The AD9166 contains a low jitter, differential clock receiver that is capable of interfacing directly to a differential or single-ended clock source. Because the input is self-biased with a nominal impedance of 90 Ω, it is recommended that the clock source be ac-coupled to the CLK± input pins. The nominal differential input is 1 Vp-p, but the clock receiver can operate with a span that ranges from 250 mVp-p to 2.0 Vp-p.

Figure 10 shows the clock source for the AD9166 based on the ADF4372 low phase noise, low jitter PLL.

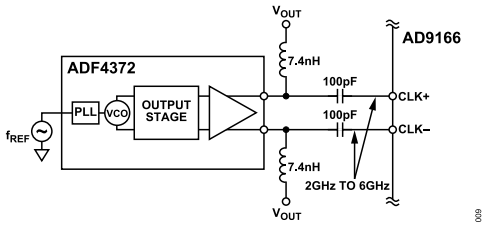

Figure 10. Circuit Connection between the ADF4372 and the AD9166

The quality of the clock source, as well as its interface to the AD9166 clock input, directly impacts ac performance. Select a clock source which exhibits the phase noise and spur characteristics to meet the target application requirements. Phase noise and spurs at a given frequency offset on the clock source are directly translated to the output signal.

The improvement in performance also depends on the phase balance of the external components as well as on the internal clock path. Process variations may result in varying phase balance across devices of the same population. Thus, if higher levels of image rejection are desired, it may be beneficial to calibrate each system independently. The AD9166 can compensate for phase imbalance through the Clock Phase Tune register. Up to 620 fF can be added to either CLK+ or CLK- in 20 fF steps.

POWER SUPPLY ARCHITECTURE

The system consumes nearly 6 W when the RF amplifier is enabled which is sourced from the Raspberry Pi. Figure 11 shows the system power map which provides the information about the efficiency and the power losses for each switching and linear regulators.

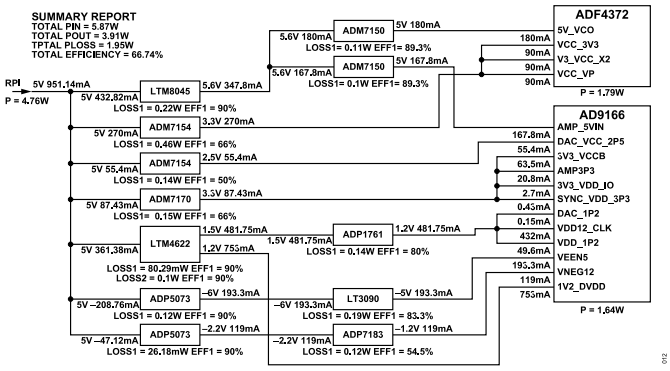

Figure 11. CN0511 System Power Tree

The AD9166 clock supply is the most noise sensitive supply on the device, where phase noise and other spectral content are modulated directly onto the output signal. The AD9166 DAC output supply rails (+2.5 V and -1.2 V) and amplifier supply rails (+5 V, +3.3 V, and -5 V) are also areas for concern when it comes to modulating noise directing into the output signal of the generator.

The power distribution for the AD9166 and ADF4372 are shown in Table 1. The LTM8045, LTM4622, and ADP5073 switching regulators were chosen to achieve 90% efficiency based on the system load requirements. The low dropout linear regulators (LDOs), such as the ADM7150, ADM7154, and ADP1761, were chosen to supply the, DAC, amplifier, PLL, and VCO for their ultralow noise and high PSRR to achieve the best phase noise performance possible.

Table 1. CN-0511 Power Distribution and Consumption

RF Device	Switching Regulator	Linear Regulator	Voltage Supply (V)	I_{LOAD} (mA)	Power Consumed (W)
AD9166	LTM8045	ADM7150	5	167.8	0.84
		ADM7170	3.3	87.43	0.29
		ADM7154	2.5	55.4	0.14
	LTM4622 (CH1)	ADP1761	1.2	481.75	0.58
	LTM4622 (CH2)	None	1.2	753	0.90
	ADP5073	ADP1783	-1.2	119	0.14
	ADP5073	LT3090	-5	193.3	0.97
ADF4372	LTM8045	ADM7150	5	180	0.90
	None	ADM7154	3.3	270	0.89

POWER SUPPLY SEQUENCING

The AD9166 requires power sequencing to avoid damage to internal circuitry. The LTC2928 power sequencer chip was used to ensure that the CN0511 powers up in the correct order as shown in Figure 12.

The LTC2928 monitors and manages up to four voltage rails, individually controlling the power on time. Other supervisory functions include undervoltage and overvoltage monitoring and reporting, as well as microprocessor reset generation for the CN0511 system.

The power-up sequence used goes in order from V1 to V3 sequentially, noting that supplies in each group should power-up and settle together. Within each group, it is a good strategy to monitor the supply with the longest settling time to ensure that all the supplies settle to their target voltage before sequencing to the next group. There are no requirements for a power-down sequence in the CN0511 application.

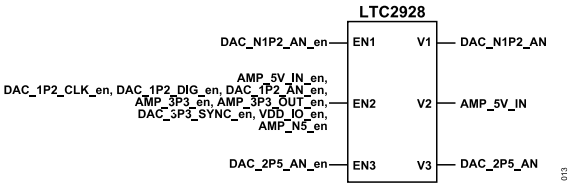

Figure 12. CN0511 Power Sequencing Simplified Diagram

THERMAL CONSIDERATIONS

The AD9166 can dissipate nearly 4 W depending on the application and configuration. The AD9166 uses an exposed die package to reduce thermal resistance and allow cooling of the die directly. A mechanical heat sink with a fan is used to dissipate the thermal heat from the package.

Figure 13 and Figure 14 show two test scenarios that were conducted for CN0511 Reference Design, one without the heat sink and the other case is with the heat sink attached. The low and high temperature reading registered in the thermal camera is the operating temperature at the surface of the CN0511. Without the heat sink, the ADF4372 device registered with the highest thermal reading that is around 86.5ºC.

And with the heat sinks attached, the LTM4622 shows the highest thermal reading that is around 60.6ºC.

Figure 13. CN0511 Thermal Performance without Heat Sinks Attached

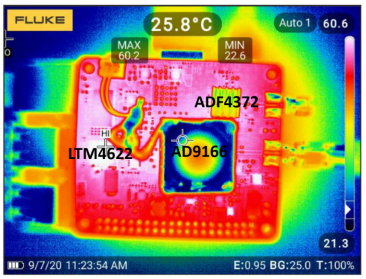

Figure 14. CN0511 Thermal Performance with Heat Sinks Attached

Software readings were also taken from the device junction temperature for both the ADF4372 and the AD9166, as both devices have an on-chip temperature sensor which can be accessed through software. The junction temperature determines the maximum safe operating temperature for both the ADF4372 and the AD9166.

As shown in Table 2, without the heat sink, the ADF4372 has the highest temperature of 95.5ºC. While this is still below the absolute maximum operating temperature of 105ºC, ambient temperature was about 25ºC. A heat sink is required at higher ambient temperatures in order to prevent exceeding 105ºC.

Table 2. Thermal Dissipation Summary

Thermal Test	AD9166 Junction Temperature (°C)	ADF4372 Junction Temperature (°C)
CN0511 without Heat sink	42.5	95.5
CN0511 with Heat sink	39.4	63.5

With the heat sink attached, the operating temperature of the ADF4372 drops to 63.5ºC (about 30ºC lower). The significant improvement in ADF4372 junction temperature after the heat sink is placed also resulted in an improvement in phase noise by 2 dBc/Hz to 3 dBc/Hz.

LAYOUT CONSIDERATIONS

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. To improve the thermal performance of the design, thermal vias on the PCB thermal pad is used. The via diameter is between 0.3 mm and 0.33 mm and the via barrel is plated with 1 oz. of copper.

For this application, where highest performance and higher output frequencies are required, the choice of PCB materials significantly impacts results. Figure 15 shows the PCB stackup which uses Rogers 4350 dielectric material on the layers that contain RF traces to minimize the signal attenuation in signals greater than 3 GHz and to ensure the best signal integrity at the RF output.

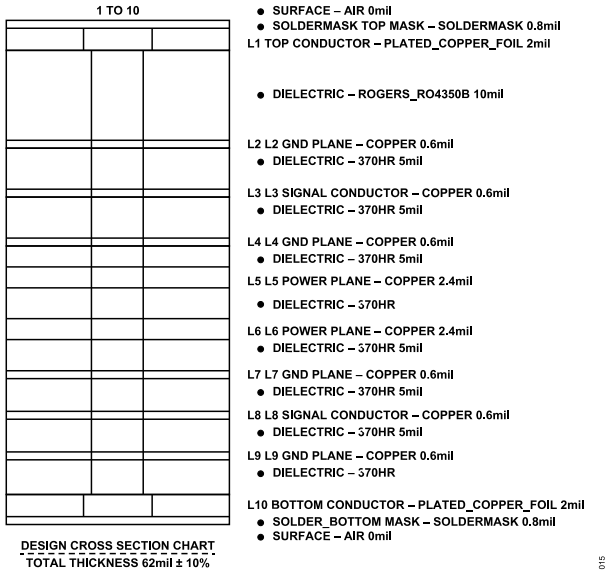

Figure 15. CN0511 PCB Cross Section and Stackup

COMMON VARIATIONS

The AD9164 can be used for applications that require differential output direct RF synthesizer, but this requires impedance matching at the output side.

For the VCO operating at a higher frequency for DAC clock reference, the ADF4371 can be used at the expense of a noise performance.

CIRCUIT EVALUATION AND TEST

The following sections outline the general setup and getting started procedure. For complete step by step details, please visit the CN-0511 User Guide

EQUIPMENT NEEDED

- EVAL-CN0511-RPIZ
- Raspberry PI 3B+
- 5 V, 2.5 A power supply with micro USB connector (Standard RPI 3B+ power supply recommended)
- 16 GB MicroSD Card (or larger)
- ADI Kuiper Linux
- USB keyboard and mouse
- HDMI to HDMI Cable
- Monitor with HDMI input port
- Male SMA to SMA Cable
- Spectrum Analyzer: Keysight E5052B/R&S FSUP

GETTING STARTED

1. Load the ADI Kuiper Linux Image onto a micro SD card.
2. Place the micro SD Card into the Raspberry Pi 3B+.
3. Connect the EVAL-CN0511-RPIZ board on top of the Raspberry Pi 3B+ using the 40-pin connector.
4. Plug in the HDMI cable from the Raspberry Pi 3B+ to the monitor
5. Plug in the USB keyboard and mouse into the Raspberry Pi 3B+
6. Connect the 5 V, 2.5 A power supply into the micro USB connector on the Raspberry Pi 3B+
7. Connect the SMA cable from the EVAL-CN0511-RPIZ to the Keysight E5052B/R&S FSUP or equivalent spectrum analyzer.
8. Once ADI Kuiper Linux boots, open the IIO Oscilloscope application.
9. The IIO Oscilloscope then opens the CN0511 software plugin. Set the frequency to 2.5 GHz and an output amplitude of -10 dBm and enable the output.
10. Using the spectrum analyzer, find the 2.5 GHz output signal and verify if it is approximately -10 dBm.

FUNCTIONAL TEST SETUP

Raspberry Pi connects to the EVAL-CN0511-RPIZ through P3 which is a 40-pin connector as shown in Figure 16 and Figure 17.

Additional peripherals such as HDMI monitor and USB wired or wireless keyboard/mouse are necessary to configure the device.

Another way to remotely access and connect to the device is by connecting the device to the internet either via LAN cable or WLAN.

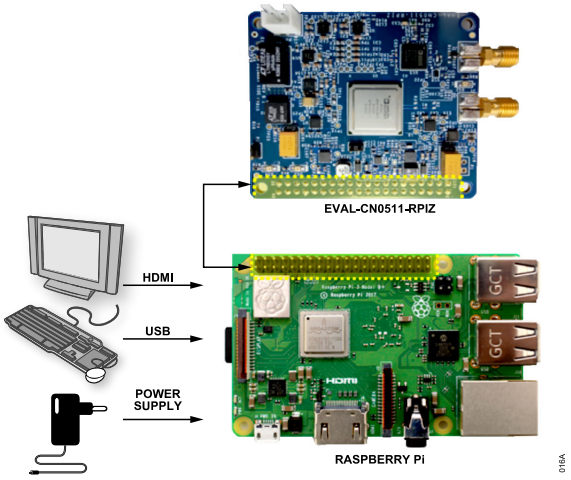

Figure 16. CN0511 System Test Materials

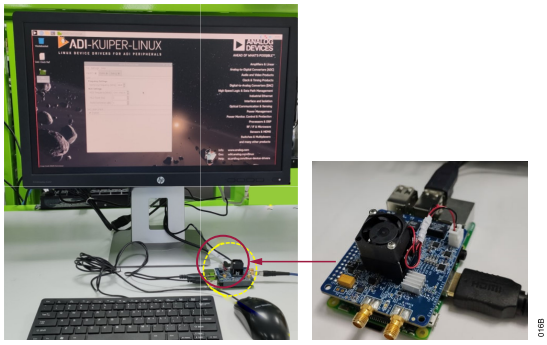

Figure 17. CN0511 System Test Setup

TEST RESULTS

Phase noise is a critical RF signal generator performance metric. Phase noise is the ratio of the spectral power density measured at an offset frequency from the carrier to the total power of the carrier signal. Phase noise is an indicator of the signal quality. An ideal signal spectrum representation shows its total energy is concentrated in a singular frequency. However, the real signals have a spectral distribution, and their energy is spread. The better the signal quality, the higher the energy concentrated close to the carrier.

In general, phase noise refers to short-term, random fluctuations in the phase of the signal, and is usually expressed as value normalized to a 1 Hz bandwidth and at some offset frequency away from the signal frequency and relative to the amplitude of the signal. In the time domain, phase noise is exhibited as a jitter in the zero crossings of a sine wave.

The quality of the clock source, as well as its interface to the AD9166 clock input, directly impacts phase noise performance.

Phase noise and spurs at a given frequency offset on the clock source are directly transferred to the output signal.

Table 3. CN0511 Phase Noise Test Settings

Device	Device Settings
AD9166	Buffer Amplifier: Enabled FIR85 Filter: Enabled Clock Sampling Rate: 6 GHz NCO Output Frequency: 100 MHz, 1 GHz, 4 GHz, 5 GHz, 5.5 GHz NCO Digital Scale: 0 dBm

The graph displayed in Figure 18 is the 0 dBm output power, single side band (SSB) Phase Noise vs. Frequency Offset plot measured from the EVAL-CN0511-RPIZ. The plot shows the phase noise of the CN0511 using the onboard 122.88 MHz VCXO.

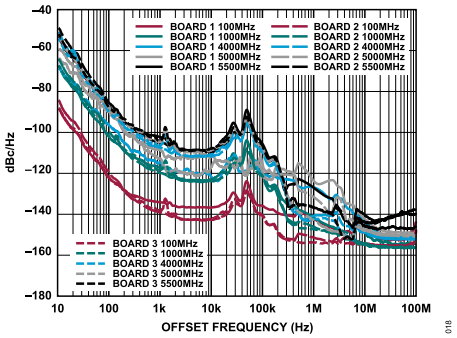

Figure 18. Single Side Band(SSB) Phase Noise vs. Output Frequency

LEARN MORE

Bergeron, Jarrah Analyzing and Managing the Impact of Supply Noise and Clock Jitter on High Speed DAC Phase Noise, Analog Dialogue 51-03, March 2017.

Brannon, Brad. Application Note AN-756, Sampled Systems and the Effects of Clock Phase Noise and Jitter. Analog Devices, Inc., 2004.

Reeder, Rob. "Designing Power Supplies for High Speed ADC." Analog Devices, Inc., February 2012.

Ardizzoni, John. *A Practical Guide to High-Speed Printed-Circuit-Board Layout*, Analog Dialogue 39-09, September 2005.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.

MT-073 Tutorial, *High Speed Variable Gain Amplifiers (VGAs)*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

AN-953 Tutorial, *Direct Digital Synthesis (DDS) with a Programmable Modulus*, Analog Devices.

Eva Murphy and Colm Slattery*Ask The Application Engineer—33: All About Direct Digital Synthesis*

DATA SHEETS AND EVALUATION BOARDS

AD9166 Data Sheet

AD9166 Evaluation Board

ADP5073 Data Sheet

ADP5073 Evaluation Board

ADP7183 Data Sheet

ADP7183 Evaluation Board

LTC2928 Data Sheet

LTC2928 Evaluation Board

ADF4372 Data Sheet

ADF4372 Evaluation Board

ADM7150 Data Sheet

ADM7150 Evaluation Board

LTM8045 Data Sheet

LTM8045 Evaluation Board

ADM7154 Data Sheet

ADM7154 Evaluation Board

AD5693R Data Sheet

AD5693R Evaluation Board

LTM4622 Data Sheet

LTM4622 Evaluation Board

ADP1761 Data Sheet

ADP1761 Evaluation Board

LT3090 Data Sheet

LT3090 Evaluation Board

REVISION HISTORY

05/2022—Revision 0: Initial Version

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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EVAL-CN0511-RPIZ