# 2-Channel, 2-Wire Bus Multiplexer with Capacitance Buffering

## FEATURES

- **1:2 2-Wire Multiplexer/Switch**
- **Connect SDA and SCL Lines with 2-Wire Bus Commands**
- **Supply Independent Bidirectional Buffer for SDA and SCL Lines Increases Fan-Out**
- **Programmable Disconnect from Stuck Bus**
- Compatible with I²C and SMBus Standards
- Rise Time Accelerator Circuitry
- SMBus Compatible ALERT Response Protocol
- Prevents SDA and SCL Corruption During Live Board Insertion and Removal from Backplane
- ±10kV Human Body Model ESD Ruggedness
- 16-Lead (4mm × 5mm) DFN and SSOP Packages

## APPLICATIONS

- Nested Addressing
- 5V/3.3V Level Translator
- Capacitance Buffer/Bus Extender

## DESCRIPTION

The LTC®4305 is a 2-channel, 2-wire bus multiplexer with bus buffers to provide capacitive isolation between the upstream bus and downstream buses. Through software control, the LTC4305 connects the upstream 2-wire bus to any desired combination of downstream channels. Each channel can be pulled up to a supply voltage ranging from 2.2V to 5.5V, independent of the LTC4305 supply voltage. The downstream channels are also provided with an $\overline{\text{ALERT1}}$–$\overline{\text{ALERT2}}$ inputs for fault reporting.

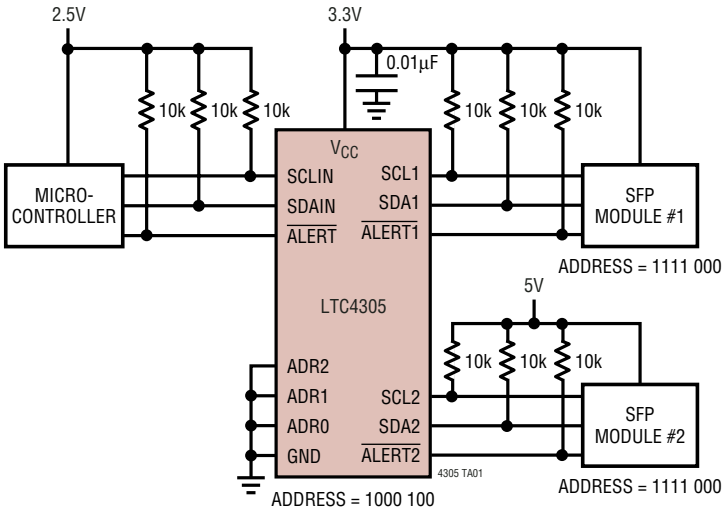
Programmable timeout circuitry disconnects the downstream buses if the bus is stuck low. When activated, rise time accelerators source currents into the 2-wire bus pins to reduce rise time. Driving the ENABLE pin low restores all features to their default states. Three address pins provide 27 distinct addresses.

The LTC4305 is available in 16-lead (4mm × 5mm) DFN and SSOP packages.

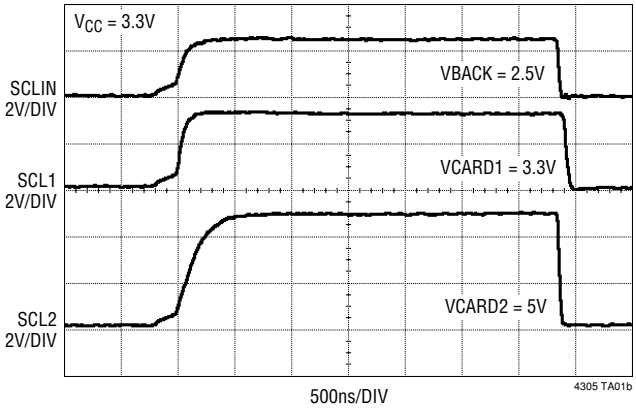


## TYPICAL APPLICATION

**A Level-Shifting and Nested Addressing Application**




**I²C Bus Waveforms**

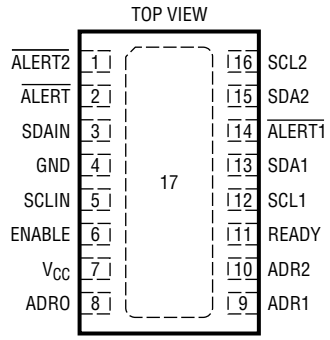


## ABSOLUTE MAXIMUM RATINGS (Note 1)

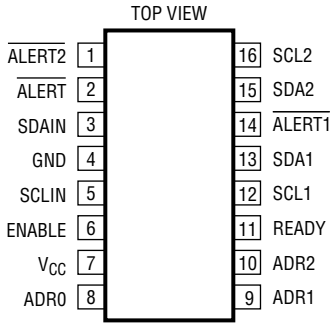
Supply Voltage ($V_{CC}$) ..... –0.3V to 7V
Input Voltages (ADR0, ADR1, ADR2, ENABLE, $\overline{ALERT1}$, $\overline{ALERT2}$) ..... –0.3V to 7V
Output Voltages ($\overline{ALERT}$, READY) ..... –0.3V to 7V
Input/Output Voltages (SDAIN, SCLIN, SCL1, SDA1, SCL2, SDA2) ..... –0.3V to 7V
Output Sink Current (SDAIN, SCLIN, SCL1, SDA1, SCL2, SDA2, $\overline{ALERT}$, READY) ..... 10mA

Operating Temperature Range
LTC4305C ..... 0°C to 70°C
LTC4305I ..... –40°C to 85°C
Storage Temperature Range
DHD Package ..... –65°C to 125°C
GN Package ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
GN Package ..... 300°C

## PACKAGE/ORDER INFORMATION




DHD PACKAGE
16-LEAD (4mm × 5mm) PLASTIC DFN
EXPOSED PAD (PIN 17) PCB CONNECTION OPTIONAL
MUST BE CONNECTED TO PCB TO OBTAIN
$\theta_{JA}$ = 43°C/W OTHERWISE $\theta_{JA}$ = 140°C/W. $T_{JMAX}$ = 125°C




GN PACKAGE
16-LEAD NARROW PLASTIC SSOP
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 135°C/W

| ORDER PART NUMBER | DHD PART MARKING | ORDER PART NUMBER | GN PART MARKING |
|---|---|---|---|
| LTC4305CDHD<br>LTC4305IDHD | 4305<br>4305 | LTC4305CGN<br>LTC4305IGN | 4305<br>4305I |

**Order Options** Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marketing: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

**The ● denotes specifications which apply over the full specified temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 3.3V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Power Supply/Start-Up** | | | | | | | |
| $V_{CC}$ | Input Supply Range | | ● | 2.7 | | 5.5 | V |
| $I_{CC}$ | Input Supply Current | Downstream Connected, $V_{CC}$ = 5.5V SCL Bus Low, SDA Bus High | ● | | 5.2 | 8 | mA |
| $I_{CC\ ENABLE}$ = 0V | Input Supply Current | $V_{ENABLE}$ = 0V, $V_{CC}$ = 5.5V | ● | | 1.25 | 2.5 | mA |
| $V_{UVLOU}$ | UVLO Upper Threshold Voltage | | ● | 2.3 | 2.5 | 2.7 | V |
| $V_{UVLOHYST}$ | UVLO Threshold Hysteresis Voltage | | ● | 100 | 175 | 250 | mV |

## ELECTRICAL CHARACTERISTICS

**The ● denotes specifications which apply over the full specified temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 3.3V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Power Supply/Start-Up** | | | | | | | |
| $V_{TH\ EN}$ | ENABLE Falling Threshold Voltage | | ● | 0.8 | 1.0 | 1.2 | V |
| $V_{EN\ HYST}$ | ENABLE Threshold Hysteresis Voltage | | | | 60 | | mV |
| $t_{PHL\ EN}$ | ENABLE Delay, On-Off | | | | 60 | | ns |
| $t_{PLH\ EN}$ | ENABLE Delay, Off-On | | | | 20 | | ns |
| $I_{IN\ EN}$ | ENABLE Input Leakage Current | $V_{ENABLE}$ = 0V, 5.5V, $V_{CC}$ = 5.5V | ● | | 0.1 | ±1 | µA |
| $V_{LOW\ READY}$ | READY Pin Logic Low Output Voltage | $I_{PULL-UP}$ = 3mA, $V_{CC}$ = 2.7V | ● | | 0.18 | 0.4 | V |
| $I_{OFF\ READY}$ | READY Off State Input Leakage Current | $V_{READY}$ = 0V, 5.5V, $V_{CC}$ = 5.5V | ● | | 0 | ±1 | µA |
| **ALERT** | | | | | | | |
| $V_{\overline{ALERT}(OL)}$ | $\overline{ALERT}$ Output Low Voltage | $I_{\overline{ALERT}}$ = 3mA, $V_{CC}$ = 2.7V | ● | | 0.2 | 0.4 | V |
| $I_{OFF,\ \overline{ALERT}}$ | $\overline{ALERT}$ Off State Input Leakage Current | $V_{\overline{ALERT}}$ = 0V, 5.5V | ● | | 0 | ±1 | µA |
| $I_{IN,\ \overline{ALERT1-2}}$ | $\overline{ALERT1}$–$\overline{ALERT2}$ Input Current | $V_{\overline{ALERT1-2}}$ = 0V, 5.5V | ● | | 0 | ±1 | µA |
| $V_{\overline{ALERT1-2}(IN)}$ | $\overline{ALERT1}$–$\overline{ALERT2}$ Pin Input Falling Threshold Voltages | | ● | 0.8 | 1.0 | 1.2 | V |
| $V_{\overline{ALERT1-2}(HY)}$ | $\overline{ALERT1}$–$\overline{ALERT2}$ Pin Input Threshold Hysteresis Voltages | | | | 80 | | mV |
| **Rise Time Accelerators** | | | | | | | |
| $V_{SDA,SCL\ slew}$ | Initial Slew Requirement to Activate Rise Time Accelerator Currents | SDAIN, SCLIN, SDA1–2, SCL1–2 Pins | ● | | 0.4 | 0.8 | V/µs |
| $V_{RISE,DC}$ | Rise Time Accelerator DC Threshold Voltage | SDAIN, SCLIN, SDA1–2, SCL1–2 Pins | ● | 0.7 | 0.8 | 1 | V |
| $I_{BOOST}$ | Rise Time Accelerator Pull-Up Current | SDAIN, SCLIN, SDA1–2, SCL1–2 Pins (Note 3) | | 4 | 5.5 | | mA |
| **Stuck Low Timeout Circuitry** | | | | | | | |
| $V_{TIMER(L)}$ | Stuck Low Falling Threshold Voltage | $V_{CC}$ = 2.7V, 5.5V | ● | 0.4 | 0.52 | 0.64 | V |
| $V_{TIMER(HYST)}$ | Stuck Low Threshold Hysteresis Voltage | | | | 80 | | mV |
| $T_{TIMER1}$ | Timeout Time #1 | TIMSET1,0 = 01 | ● | 25 | 30 | 35 | ms |
| $T_{TIMER2}$ | Timeout Time #2 | TIMSET1,0 = 10 | ● | 12.5 | 15 | 17.5 | ms |
| $T_{TIMER3}$ | Timeout Time #3 | TIMSET1,0 = 11 | ● | 6.25 | 7.5 | 8.75 | ms |
| **Upstream-Downstream Buffers** | | | | | | | |
| $V_{OS,BUF}$ | Buffer Offset Voltage | $R_{BUS}$ = 10k, $V_{CC}$ = 2.7V, 5.5V (Note 4) | ● | 25 | 60 | 100 | mV |
| $V_{OS,UP-BUF}$ | Upstream Buffer Offset Voltage<br>$V_{IN,BUFFER}$ = 0V | $V_{CC}$ = 2.7V, $R_{BUS}$ = 2.7k (Note 4)<br>$V_{CC}$ = 5.5V, $R_{BUS}$ = 2.7k (Note 4) | ●<br>● | 40<br>70 | 80<br>110 | 120<br>150 | mV<br>mV |
| $V_{OS,DOWN-BUF}$ | Downstream Buffer Offset Voltage<br>$V_{IN,BUFFER}$ = 0V | $V_{CC}$ = 2.7V, $R_{BUS}$ = 2.7k (Note 4)<br>$V_{CC}$ = 5.5V, $R_{BUS}$ = 2.7k (Note 4) | ●<br>● | 60<br>80 | 110<br>140 | 160<br>200 | mV<br>mV |
| $V_{OL}$ | Output Low Voltage, $V_{IN,BUFFER}$ = 0V | SDA, SCL Pins; $I_{SINK}$ = 4mA, $V_{CC}$ = 3V, 5.5V | ● | | | 400 | mV |
| $V_{OL}$ | Output Low Voltage, $V_{IN,BUFFER}$ = 0.2V | SDA, SCL Pins; $I_{SINK}$ = 500µA, $V_{CC}$ = 2.7V, 5.5V | ● | | | 320 | mV |
| $V_{IL,MAX}$ | Buffer Input Logic Low Voltage | $V_{CC}$ = 2.7V, 5.5V | ● | 0.4 | 0.52 | 0.64 | V |
| $V_{THSDA,SCL}$ | Downstream SDA, SCL Logic Threshold Voltage | | ● | 0.8 | 1.0 | 1.2 | V |
| $I_{LEAK}$ | Input Leakage Current | SDA, SCL Pins; $V_{CC}$ = 0 to 5.5V; Buffers Inactive | ● | | | ±5 | µA |

## ELECTRICAL CHARACTERISTICS

**The ● denotes specifications which apply over the full specified temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{CC}$ = 3.3V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **I²C Interface** | | | | | | | |
| $V_{ADR(H)}$ | ADR0–2 Input High Voltage | | ● | | 0.75 • $V_{CC}$ | 0.9 • $V_{CC}$ | V |
| $V_{ADR(L)}$ | ADR0–2 Input Low Voltage | | ● | 0.1 • $V_{CC}$ | 0.25 • $V_{CC}$ | | V |
| $I_{ADR(IN, L)}$ | ADR0–2 Logic Low Input Current | ADR0–2 = 0V, $V_{CC}$ = 5.5V | ● | –30 | –60 | –80 | µA |
| $I_{ADR(IN, H)}$ | ADR0–2 Logic High Input Current | ADR0–2 = $V_{CC}$ = 5.5V | ● | 30 | 60 | 80 | µA |
| $I_{ADR,FLOAT}$ | ADR0–2 Allowed Input Current | $V_{CC}$ = 2.7V, 5.5V (Note 5) | ● | ±5 | ±13 | | µA |
| $V_{SDAIN,SCLIN(TH)}$ | SDAIN, SCLIN Input Falling Threshold Voltages | $V_{CC}$ = 5.5V | ● | 1.4 | 1.6 | 1.8 | V |
| $V_{SDAIN,SCLIN(HY)}$ | SDAIN, SCLIN Hysteresis | | | | 30 | | mV |
| $I_{SDAIN,SCLIN(OH)}$ | SDAIN, SCLIN Input Current | SCL, SDA = $V_{CC}$ | ● | | | ±5 | µA |
| $C_{IN}$ | SDA, SCL Input Capacitance | (Note 2) | | | 6 | 10 | pF |
| $V_{SDAIN(OL)}$ | SDAIN Output Low Voltage | $I_{SDA}$ = 4mA, $V_{CC}$ = 2.7V | ● | | 0.2 | 0.4 | V |
| **I²C Interface Timing** | | | | | | | |
| $f_{SCL}$ | Maximum SCL Clock Frequency | (Note 2) | | 400 | | | kHz |
| $t_{BUF}$ | Bus Free Time Between Stop/Start Condition | (Note 2) | | | 0.75 | 1.3 | µs |
| $t_{HD, STA}$ | Hold Time After (Repeated) Start Condition | (Note 2) | | | 45 | 100 | ns |
| $t_{SU, STA}$ | Repeated Start Condition Set-Up Time | (Note 2) | | | –30 | 0 | ns |
| $t_{SU, STO}$ | Stop Condition Set-Up Time | (Note 2) | | | –30 | 0 | ns |
| $t_{HD, DATI}$ | Data Hold Time Input | (Note 2) | | | –25 | 0 | ns |
| $t_{HD, DATO}$ | Data Hold Time Output | (Note 2) | | 300 | 600 | 900 | ns |
| $t_{SU, DAT}$ | Data Set-Up Time | (Note 2) | | | 50 | 100 | ns |
| $t_f$ | SCL, SDA Fall Times | (Note 2) | | 20 + 0.1 • $C_{BUS}$ | | 300 | ns |
| $t_{SP}$ | Pulse Width of Spikes Suppressed by the Input Filter | (Note 2) | | 50 | 150 | 250 | ns |

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** Guaranteed by design and not subject to test, unless stated otherwise in the Conditions.

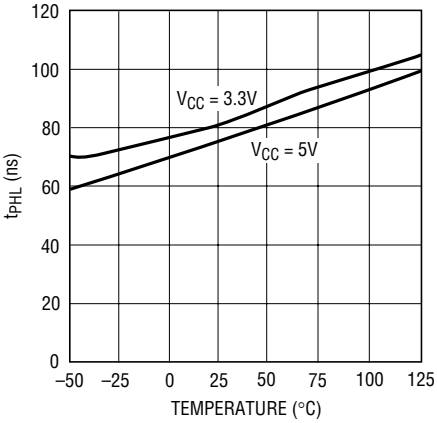
**Note 3:** The boosted pull-up currents are regulated to prevent excessively fast edges for light loads. See the Typical Performance Characteristics for rise time as a function of $V_{CC}$ and parasitic bus capacitance $C_{BUS}$ and for $I_{BOOST}$ as a function of $V_{CC}$ and temperature.

**Note 4:** When a logic low voltage $V_{LOW}$ is forced on one side of the upstream-downstream buffers, the voltage on the other side is regulated to a voltage $V_{LOW2} = V_{LOW} + V_{OS}$ is a positive offset voltage. $V_{OS,DOWN-BUF}$ is the offset voltage when the LTC4305 is driving the upstream pin (e.g., SDAIN) and $V_{OS,DOWN-BUF}$ is the offset voltage when the LTC4305 is driving the downstream pin (e.g., SDA1). See the Typical Performance Characteristics for $V_{OS,UP-BUF}$ and $V_{OS,DOWN-BUF}$ as a function of $V_{CC}$ and bus pull-up current.

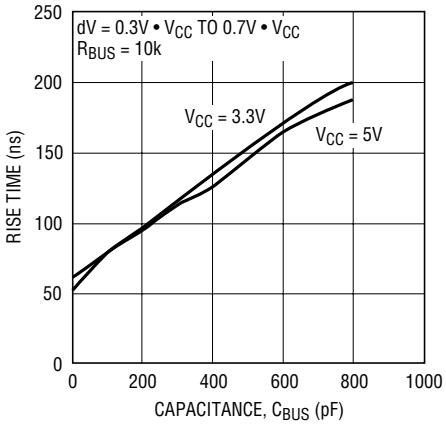
**Note 5:** When floating, the ADR0–ADR2 pins can tolerate pin leakage currents up to $I_{ADR,FLOAT}$ and still convert the address correctly.

## TYPICAL PERFORMANCE CHARACTERISTICS ($T_A$ = 25°C unless otherwise specified.)

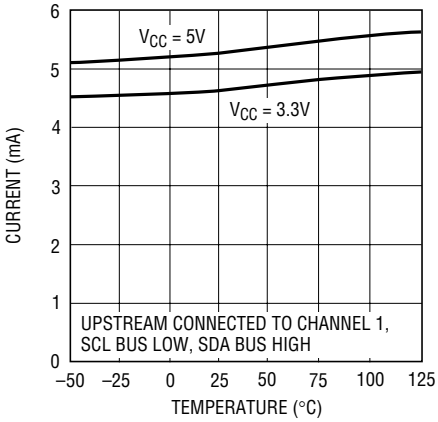
### Buffer Circuitry $t_{PHL}$ vs Temperature



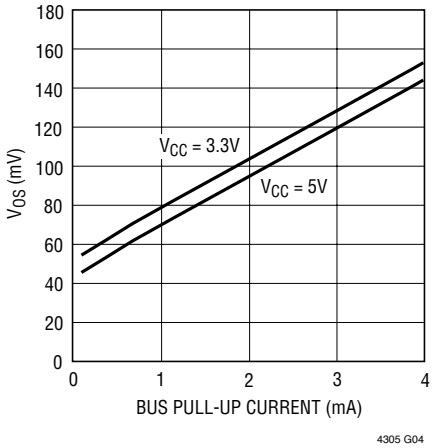

### Rise Time vs $C_{BUS}$ vs $V_{CC}$



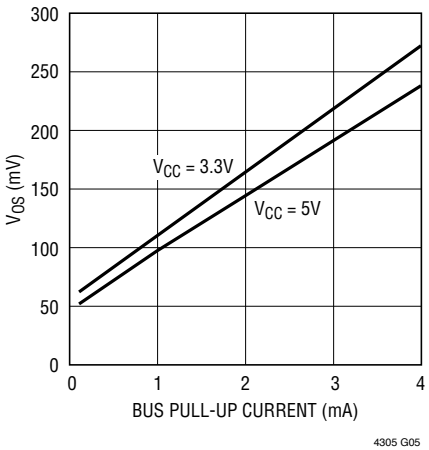

### $I_{CC}$ vs Temperature



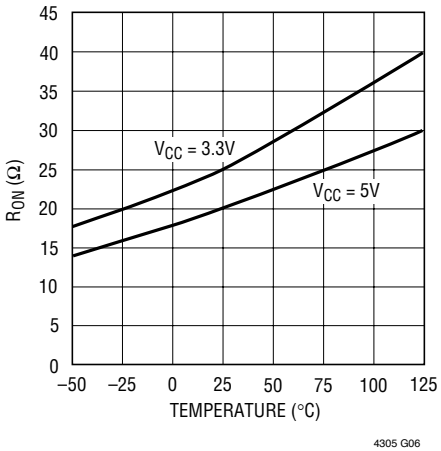

### $V_{OS,UP-BUF}$ vs Bus Pull-Up Current



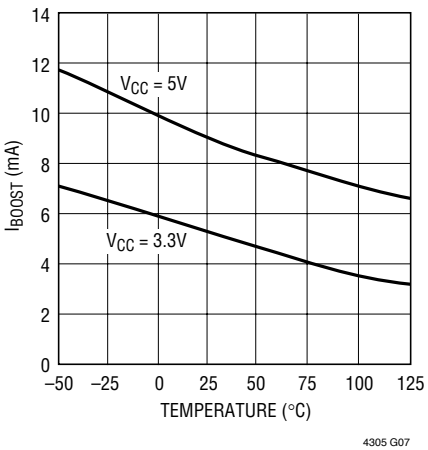

### $V_{OS,DOWN-BUF}$ vs Bus Pull-Up Current




### Downstream $R_{FET}$ on Resistance vs $V_{CC}$ and Temperature




### $I_{BOOST}$ vs Temperature



## PIN FUNCTIONS

**$\overline{\text{ALERT1}}$–$\overline{\text{ALERT2}}$ (Pins 14, 1):** Fault Alert Inputs, Channels 1–2. Devices on each of the two output channels can pull their respective pin low to indicate that a fault has occurred. The LTC4305 then pulls the $\overline{\text{ALERT}}$ low to pass the fault indication on to the host. See the "Operation" section below for the details of how $\overline{\text{ALERT}}$ is set and cleared. Connect unused fault alert inputs to $V_{CC}$.

**$\overline{\text{ALERT}}$ (Pin 2):** Fault Alert Output. An open-drain output that is pulled low when a fault occurs to alert the host controller. The LTC4305 pulls $\overline{\text{ALERT}}$ low when any of the $\overline{\text{ALERT1}}$–$\overline{\text{ALERT2}}$ pins is low; when the two-wire bus is stuck low; or when the Connection Requirement bit of register 2 is low and a master tries to connect to a downstream channel that is low. See the "Operation" section below for the details of how $\overline{\text{ALERT}}$ is set and cleared. The LTC4305 is compatible with the SMBus Alert Response Address protocol. Connect a 10k resistor to a power supply voltage to provide the pull-up. Tie to ground if unused.

**SDAIN (Pin 3):** Serial Bus Data Input and Output. Connect this pin to the SDA line on the master side. An external pull-up resistor or current source is required.

**GND (Pin 4):** Device Ground.

**SCLIN (Pin 5):** Serial Bus Clock Input. Connect this pin to the SCL line on the master side. An external pull-up resistor or current source is required.

**ENABLE (Pin 6):** Digital Interface Enable and Register Reset. Driving ENABLE high enables $I^2C$ communication to the LTC4305. Driving ENABLE low disables $I^2C$ communication to the LTC4305 and resets the registers to their default state as shown in the Operations section. When ENABLE returns high, masters can read and write the LTC4305 again. If unused, tie ENABLE to $V_{CC}$.

**$V_{CC}$ (Pin 7):** Power Supply Voltage. Connect a bypass capacitor of at least 0.01µF directly between $V_{CC}$ and GND for best results.

**ADR0–ADR2 (Pins 8–10):** Three-State Serial Bus Address Inputs. Each pin may be floated, tied to ground, or tied to $V_{CC}$. There are therefore 27 possible addresses. See Table 1 in Applications Information section. When the pins are floated, they can tolerate ±5µA of leakage current and still convert the address correctly.

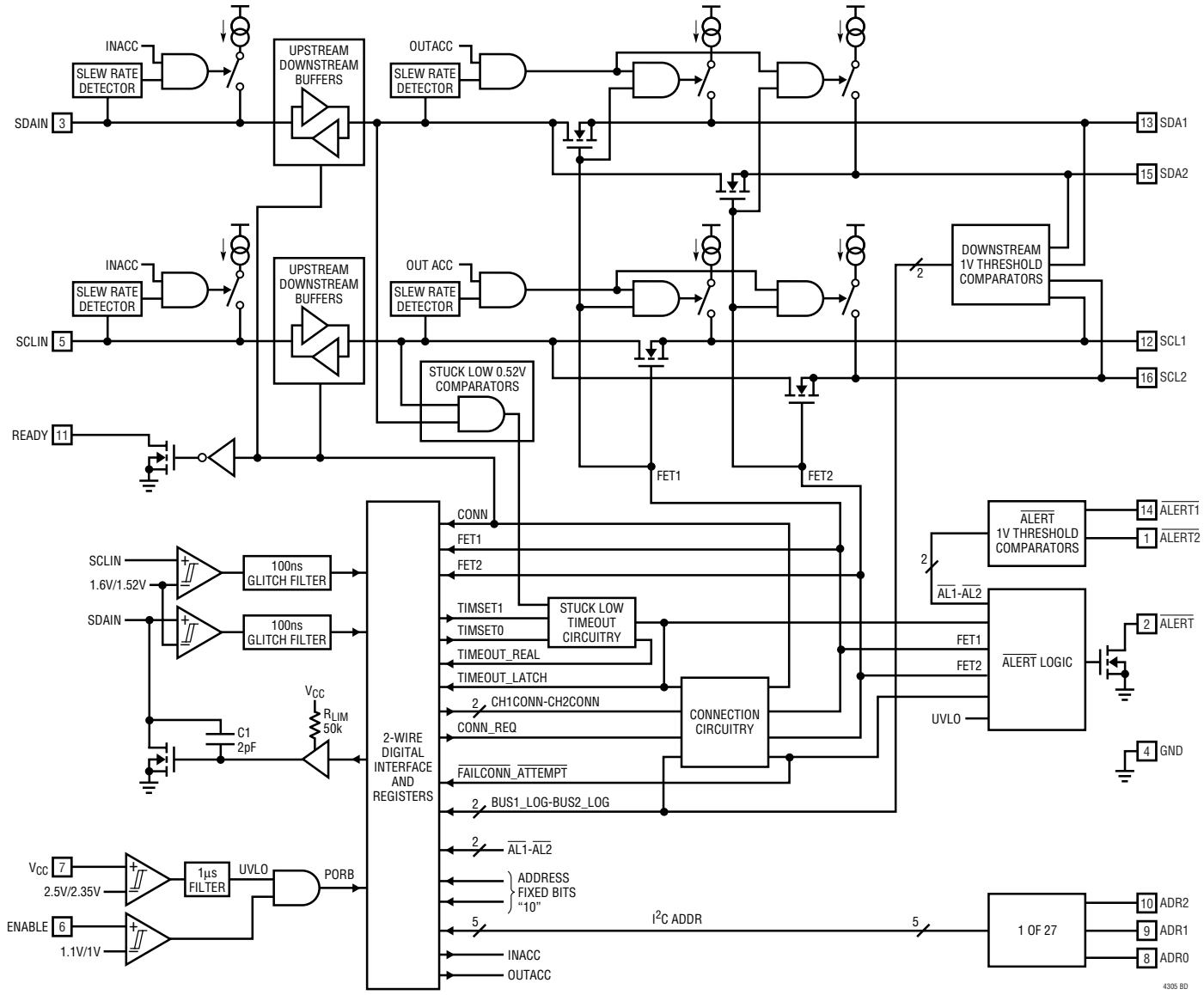
**READY (Pin 11):** Connection Ready Digital Output. An N-channel MOSFET open-drain output transistor that pulls down when none of the downstream channels is connected to the upstream bus and turns off when one or more downstream channels is connected to the upstream bus. Connect a 10k resistor to a power supply voltage to provide the pull-up. Tie to ground if unused.

**SCL1–SCL2 (Pins 12, 16):** Serial Bus Clock Outputs Channels 1–2. Connect pins SCL1–SCL2 to the SCL lines on the downstream channels 1–2, respectively. It is acceptable to float any pin that will never be connected to the upstream bus. Otherwise, an external pull-up resistor or current source is required on each pin.

**SDA1–SDA2 (Pins 13, 15):** Serial Bus Data Output Channels 1–2. Connect pins SDA1–SDA2 to the SDA lines on downstream channels 1–2, respectively. It is acceptable to float any pin that will never be connected to the upstream bus. Otherwise, an external pull-up resistor or current source is required on each pin.

**Exposed Pad (Pin 17, DHD Package Only):** Exposed pad may be left open or connected to device ground.

## BLOCK DIAGRAM



# OPERATION

## Control Register Bit Definitions

### Register 0 (00h)

| BIT | NAME | TYPE* | DESCRIPTION |
|---|---|---|---|
| d7 | Downstream Connected | R | Indicates if upstream bus is connected to any downstream buses<br>0 = upstream bus disconnected from all downstream buses<br>1 = upstream bus connected to one or more downstream buses |
| d6 | $\overline{\text{ALERT1}}$ Logic State | R | Logic state of $\overline{\text{ALERT1}}$ pin, noninverting |
| d5 | $\overline{\text{ALERT2}}$ Logic State | R | Logic state of $\overline{\text{ALERT2}}$ pin, noninverting |
| d4 | Reserved | R | Not Used |
| d3 | Reserved | R | Not Used |
| d2 | $\overline{\text{Failed Connection}}$ Attempt | R | Indicates if an attempt to connect to a downstream bus failed because the "Connection Requirement" bit in Register 2 was low and the downstream bus was low<br>0 = Failed connection attempt occurred<br>1 = No failed attempts at connection occurred |
| d1 | Latched Timeout | R | Latched bit indicating if a timeout has occurred and has not yet been cleared.<br>0 = no latched timeout<br>1 = latched timeout |
| d0 | Timeout Real Time | R | Indicates real-time status of Stuck Low Timeout Circuitry<br>0 = no timeout is occurring<br>1 = timeout is occurring |

**Note: Masters write to Register 0 to reset the fault circuitry after a fault has occurred and been resolved. Because Register 0 is Read-Only, no other functionality is affected.**

* For Type, "R/W" = Read Write, "R" = Read Only

### Register 1 (01h)

| BIT | NAME | TYPE* | DESCRIPTION |
|---|---|---|---|
| d7 | Upstream Accelerators Enable | R/W | Activates upstream rise time accelerator currents<br>0 = upstream rise time accelerator currents inactive (default)<br>1 = upstream rise time accelerator currents active |
| d6 | Downstream Accelerators Enable | R/W | Activates downstream rise time accelerator currents<br>0 = downstream rise time accelerator currents inactive (default)<br>1 = downstream rise time accelerator currents active |
| d5-d0 | Reserved | R | Not Used |

* For Type, "R/W" = Read Write, "R" = Read Only

## OPERATION

**Register 2 (02h)**

| BIT | NAME | TYPE* | DESCRIPTION |
|---|---|---|---|
| d7 | Reserved | R | Not Used |
| d6 | Reserved | R | Not Used |
| d5 | Connection Requirement | R/W | Sets logic requirements for downstream buses to be connected to upstream bus<br>0 = Bus Logic State bits (see register 3) of buses to be connected must be high for connection to occur (default)<br>1 = Connect regardless of downstream logic state |
| d4 | Reserved | R | Not Used |
| d3 | Reserved | R | Not Used |
| d2 | Mass Write Enable | R/W | Enable Mass Write Address using address (1011 110)b<br>0 = Disable Mass Write<br>1 = Enable Mass Write (default) |
| d1 | Timeout Mode Bit 1 | R/W | Stuck Low Timeout Set Bit 1** |
| d0 | Timeout Mode Bit 0 | R/W | Stuck Low Timeout Set Bit 0** |

* For Type, “R/W” = Read Write, “R” = Read Only

**

| TIMSET1 | TIMSET0 | TIMEOUT MODE |
|---|---|---|
| 0 | 0 | Timeout Disabled (Default) |
| 0 | 1 | Timeout After 30ms |
| 1 | 0 | Timeout After 15ms |
| 1 | 1 | Timeout After 7.5ms |

**Register 3 (03h)**

| BIT | NAME | TYPE* | DESCRIPTION |
|---|---|---|---|
| d7 | Bus 1 FET State | R/W | Sets and indicates state of FET switches connected to downstream bus 1<br>0 = switch open (default)<br>1 = switch closed |
| d6 | Bus 2 FET State | R/W | Sets and indicates state of FET switches connected to downstream bus 2<br>0 = switch open (default)<br>1 = switch closed |
| d5 | Reserved | R | Not Used |
| d4 | Reserved | R | Not Used |
| d3 | Bus 1 Logic State | R | Indicates logic state of downstream bus 1; only valid when disconnected from upstream bus†<br>0 = SDA1, SCL1 or both are below 1V<br>1 = SDA1 and SCL1 are both above 1V |
| d2 | Bus 2 Logic State | R | Indicates logic state of downstream bus 2; only valid when disconnected from upstream bus†<br>0 = SDA2, SCL2 or both are below 1V<br>1 = SDA2 and SCL2 are both above 1V |
| d1 | Reserved | R | Not Used |
| d0 | Reserved | R | Not Used |

* For Type, “R/W” = Read Write, “R” = Read Only

† These bits are meant to give the logic state of disconnected downstream buses to the master, so that the master can choose not to connect to a low downstream bus. A given bit is a “don’t care” if its associated downstream bus is already connected to the upstream bus.

## OPERATION

The LTC4305 is a 2-channel 2-wire bus multiplexer/switch with bus buffers to provide capacitive isolation between the upstream bus and downstream buses. Masters on the upstream 2-wire bus (SDAIN and SCLIN) can command the LTC4305 to neither, either or both of the 2 downstream buses. Masters can also program the LTC4305 to disconnect the upstream bus from the downstream buses if the bus is stuck low.

### Undervoltage Lockout (UVLO) and ENABLE Functionality

The LTC4305 contains undervoltage lockout circuitry that maintains all of its SDA, SCL and $\overline{\text{ALERT}}$ pins in high impedance states until the device has sufficient $V_{CC}$ supply voltage to function properly. It also ignores any attempts to communicate with it via the 2-wire buses in this condition. When the ENABLE pin voltage is low (below 0.8V), all control bits are reset to their default high impedance states, and the LTC4305 ignores 2-wire bus commands. However, with ENABLE low, the LTC4305 still monitors the $\overline{\text{ALERT1}}$–$\overline{\text{ALERT2}}$ pin voltages and pulls the $\overline{\text{ALERT}}$ pin low if any of $\overline{\text{ALERT1}}$–$\overline{\text{ALERT2}}$ is low. When ENABLE is high, devices can read from and write to the LTC4305.

### Connection Circuitry

Masters on the upstream SDAIN/SCLIN bus can write to the Bus 1 FET State and Bus 2 FET State bits of register 3 to connect to any combination of downstream channels. By default, the Connection Circuitry shown in the block diagram will only connect to downstream channels whose corresponding Bus Logic State bits in register 3 are high at the moment that it receives the connection command. If the LTC4305 is commanded to connect to multiple channels at once, it will only connect to the channels that are high. This prevents the master on the upstream bus from connnecting to a downstream channel that may be stuck low. Masters can override this feature by setting the Connection Requirement Bit of register 2 high. With this bit high, the LTC4305 executes connection commands without regard to the logic states of the downstream channels.

Upon receiving the connection command, the Connection Circuitry shown in the block diagram will activate the Upstream-Downstream Buffers under two conditions: first, the master must be commanding connection to one or more downstream channels, and second, there must be no stuck low condition (see “Stuck Low Timeout Fault” discussion that follows). If the connection command is successful, the Upstream-Downstream Buffer circuitry passes signals between the upstream bus and the connected downstream buses. The LTC4305 also turns off its N-channel MOSFET open-drain pull-down on the READY pin, so that READY can be pulled high by its external pull-up resistor.

### Upstream-Downstream Buffers

Once the Upstream-Downstream Buffers are activated, the functionality of the SDAIN and any connected downstream SDA pins is identical. A low forced on any connected SDA pin at any time results in all pins being low. **External devices must pull the pin voltages below 0.4V worst-case with respect to the LTC4305’s ground pin to ensure proper operation.** The SDA pins enter a logic high state only when all devices on all connected SDA pins force a high. The same is true for SCLIN and the connected downstream SCL pins. This important feature ensures that clock stretching, clock arbitration and the acknowledge protocol always work, regardless of the how the devices in the system are connected to the LTC4305.

The Upstream-Downstream Buffers provide capacitive isolation between SDAIN/SCLIN and the downstream connected buses. Note that there is no capacitive isolation between connected downstream buses; they are only

## OPERATION

separated by the series combination of their switches' on resistances. While neither, either or both downstream buses may be connected at the same time, logic high levels are corrupted if both downstream buses are active and both the $V_{CC}$ voltage and one downstream bus pull-up voltage are larger than the pull-up supply voltage of the other downstream bus. An example of this issue is shown in Figure 1. During logic highs, DC current flows from $V_{BUS1}$ through the series combination of R1, N1, N2 and R2 and into $V_{BUS2}$, causing the SDA1 voltage to drop and current to be sourced into $V_{BUS2}$. To avoid this problem, do not activate bus 1 when bus 2 is active.

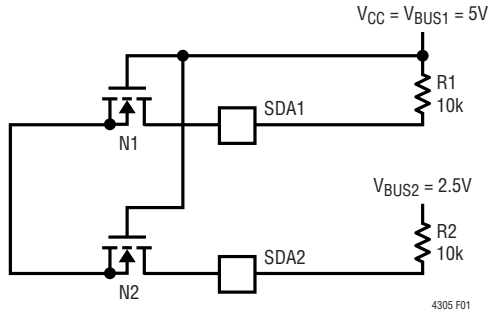



**Figure 1. Example of Unacceptable Level Shifting**

### Rise Time Accelerators

The Upstream Accelerators Enable and Downstream Accelerators Enable bits of register 1 activate the upstream and downstream rise time accelerators, respectively. When activated, the accelerators turn on in a controlled manner and source current into the pins during positive bus transitions.

When no downstream buses are connected, an upstream accelerator turns on when its pin voltage exceeds 0.8V and is rising at a minimum slew rate of 0.8V/µs. When one or more downstream buses are connected, the accelerator on a given pin turns on when these conditions are met: first, the pin's voltage is rising at a minimum slew rate of 0.8V/µs; second, the voltages on both the upstream bus and the connected downstream buses exceed 0.8V.

Note that a downstream bus must be connected to the upstream bus in order for its rise time accelerator current to be active. See the Applications Section for choosing a bus pull-up resistor value to ensure that the rise time accelerator switches turn on. **Do not activate boost currents on a bus whose pull-up supply voltage $V_{BUS} < V_{CC}$. Doing so would cause the boost currents to source current from $V_{CC}$ into the $V_{BUS}$ supply during rising edges.**

### Downstream Bus Connection Fault

By default, the LTC4305 will only connect to downstream buses whose SDA and SCL pins are both high (above 1V) at the moment that it receives the connection command. In this case, the LTC4305 sets the Failed Connection Attempt bit of register 0 low and pulls the ALERT low when the master tries to connect to a low downstream bus. Note that users can write a high to the Connection Requirement bit of register 2 to program the LTC4305 to connect to downstream buses regardless of their logic state at the moment of connection. In this case, the Downstream Channel Connection Fault never occurs.

### Stuck Low Timeout Fault

The Stuck Low Timeout Circuitry monitors the two common internal nodes of the downstream SDA and SCL switches and runs a timer whenever either of the internal node voltages is below 0.52V. The timer is reset whenever both internal node voltages are above 0.6V. If the timer ever reaches the time programmed by Timeout Mode Bits 1 and 0 of register 2, the LTC4305 pulls ALERT low and

## OPERATION

disconnects the downstream buses from the upstream bus by de-biasing the Upstream-Downstream Buffers. Note that the downstream switches remain in their existing state. The Timeout Real Time bit of register 0 indicates the real-time status of the stuck low situation. The Latched Timeout Bit of register 0 is a latched bit that is set high when a timeout occurs.

### External Faults on the Downstream Channels

When a slave on downstream channel 1 pulls the $\overline{\text{ALERT1}}$ pin below 1V, the LTC4305 passes this information to master on the upstream bus by pulling the $\overline{\text{ALERT}}$ pin low. The functionality is the same for the slaves on downstream channel 2 and the $\overline{\text{ALERT2}}$ pin. Each channel has its own dedicated fault bit in Register 0, so that masters can read Register 0 to determine which channels have faults.

### $\overline{\text{ALERT}}$ Functionality and Fault Resolution

When a fault occurs, the LTC4305 pulls the $\overline{\text{ALERT}}$ pin low, as described previously. The procedure for resolving faults depends on the type of fault. If a master on the upstream bus is communicating with devices on a downstream bus via the upstream-downstream buffer circuitry—channel 1, for example—and a device on this bus pulls the $\overline{\text{ALERT1}}$ pin low, the LTC4305 acts transparently, and the master communicates directly with the device that caused the fault via the Upstream-Downstream Buffer circuitry to resolve the fault.

In all other cases, the LTC4305 communicates with the master to resolve the fault. After the master broadcasts the Alert Response Address (ARA), the LTC4305 will respond with its address on the SDAIN line and release the $\overline{\text{ALERT}}$ pin. The $\overline{\text{ALERT}}$ line will also be released if the LTC4305 is addressed by the master.

The $\overline{\text{ALERT}}$ signal will not be pulled low again until a different type of fault has occurred or the original fault is cleared and has occurred again. Figure 2 shows the details of how the fault latches and $\overline{\text{ALERT}}$ pin are set and reset. The Downstream Bus Connection Fault and faults that

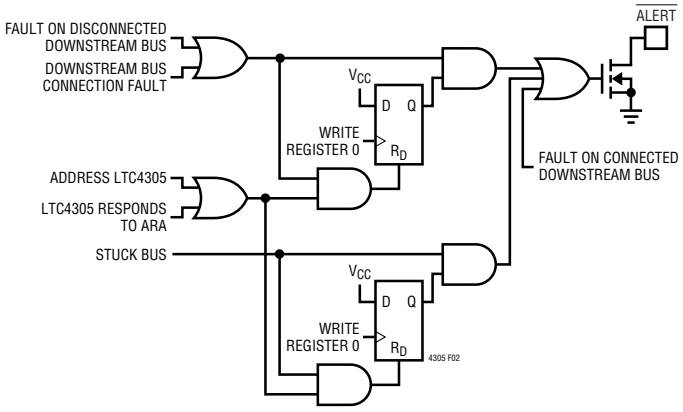



**Figure 2. Setting and Resetting the $\overline{\text{ALERT}}$ Pin**

occur on unconnected downstream buses are grouped together and generate a single signal to drive $\overline{\text{ALERT}}$. The Stuck Low Timeout Fault has its own dedicated pathway to $\overline{\text{ALERT}}$; however, once a stuck low occurs, another one will not occur until the first one is cleared. For these reasons, once the master has established the LTC4305 as the source of the fault, it should read register 0 to determine the specific problem, take action to solve the problem, and clear the fault promptly. All faults are cleared by writing a dummy databyte to register 0, which is a read-only register.

For example, assume that a fault occurs, the master sends out the ARA, and the LTC4305 successfully writes its address onto SDAIN and releases its $\overline{\text{ALERT}}$ pin. The master reads register 0 and learns that the $\overline{\text{ALERT2}}$ logic state bit is low. The master now knows that a device on downstream bus 2 has a fault and writes to register 3 to connect to bus 2, so that it can communicate with the source of the fault. At this point, the master writes to register 0 to clear the fault.

### I²C Device Addressing

Twenty-seven distinct bus addresses are configurable using the three state ADR0, ADR1 and ADR2 pins. Table 1 shows the correspondence between pin states and addresses. Note that address bits a6 and a5 are internally configured to 1 and 0, respectively. In addition, the LTC4305 responds to two special addresses. Address (1011 110) is a mass write used to write all LTC4305's,

## OPERATION

regardless of their individual address settings. The mass write can be masked by setting the mass write enable bit of register 2 to zero. Address (0001 100) is the SMBus Alert Response Address. Figure 3 shows data transfer over a 2-wire bus.

### Supported Commands

Users must write to the LTC4305 using the SMBus Write Byte protocol and read from it using the Read Byte protocol. During fault resolution, the LTC4305 also supports the Alert Response Address protocol. The formats for these protocols are shown in Figure 4. Users must follow the Write Byte protocol exactly to write to the LTC4305; if a Repeated Start Bit is issued before a Stop Bit, the LTC4305 ignores the attempted write, and its control bits remain in their preexisting state. When users follow the WriteByte protocol exactly, the new data contained in the Data Byte is written into the register selected by r1 and r0 on the Stop Bit.

### Glitch Filters

The LTC4305 provides glitch filters on the SDAIN and SCLIN pins as required by the I²C Fast Mode (400kHz) Specification. The filters prevent signals of up to 50ns (minimum) time duration and rail-to-rail voltage magnitude from passing into the two-wire bus digital interface circuitry.

### Fall Time Control

Per the I²C Fast Mode (400kHz) Specification, the two-wire bus digital interface circuitry provides fall time control when forcing logic lows onto the SDAIN bus. The fall time always meets the limits:

$$(20 + 0.1 \bullet C_B) < t_f < 300ns$$

where $t_f$ is the fall time in ns and $C_B$ is the equivalent bus capacitance in pF. Whenever the upstream-downstream buffer circuitry is active, its output signal will meet the fall time requirements, provided that its input signal meets the fall time requirements.

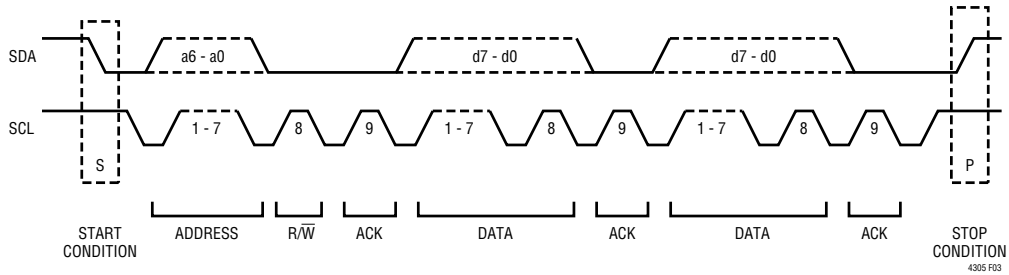



**Figure 3. Data Transfer Over I²C/SMBus**

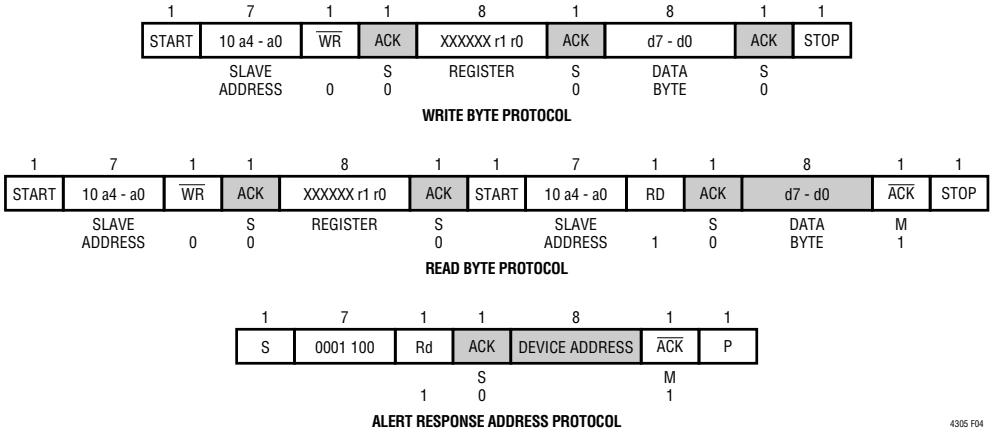



**Figure 4. Protocols Accepted by LTC4305**

## OPERATION

**Table 1. LTC4305 I²C Device Addressing**

| DESCRIPTION | HEX DEVICE ADDRESS | BINARY DEVICE ADDRESS | | | | | | | | LTC4305 ADDRESS PINS | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | h | a6 | a5 | a4 | a3 | a2 | a1 | a0 | R/$\overline{W}$ | ADR2 | ADR1 | ADR0 |
| Mass Write | BC | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | X | X | X |
| Alert Response | 19 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | X | X | X |
| 0 | 80 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | X | L | NC | L |
| 1 | 82 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | X | L | H | NC |
| 2 | 84 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | X | L | NC | NC |
| 3 | 86 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | X | L | NC | H |
| 4 | 88 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | X | L | L | L |
| 5 | 8A | 1 | 0 | 0 | 0 | 1 | 0 | 1 | X | L | H | H |
| 6 | 8C | 1 | 0 | 0 | 0 | 1 | 1 | 0 | X | L | L | NC |
| 7 | 8E | 1 | 0 | 0 | 0 | 1 | 1 | 1 | X | L | L | H |
| 8 | 90 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | X | NC | NC | L |
| 9 | 92 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | X | NC | H | NC |
| 10 | 94 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | X | NC | NC | NC |
| 11 | 96 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | X | NC | NC | H |
| 12 | 98 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | X | NC | L | L |
| 13 | 9A | 1 | 0 | 0 | 1 | 1 | 0 | 1 | X | NC | H | H |
| 14 | 9C | 1 | 0 | 0 | 1 | 1 | 1 | 0 | X | NC | L | NC |
| 15 | 9E | 1 | 0 | 0 | 1 | 1 | 1 | 1 | X | NC | L | H |
| 16 | A0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | X | H | NC | L |
| 17 | A2 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | X | H | H | NC |
| 18 | A4 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | X | H | NC | NC |
| 19 | A6 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | X | H | NC | H |
| 20 | A8 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | X | H | L | L |
| 21 | AA | 1 | 0 | 1 | 0 | 1 | 0 | 1 | X | H | H | H |
| 22 | AC | 1 | 0 | 1 | 0 | 1 | 1 | 0 | X | H | L | NC |
| 23 | AE | 1 | 0 | 1 | 0 | 1 | 1 | 1 | X | H | L | H |
| 24 | B0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | X | H | H | L |
| 25 | B2 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | X | L | H | L |
| 26 | B4 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | X | NC | H | L |

## APPLICATIONS INFORMATION

### Design Example

A typical LTC4305 application circuit is shown in Figure 5. The circuit illustrates the level-shifting, multiplexer/switch and capacitance buffering features of the LTC4305. In this application, the LTC4305 $V_{CC}$ voltage and downstream bus 1 are powered from 3.3V, downstream bus 2 is powered from 5V, and the upstream bus is powered from 2.5V. The following sections describe a methodology for choosing the external components in Figure 5.

### SDA, SCL Pull-Up Resistor Selection

The pull-up resistors on the SDA and SCL pins must be strong enough to provide a minimum of 100µA pull-up current, per the SMBus Specification. In most systems, the required minimum strength of the pull-up resistors is determined by the minimum slew requirement to guarantee that the LTC4305's rise time accelerators are activated during rising edges. At the same time, the pull-up value should be kept low to maximize the logic low noise margin and minimize the offset voltage of the Upstream-Downstream Buffer circuitry. The LTC4305 is designed to function for a maximum DC pull-up current of 4mA. If multiple downstream channels are active at the same time, this means that the sum total of the pull-up currents from these channels must be less than 4mA. At supply voltages of 2.7V and 5.5V, pull-up resistor values of 10k work well for capacitive loads up to 215pF and 420pF, respectively.

For larger bus capacitances, refer to equation (1) below. The LTC4305 works with capacitive loads up to 2nF.

Assume in Figure 5 that the total parasitic bus capacitance on SDA1 due to trace and device capacitance is 100pF. To ensure that the boost currents are active during rising edges, the pull-up resistor must be strong enough to cause the SDA1 pin voltage to rise at a rate of 0.8V/µs as the pin voltage is rising above 0.8V. The equation is:

$$R_{PULL-UP,MAX}\,[k\Omega] = \frac{\left\{(V_{BUSMIN} - 0.8V) \bullet 1250\left[\frac{ns}{V}\right]\right\}}{C_{BUS}\,[pF]} \quad (1)$$

where $V_{BUSMIN}$ is the minimum operating pull-up supply voltage, and $C_{BUS}$ is the bus parasitic capacitance. In our example, $V_{BUS1} = V_{CC} = 3.3V$, and assuming ±10% supply tolerance, $V_{BUS1MIN}$ = 2.97V. With $C_{BUS}$ = 100pF, $R_{PULL-UP,MAX}$ = 27.1kΩ. Therefore, we must choose a pull-up resistor smaller (i.e., stronger pull-up) than 27.1k, so a 10k resistor works fine.

### $\overline{\text{ALERT}}$ and READY Component Selection

The pull-up resistors on the $\overline{\text{ALERT}}$ and READY pins must provide a maximum pull-up current of 3mA, so that the LTC4305 is capable of holding the pins at logic low voltages below 0.4V.

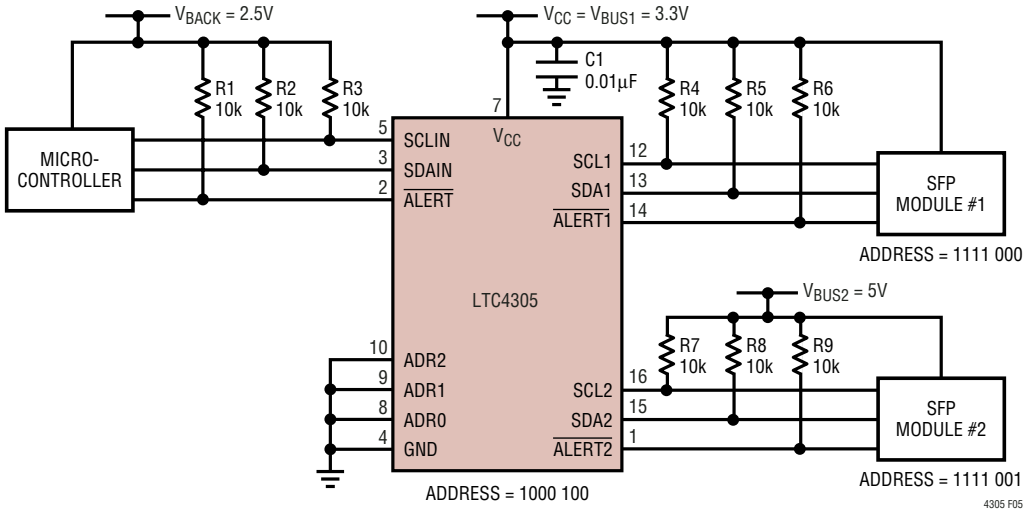



**Figure 5. A Level Shifting Circuit**

## APPLICATIONS INFORMATION

### Level Shifting Considerations

In Figure 5, the LTC4305 $V_{CC}$ voltage is less than or equal to both of the downstream bus pull-up voltages, so both downstream buses can be active at the same time. Likewise, the rise time accelerators can be turned on for the downstream buses, but must never be activated on SCLIN and SDAIN, because doing so would result in significant current flow from $V_{CC}$ to $V_{BACK}$ during rising edges.

### Other Application Circuits

Figure 6 illustrates how the LTC4305 can be used to expand the number of devices in a system by using nested addressing. Each I/O card contains a temperature sensor having device address 1001 000. If both I/O cards were plugged directly into the backplane, the two sensors would require two unique addresses. However, if masters use the LTC4305 in multiplexer mode, where only one downstream channel is connected at a time, then each I/O card can have a device with address 1001 000 and no problems will occur.

Figures 7 and 8 show two different methods for hot-swapping I/O cards onto a live two-wire bus using the LTC4305. The circuitry of Figure 7 consists of an LTC4305 residing on the edge of an I/O card having two separate downstream buses. Connect a 200k resistor to ground from the ENABLE pin and make the ENABLE pin the shortest pin on the card connector, so that the ENABLE pin remains at a constant logic low while all other pins are connecting. This ensures that the LTC4305 remains in its default high impedance state and ignores connection transients on its SDAIN and SCLIN pins until they have established solid contact with the backplane 2-wire bus. In addition, make sure that the $\overline{\text{ALERT}}$ card connector pin is shorter than the $V_{CC}$ pin, so that $V_{CC}$ establishes solid contact with the I/O card pull-up supply pin and powers the pull-up resistors on $\overline{\text{ALERT1}}$–$\overline{\text{ALERT2}}$ before $\overline{\text{ALERT}}$ makes contact.

Figure 8 illustrates an alternate SDA and SCL hot-swapping technique, where the LTC4305 is located on the backplane and an I/O card plugs into downstream channel 2. Before plugging and unplugging the I/O card, make sure that channel 2's downstream switch is open, so that it does not disturb any 2-wire transaction that may be occurring at the moment of connection/disconnection. Note that pull-up resistor R10 on $\overline{\text{ALERT2}}$ should be located on the backplane and not the I/O card to ensure proper operation of the LTC4305 when the I/O card is not present. The pull-up resistors on SCL2 and SDA2—R8 and R9, respectively—may be located on the I/O card, provided that downstream bus 2 is never activated when the I/O card is not present. Otherwise, locate R8 and R9 on the backplane.

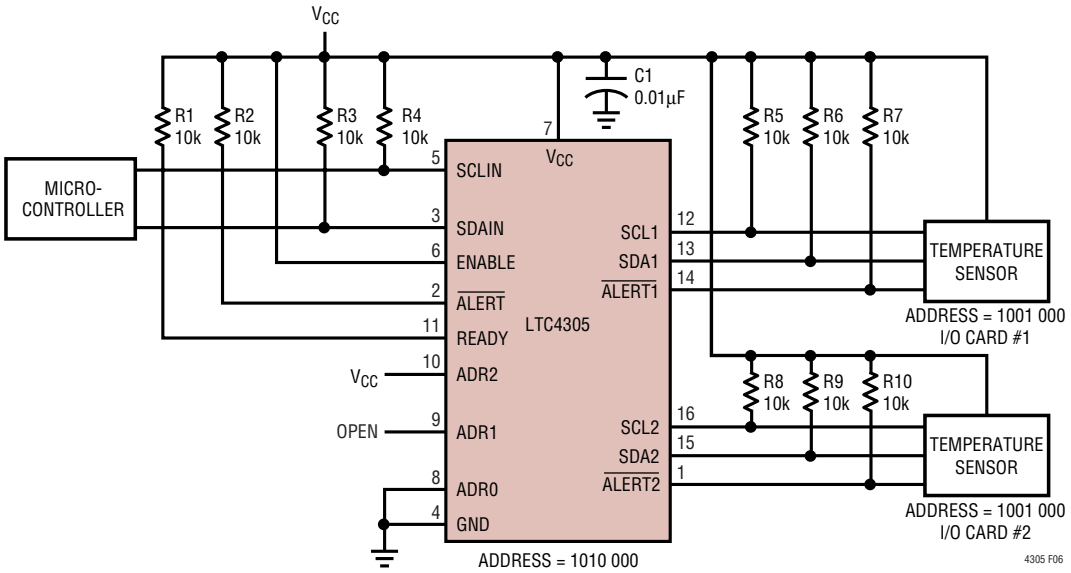



**Figure 6. Nested Addressing Application**

## APPLICATIONS INFORMATION

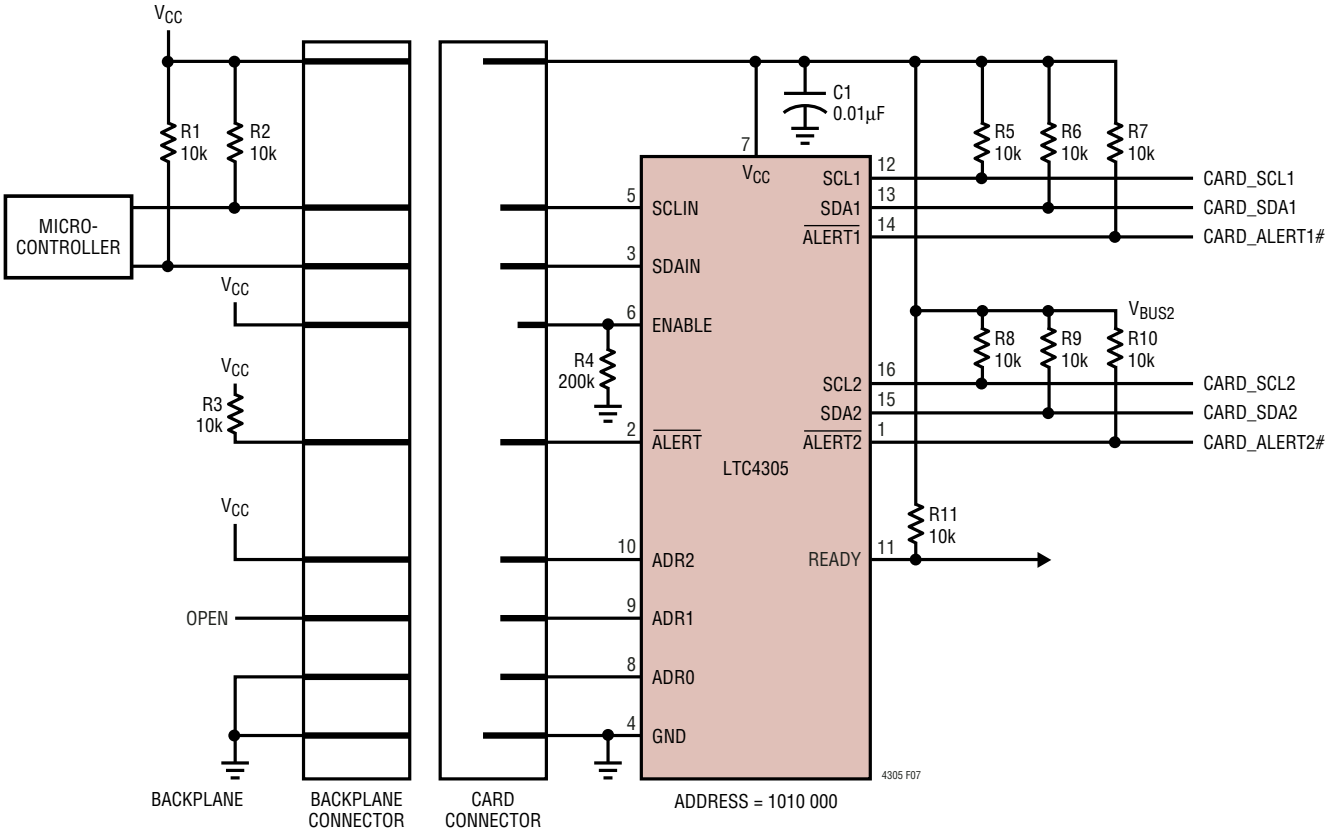
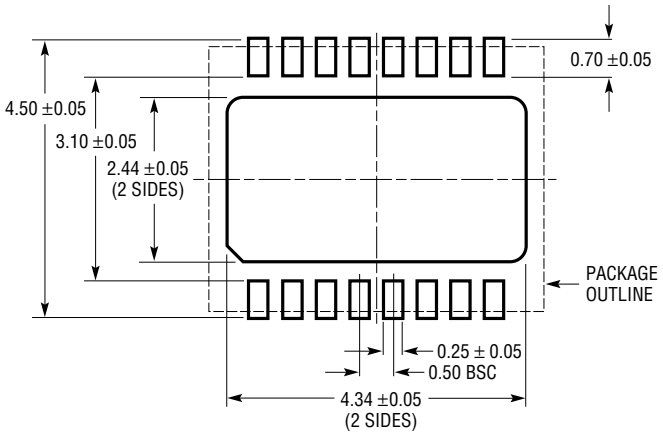


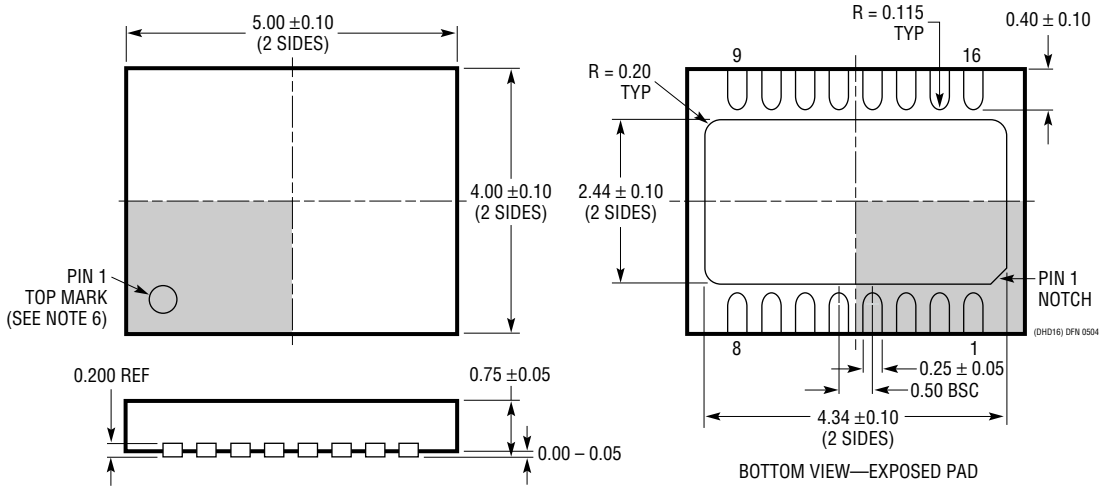

**Figure 7. Hot-Swapping Application**

# PACKAGE DESCRIPTION

**DHD Package**
**16-Lead Plastic DFN (4mm x 5mm)**
(Reference LTC DWG # 05-08-1707)




**RECOMMENDED** SOLDER PAD PITCH AND DIMENSIONS

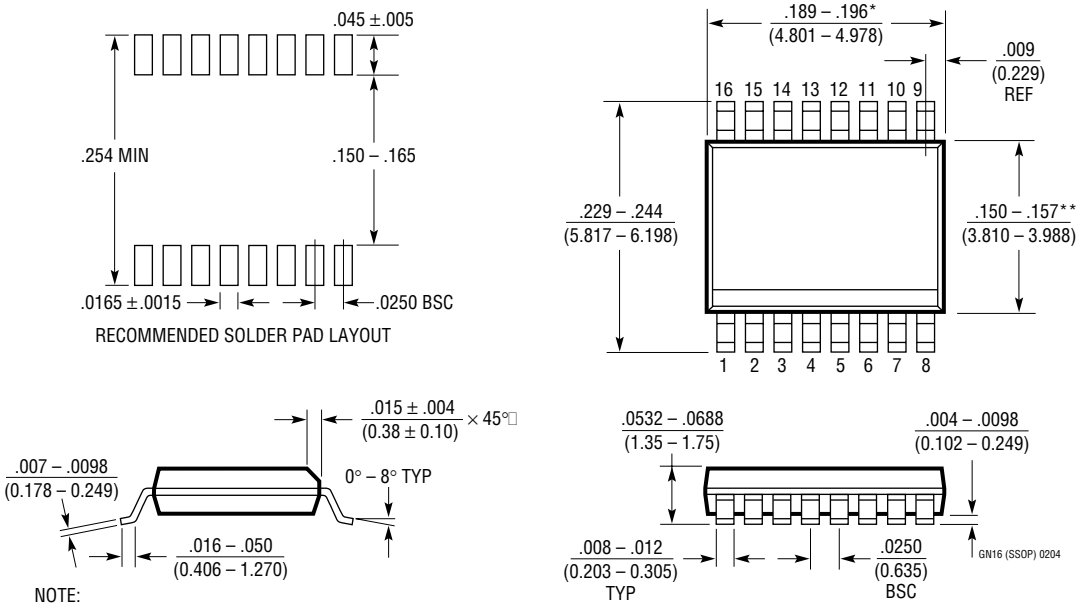



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJGD-2) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

# PACKAGE DESCRIPTION

**GN Package**
**16-Lead Narrow Plastic SSOP**
(Reference LTC DWG # 05-08-1641)




NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

## TYPICAL APPLICATION

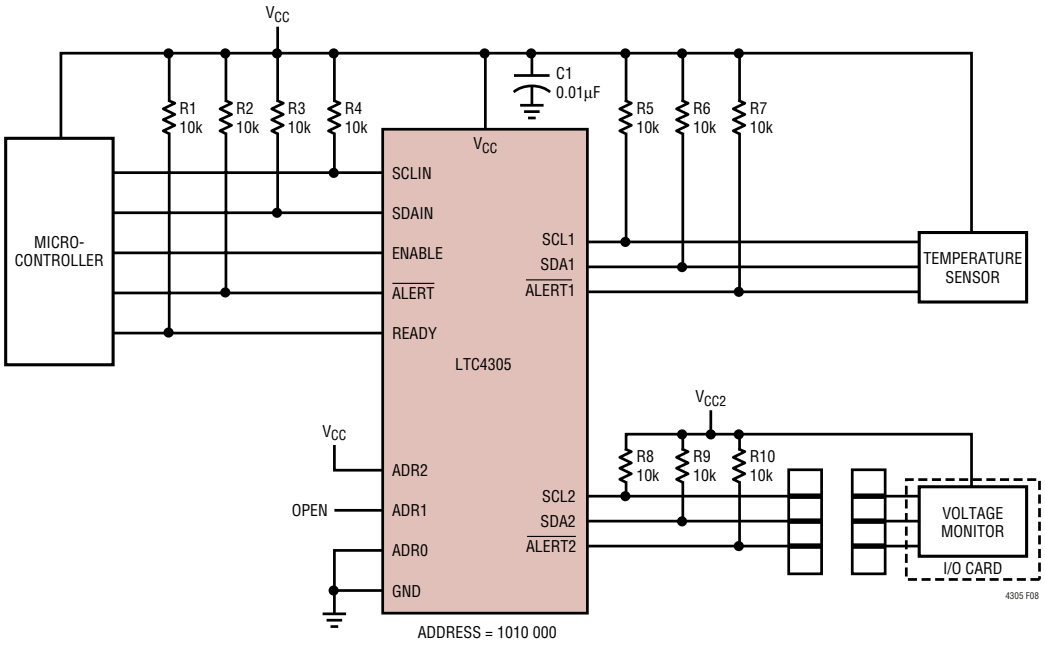



**Figure 8. Alternate Hot-Swapping Application**

## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC1380/LTC1393 | Single-Ended 8-Channel/Differential 4-Channel Analog Mux with SMBus Interface | Low $R_{ON}$: 35Ω Single-Ended/70Ω Differential, Expandable to 32 Single or 16 Differential Channels |
| LTC1427-50 | Micropower, 10-Bit Current Output DAC with SMBus Interface | Precision 50µA ± 2.5% Tolerance Over Temperature, 4 Selectable SMBus Addresses, DAC Powers up at Zero or Midscale |
| LTC1623 | Dual High Side Switch Controller with SMBus Interface | 8 Selectable Addresses/16-Channel Capability |
| LTC1663 | SMBus Interface 10-Bit Rail-to-Rail Micropower DAC | DNL < 0.75LSB Max, 5-Lead SOT-23 Package |
| LTC1694/LTC1694-1 | SMBus Accelerator | Improved SMBus/$I^2C$ Rise-Time, Ensures Data Integrity with Multiple SMBus/$I^2C$ Devices |
| LT1786F | SMBus Controlled CCFL Switching Regulator | 1.25A, 200kHz, Floating or Grounded Lamp Configurations |
| LTC1695 | SMBus/$I^2C$ Fan Speed Controller in ThinSOT™ | 0.75Ω PMOS 180mA Regulator, 6-Bit DAC |
| LTC1840 | Dual $I^2C$ Fan Speed Controller | Two 100µA 8-Bit DACs, Two Tach Inputs, Four GPIO |
| LTC4300A-1/LTC4300A-2 | Hot Swappable 2-Wire Bus Buffer | Isolates Backplane and Card Capacitances |
| LTC4300A-3 | Hot Swappable 2-Wire Bus Buffer | Provides Level Shifting and Enable Functions |
| LTC4301 | Supply Independent Hot Swappable 2-Wire Bus Buffer | Supply Independent |
| LTC4301L | Hot Swappable 2-Wire Bus Buffer with Low Voltage Level Translation | Allows Bus Pull-Up Voltages as Low as 1V on SDAIN and SCLIN |
| LTC4302-1/LTC4302-2 | Addressable 2-Wire Bus Buffer | Address Expansion, GPIO, Software Controlled |
| LTC4303/LTC4304 | Hot Swappable 2-Wire Bus Buffer with Stuck Bus Recovery | Provides Automatic Clocking to Free Stuck $I^2C$ Busses |
| LTC4306 | 4-Channel 2-Wire Multiplexer with Capacitance Buffering | 4 Selectable Downstream Buses, Stuck Bus Disconnect, Rise Time Accelerators, Fault Reporting, ±10kV HBM ESD Tolerance |

ThinSOT is a trademark of Linear Technology Corporation.





Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

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