Synchronous Step-Down DC/DC Controller

FEATURES

- **High Efficiency: Up to 95%**
- **Constant Frequency 550kHz Operation**
- **V_{IN} from 2.65V to 8.5V**
- **V_{OUT} from 0.8V to V_{IN}**
- **OPTI-LOOP® Compensation Minimizes C_{OUT}**
- **Synchronizable up to 750kHz**
- **Selectable Burst Mode Operation**
- **Low Quiescent Current: 80µA**
- Low Dropout Operation: 100% Duty Cycle
- Secondary Winding Regulation
- Soft-Start
- Current Mode Operation for Excellent Line and Load Transient Response
- Low Shutdown I_Q = 10µA
- ±1.5% Reference Accuracy
- Precision 2.5V Undervoltage Lockout
- Available in 10-Lead MSOP

APPLICATIONS

- Cellular Telephones
- RF PA Supplies
- Portable Instruments
- Wireless MODEMS
- Distributed Power Systems
- Notebook and Palm Top Computers, PDAs
- Single and Dual Cell Lithium-Ion Powered Devices

DESCRIPTION

The LTC®1773 is a current mode synchronous buck regulator controller that drives external complementary power MOSFETs using a fixed frequency architecture. The operating supply range is from 2.65V to 8.5V, making it suitable for 1- or 2-cell lithium-ion battery powered applications. Burst Mode® operation provides high efficiency at low load currents. 100% duty cycle provides low dropout operation which extends operating time in battery-operated systems.

The operating frequency is internally set at 550kHz, allowing the use of small surface mount inductors. For switching-noise sensitive applications, it can be synchronized up to 750kHz. Peak current limit is user programmable with an external high side sense resistor. A SYNC/FCB control pin guarantees regulation of secondary windings regardless of load on the main output by forcing continuous operation. Burst Mode operation is inhibited during synchronization or when the SYNC/FCB pin is pulled low to reduce noise and RF interference. Soft-start is provided by an external capacitor.

Synchronous rectification increases efficiency and eliminates the need for a Schottky diode, saving components and board space. The LTC1773 comes in a 10-lead MSOP package.

TYPICAL APPLICATION

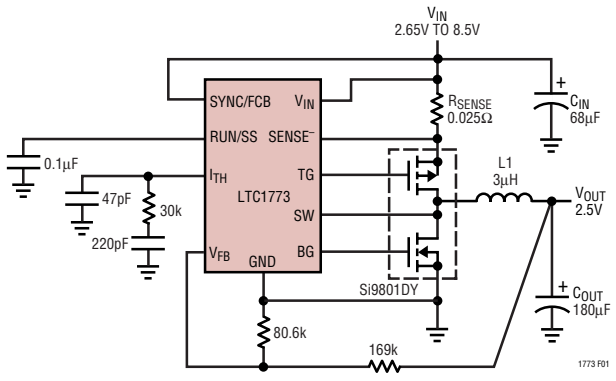
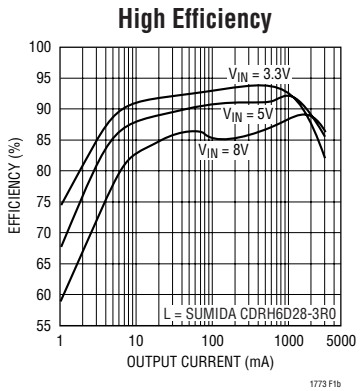


Figure 1. Step-Down Converter

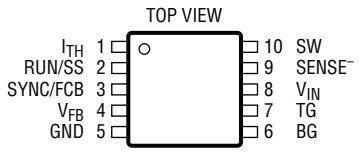


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage ..... –0.3V to 10.0V
I_{TH} Voltage ..... –0.3V to 2.5V
RUN/SS, V_{FB}, SENSE$^-$ Voltages ..... –0.3V to V_{IN}
SYNC/FCB Voltage ..... –0.3V to V_{IN}
BG, TG Voltages ..... –0.3V to V_{IN}
SW Voltage ..... –5V to 11V
Operating Ambient Temperature Range
(Note 2) ..... –40°C to 85°C
Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



MS PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 120°C/W

ORDER PART NUMBER
LTC1773EMS
MS PART MARKING
LTMV

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, T_A = 25°C. V_{IN} = 5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{VFB}	Feedback Current	(Note 4)			20	60	nA
V_{FB}	Regulated Feedback Voltage	(Note 4)	●	0.788	0.80	0.812	V
ΔV_{OVL}	ΔOutput Overvoltage Lockout	$\Delta V_{OVL} = V_{OVL} - V_{FB}$		40	60	80	mV
ΔV_{FB}	Reference Voltage Line Regulation	V_{IN} = 2.7V to 8.5V (Note 4)			0.002	0.02	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	I_{TH} at 1.0V (Note 4)			0.2	0.8	%
		I_{TH} at 0.6V (Note 4)			–0.2	–0.8	%
I_S	Input DC Bias Current Normal Mode	(Note 5) V_{IN} = 5V, V_{ITH} = OPEN, $V_{SYNC/MODE}$ = OPEN			400	600	µA
	Burst Mode Operation	V_{ITH} = 0V, V_{IN} = 5V, $V_{SYNC/MODE}$ = OPEN			80		µA
	Shutdown	$V_{RUN/SS}$ = 0V, 2.7V < V_{IN} < 8.5V			10	30	µA
	Shutdown	$V_{RUN/SS}$ = 0V, V_{IN} < 2.4V			2	5	µA
$V_{RUN/SS}$	RUN/SS Threshold			0.4	0.7	1.0	V
$I_{RUN/SS}$	Soft-Start Current Source	$V_{RUN/SS}$ = 0V		0.75	1.5	2.5	µA
$V_{SYNC/FCB}$	Auxiliary Feedback Threshold	$V_{SYNC/FCB}$ Ramping Negative		0.76	0.8	0.84	V
$I_{SYNC/FCB}$	SYNC/FCB Pull-Up Current	$V_{SYNC/FCB}$ = 0V		0.1	0.4	1.0	µA
f_{OSC}	Oscillator Frequency	V_{FB} = 0.8V		500	550	600	kHz
		V_{FB} = 0V			55		kHz
V_{UVLO}	Undervoltage Lockout	V_{IN} Ramping Down from 3V	●	2.35	2.5	2.65	V
		V_{IN} Ramping Up from 0V	●		2.65	2.8	V
$\Delta V_{SENSE(MAX)}$		Maximum Current Sense Voltage	●	85	100	115	mV
TG t_r	Top Gate Drive Rise Time	C_{LOAD} = 3000pF (Note 6)			45	160	ns
TG t_f	Top Gate Drive Fall Time	C_{LOAD} = 3000pF (Note 6)			48	150	ns
BG t_r	Bottom Gate Drive Rise Time	C_{LOAD} = 3000pF (Note 6)			80	180	ns
BG t_f	Bottom Gate Drive Fall Time	C_{LOAD} = 3000pF (Note 6)			45	150	ns

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC1773 is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

LTC1773: $T_J = T_A + (P_D \bullet 120°C/W)$

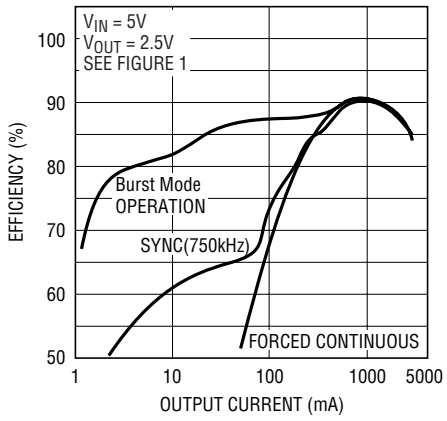
Note 4: The LTC1773 is tested in a feedback loop which servos V_{FB} to the balance point for the error amplifier (V_{ITH} = 0.8V)

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

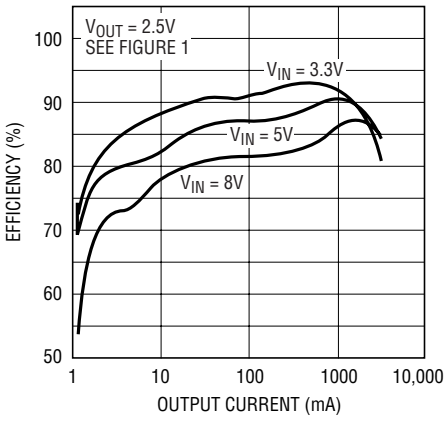
Note 6: Rise and fall times are measured using 10% and 90% levels.

TYPICAL PERFORMANCE CHARACTERISTICS

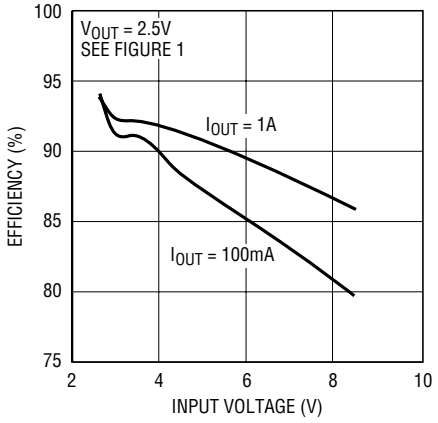
Efficiency vs Load Current



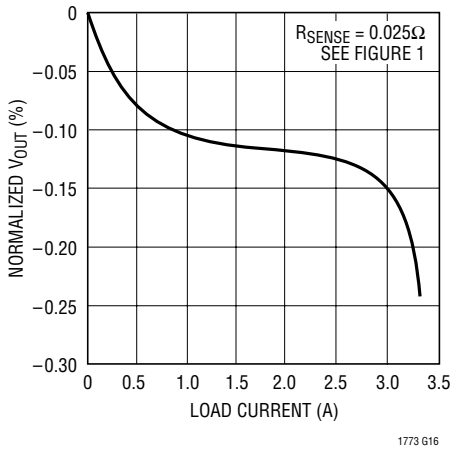
Efficiency vs Load Current



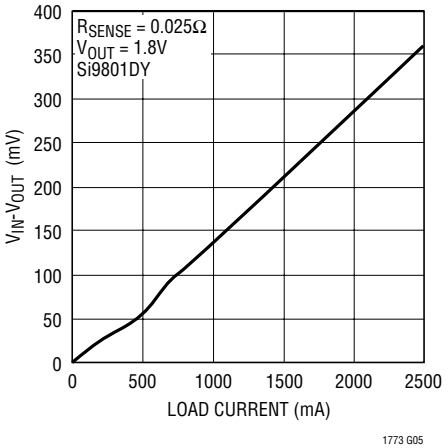
Efficiency vs Input Voltage



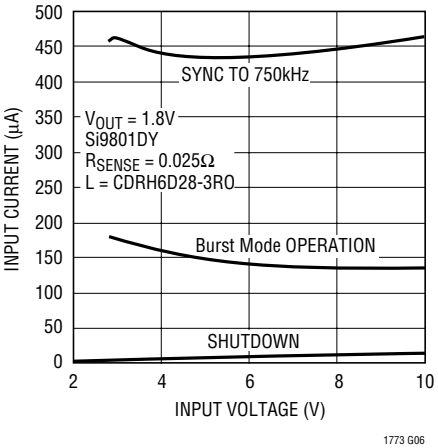
Load Regulation



V_{IN}-V_{OUT} Dropout Voltage vs Load Current

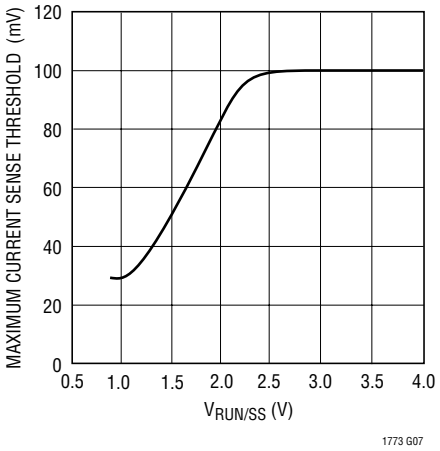


Input and Shutdown Currents vs Input Voltage

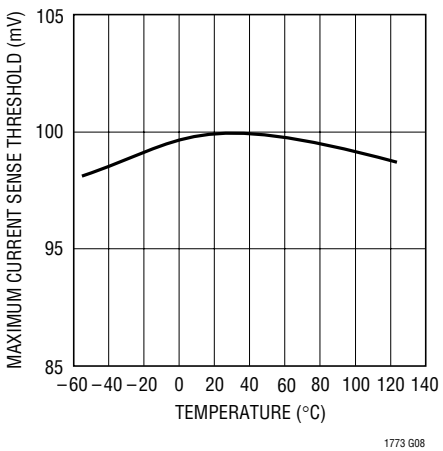


TYPICAL PERFORMANCE CHARACTERISTICS

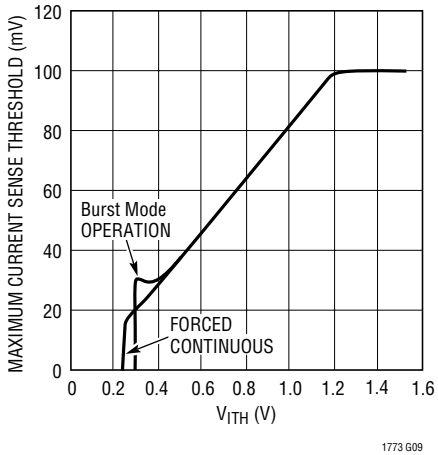
Maximum Current Sense Threshold vs $V_{RUN/SS}$



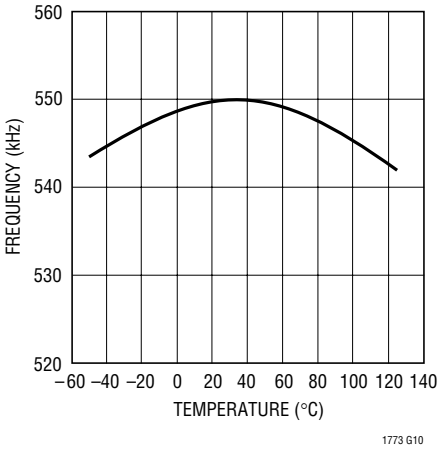
Maximum Current Sense Threshold vs Temperature



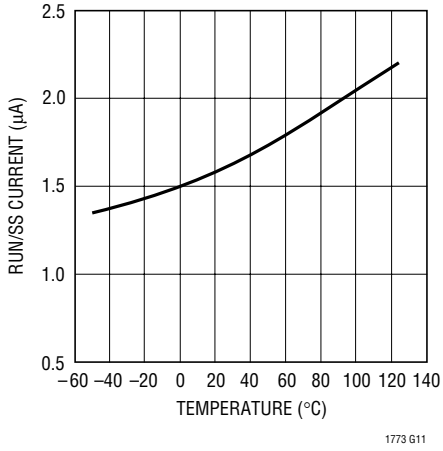
Maximum Current Sense Threshold vs V_{ITH}



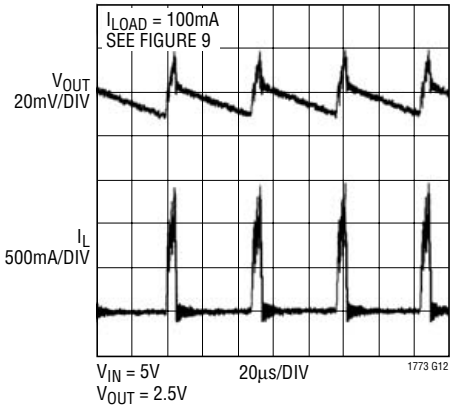
Oscillator Frequency vs Temperature



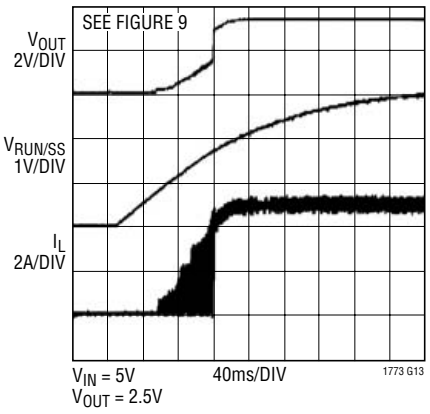
RUN/SS Pin Current vs Temperature



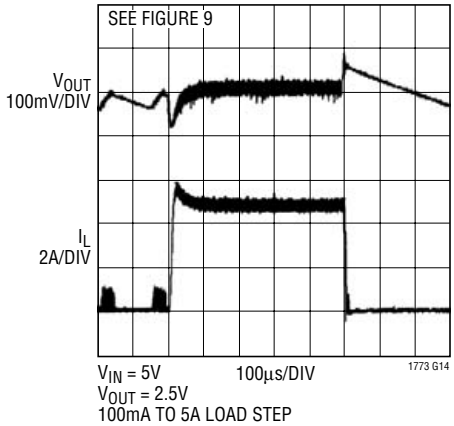
Burst Mode Operation



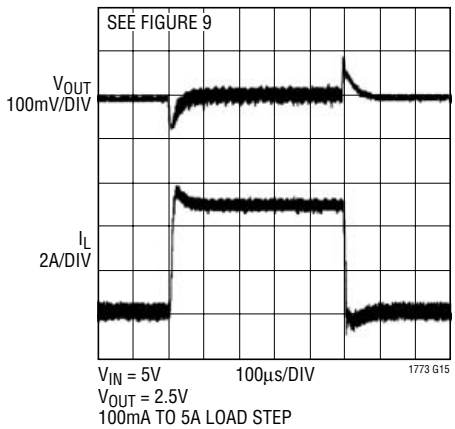
Start-Up



Load Step (Burst Mode Operation)



Load Step (Continuous Mode)



PIN FUNCTIONS

I_{TH} (Pin 1): Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is 0V to 1.2V. Under high duty cycle and nearing current limit, I_{TH} can swing up to 2.4V.

RUN/SS (Pin 2): Combination of Soft-Start and Run Control Inputs. A capacitor to ground at this pin sets the ramp time to full current output. The time is approximately 0.8s/μF. Forcing this pin below 0.4V shuts down all the circuitry.

SYNC/FCB (Pin 3): Multifunction Pin. This pin performs three functions: 1) secondary winding feedback input, 2) external clock synchronization and 3) Burst Mode operation or forced continuous mode select. For secondary winding applications, connect to a resistive divider from the secondary output. To synchronize with an external clock, apply a TTL/CMOS compatible clock with a frequency between 585kHz and 750kHz. To select Burst Mode operation, tie SYNC/FCB to V_{IN}. Grounding this pin forces continuous operation.

V_{FB} (Pin 4): Feedback Pin. Receives the feedback voltage from an external resistive divider across the output. Do not use more than 0.01μF of feedforward capacitance from FB to the output.

GND (Pin 5): Ground Pin.

BG (Pin 6): Bottom Gate Driver of External N-Channel Power MOSFET. This pin swings from 0V to V_{IN}.

TG (Pin 7): Top Gate Driver of External P-Channel Power MOSFET. This pin swings from 0V to V_{IN}.

V_{IN} (Pin 8) : Main Supply Pin. Must be closely decoupled to GND (pin 5).

$SENSE^-$(Pin 9): The Negative Input to the Current Comparator. A sense resistor between this pin and V_{IN} sets the peak current in the top switch. Connect this pin to the source of the external P-Channel power MOSFET.

SW (Pin 10): Switch Node Connection to Inductor. This pin connects to the drains of the external main and synchronous power MOSFET switches.

FUNCTIONAL DIAGRAM

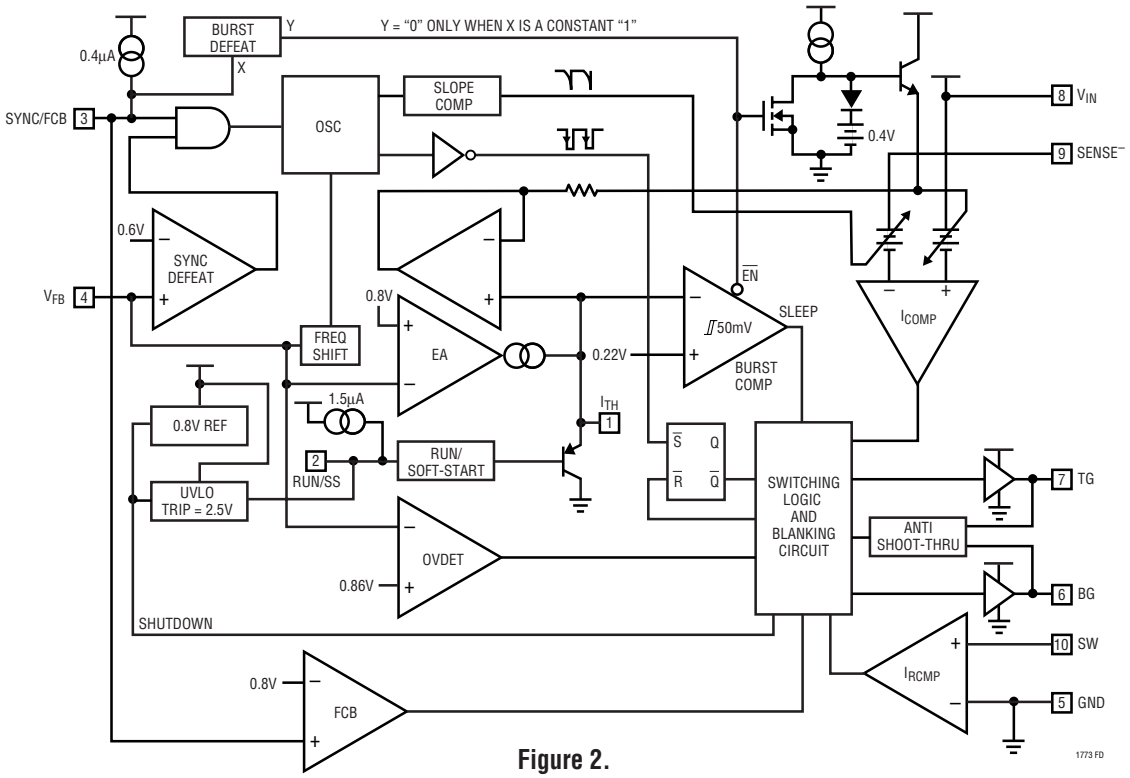


Figure 2.

OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC1773 uses a constant frequency, current mode step-down architecture to drive an external pair of complementary power MOSFETs. During normal operation, the external top P-channel power MOSFET turns on each cycle when the oscillator sets the RS latch, and turns off when the current comparator I_{COMP} resets the RS latch. The peak inductor current at which I_{COMP} resets the RS latch is controlled by the voltage on the I_{TH} pin, which is the output of error amplifier EA. The V_{FB} pin, described in the Pin Functions section, allows EA to receive an output feedback voltage from an external resistive divider. When the load current increases, it causes a slight decrease in the feedback voltage relative to the 0.8V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current. While the top P-channel MOSFET is off, the bottom N-channel MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current reversal comparator I_{RCMP}, or the beginning of the next cycle.

The main control loop is shut down by pulling the RUN/SS pin low. Releasing RUN/SS allows an internal 1.5µA current source to charge the external soft-start capacitor C_{SS}. When C_{SS} reaches 0.7V, the main control loop is enabled with the internal buffered I_{TH} voltage clamped at approximately 5% of its maximum value. As C_{SS} continues to charge, the internal buffered I_{TH} is gradually released allowing normal operation to resume.

An overvoltage comparator, 0V, guards against transient overshoots (>7.5%) as well as other more serious conditions that may overvoltage the output. In this case, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

Burst Mode Operation

The LTC1773 is capable of Burst Mode operation in which the external power MOSFETs operate intermittently based on load demand. To enable Burst Mode operation, simply allow the SYNC/FCB pin to float or connect it to a logic high. To disable Burst Mode operation and force continuous mode, connect the SYNC/FCB pin to GND. The threshold voltage between Burst Mode operation and forced continuous mode is 0.8V. This can be used to assist in secondary winding regulation as described in Auxiliary Winding Control Using SYNC/FCB Pin in the Applications Information section.

When the converter operates in Burst Mode operation the peak current of the inductor is set to approximately a third of the maximum peak current value during normal operation even though the voltage at the I_{TH} pin indicates a lower value. The voltage at the I_{TH} pin drops when the inductor's average current is greater than the load requirement. As the I_{TH} voltage drops below 0.22V, the BURST comparator trips, causing the internal sleep line to go high and turn off both power MOSFETs.

The circuit enters sleep mode with both power MOSFETs turned off. In sleep mode, the internal circuitry is partially turned off, reducing the quiescent current to about 80µA. The load current is now being supplied from the output capacitor. When the output voltage drops, causing I_{TH} to rise above 0.27V, the internal sleep line goes low, and the LTC1773 resumes normal operation. The next oscillator cycle will turn on the external top MOSFET and the switching cycle repeats.

Short-Circuit Protection

When the output is shorted to ground, the frequency of the oscillator is reduced to about 55kHz, 1/10 the nominal frequency. This frequency foldback ensures that the inductor current has more time to decay, thereby preventing runaway. The oscillator's frequency will gradually increase to 550kHz after V_{FB} rises above 0.4V.

Frequency Synchronization

The LTC1773 can be synchronized with an external TTL/CMOS compatible clock signal. The frequency range of this signal must be from 585kHz to 750kHz. *Do not* synchronize the LTC1773 below 585kHz as this may cause abnormal operation and an undesired frequency spectrum. The top MOSFET turn-on follows the rising edge of the external source.

When the LTC1773 is clocked by an external source, Burst Mode operation is disabled; the LTC1773 then operates in PWM pulse skipping mode preventing current reversal. In this mode, when the output load is very low, current comparator I_{COMP} remains tripped for more than one cycle

OPERATION (Refer to Functional Diagram)

and forces the main switch to stay off for the same number of cycles. Increasing the output load current slightly, above the minimum required for discontinuous conduction mode, allows constant frequency PWM.

Frequency synchronization is inhibited when the feedback voltage, V_{FB}, is below 0.6V. This prevents the external clock from interfering with the frequency foldback for short-circuit protection.

Dropout Operation

When the input supply voltage decreases toward the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle until it reaches 100% duty cycle. The output voltage will then be determined by the input voltage minus the IR voltage drop across the external P-channel MOSFET, sense resistor, and the inductor.

Undervoltage Lockout

A precision undervoltage lockout shuts down the LTC1773 when V_{IN} drops below 2.5V, making it ideal for single lithium-ion battery applications. In shutdown, the LTC1773 draws only several microamperes, which is low enough to prevent deep discharge and possible damage to the lithium-ion battery that's nearing its end of charge. A 150mV hysteresis ensures reliable operation with noisy supplies.

Low Supply Operation

The LTC1773 is designed to operate down to a 2.65V supply voltage. For proper operation at this low input voltage, sub-logic level MOSFETs are required. When the value of the output voltage is very close to the input voltage, the converter is running at high duty cycles or in dropout where the main switch is on continuously. See Efficiency Considerations in the Applications Information section.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability by preventing subharmonic oscillations. It works by internally adding a ramp to the inductor current signal at duty cycles in excess of 30%. This causes the internal current comparator to trip earlier. The I_{TH} clamp level is also reached earlier than conditions in which the duty cycle is below 30%. As a result, the maximum inductor peak current is lower for $V_{OUT}/V_{IN} > 0.3$ than when $V_{OUT}/V_{IN} < 0.3$.

To compensate for this loss in maximum inductor peak current during high duty cycles, the LTC1773 uses a patent pending scheme that raises the I_{TH} clamp level (proportional to the amount of slope compensation) when duty cycle is above 30%.

APPLICATIONS INFORMATION

The basic LTC1773 application circuit is shown in Figure 1. External component selection is driven by the load requirement and begins with the selection of R_{SENSE}. Once R_{SENSE} is known, L can be chosen, followed by the external power MOSFETs. Finally, C_{IN} and C_{OUT} are selected.

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The LTC1773 current comparator has a maximum threshold of $100mV/R_{SENSE}$. The current comparator threshold sets the peak of the inductor current, yielding a maximum average output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current ΔI_L.

Allowing a margin for variations in the LTC1773 and external component values yields:

$$R_{SENSE} = 70mV/I_{MAX}$$

Inductor Value Calculation

The inductor selection will depend on the operating frequency of the LTC1773. The internal preset frequency is 550kHz, but can be externally synchronized up to 750kHz.

APPLICATIONS INFORMATION

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. However, operating at a higher frequency generally results in lower efficiency because of external MOSFET gate charge losses.

The inductor value has a direct effect on ripple current. The ripple current, ΔI_L, decreases with higher inductance or frequency and increases with higher V_{IN} or V_{OUT}.

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (1)$$

Accepting larger values of ΔI_L allows the use of lower inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is 30% to 40% of I_{MAX}. Remember, the maximum ΔI_L occurs at the maximum input voltage.

The inductor value also has an effect on Burst Mode operation. The transition to low current operation begins when the inductor current peaks fall to approximately 1/3 its original value. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to increase.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy, or Kool Mμ® cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase. Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, new designs for surface mount are available which do not increase the height significantly.

Power MOSFET and Schottky Diode Selection

Two external power MOSFETs must be selected for use with the LTC1773: a P-channel MOSFET for the top (main) switch, and an N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak gate drive levels are set by the V_{IN} voltage. Therefore, for $V_{IN} > 5V$, logic-level threshold MOSFETs should be used. But, for $V_{IN} < 5V$, sub-logic level threshold MOSFETs ($V_{GS(TH)} < 3V$) should be used. In these applications, make sure that the V_{IN} to the LTC1773 is less than 8V because the absolute maximum V_{GS} rating of the majority of these sub-logic threshold MOSFETs is 8V.

Selection criteria for the power MOSFETs include the "ON" resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, input voltage, maximum output current, and total gate charge. When the LTC1773 is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

Main Switch Duty Cycle = V_{OUT}/V_{IN}

Synchronous Switch Duty Cycle = $(V_{IN} - V_{OUT})/V_{IN}$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DSON} + K(V_{IN})^2(I_{MAX})(C_{RSS})(f)$$

APPLICATIONS INFORMATION

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}} (I_{MAX})^2 (1+\delta) R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ and K is a constant inversely related to the gate drive current.

Both MOSFETs have I^2R losses while the topside P-channel equation includes an additional term for transition losses, which are highest at high input voltages. The synchronous MOSFET losses are greatest at high input voltage or during a short-circuit when the duty cycle in this switch is nearly 100%.

The term $(1 + \delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs. C_{RSS} is usually specified in the MOSFET characteristics. The constant K = 1.7 can be used to estimate the contributions of the two terms in the main switch dissipation equation.

Typical gate charge for the selected P-channel MOSFET should be less than 30nC (at $4.5V_{GS}$) while the turn-off delay should be less than 150ns. However, due to differences in test and specification methods of various MOSFET manufacturers, the P-channel MOSFET ultimately should be evaluated in the actual LTC1773 application circuit to ensure proper operation.

A Schottky diode can be placed in parallel with the synchronous MOSFET to improve efficiency. It conducts during the dead-time between the conduction of the two power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on and storing charge during the dead-time, which could cost as much as 1% in efficiency. A 1A Schottky is generally a good size for 5A to 8A regulators due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance. The diode may be omitted if the efficiency loss can be tolerated.

C_{IN} Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ required } I_{RMS} \cong I_{MAX} \frac{\left[V_{OUT}(V_{IN} - V_{OUT})\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question.

C_{OUT} Selection

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement is satisfied the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. With $\Delta I_L = 0.4 I_{OUT(MAX)}$ and allowing for 2/3 of the ripple due to ESR, the output ripple will be less than 50mV at max V_{IN} assuming:

C_{OUT} required ESR < 2 R_{SENSE}

$C_{OUT} > 1/(8fR_{SENSE})$

The first condition relates to the ripple current into the ESR of the output capacitance while the second term guarantees that the output voltage does not significantly discharge during the operating frequency period due to ripple current. The choice of using smaller output capacitance increases the ripple voltage due to the discharging term but can be compensated for by using capacitors of very low ESR to maintain the ripple voltage at or below 50mV.

APPLICATIONS INFORMATION

The I_{TH} pin OPTI-LOOP compensation components can be optimized to provide stable, high performance transient response regardless of the output capacitors selected.

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR/size ratio of any aluminum electrolytic at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum, available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo OS-CON and POSCAP, Nichicon PL series, Panisonic SP series and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

Output Voltage Programming

The output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 0.8V\left(1+\frac{R2}{R1}\right) \quad (2)$$

The external resistive divider is connected to the output as shown in Figure 3, allowing remote voltage sensing.

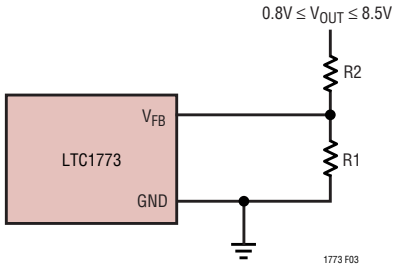


Figure 3. Setting the LTC1773 Output Voltage

Run/Soft-Start Function

The RUN/SS pin is a dual purpose pin that provides the soft-start function and a means to shut down the LTC1773. Soft-start reduces surge currents from V_{IN} by gradually increasing the internal current limit. Power supply sequencing can also be accomplished using this pin.

An internal 1.5µA current source charges up an external capacitor C_{SS}. When the voltage on RUN/SS reaches 0.7V the LTC1773 begins operating. As the voltage on RUN/SS continues to ramp from 0.7V to 1.8V, the I_{TH} clamp is also ramped at a proportionally linear rate. Depending on the external R_{SENSE} used, the peak inductor current, and thus the internal current limit, rises with the RUN/SS voltage. The output current thus ramps up slowly, charging the output capacitor. If RUN/SS has been pulled all the way to ground, there will be a delay before the current starts increasing and is given by:

$$t_{DELAY} = \frac{0.7C_{SS}}{1.5\mu A} = \left(0.47s/\mu F\right)C_{SS}$$

Pulling the RUN/SS pin below 0.4V puts the LTC1773 into a low quiescent current shutdown mode ($I_Q < 10\mu A$). This pin can be driven directly from logic as shown in Figure 4. Diode D1 in Figure 4 reduces the start delay but allows C_{SS} to ramp up slowly providing the soft-start function. This diode can be deleted if soft-start is not needed.

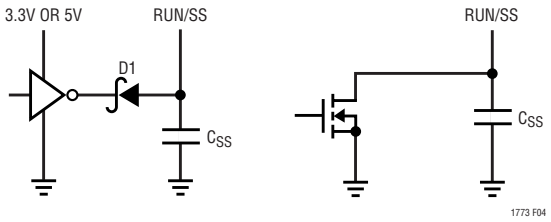


Figure 4. RUN/SS Pin Interfacing

Auxiliary Winding Control Using SYNC/FCB Pin

The SYNC/FCB pin can be used as a secondary feedback to provide a means of regulating a flyback winding output. When this pin drops below its ground referenced 0.8V threshold, continuous mode operation is forced. In continuous mode, the P-channel main and N-channel synchronous switches are switched continuously regardless of the load on the main output.

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Synchronous switching removes the normal limitation that power must be drawn from the inductor primary winding in order to extract power from auxiliary windings. With continuous synchronous operation, power can be drawn from the auxiliary windings without regard to the primary output load.

The secondary output voltage is set by the turns ratio of the transformer in conjunction with a pair of external resistors returned to the SYNC/FCB pin as shown in Figure 5. The secondary regulated voltage, V_{SEC}, in Figure 5 is given by:

$$V_{SEC} \cong (N+1)V_{OUT} - V_{DIODE} > 0.8V\left(1+\frac{R4}{R3}\right)$$

where N is the turns ratio of the transformer and V_{OUT} is the main output voltage sensed by V_{FB}.

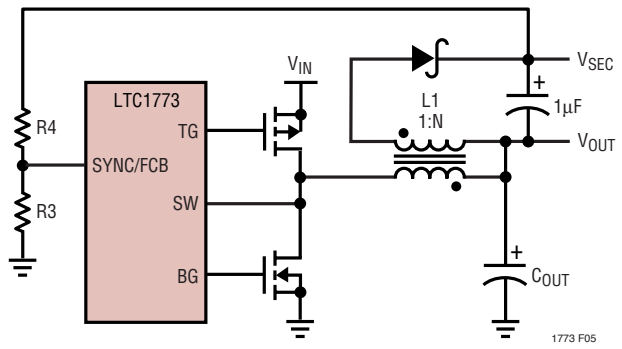

Figure 5. Secondary Output Loop Connection

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1773 circuits: V_{IN} quiescent current, external power MOSFET gate charge current, I^2R losses, and topside MOSFET transition losses.

1. The V_{IN} quiescent current is due to the DC bias current as given in the electrical characteristics, it excludes MOSFET driver and control currents. V_{IN} current results in a small loss which increases with V_{IN}.
2. The external MOSFET gate charge current results from switching the gate capacitance of the external power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is the current out of V_{IN}; it is typically larger than the DC bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$ where Q_T and Q_B are the gate charges of the external main and synchronous switches. Both the DC bias and gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.
3. I^2R losses are calculated from the resistances of the external R_{SENSE}, the external power MOSFETs (R_{SW}) and the external inductor (R_L). In continuous mode, the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin from L is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC), as follows:

$$R_{SW} = (R_{DS(ON)TOP} + R_{SENSE}) \bullet DC + R_{DS(ON)BOT} \bullet (1 - DC)$$

   The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the MOSFET manufactures's datasheets. Thus, to obtain I^2R losses, simply add R_{SW} and R_L together and multiply their sum by the square of the average output current.
4. Transition losses apply to the topside MOSFET and increase when operating at high input voltages and higher operating frequencies. Transition losses can be estimated from:

   $$\text{Transition Loss} = 2(V_{IN})^2 I_{O(MAX)} C_{RSS}(f)$$

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Other losses including C_{IN} and C_{OUT} ESR dissipative losses, and inductor core losses, generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $(\Delta I_{LOAD})(ESR)$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, which generates a feedback error signal. The regulator loop then returns V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The availability of the I_{TH} pin not only allows optimization of control loop behavior but also provides a DC coupled and an AC filtered closed-loop response test point. The DC step, rise time and settling at this test point reflects the closed loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The I_{TH} external components shown in the Figure 1 circuit will provide an adequate starting point for most applications.

The I_{TH} series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be decided upon because the various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. The gain of the loop will be increased by increasing R_C, and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Application Note 76.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately $(25)(C_{LOAD})$. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest amount of time that the LTC1773 is capable of turning the top MOSFET on and off again. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. The minimum on-time for the LTC1773 is about 250ns. Low duty cycle and high frequency synchronous applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{f \bullet V_{IN}}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the LTC1773 will begin to skip cycles. The output voltage will continue to be regulated, but the ripple current and ripple voltage will increase.

If an application can operate close to the minimum on-time limit, an inductor must be chosen that has low enough inductance to provide sufficient ripple amplitude to meet the minimum on-time requirement. As a general rule, keep the inductor ripple current equal or greater than 30% of the $I_{OUT(MAX)}$ at $V_{IN(MAX)}$.

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PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1773. These items are also illustrated graphically in the layout diagram of Figure 6. Check the following in your layout:

1) Are the signal and power grounds segregated? The LTC1773 signal ground consists of the resistive divider, the compensation network and C_{SS}. The power ground consists of the (–) plate of C_{IN}, the (–) plate of C_{OUT}, the source of the external synchronous NMOS, and Pin 5 of the LTC1773. The power ground traces should be kept short, direct and wide. Connect the synchronous MOSFETs source directly to the input capacitor ground.

2) Does the V_{FB} pin connect directly to the feedback resistors? The resistive divider of R1 and R2 must be connected between the (+) plate of C_{OUT} and signal ground. Be careful locating the feedback resistors too far away from the LTC1773. The V_{FB} line should not be routed close to any other nodes with high slew rates.

3) Does the (+) terminal of C_{IN} connect to V_{IN} as closely as possible? This capacitor provides the AC current to the external power MOSFETs.

4) Keep the switching nodes SW, TG and BG away from sensitive small-signal nodes, especially from the voltage and current sensing feedback pins.

Design Example

As a design example, assume the LTC1773 is used in a single lithium-ion battery powered cellular phone application. The V_{IN} will be operating from a maximum of 4.2V down to about 2.7V. The load current requirement is a maximum of 2A but most of the time it will be on standby mode, requiring only 2mA. Efficiency at both low and high load currents is important. Output voltage is 2.5V. With this information we can calculate R_{SENSE} to be around 33mΩ. For the inductor L, using equation (1),

$$L = \frac{1}{(f)(\Delta I_L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

Substituting V_{OUT} = 2.5V, V_{IN} = 4.2V, ΔI_L = 800mA and f = 550kHz in equation (3) gives:

$$L = \frac{2.5V}{550kHz\,(800mA)}\left(1 - \frac{2.5V}{4.2V}\right) = 2.3\mu H$$

A 2.5µH inductor works well for this application. For good efficiency choose a 4A inductor with less than 0.1Ω series resistance.

C_{IN} will require an RMS current rating of at least 1A at temperature and C_{OUT} will require an ESR of less than 0.066Ω. In most applications, the requirements for these capacitors are fairly similar.

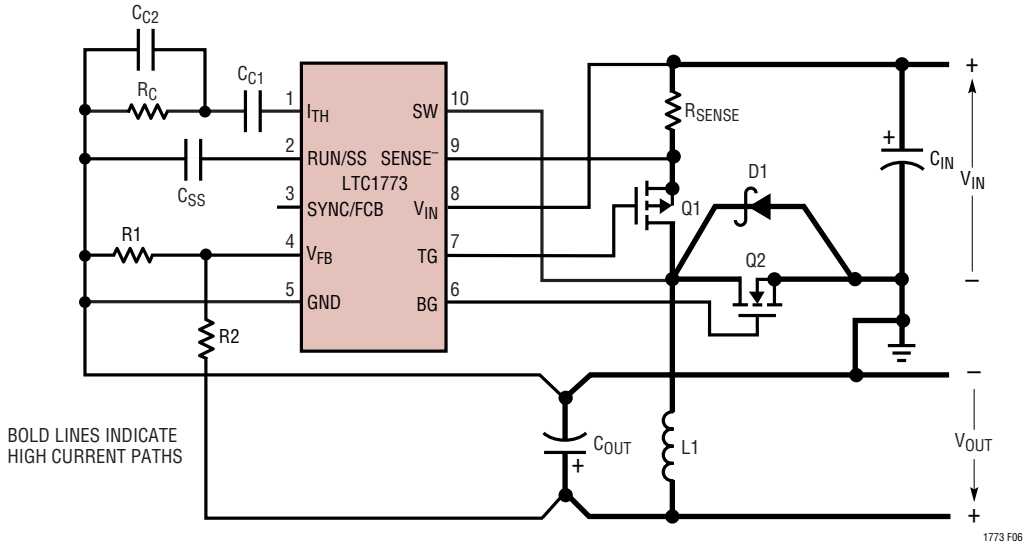


Figure 6. LTC1773 Layout Diagram

APPLICATIONS INFORMATION

For the selection of the external MOSFETs, the $R_{DS(ON)}$ must be guaranteed at 2.5V since the LTC1773 has to operate down to 2.7V. This requirement can be met by the Si9801DY.

For the feedback resistors, choose R1 = 80.6k. R2 can then be calculated from equation (2) to be:

$$R2 = \left(\frac{V_{OUT}}{0.8} - 1\right) R1 = 171k; \text{ use } 169k$$

Figure 7 shows the complete circuit along with its efficiency curve.

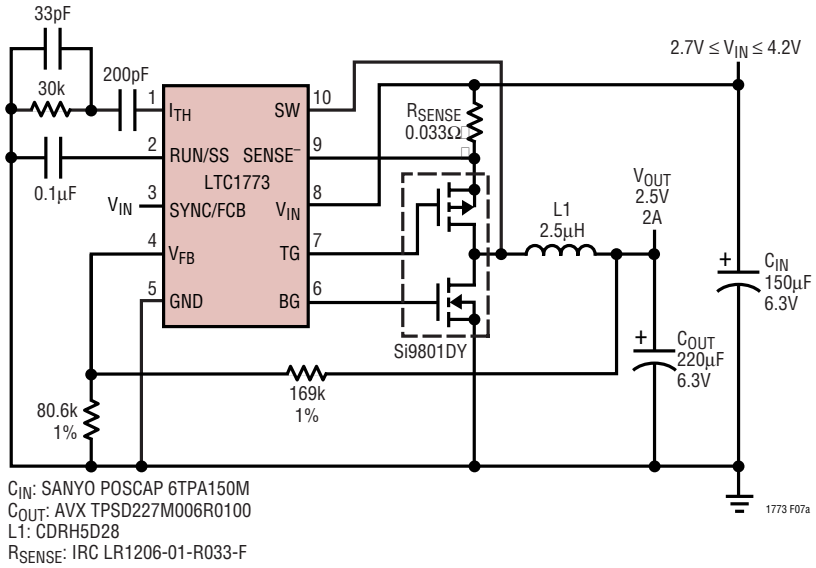
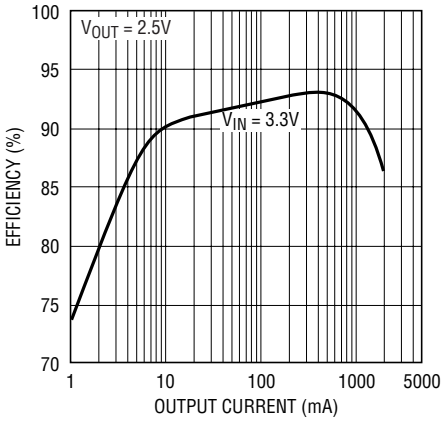
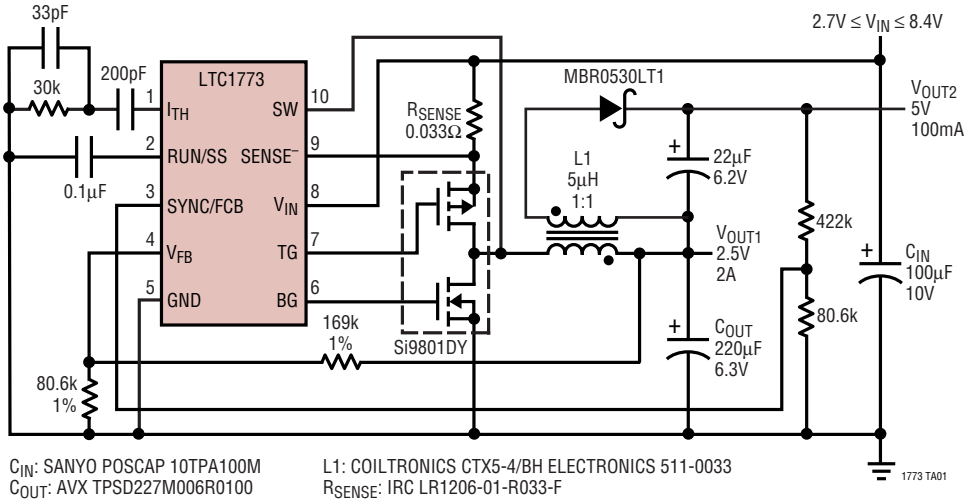


Figure 7. Single Lithium-Ion to 2.5V/2A Regulator

Efficiency Curve for Figure 7

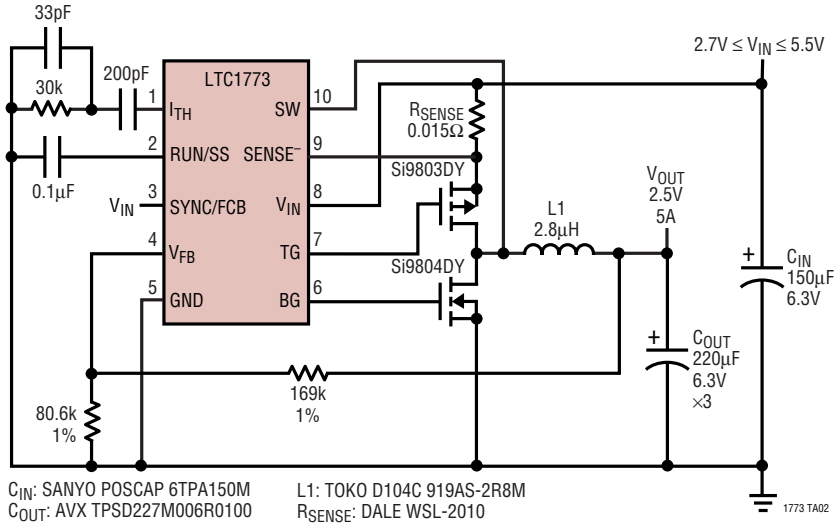


TYPICAL APPLICATIONS



CIN: SANYO POSCAP 10TPA100M
COUT: AVX TPSD227M006R0100
L1: COILTRONICS CTX5-4/BH ELECTRONICS 511-0033
RSENSE: IRC LR1206-01-R033-F

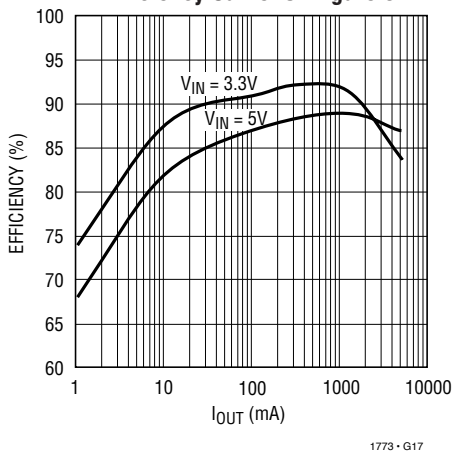
Figure 8. Dual Output 2.5V/2A and 5V/100mA Application



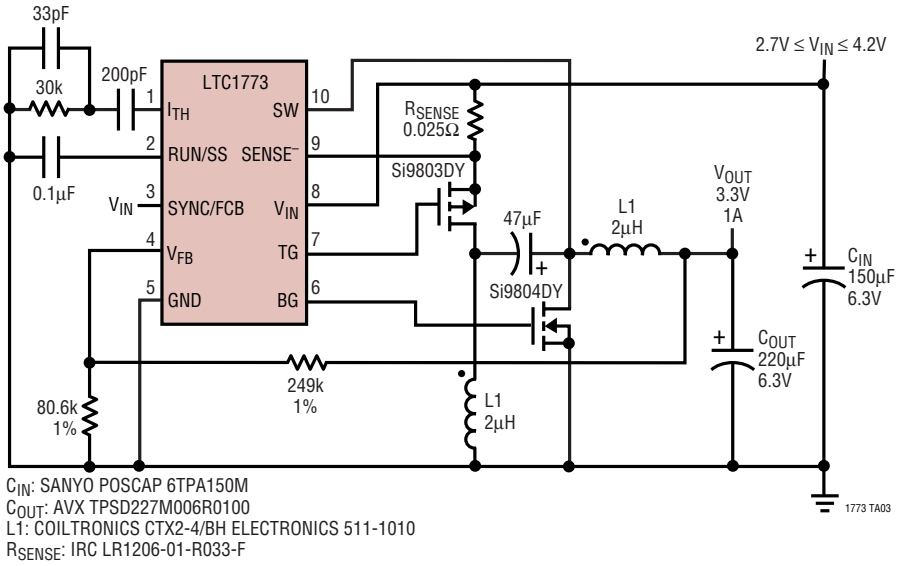
CIN: SANYO POSCAP 6TPA150M
COUT: AVX TPSD227M006R0100
L1: TOKO D104C 919AS-2R8M
RSENSE: DALE WSL-2010

Figure 9. Single Lithium-Ion to 2.5V/5A Regulator

Efficiency Curve for Figure 9



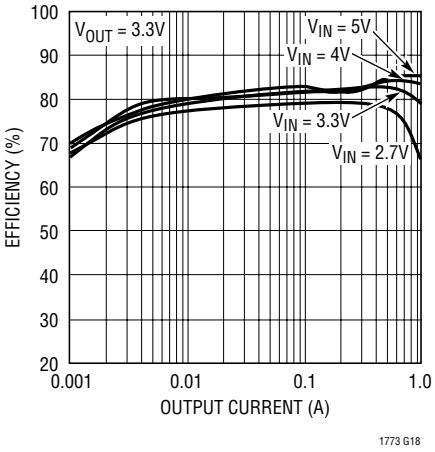
TYPICAL APPLICATIONS



CIN: SANYO POSCAP 6TPA150M
COUT: AVX TPSD227M006R0100
L1: COILTRONICS CTX2-4/BH ELECTRONICS 511-1010
RSENSE: IRC LR1206-01-R033-F

Figure 10. Single Lithium-Ion to 3.3V/1A Synchronous Zeta Converter

Efficiency Curve for Figure 10



TYPICAL APPLICATIONS

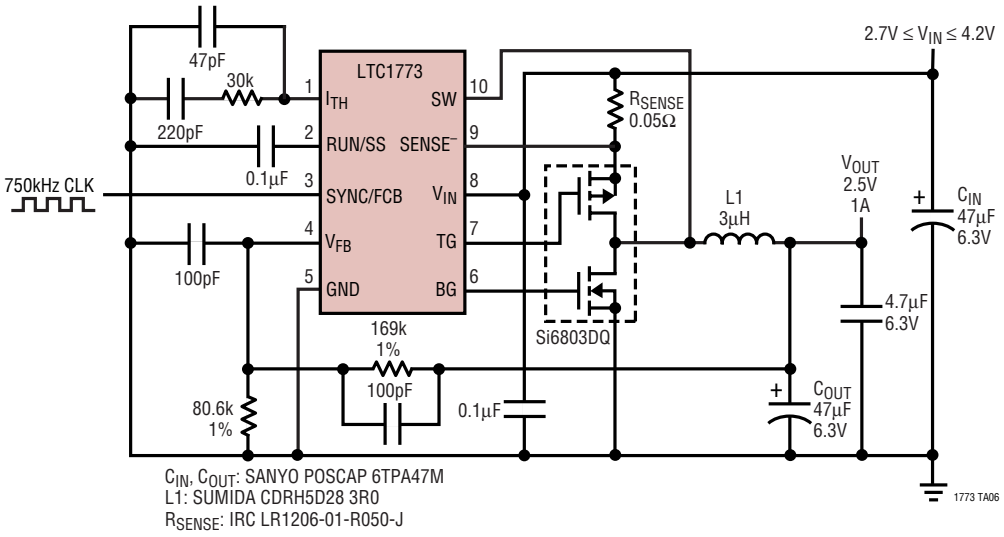


Figure 11. 750kHz Single Lithium-Ion to 2.5V/1A Regulator

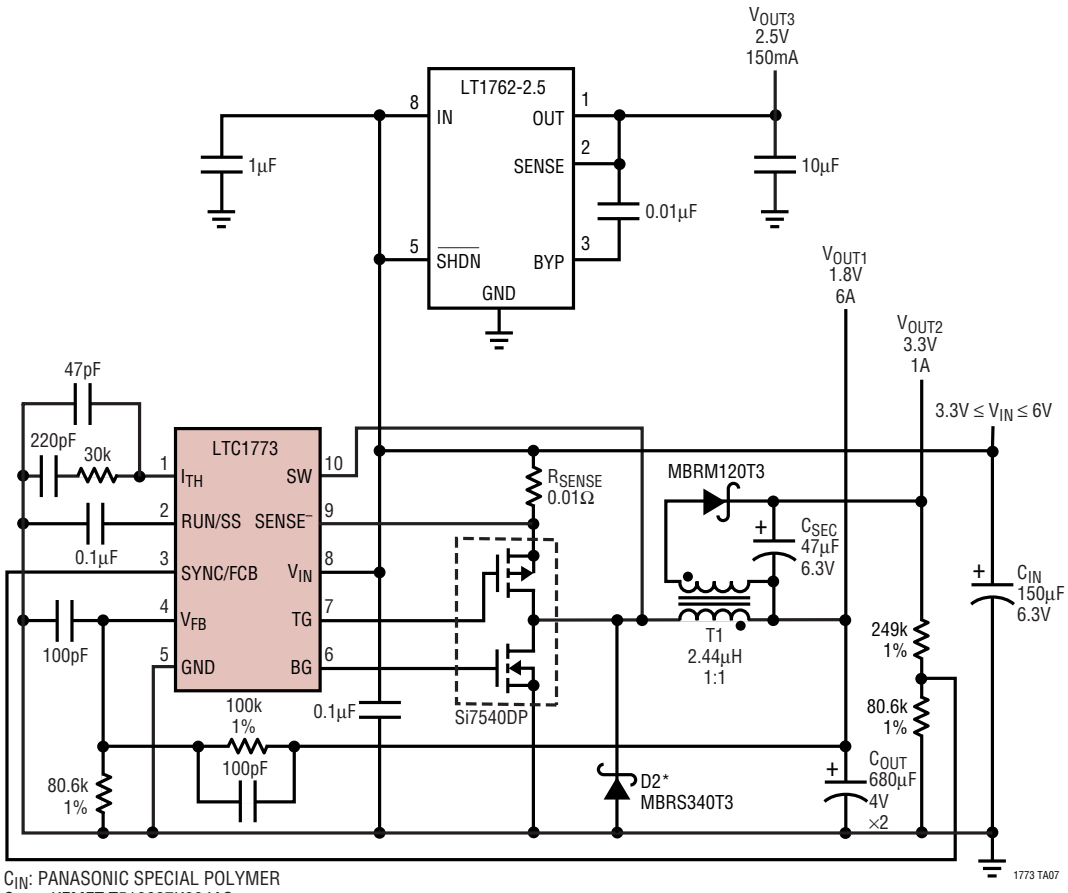


Figure 12. Triple Output 1.8V/6A, 2.5V/150mA,and 3.3V/1A Application

TYPICAL APPLICATIONS

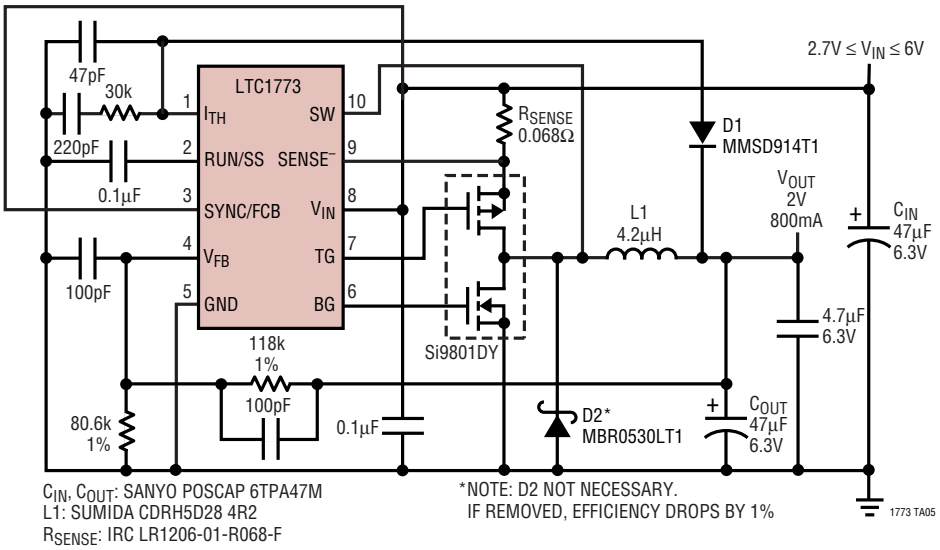


Figure 13. Single Lithium-Ion to 2V/800mA Regulator with Current Foldback

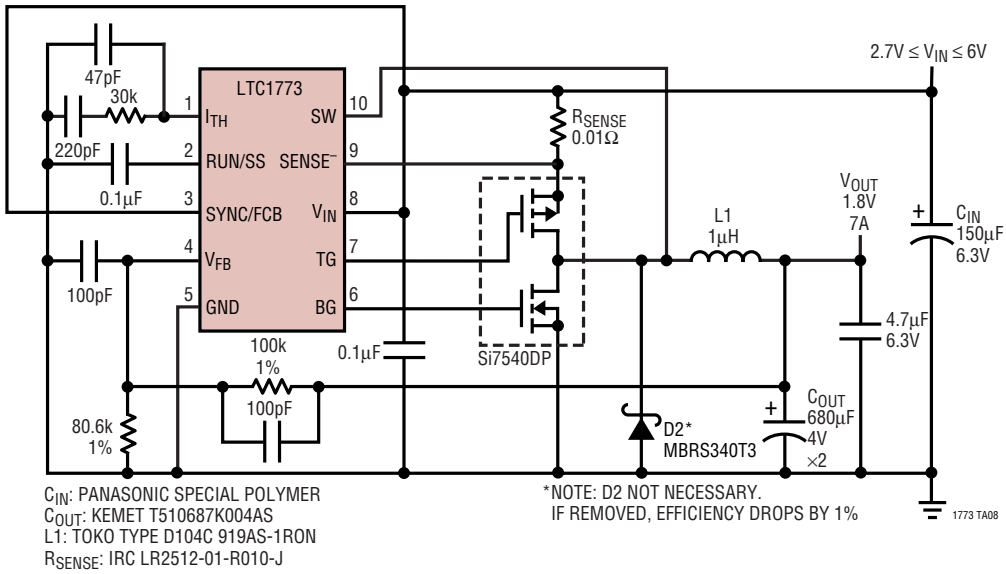


Figure 14. 3.3V to 1.8V/7A Regulator

TYPICAL APPLICATIONS

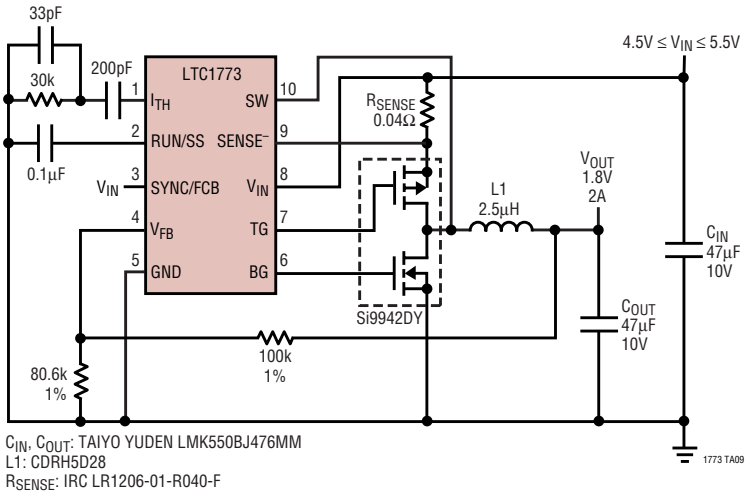
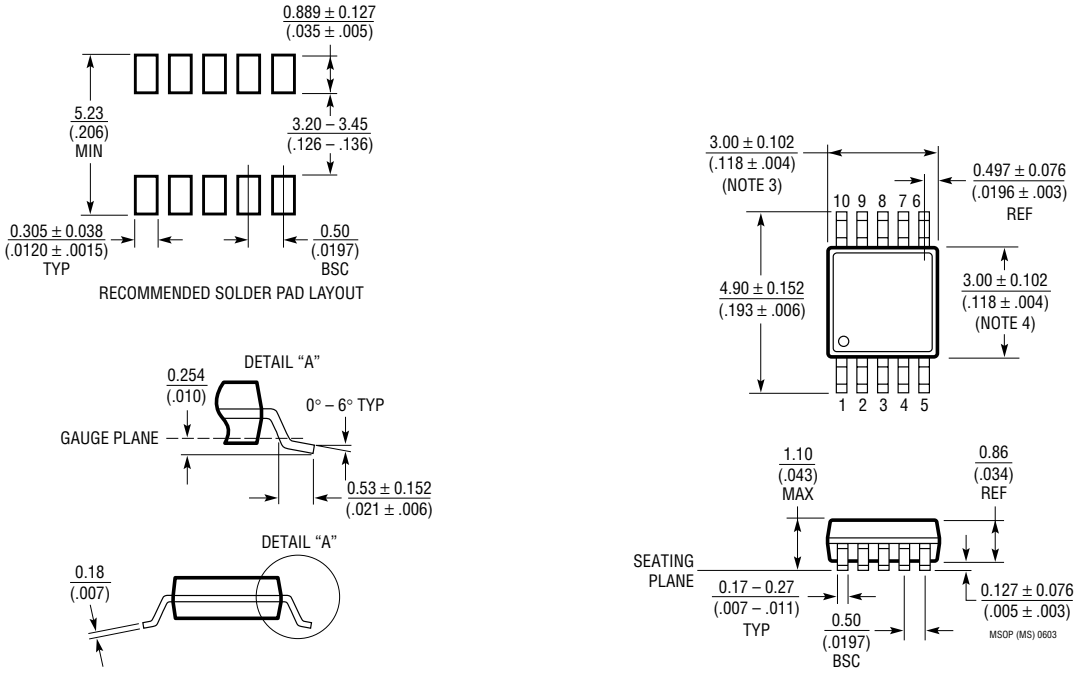


Figure 15. 5V to 1.8V/2A Regulator with Ceramic Capacitors

PACKAGE DESCRIPTION

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

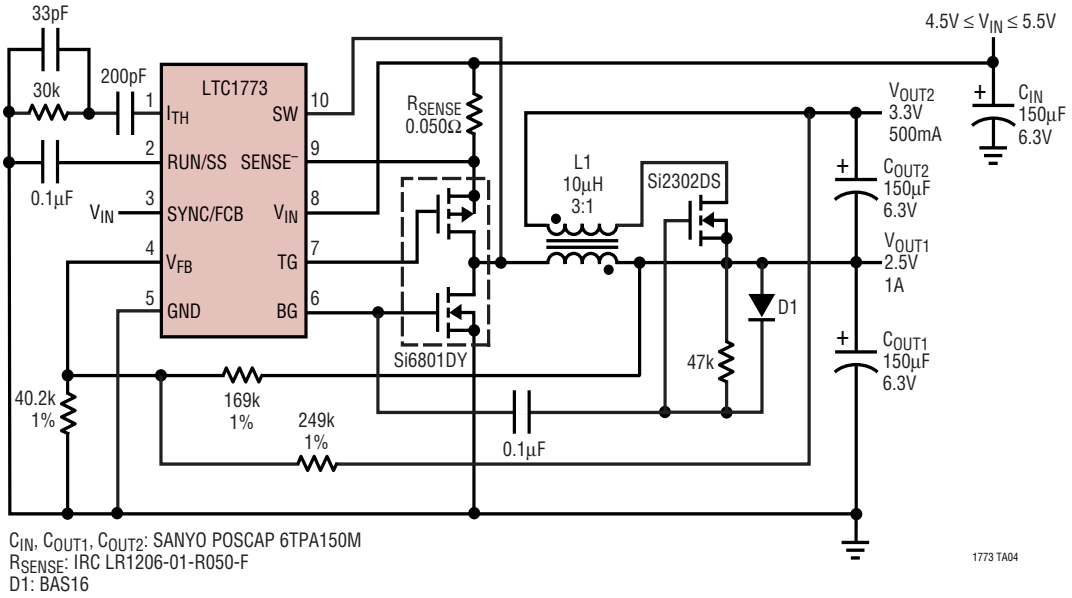


Figure 16. Dual Output Synchronous Buck Converter

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1622	Low Voltage Current Mode Step-Down DC/DC Controller	V_{IN}: 2V to 10V, 550kHz, Burst Mode Operation, Synchronizable
LTC1627/LTC1707	Low Voltage, Monolithic Synchronous Step-Down Regulator	Low Supply Voltage Range: 2.65V to 8V, I_{OUT} to 0.5A
LTC1735	High Efficiency Synchronous Step-Down Switching Controller	Burst Mode Operation, 16-Pin Narrow SO, Fault Protection
LTC1735-1	High Efficiency Synchronous Step-Down Switching Controller	Output Fault Protection 16-Pin GN, Burst Mode Operation, Power Good
LTC1771	Low Quiescent Current Step-Down DC/DC Controller	V_{IN}: 2.8V to 18V, 10µA I_Q, MS8 Package
LTC1772/B	SOT-23 Low Voltage Step-Down Controller	6-Pin SOT-23, 2V ≤ V_{IN} ≤ 10V, 550kHz
LTC1778	Wide Operating Range/Step-Down Controller, No R_{SENSE}	V_{IN} up to 36V, Current Mode, Power Good
LTC1779	SOT-23 Current Mode Step-Down Converter	250mA Output Current, 2.5V ≤ V_{IN} ≤ 9.8V, Up to 94% Efficiency
LTC1877	High Efficiency Monolithic Synchronous Step-Down Regulator	V_{IN} from 2.65V to 10V, 10µA I_Q, 550kHz, I_{OUT} to 600mA,MS8
LTC1878	High Efficiency Monolithic Synchronous Step-Down Regulator	V_{IN} from 2.65V to 7V, 10µA I_Q, 550kHz, I_{OUT} to 600mA,MS8
LTC3404	1.4MHz Monolithic Synchronous Step-Down Regulator	Up to 95% Efficiency, I_{OUT} = 600mA at V_{IN} = 3.3V No Schottky Diode Required, 8-Lead MSOP

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