

## FEATURES

- Improves SMBus/I<sup>2</sup>C™ Rise Time Transition
- Ensures Data Integrity with Multiple Devices on the SMBus/I<sup>2</sup>C
- Improves Low State Noise Margin
- Wide Supply Voltage Range: 2.7V to 6V
- Parallel Multiple LTC1694-1 Devices for Increased Drive
- Low Profile (1mm) SOT-23 (ThinSOT™) Package

## APPLICATIONS

- Notebook and Palmtop Computers
- Portable Instruments
- Battery Chargers
- Industrial Control Application
- TV/Video Products
- ACPI SMBus Interface

## DESCRIPTION

The LTC®1694-1 is a dual SMBus active pull-up designed to enhance data transmission speed and reliability under all specified SMBus loading conditions. The LTC1694-1 is also compatible with the Philips I<sup>2</sup>C Bus.

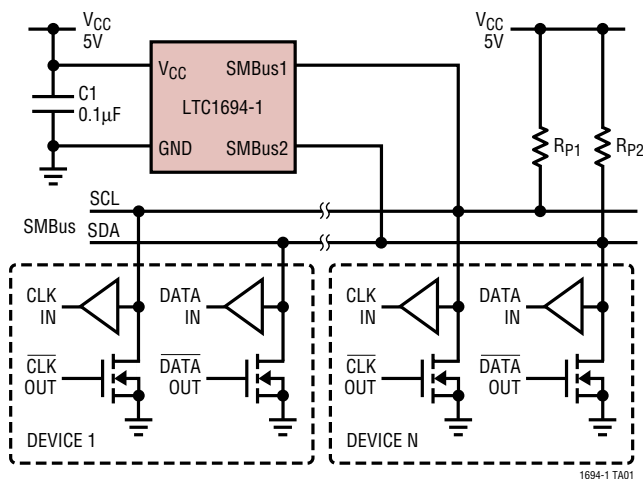
The LTC1694-1 allows multiple device connections or a longer, more capacitive interconnect, without compromising slew rates or bus performance, by supplying a high pull-up current of 2.2mA to slew the SMBus or I<sup>2</sup>C lines during positive bus transitions.

During negative transitions or steady DC levels, the LTC1694-1 sources zero current. External resistors, one on each bus line, trigger the LTC1694-1 during positive bus transitions and set the pull-down current level. These resistors determine the slew rate during negative bus transitions and the logic low DC level.

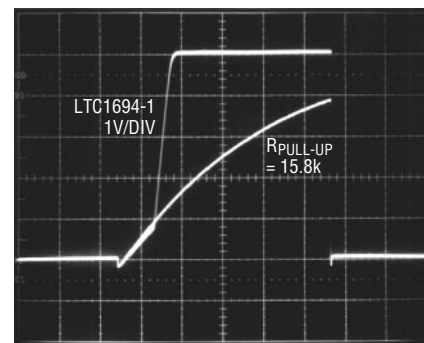
The LTC1694-1 is available in a 5-pin SOT-23 package.

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 ThinSOT is a trademark of Linear Technology Corporation.  
 I<sup>2</sup>C is a trademark of Philips Electronics N.V.  
 \*U.S. Patent No. 6,650,174

## TYPICAL APPLICATION



Comparison of SMBus Waveforms for the LTC1694-1 vs Resistor Pull-Up



V<sub>CC</sub> = 5V  
 C<sub>LD</sub> = 200pF  
 f<sub>SMBus</sub> = 100kHz

1694-1 TA02

## ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage ( $V_{CC}$ )	7V
SMBus1, SMBus2 Inputs	–0.3V to ( $V_{CC} + 0.3V$ )
Operating Ambient Temperature Range	
LTC1694-1C	0°C to 70°C
LTC1694-1I	–40°C to 85°C
Junction Temperature	125°C
Storage Temperature Range	–65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

## PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p><math>V_{CC}</math> 1      5 SMBus1</p> <p>GND 2</p> <p>NC 3      4 SMBus2</p> <p>S5 PACKAGE 5-LEAD PLASTIC TSOT-23</p> <p><math>T_{JMAX} = 125^{\circ}\text{C}</math>, <math>\theta_{JA} = 256^{\circ}\text{C/W}</math></p>	ORDER PART NUMBER
	LTC1694-1CS5 LTC1694-1IS5
	S5 PART MARKING
	LTHE LTA9

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}\text{C}$ .  $V_{CC} = 2.7V$  to  $6V$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{CC}$	Supply Voltage Range		2.7		6	V
$I_{CC}$	Supply Current	SMBus1 = SMBus2 = $V_{CC}$	● 15	45	80	$\mu\text{A}$
$I_{PULL-UP}$	Pull-Up Current	Positive Transition on SMBus (Figure 1) Slew Rate = $0.5V/\mu\text{s}$ , SMBus > $V_{THRES}$	● 1.0	2.2		mA
$V_{THRES}$	Input Threshold Voltage	Slew Rate = $0.5V/\mu\text{s}$ (Figure 1)	● 0.4	0.65	0.9	V
$SR_{THRES}$	Slew Rate Detector Threshold	SMBus > $V_{THRES}$	●	0.2	0.5	$V/\mu\text{s}$
$t_r$	SMBus Rise Time Standard Mode I <sup>2</sup> C Bus Rise Time	Bus Capacitance = 200pF (Note 2) Bus Capacitance = 400pF (Note 3)	● ●	0.32 0.30	1.0 1.0	$\mu\text{s}$ $\mu\text{s}$
$f_{MAX}$	SMBus Maximum Operating Frequency	(Note 4)	●		100	kHz

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** The rise time of an SMBus line is calculated from ( $V_{IL(MAX)} - 0.15V$ ) to ( $V_{IH(MIN)} + 0.15V$ ) or  $0.65V$  to  $2.25V$ . This parameter is guaranteed by design and not tested. With a minimum initial slew rate of  $0.5V/\mu\text{s}$ , a minimum pull-up current of  $1mA$  and a maximum input threshold voltage of  $0.9V$ :

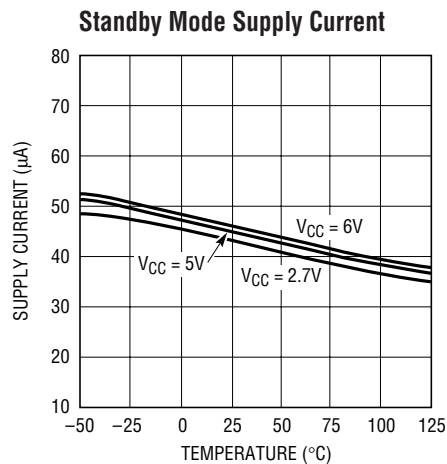
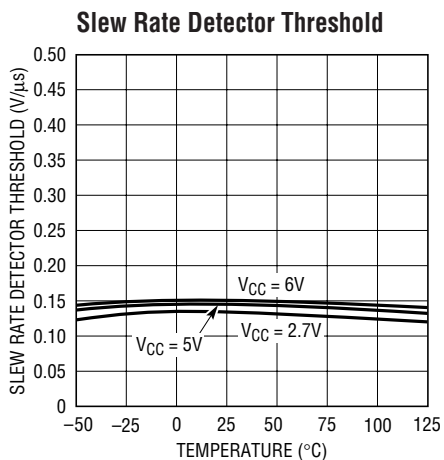
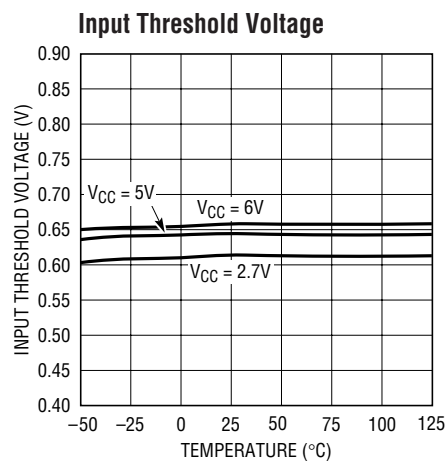
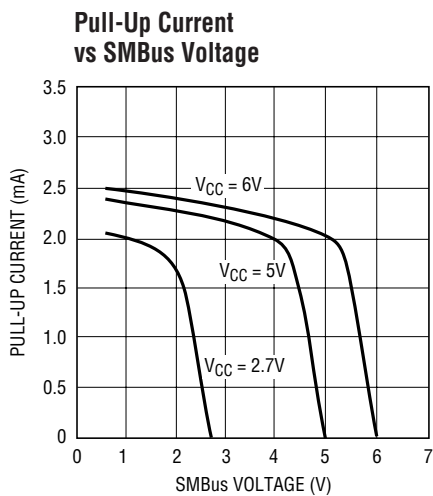
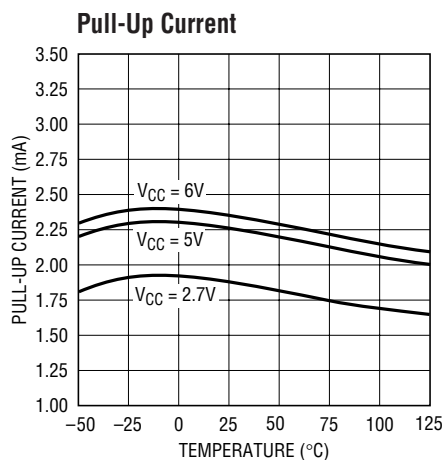
$$\text{Rise Time} = [(0.9V - 0.65V)/0.5V/\mu\text{s}] + [(2.25V - 0.9V) \cdot 200pF/1mA] = 0.77\mu\text{s}$$

**Note 3:** The rise time of an I<sup>2</sup>C bus line is calculated from  $V_{IL(MAX)}$  to  $V_{IH(MIN)}$  or  $1.5V$  to  $3V$  (with  $V_{CC} = 5V$ ). This parameter is guaranteed by design and not tested. With a minimum boosted pull-up current of  $1mA$ :

$$\text{Rise Time} = (3V - 1.5V) \cdot 400pF/1mA = 0.6\mu\text{s}$$

**Note 4:** This parameter is guaranteed by design and not tested.

# TYPICAL PERFORMANCE CHARACTERISTICS



## PIN FUNCTIONS

**V<sub>CC</sub> (Pin 1):** Power Supply Input. V<sub>CC</sub> can range from 2.7V to 6V and requires a 0.1μF bypass capacitor to GND. Supply current is typically 45μA when the SMBus or I<sup>2</sup>C lines are inactive (SCL and SDA are a logic high level).

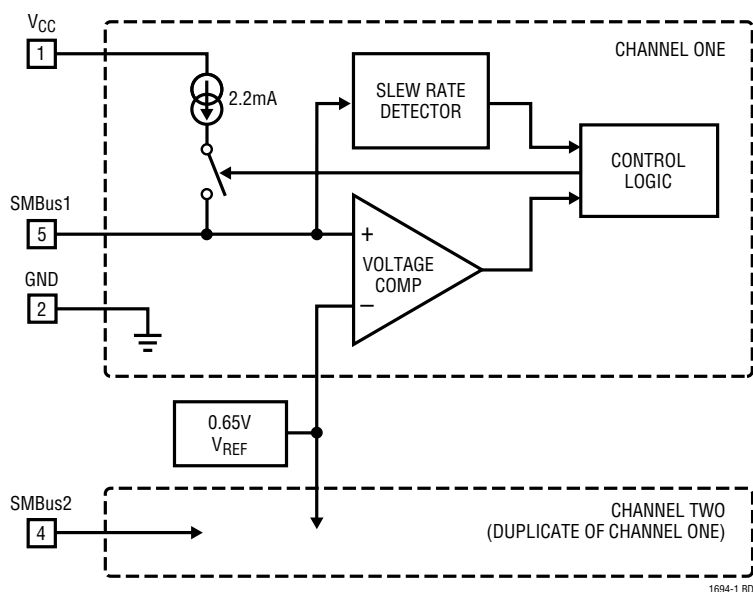
**GND (Pin 2):** Ground.

**NC (Pin 3):** No Connection.

**SMBus2 (Pin 4):** Active Pull-Up for SMBus.

**SMBus1 (Pin 5):** Active Pull-Up for SMBus.

## BLOCK DIAGRAM



## TEST CIRCUITS

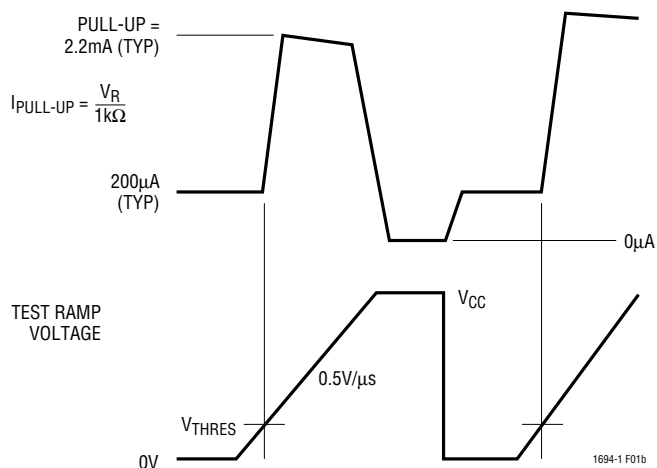
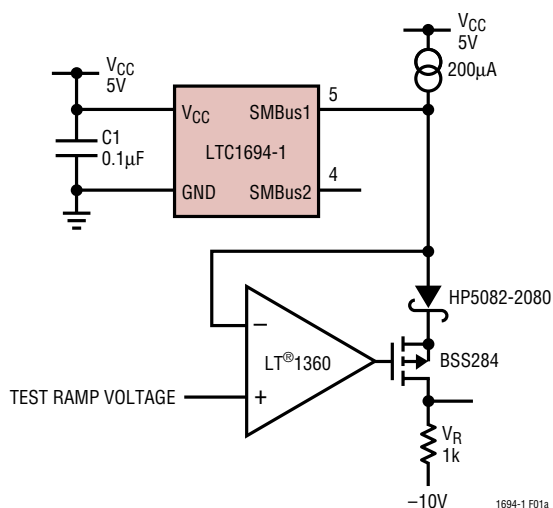


Figure 1

## APPLICATIONS INFORMATION

### SMBus Overview

SMBus communication protocol employs open-drain drives with resistive or current source pull-ups. This protocol allows multiple devices to drive and monitor the bus without bus contention. The simplicity of resistive or fixed current source pull-ups is offset by the slow rise times resulting when bus capacitance is high. Rise times can be improved by using lower pull-up resistor values or higher fixed current source values, but the additional current increases the low state bus voltage, decreasing noise margins. Slow rise times can seriously impact data reliability, enforcing a maximum practical bus speed well below the established SMBus maximum transmission rate.

### Theory of Operation

The LTC1694-1 overcomes these limitations by providing a 2.2mA pull-up current only during positive bus transitions to quickly slew any bus capacitance. Therefore, rise time is dramatically improved, especially with maximum SMBus loading conditions.

The LTC1694-1 has separate but identical circuitry for each SMBus output pin. The circuitry consists of a positive edge slew rate detector and a voltage comparator.

The 2.2mA pull-up current is only turned on if the voltage on the SMBus line voltage is greater than the 0.65V comparator threshold voltage and the positive slew rate of the SMBus line is greater than the 0.2V/ $\mu$ s threshold of the slew rate detector. The pull-up current remains on until the voltage on the SMBus line is within 0.5V of  $V_{CC}$  and/or the slew rate drops below 0.2V/ $\mu$ s.

### Selecting the Values of $R_S$ and $R_P$

An external pull-up resistor  $R_P$  is required in each SMBus line to supply a steady state pull-up current if the SMBus is at logic zero. This pull-up current is used for slewing the SMBus line during the initial portion of the positive transition in order to activate the LTC1694-1 2.2mA pull-up current.

Using an external  $R_P$  to supply the steady state pull-up current permits the user the freedom to adjust rise time versus fall time as well as defining the low state logic level ( $V_{OL}$ ).

For I/O stage protection from ESD and high voltage spikes on the SMBus, a series resistor  $R_S$  (Figure 2) is sometimes added to the open-drain driver of the bus agents. This is especially common in SMBus-controlled smart batteries.

Both the values of  $R_P$  and  $R_S$  must be chosen carefully to meet the low state noise margin and all timing requirements of the SMBus.

A discussion of the electrical parameters affected by the values of  $R_S$  and  $R_P$ , as well as a general procedure for selecting the values of  $R_S$  and  $R_P$  follows.

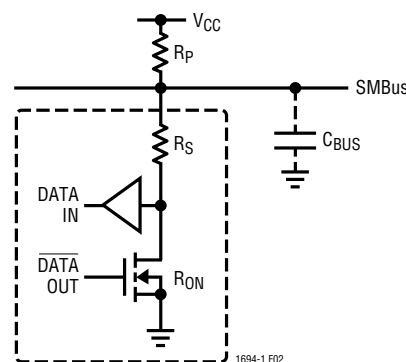


Figure 2

### Low State Noise Margin

A low value of  $V_{OL}$ , the low state logic level, is desired for good noise margin.  $V_{OL}$  is calculated as follows:

$$V_{OL} = (R_L \cdot V_{CC}) / (R_L + R_P) \quad (1)$$

$R_L$  is the series sum of  $R_S$  and  $R_{ON}$ , the on-resistance of the open-drain driver.

Increasing the value of  $R_P$  decreases the value of  $V_{OL}$ . Increasing  $R_L$  increases the value of  $V_{OL}$ .

### Initial Slew Rate

The initial slew rate, SR, of the Bus is determined by:

$$SR = (V_{CC} - V_{OL}) / (R_P \cdot C_{BUS}) \quad (2)$$

SR must be greater than  $SR_{THRES}$ , the LTC1694-1 slew rate detector threshold (0.5/ $\mu$ s max) in order to activate the 2.2mA pull-up current.

## APPLICATIONS INFORMATION

### SMBus Rise Time

Rise time of an SMBus line is derived using equations 3, 4 and 5.

$$t_r = t_1 + t_2 \quad (3)$$

$$t_1 = -R_P \cdot C_{BUS} \cdot \ln[(V_{THRES} - V_{CC}) / (V_{ILMAX} - 0.15 - V_{CC})] \quad (4)$$

if  $(V_{ILMAX} - 0.15) > V_{THRES}$ , then  $t_1 = 0\mu s$ .

$$t_2 = -R_P \cdot C_{BUS} \cdot \ln\{[V_{IHMIN} + 0.15 - V_{CC} - (R_P \cdot I_{PULL-UP})] / [V_{THRES} - V_{CC} - (R_P \cdot I_{PULL-UP})]\} \quad (5)$$

By ignoring the current through  $R_P$ , a simplified version of equation 3 is obtained:

$$t_2 = (V_{IHMIN} + 0.15 - V_{THRES}) \cdot C_{BUS} / I_{PULL-UP} \quad (6)$$

For an SMBus system,  $V_{ILMAX} = 0.8V$  and  $V_{IHMIN} = 2.1V$ . For the LTC1694-1, typically  $V_{THRES} = 0.65V$  and  $I_{PULL-UP} = 2.2mA$ .

$C_{BUS}$  is the total capacitance of the SMBus line.

Increasing the value of  $R_P$  increases the rise time.

### SMBus Fall Time

Fall time of an SMBus line is derived using equation 7:

$$t_f = R_T \cdot C_{BUS} \cdot \ln\{[0.9 \cdot (R_P + R_L) - R_L] / [(V_{ILMAX} - 0.15) \cdot (R_P + R_L) / V_{CC} - R_L]\} \quad (7)$$

where  $R_T$  is the parallel equivalent of  $R_P$  and  $R_L$ .

The rise and fall time calculation for an I<sup>2</sup>C system is as follows.

### I<sup>2</sup>C Bus Rise and Fall Time

Rise time of an I<sup>2</sup>C line is derived using equation 8.

$$t_r = -R_P \cdot C_{BUS} \cdot \ln\{[V_{IHMIN} - V_{CC} - (R_P \cdot I_{PULL-UP})] / [V_{ILMAX} - V_{CC} - (R_P \cdot I_{PULL-UP})]\} \quad (8)$$

Fall time of an I<sup>2</sup>C line is derived using equation 9:

$$t_f = R_T \cdot C_{BUS} \cdot \ln\{[(V_{IHMIN}/V_{CC}) \cdot (R_P + R_L) - R_L] / [(V_{ILMAX}/V_{CC}) \cdot (R_P + R_L) - R_L]\} \quad (9)$$

For an I<sup>2</sup>C system with fixed input levels,  $V_{ILMAX} = 1.5V$  and  $V_{IHMIN} = 3V$ .

For an I<sup>2</sup>C system with  $V_{CC}$  related input levels,  $V_{ILMAX} = 0.3V_{CC}$  and  $V_{IHMIN} = 0.7V_{CC}$ .

$C_{BUS}$  is the total capacitance of the I<sup>2</sup>C line.

A general procedure for selecting  $R_P$  and  $R_L$  is as follows:

1.  $R_L$  is first selected based on the I/O protection requirement. Generally, an  $R_S$  of  $100\Omega$  is sufficient for high voltage spike and ESD protection.  $R_{ON}$  is determined by the size of the open-drain driver, a large driver will have a lower  $R_{ON}$ .
2. Next, the value of  $R_P$  is determined based on the rise and fall time requirements using equations 3 to 7 (for an SMBus system) or 8 and 9 (for an I<sup>2</sup>C system). The value chosen for  $R_P$  must ensure that both the rise and fall time specifications are met simultaneously.
3. After  $R_P$  and  $R_L$  are selected, use equations 1 and 2 to check if the  $V_{OL}$  and SR requirements are fulfilled.

If SR is too low, decrease the value of  $R_P$ . If  $V_{OL}$  is too high, increase the value of  $R_P$ .

### SMBus Design Example

Given the following conditions and requirements:

$$\begin{aligned} V_{CC} &= 3.3V \text{ nom} \\ V_{OL} &= 0.4V \text{ max} \\ C_{BUS} &= 200pF \text{ max} \\ V_{ILMAX} &= 0.8V, V_{IHMIN} = 2.1V \\ t_r &= 0.8\mu s \text{ max}, t_f = 0.3\mu s \text{ max} \end{aligned}$$

If an  $R_S$  of  $500\Omega$  is used and the max  $R_{ON}$  of the driver is  $200\Omega$ , then  $R_L = 500 + 200 = 700\Omega$ . Using the max  $V_{THRES}$  of  $0.9V$  and a min  $I_{PULL-UP}$  of  $1mA$ .

Using equation 6 to calculate the approximate value of  $t_2$ :

$$t_2 = (2.1 + 0.15 - 0.9) \cdot [(200 \cdot 10^{-12}) / (1 \cdot 10^{-3})] = 0.27\mu s$$

$$t_1 = 0.8 - 0.27 = 0.53\mu s$$

Using equation 4 to find the required  $R_P$  to meet  $t_r$ :

$$R_P = -t_1 / \{C_{BUS} \cdot \ln[(V_{THRES} - V_{CC}) / (V_{ILMAX} - 0.15 - V_{CC})]\} = 27k$$

$$R_T = (R_P \cdot R_L) / (R_P + R_L)$$

## APPLICATIONS INFORMATION

Using equations 4 and 5 to check exact value of  $t_r$ :

$$t_r = 0.535\mu\text{s} + 0.254\mu\text{s} = 0.79\mu\text{s}$$

Using equation 7 to check  $t_f$ :

$$t_f = 0.222\mu\text{s}$$

which is less than  $0.3\mu\text{s}$ .

Using equation 1 to check  $V_{OL}$ :

$$V_{OL} = (3.3 \cdot 700) / [700 + (27 \cdot 10^3)] = 83\text{mV}$$

which is less than  $0.4\text{V}$ .

And using equation 2 to check the initial slew rate:

$$\text{SR} = 3.3 / [(27 \cdot 10^3) \cdot (200 \cdot 10^{-12})] = 0.61\text{V}/\mu\text{s}$$

which is greater than  $0.5\text{V}/\mu\text{s}$ .

Therefore, the value of  $R_P$  chosen is  $27\text{k}\Omega$ .

### ACK Data Setup Time

Care must be taken in selecting the value of  $R_S$  (in series with the pull-down driver) to ensure that the data setup time requirement for ACK (acknowledge) is fulfilled. An acknowledge is accomplished by the SMBus host releasing the SDA line (pulling high) at the end of the last bit sent and the SMBus slave device pulling the SDA line low before the rising edge of the ACK clock pulse.

The LTC1694-1  $2.2\text{mA}$  pull-up current is activated when the SMBus host releases the SDA line, allowing the voltage to rise above the LTC1694-1's comparator threshold of  $0.65\text{V}$ . If an SMBus slave device has a high value of  $R_S$ , a longer time is required for this SMBus slave device to pull SDA low before the rising edge of the ACK clock pulse.

To ensure sufficient data setup time for ACK, SMBus slave devices with high values of  $R_S$ , should pull the SDA low earlier. Typically, a minimum setup time of  $1.5\mu\text{s}$  is needed for an SMBus device with an  $R_S$  of  $700\Omega$  and a bus capacitance of  $200\text{pF}$ .

An alternative is that the SMBus slave device can hold SCL line low until the SDA line reaches a stable state. Then, SCL can be released to generate the ACK clock pulse.

### Connecting Multiple LTC1694-1 in Parallel

The LTC1694-1 is designed to guarantee a maximum SMBus rise time of  $1\mu\text{s}$  with a bus capacitance of  $200\text{pF}$ . In some cases where the bus capacitance is higher than  $200\text{pF}$ , multiple LTC1694-1s can be connected in parallel to provide a higher pull-up current to meet the rise time requirement. Figure 3 shows a typical application with two LTC1694-1s connected in parallel to supply a pull-up current of  $4.4\text{mA}$ .

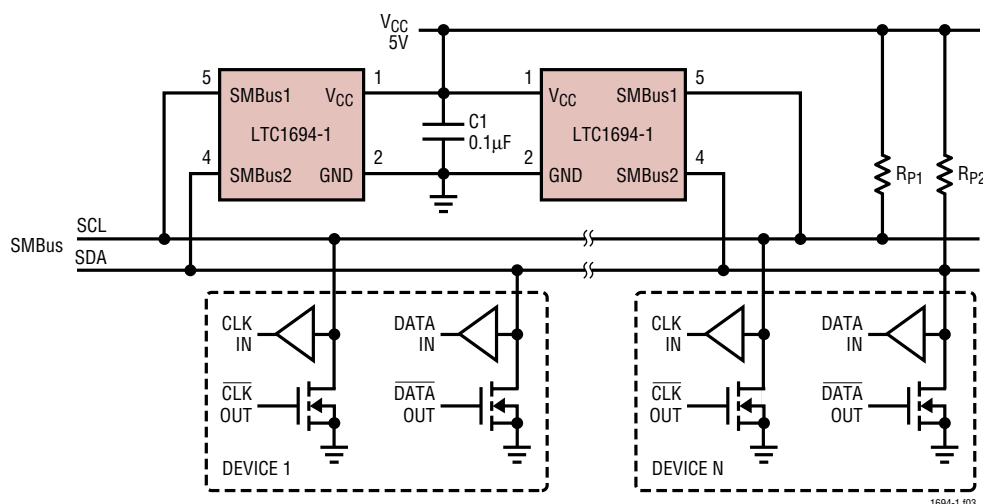
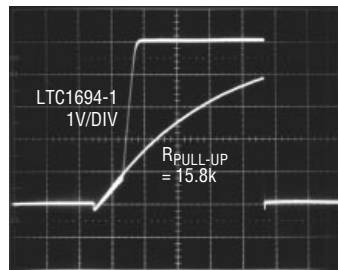


Figure 3. Paralleling Two LTC1694-1 to Provide  $4.4\text{mA}$  of Pull-Up Current

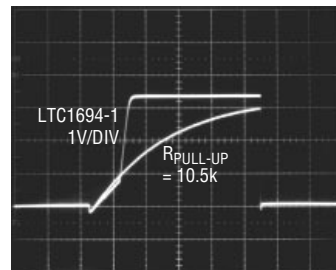
## APPLICATIONS INFORMATION

## Comparison of SMBus Waveforms for the LTC1694-1 vs Resistor Pull-Up



$V_{CC} = 5V$   
 $C_{LD} = 200pF$   
 $f_{SMBus} = 100kHz$

1694 TA03

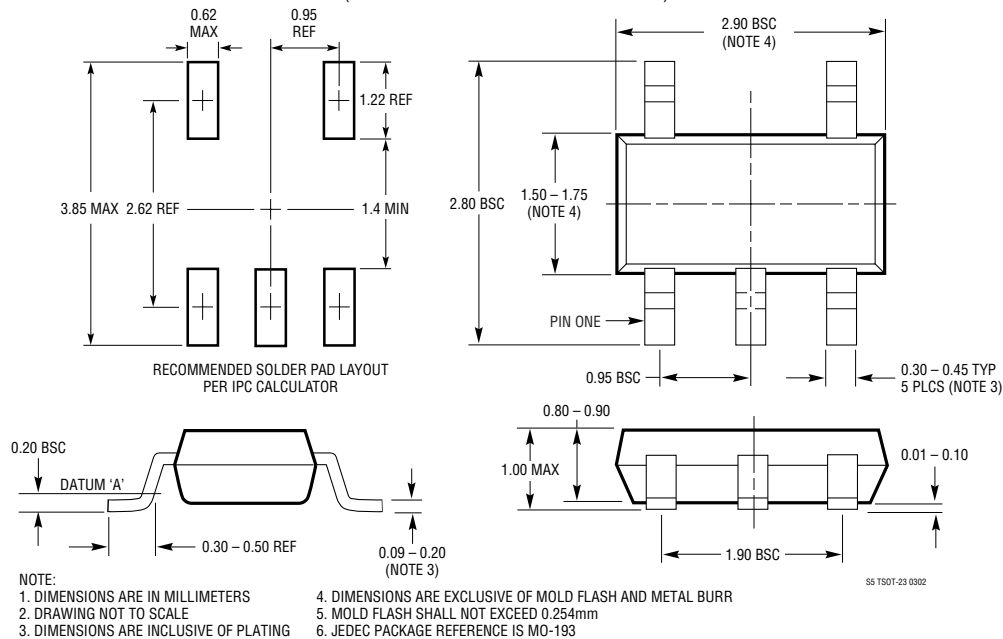


$V_{CC} = 3.3V$   
 $C_{LD} = 200pF$   
 $f_{SMBus} = 100kHz$

1694 TA04

## PACKAGE DESCRIPTION

**S5 Package**  
**5-Lead Plastic TSOT-23**  
 (Reference LTC DWG # 05-08-1635)



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1380/LTC1393	8-Channel/4-Channel Analog Multiplexer with SMBus interface	Low $R_{ON}$ and Low Charge Injection
LTC1427	10-Bit Current DAC with SMBus Interface	50 $\mu$ A Full-Scale Current
LTC1623	Dual High Side Switch Controller with SMBus Interface	8 Selectable Addresses/16 Channel Capability
LTC1663	SMBus Interface 10-Bit Rail-to-Rail Micropower DAC	DNL < 0.75LSB Max, 5-Lead SOT-23 Package
LTC1694	SMBus Accelerator	Includes DC and AC Pull-Up Current
LT1786F	SMBus-Controlled CCFL Switching Regulator	1.25A, 200kHz, Floating or Grounded Lamp Configurations
LTC4300A-1/LTC4300A-2	Hot Swappable 2-Wire Bus Buffers	Provides Capacitance Buffering, SDA and SCL Hot Swapping, Level Shifting

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