Data Sheet

LT8292

60V Low I_Q Full-Featured Synchronous Buck-Boost Controller

FEATURES

- **4-Switch Single Inductor Architecture that Allows V_{IN} Above, Below, or Equal to V_{OUT}**
- **Proprietary Buck-Boost Peak Current Mode**
- **Low Ripple Burst Mode: 30µA I_Q**
- **Forced Continuous Mode or Pulse-Skipping Operation**
- **Split Gate Driver Outputs**
- **Selectable Dead Time Settings**
- **Leaderless Current Sharing**
- Adjustable and Phase-lockable: 100kHz to 650kHz
- Spread Spectrum Frequency Modulation
- ±2% Output Voltage Accuracy: 1V ≤ V_{OUT} ≤ 60V
- ±5% Input or Output Average Current Accuracy
- Integrated Bootstrap Diodes
- V_{OUT} Disconnected from V_{IN} During Shutdown
- 38-Lead Thin Shrink Small Outline Package (TSSOP) with Exposed Pad
- Automotive Qualified

GENERAL DESCRIPTION

The LT8292 is a synchronous 4-switch buck-boost controller that regulates output voltage and output or input current from an input voltage above, below, or equal to the output voltage. The proprietary buck-boost peak current mode architecture allows adjustable and phase-lockable 100kHz to 650kHz fixed frequency operation, or internal spread spectrum operation for low electromagnetic interference (EMI). When the output is regulated above 5V, the LT8292 can operate from an input supply as low as 3V after start-up.

The low quiescent current at no-load extends operating run time in battery-powered systems. At light load, either forced continuous, pulse-skipping, or low-ripple Burst Mode can be selected.

The LT8292 features split pull-up/pull-down gate drivers and four selectable dead time settings with shoot-through protection, which allows both optimized efficiency and EMI. Fault protection is also provided to detect output short-circuit conditions, during which the LT8292 runs in low-duty cycle auto-retry mode.

APPLICATIONS

- Automotive, Industrial, Telecom Systems
- General Purpose Buck-Boost Power Supplies
- High-Power Battery-Powered Systems

TYPICAL APPLICATION DIAGRAM

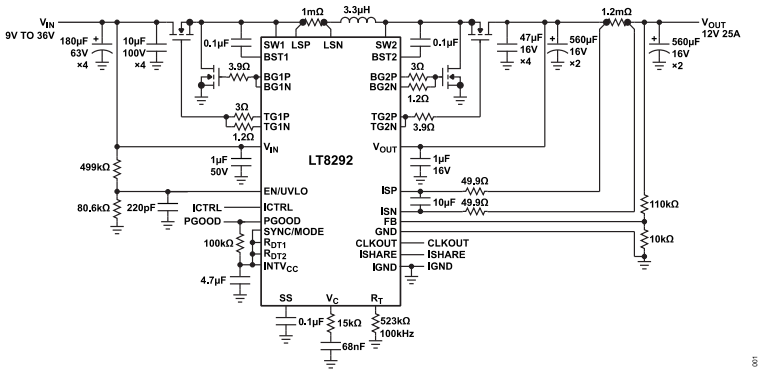

Figure 1. 98% Efficient 300W (12V 25A) Buck-Boost Voltage Regulator

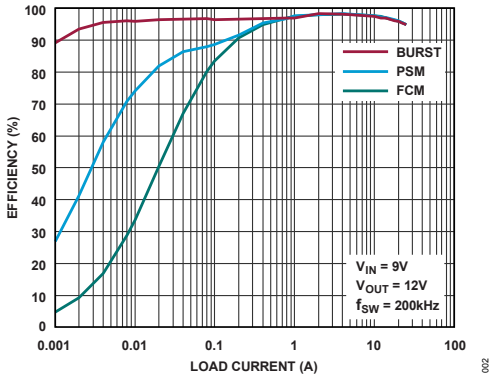

Figure 2. Efficiency vs Load Current

One Analog Way, Wilmington, MA 01887-2356, U.S.A. | Tel: 781.329.4700

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/24	Initial release	—

SPECIFICATIONS

Table 1. Electrical Characteristics

(Specifications are at T_A = 25°C[3]. V_{IN} = 12V, $V_{EN/UVLO}$ = 1.5V, R_T = 147kΩ to GND, C_{INTVCC} = 4.7µF to GND, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Supply						
V_{IN} Operating Voltage Range	V_{IN}	-40°C ≤ T_J ≤ 125°C, V_{OUT} < 5V	5.5		60	V
V_{IN} Quiescent Current	$I_{Q(IN)}$	$V_{EN/UVLO}$ = 0.3V		0.3	0.1	µA
		SYNC/MODE = OPEN, Not Switching		3.5	5	mA
		SYNC/MODE = 0V, Not Switching		30	50	µA
V_{OUT} Quiescent Current	$I_{Q(OUT)}$	$V_{EN/UVLO}$ = 0.3V, V_{OUT} = 12V		0.1	0.5	µA
		SYNC/MODE = OPEN, V_{OUT} = 12V		70		µA
Linear Regulators						
$INTV_{CC}$ Regulation Voltage	V_{INTVCC}	I_{INTVCC} = 20mA	4.85	5.0	5.15	V
$INTV_{CC}$ Current Limit	I_{INTVCC}	V_{INTVCC} = 4.7V, V_{OUT} = 0V		170	230	mA
$INTV_{CC}$ Undervoltage Lockout Threshold	V_{INTVCC}	Falling	3.4	3.55	3.7	V
$INTV_{CC}$ Undervoltage Lockout Hysteresis	V_{INTVCC}			0.25		V
Control Inputs/Outputs						
EN/UVLO Shutdown Threshold	$V_{EN/UVLO}$	Falling	0.3	0.6	1.0	V
EN/UVLO Enable Threshold	$V_{EN/UVLO}$	Rising, -40°C ≤ T_J ≤ 125°C	1.219	1.239	1.259	V
EN/UVLO Enable Hysteresis	$V_{EN/UVLO}$			55		mV
EN/UVLO Input Bias Current	$I_{EN/UVLO}$			0	0.1	µA
ICTRL Output Current	I_{ICTRL}	V_{ICTRL} = 1V, -40°C ≤ T_J ≤ 125°C	9.5	10	10.5	µA
Error Amplifier						
Full-Scale Current Regulation	$V_{(ISP-ISN)}$	V_{ICTRL} = 2V, V_{ISP} = 12V -40°C ≤ T_J ≤ 125°C	46	50	52	mV
		V_{ICTRL} = 2V, V_{ISP} = 0V -40°C ≤ T_J ≤ 125°C	47	50	52	
1/10th Current Regulation	$V_{(ISP-ISN)}$	V_{ICTRL} = 0.35V, V_{ISP} = 12V -40°C ≤ T_J ≤ 125°C	3	5	7	mV
		V_{ICTRL} = 0.35V, V_{ISP} = 0V -40°C ≤ T_J ≤ 125°C	3	5	7	
ISP/ISN Input Common Mode Range	V_{ISP}, V_{ISN}	-40°C ≤ T_J ≤ 125°C	0		60	V

(Specifications are at T_A = 25°C[3]. V_{IN} = 12V, $V_{EN/UVLO}$ = 1.5V, R_T = 147kΩ to GND, C_{INTVCC} = 4.7µF to GND, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
ISP Input Bias Current	I_{ISP}	V_{ISP} = V_{ISN} = 12V		20		µA
		V_{ISP} = V_{ISN} = 0V		-10		
		$V_{EN/UVLO}$ = 0V, V_{ISP} = V_{ISN} = 12V or 0V	-0.3	0	0.3	
ISP/ISN Input Bias Current Mismatch	I_{ISP} - I_{ISN}	V_{ISP} = V_{ISN} = 12V, -40°C ≤ T_J ≤ 125°C	-3	0	3	µA
		V_{ISP} = V_{ISN} = 0V, -40°C ≤ T_J ≤ 125°C	-10	0	10	
ISP/ISN Current Regulation Amplifier g_m	$g_{M(ISP-ISN)}$			3600		µS
FB Regulation Voltage	V_{FB}	-40°C ≤ T_J ≤ 125°C	0.98	1.00	1.02	V
FB Line Regulation	$\Delta V_{FB(LINE)}$	4V < V_{IN} < 60V, V_{OUT} = 12V		0.2	0.5	%
FB Voltage Regulation Amplifier	$g_{M(FB)}$			570		µS
FB Input Bias Current	I_{FB}	FB in regulation, Current out of Pin	-20	0	20	nA
V_C Output Impedance	R_{VC}			0.9		MΩ
Current Comparator						
Maximum Current Sense Threshold	$V_{(LSP-LSN)}$	Buck, V_{FB} = 0.8V -40°C ≤ T_J ≤ 125°C	41	50	59	mV
		Boost, V_{FB} = 0.8V -40°C ≤ T_J ≤ 125°C	44	50	56	
Fault						
FB Short Threshold	V_{FB}	Falling	0.22	0.25	0.27	V
FB Short Hysteresis	V_{FB}	Hysteresis	40	50	60	mV
PGOOD Upper Threshold Offset from V_{FB}	ΔV_{FB}	Rising	6	8	10	%
PGOOD Lower Threshold Offset from V_{FB}	ΔV_{FB}	Falling	-10	-8	-6	%
PGOOD Pull-Down Resistance	R_{PGOOD}			100	200	Ω
SS Strong Pull-Down Resistance	R_{SS}			50		Ω
SS Pull-Up Current	I_{SS}	V_{FB} = 0.8V, V_{SS} = 0V	10.5	13	16	µA
SS Pull-Down Current	I_{SS}	V_{FB} = 1.0V, V_{SS} = 2V	0.8	1.25	1.6	µA
Oscillator						
Switching Frequency	f_{SW}	R_T = 523kΩ	95	100	105	kHz
		R_T = 258kΩ	190	200	210	
		R_T = 147kΩ	330	350	370	
SYNC Frequency	f_{SW}	$f_{SYNC/MODE}$ = f_{RT}	100		650	kHz

(Specifications are at T_A = 25°C[3]. V_{IN} = 12V, $V_{EN/UVLO}$ = 1.5V, R_T = 147kΩ to GND, C_{INTVCC} = 4.7µF to GND, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
SYNC/MODE Threshold Voltage	$V_{SYNC/MODE}$		0.4		2.5	V
Highest Spread Spectrum Above Oscillator Frequency			22	25	28	%
NMOS Drivers						
TG1P, TG2P Gate Pull-Up Resistance	$R_{TG1, TG2}$	$V_{(BST-SW)}$ = 5V		2		Ω
TG1N, TG2N Gate Pull-Down Resistance	$R_{TG1, TG2}$	$V_{(BST-SW)}$ = 5V		1		Ω
BG1P, BG2P Gate Pull-Up Resistance	$R_{BG1, BG2}$	V_{INTVCC} = 5V		2		Ω
BG1N, BG2N Gate Pull-Down Resistance	$R_{BG1, BG2}$	V_{INTVCC} = 5V		1		Ω
TG Off to BG On Delay	$t_{DELAY(TG-BG)}$	$R_{DT1,2}$ = 0Ω to $INTV_{CC}$	25	40	55	ns
		$R_{DT1,2}$ = 130kΩ to GND		20		
		$R_{DT1, DT2}$ = 82kΩ to GND		10		
		$R_{DT1, DT2}$ = 51kΩ to GND		2		
BG Off to TG On Delay	$t_{DELAY(BG-TG)}$	$R_{DT1, DT2}$ = 0Ω to $INTV_{CC}$	25	40	55	ns
		$R_{DT1, DT2}$ = 130kΩ to GND		20		
		$R_{DT1, DT2}$ = 82kΩ to GND		10		
		$R_{DT1, DT2}$ = 51kΩ to GND		2		

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ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
V_{IN}, EN/UVLO, V_{OUT}, ISP, ISN	–0.3V to 60V
(ISP–ISN)	–1V to 1V
BST1, BST2	–0.3V to 66V
SW1, SW2, LSP, LSN	–5V to 60V
$INTV_{CC}$, (BST1–SW1), (BST2–SW2)	–0.3V to 6V
(BST1–LSP), (BST1–LSN)	–0.3V to 6V
FB, SYNC/MODE, PGOOD, ICTRL	–0.3V to 6V
IGND	–0.3V to 0.3V
TG1P, TG1N, BG1P, BG1N	(*Note 2*)
TG2P, TG2N, BG2P, BG2N	(*Note 2*)
R_{DT1}, R_{DT2}, R_T, CLKOUT, ISHARE, V_C, SS	(*Note 2*)
Operating Junction Temperature Range [3,4]	-40°C to 125°C

1 Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

2 Do not apply a positive or negative voltage source to these pins, otherwise permanent damage may occur.

3 The LT8292 is specified over -40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes.

4 The LT8292 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

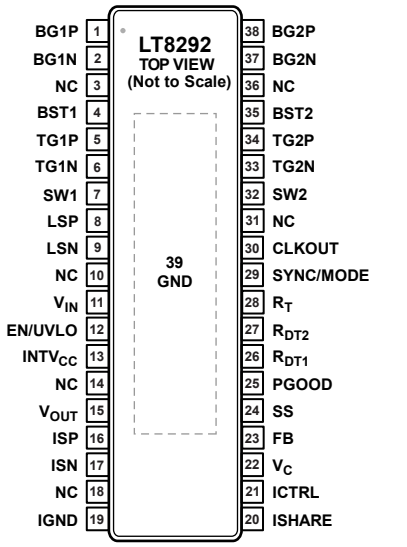


Figure 3. Pin Configuration

Table 3. Pin Descriptions

PIN	NAME	DESCRIPTION
1	BG1P	Buck Side Bottom Gate Driver Pull-Up Output. Drives the gate of buck side bottom N-Channel MOSFET with a voltage swing from ground to $INTV_{CC}$.
2	BG1N	Buck Side Bottom Gate Driver Pull-Down Output. Drives the gate of buck side bottom N-Channel MOSFET with a voltage swing from ground to $INTV_{CC}$.
4	BST1	Buck Side Bootstrap Floating Driver Supply. The BST1 pin has an integrated bootstrap Schottky diode from the $INTV_{CC}$ pin and requires an external bootstrap capacitor to be connected to the SW1 pin. The BST1 pin swings from INTVCC to (V_{IN} + $INTV_{CC}$).
5	TG1P	Buck Side Top Gate Driver Pull-Up Output. Drives the gate of buck side top N-Channel MOSFET with a voltage swing from SW1 to BST1.
6	TG1N	Buck Side Top Gate Driver Pull-Down Output. Drives the gate of buck side top N-Channel MOSFET with a voltage swing from SW1 to BST1.
7	SW1	Buck Side Switch Node. The SW1 pin swings from a Schottky diode voltage drop below ground up to V_{IN}.
8	LSP	Positive Terminal of the Inductor Current Sense Resistor (R_{SENSE}). Ensure accurate current sense with Kelvin connection.
9	LSN	Negative Terminal of the Inductor Current Sense Resistor (R_{SENSE}). Ensure accurate current sense with Kelvin connection.

11	V_{IN}	Input Supply. The V_{IN} pin must be connected to the power input to determine the buck, boost, or buck-boost operation regions. Locally bypass this pin to ground with a ceramic capacitor.
12	EN/UVLO	Enable and Undervoltage Lockout. Force the pin to the ground to shut down the part and reduce the V_{IN} quiescent current below 0.3µA. Force the pin above 1.239V for normal operation. The accurate 1.18V falling threshold can be used to program an undervoltage lockout (UVLO) threshold with a resistor divider from V_{IN} to the ground.
13	$INTV_{CC}$	Internal 5V Linear Regulator Output. The $INTV_{CC}$ linear regulator is intelligently powered from either V_{IN} or V_{OUT} pins. The split gate drivers and control circuits are powered from this voltage. Bypass this pin to the ground with a minimum 4.7µF ceramic capacitor.
15	V_{OUT}	Output Supply. The V_{OUT} pin must be tied to the power output to determine the buck, boost, or buck-boost operation regions. Locally bypass this pin to ground with a ceramic capacitor.
16	ISP	Positive Terminal of the ISP/ISN Current Sense Resistor (R_{IS}). Ensure accurate current sense with Kelvin connection.
17	ISN	Negative Terminal of the ISP/ISN Current Sense Resistor (R_{IS}). Ensure accurate current sense with Kelvin connection.
19	IGND	Local Ground for Leader-less Current Sharing. When paralleling, kelvin all IGND pins to a common ground. See the *Paralleling Multiple Regulators* in the *Applications Information* section for more details. When not in use, connect the pin to the ground.
20	ISHARE	Leaderless Current Sharing Input for Paralleling. Together with the IGND pin, this pin allows equal output current sharing among multiple LT8292s in parallel, enabling higher output current, and better heat management. Each LT8292 independently regulates the average output current, eliminating the need for a leader controller. For parallel applications, tie the ISHARE pins of all the LT8292s together. See the *Paralleling Multiple Regulators* in the *Applications Information* section for more details. When not in use, leave the pin floating.
21	ICTRL	Control Input for ISP/ISN Current Sense Threshold. The ICTRL pin generates a 10µA current and is used to program the ISP/ISN current limit: $$I_{IS(MAX)} = \frac{min(V_{ICTRL} - 0.25V, 1V)}{20 \cdot R_{IS}}$$ The V_{ICTRL} can be set by a voltage drop of an external resistor (R_{ICTRL}) from the ICTRL pin to ground: $V_{ICTRL} = 10\mu A \cdot R_{ICTRL}$ For $0.35V \le V_{ICTRL} \le 1.15V$, the current sense threshold linearly goes up from 5mV to 45mV. For $V_{ICTRL} \ge 1.35V$, the current sense threshold is constant at 50mV full-scale value. For $1.15V \le V_{ICTRL} \le 1.35V$, the current sense threshold smoothly transitions from the linear function of V_{ICTRL} to the 50mV constant value. Connect ICTRL to $INTV_{CC}$ for the 50mV full-scale threshold or when not in use.
22	V_C	Error Amplifier Output to Set Inductor Current Comparator Threshold. The V_C pin is used to compensate the control loop with an external RC network.

23	FB	Voltage Loop Feedback Input. The FB pin is used for constant-voltage regulation and output fault protection. The internal error amplifier with output V_C regulates V_{FB} to 1.0V through the DC/DC converter. During the output short circuit (V_{FB} < 0.25V) condition, the part runs in low-duty cycle auto-retry mode. During an overvoltage (V_{FB} > 1.8V) condition, the part stops switching.
24	SS	Soft-Start Timer Setting. The SS pin is used to set the soft-start timer by connecting a capacitor to the ground. An internal 13µA pull-up current charging the external SS capacitor gradually ramps up the FB regulation voltage. A 0.1µF capacitor is recommended on this pin. Any UVLO or thermal shutdown immediately pulls the SS pin to the ground and stops switching.
25	PGOOD	Power Good Open Drain Output. The PGOOD pin is pulled high externally when the FB pin is within ±8% of the final regulation voltage. To function, the pin requires an external pull-up resistor.
26	R_{DT1}	Buck Side Switching Dead Time Setting. Connect a resistor from this pin to the ground to select one of four dead time settings.
27	R_{DT2}	Boost Side Switching Dead Time Setting. Connect a resistor from this pin to the ground to select one of four dead time settings.
28	R_T	Switching Frequency Setting. Connect a resistor from this pin to the ground to set the internal oscillator frequency from 100kHz to 650kHz.
29	SYNC/MODE	External Frequency Synchronization and Operation Mode Selection. This pin allows the following selectable modes for optimization of performance: ▶ External clock: For external frequency synchronization and forced continuous mode at light load. ▶ $INTV_{CC}$: For spread spectrum around internal oscillator frequency and forced continuous mode at light load. ▶ Float: For internal oscillator frequency and forced continuous mode at light load. ▶ 100kΩ to GND: For internal oscillator frequency and pulse skipping mode at light load. ▶ GND: For internal oscillator frequency and low ripple burst mode at light load.
30	CLKOUT	Digital Clock Output. Use this pin to synchronize one or more LT8292 ICs in parallel. The CLKOUT pin provides 180° out-of-phase and 50% duty cycle clock signal at the switching frequency set by the internal oscillator or the external frequency synchronization using the SYNC/MODE pin.
32	SW2	Boost Side Switch Node. The SW2 pin swings from a Schottky diode voltage drop below ground to V_{OUT}.
33	TG2N	Boost Side Top Gate Driver Pull-Down Output. Drives the gate of buck side top N-Channel MOSFET with a voltage swing from SW2 to BST2.
34	TG2P	Boost Side Top Gate Driver Pull-Up Output. Drives the gate of buck side top N-Channel MOSFET with a voltage swing from SW2 to BST2.

35	BST2	Buck Side Bootstrap Floating Driver Supply. The BST2 pin has an integrated bootstrap Schottky diode from the $INTV_{CC}$ pin and requires an external bootstrap capacitor to be connected to the SW1 pin. The BST2 pin swings from INTVCC to (V_{IN} + $INTV_{CC}$).
37	BG2N	Boost Side Bottom Gate Driver Pull-Down Output. Drives the gate of buck side bottom N-Channel MOSFET with a voltage swing from ground to INTVCC.
38	BG2P	Boost Side Bottom Gate Driver Pull-Up Output. Drives the gate of buck side bottom N-Channel MOSFET with a voltage swing from ground to $INTV_{CC}$.
39	GND (Exposed Pad)	Ground. Solder the exposed pad directly to the ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

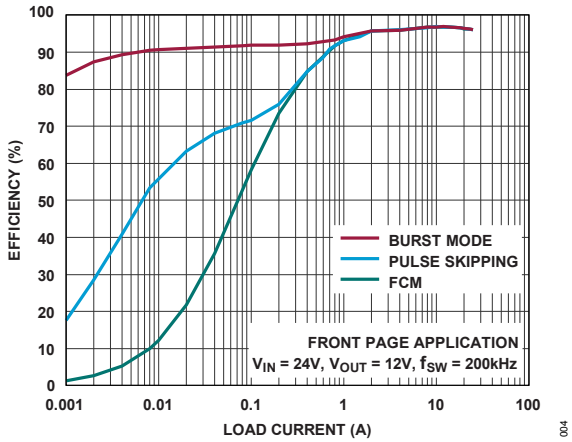


Figure 4. Efficiency vs Load Current (Buck Region)

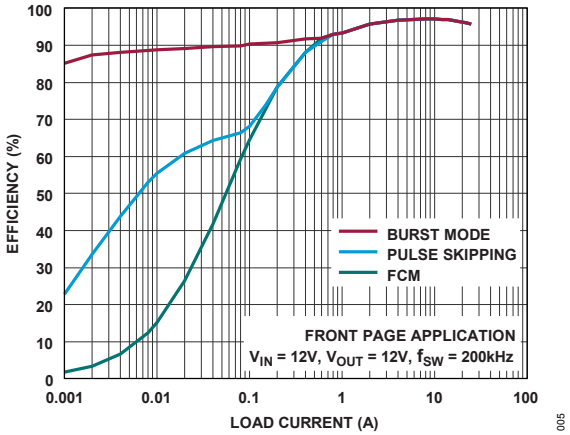


Figure 5. Efficiency vs Load Current (Buck–Boost Region)

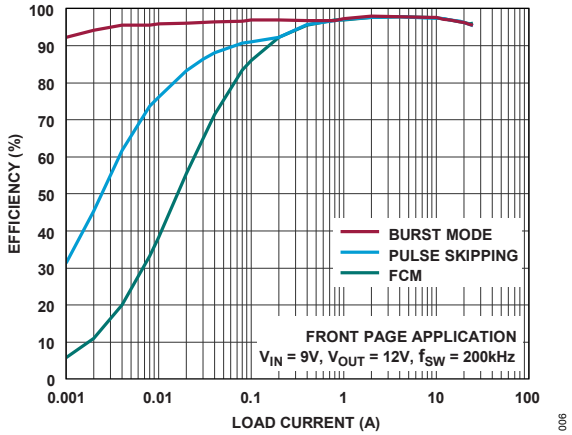


Figure 6. Efficiency vs Load Current (Boost Region)

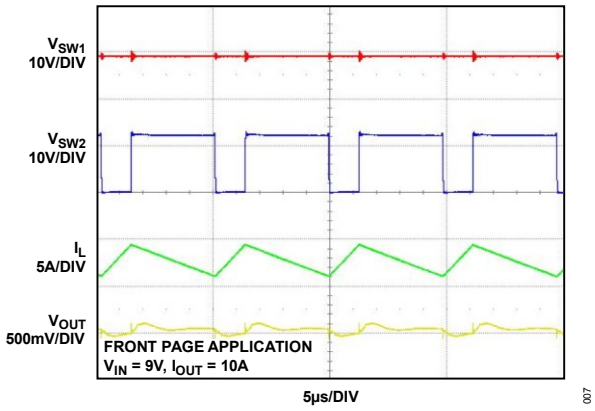


Figure 7. Switching Waveforms (Boost Region)

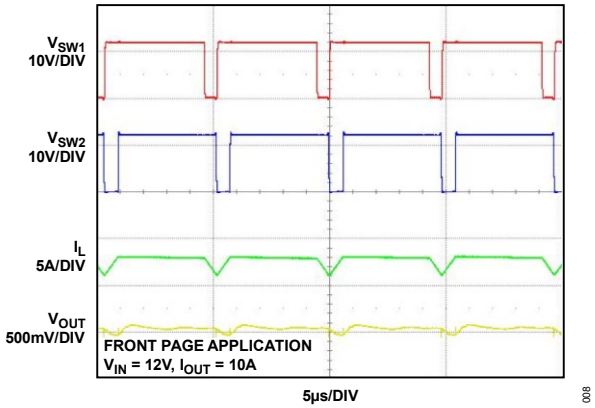


Figure 8. Switching Waveforms (Buck–Boost Region)

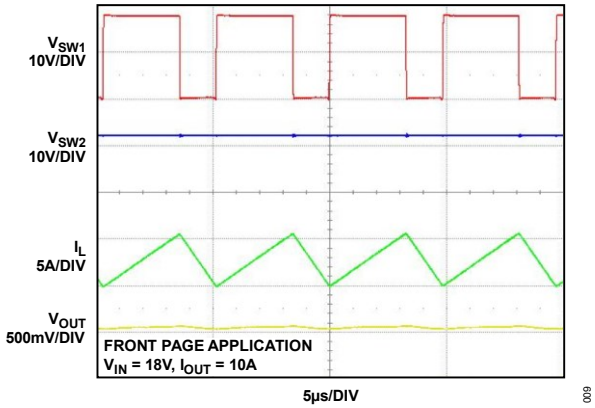


Figure 9. Switching Waveforms (Buck Region)

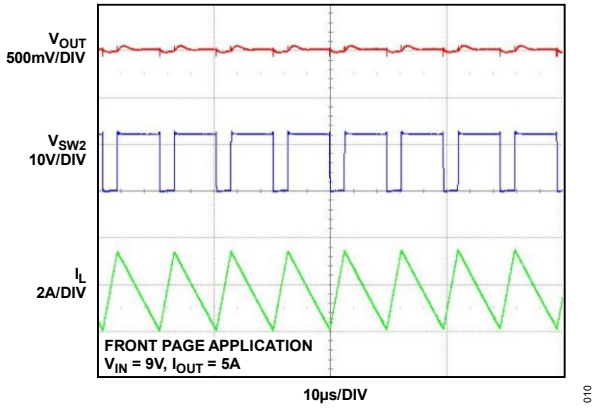


Figure 10. Switching Waveforms (FCM)

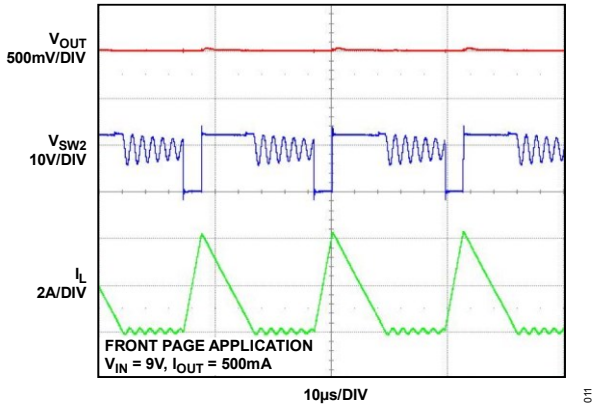


Figure 11. Switching Waveforms (PSM/Light–Burst Mode)

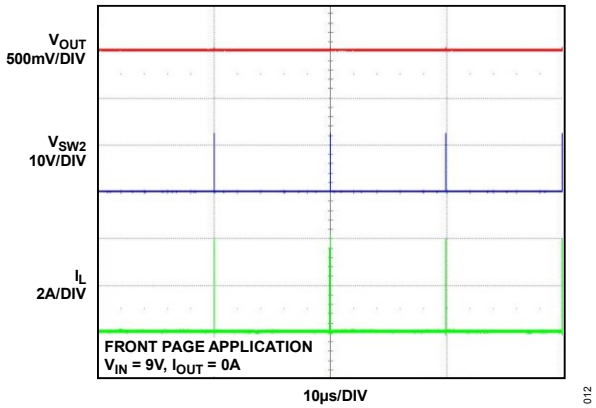


Figure 12. Switching Waveforms (Deep–Burst Mode)

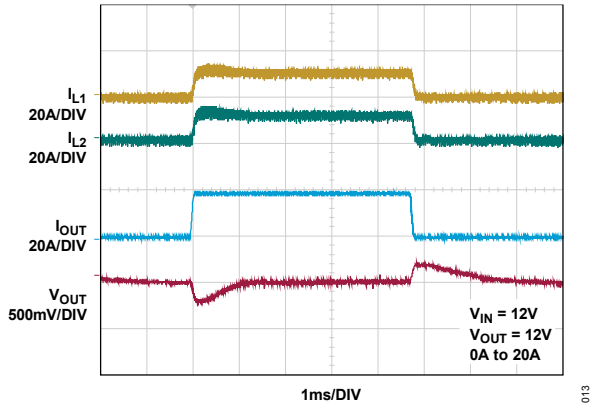


Figure 13. 2-Phase Parallel Operation (Load Transient)

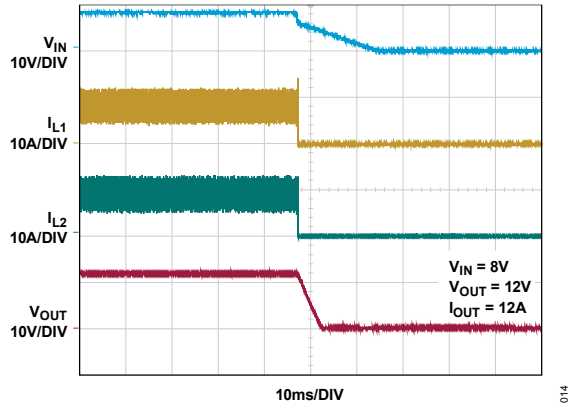


Figure 14. 2-Phase Parallel Operation (Shutdown)

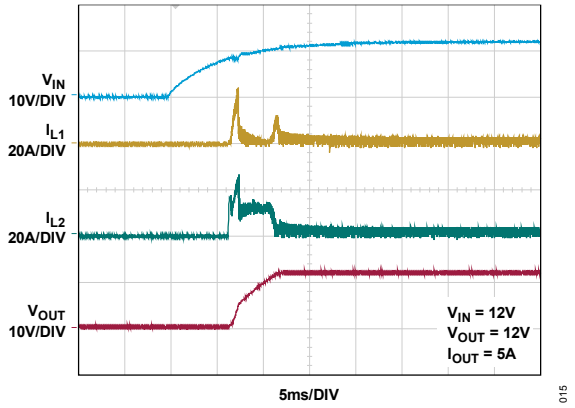


Figure 15. 2-Phase Parallel Operation (Start-Up)

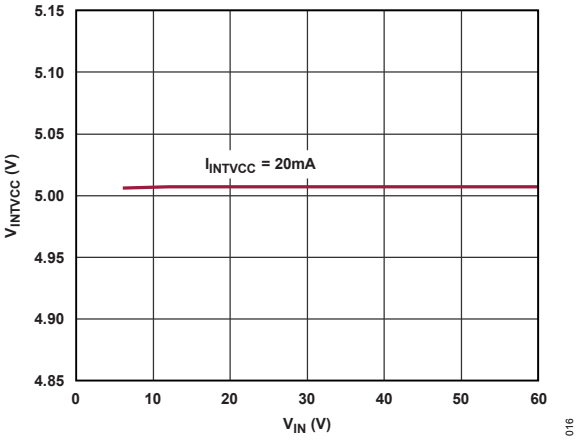


Figure 16. $INTV_{CC}$ Voltage vs V_{IN}

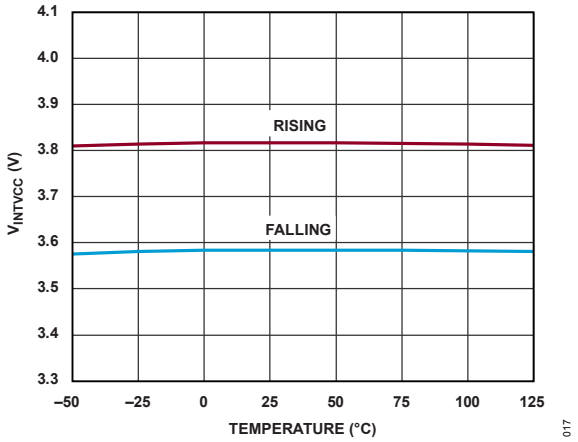


Figure 17. $INTV_{CC}$ UVLO Threshold

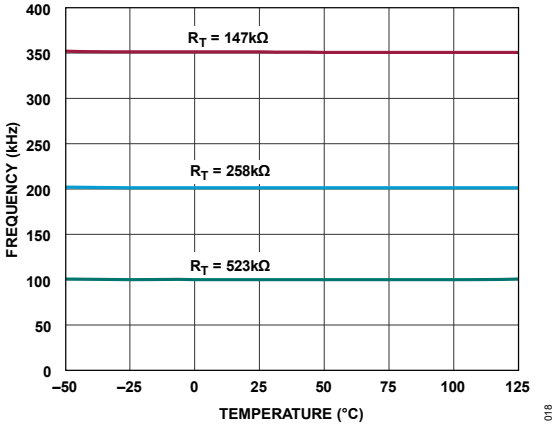


Figure 18. Oscillator Frequency vs Temperature

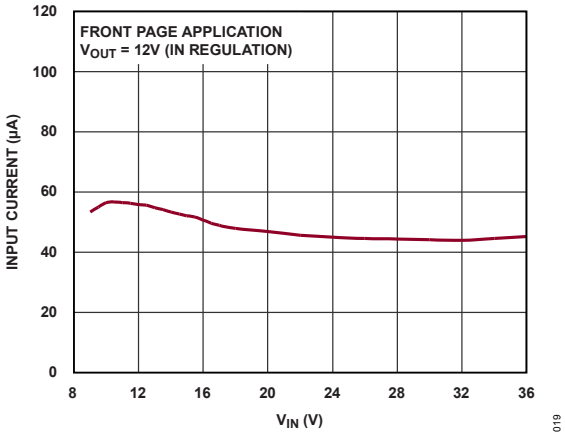


Figure 19. No Load Supply Current vs V_{IN}

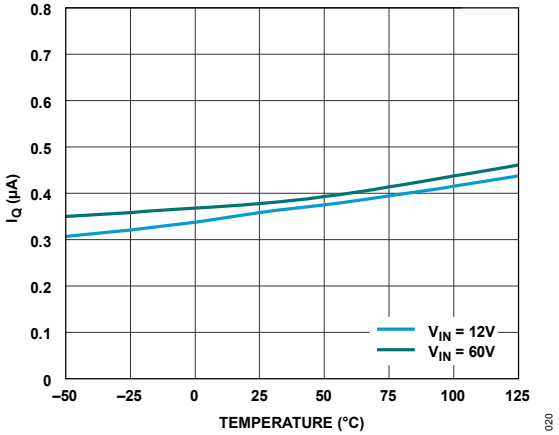


Figure 20. V_{IN} Quiescent Current (V_{EN}/V_{UVLO} = 0.3V)

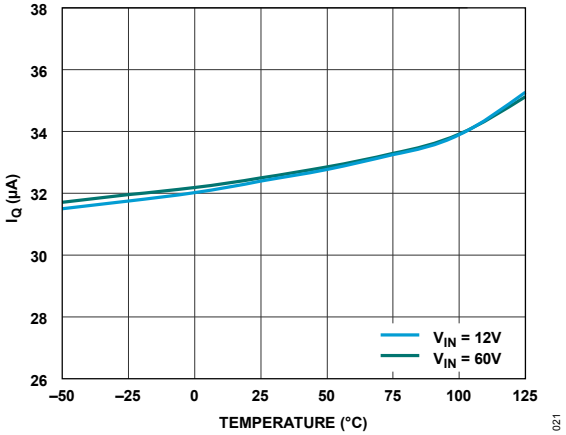


Figure 21. V_{IN} Quiescent Current (SYNC/MODE = 0V)

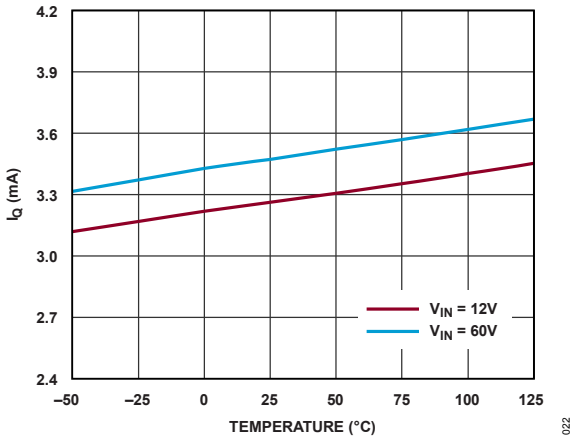


Figure 22. V_{IN} Quiescent Current (SYNC/MODE = OPEN)

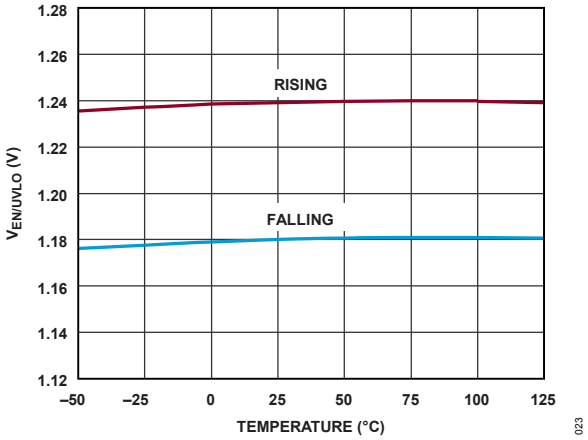


Figure 23. EN/UVLO Enable Threshold

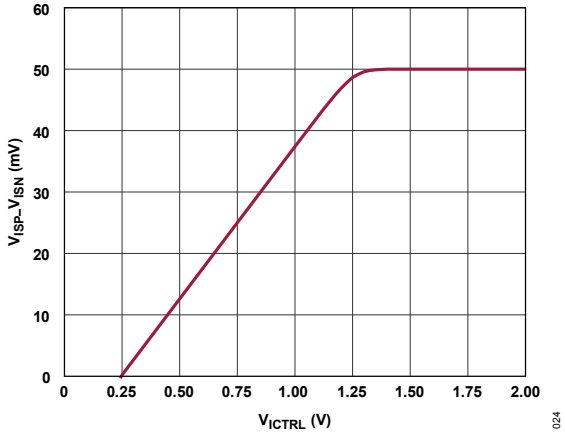


Figure 24. V_{ISP}–V_{ISN} Regulation vs V_{CTRL}

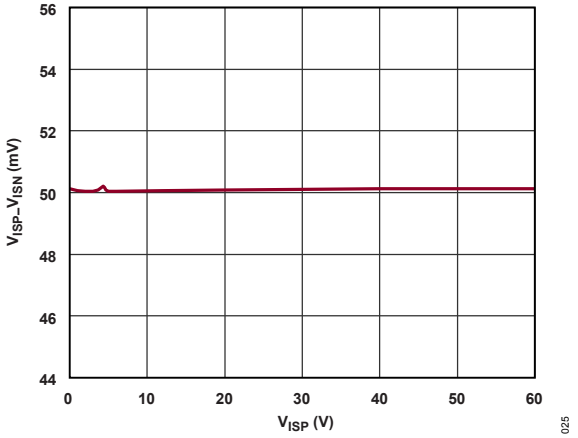


Figure 25. V_{ISP}–V_{ISN} Regulation vs V_{ISP}

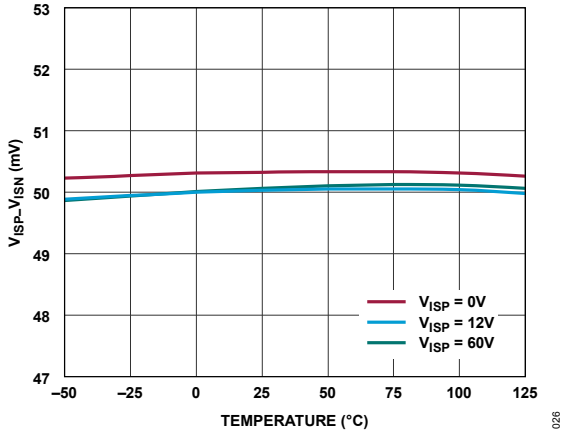


Figure 26. V_{ISP}–V_{ISN} Regulation vs Temperature

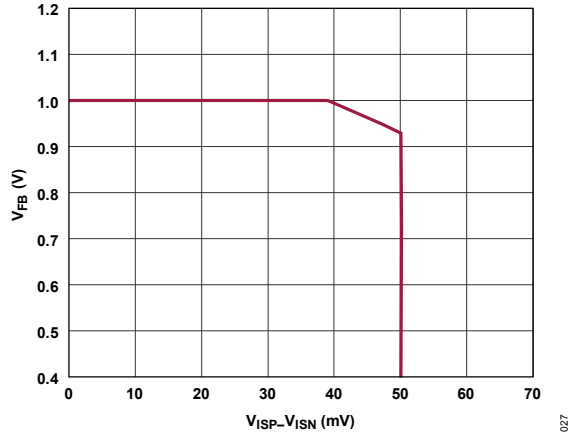


Figure 27. V_{FB} vs V_{ISP}–V_{ISN} Regulation

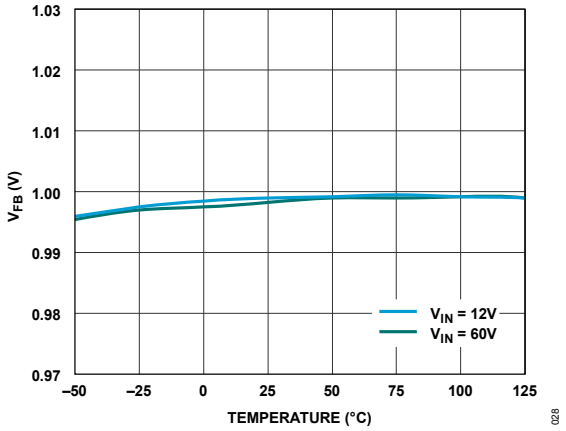


Figure 28. V_{FB} Regulation vs Temperature

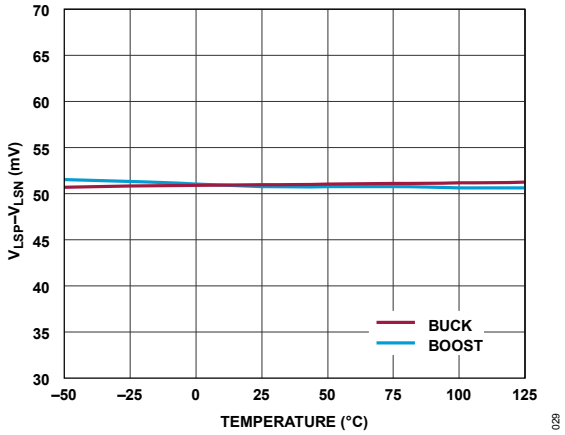


Figure 29. Maximum Current Sense vs Temperature

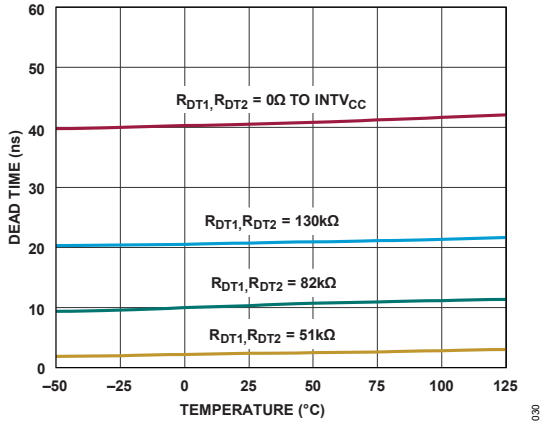


Figure 30. Switching Dead Time vs Temperature

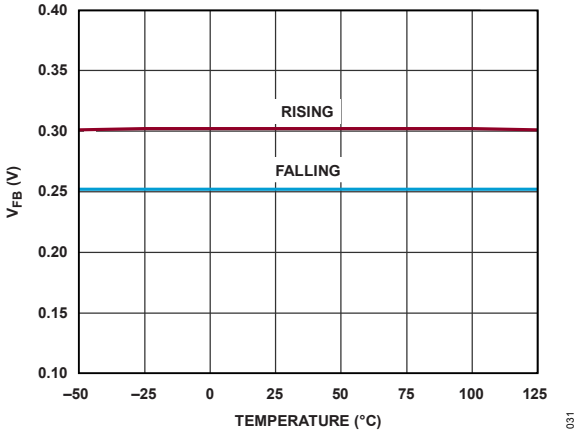


Figure 31. FB Short Threshold

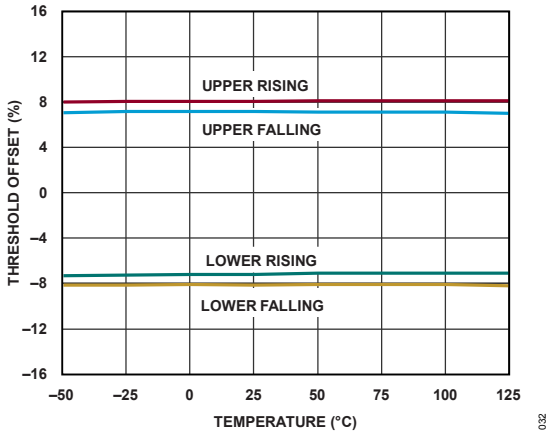


Figure 32. PGOOD Threshold

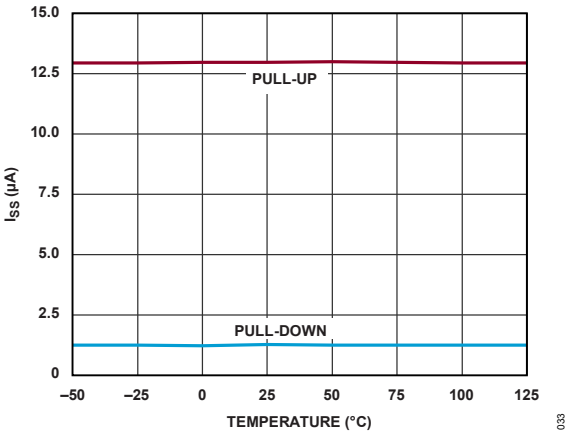


Figure 33. SS Current vs Temperature

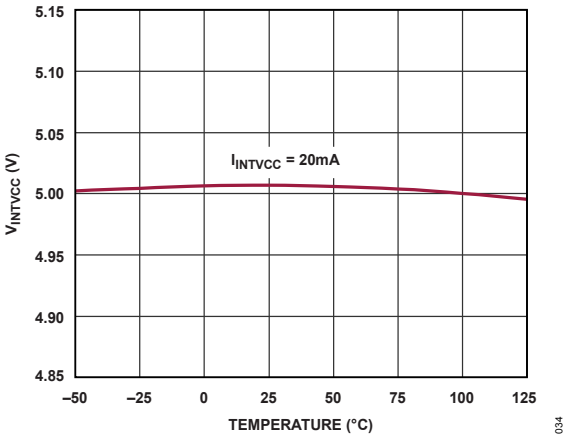


Figure 34. $INTV_{CC}$ Voltage vs Temperature

BLOCK DIAGRAM

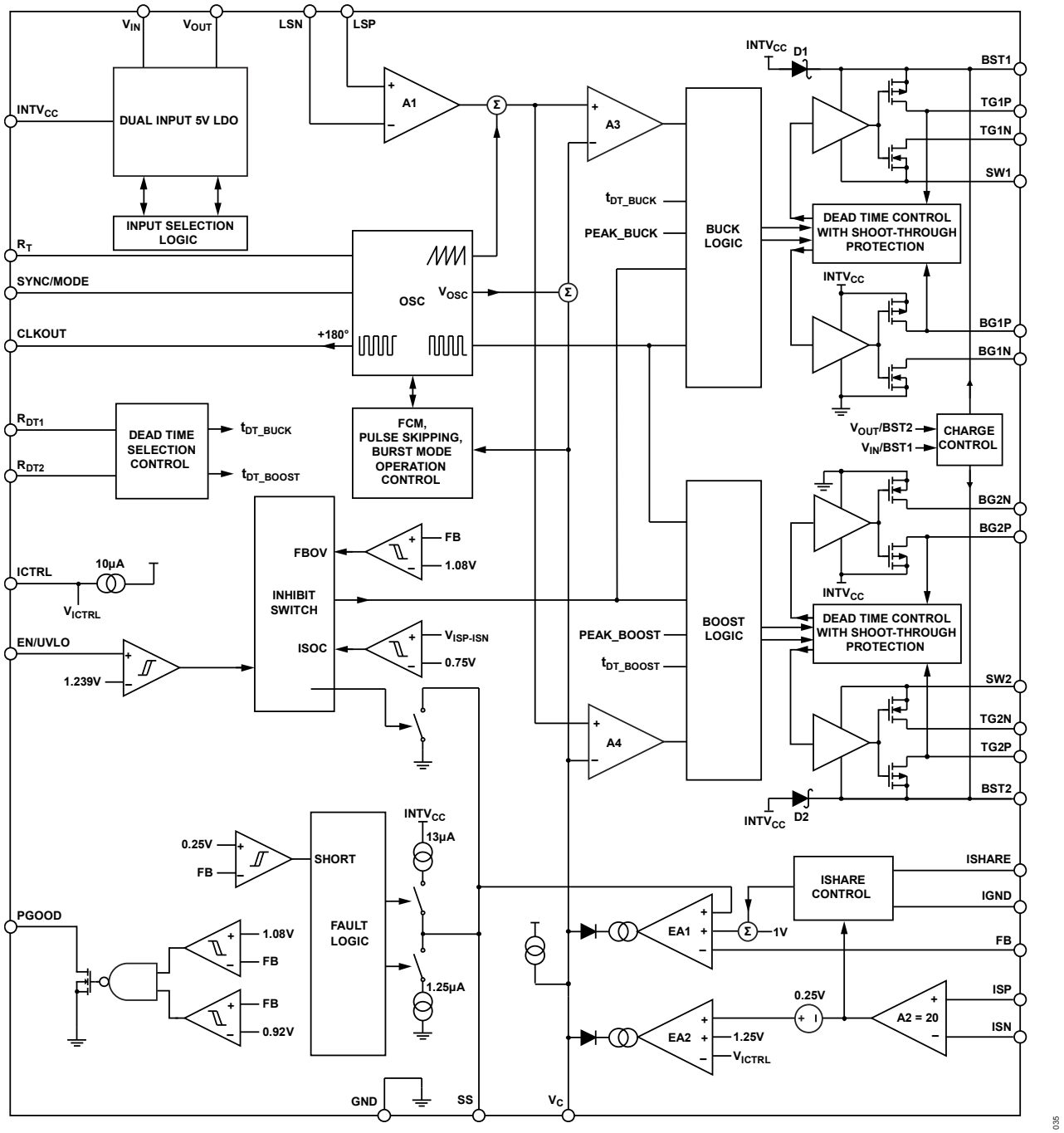


Figure 35. Block Diagram

THEORY OF OPERATION

The LT8292 is a 60V current mode synchronous DC/DC controller that can regulate output voltage, input or output current from input voltage above, below, or equal to the output voltage. The new generation ADI proprietary buck-boost dual edge peak current mode control scheme uses a direct inductor current sense resistor and guarantees the lowest inductor current ripple for improved power efficiency while enabling a smooth transition between buck region, buck-boost region, and boost region.

The synchronous power switch controller with split pull-up and pull-down gate pins allows applications to use a wide range of pull-up gate resistance to improve EMI performance without compromising the pull-down strength of the driver. Moreover, the LT8292's split gate driver architecture can monitor the true gate voltage of the power switches and thus provide more robust and accurate dead times, which can also be programmable from 2ns to 40ns.

The internal control circuitry and gate drivers in LT8292 are powered by the dual input $INTV_{CC}$ linear regulator (LDO). Intelligently selecting the input source from either the V_{IN} pin or V_{OUT} pin further optimizes efficiency across all loads and enables the controller to provide enough gate drive capability.

To optimize efficiency at light load, the LT8292 operates in low ripple Burst Mode operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the input supply current to 32µA. In a typical application, less than 60µA will be consumed from the input supply when regulating 12V output with no load. The LT8292's low-ripple Burst Mode operation guarantees only a single burst pulse switching while maintaining a tight output regulation performance with minimum ripple even under deep or no-load burst conditions. The SYNC/MODE is tied low to use Burst Mode operation and can be tied with 100kΩ to GND or float to use pulse-skipping mode or force continuous mode (FCM), respectively. If a clock is applied to the SYNC/MODE pin, the part will synchronize to an external clock frequency and operate in FCM.

When in FCM, the oscillator operates continuously, and positive SW transitions are aligned to the clock. A negative inductor current is allowed. In this mode, the LT8292 can sink current from the output and return this charge to the input, improving load-step transient response.

If the EN/UVLO pin is low, the LT8292 is shut down and consumes only 0.3µA (typical) from the input. When the EN/UV pin is above 1.239V, the switching controller will become active.

To improve EMI, the LT8292 can operate in spread spectrum mode. This feature varies the clock with a triangular frequency modulation of +25%. For example, if the LT8292 frequency is programmed to switch at 400kHz, spread spectrum mode will modulate the oscillator between 400kHz and 500kHz. The SYNC/MODE pin is to be tied high to $INTV_{CC}$ to use spread spectrum modulation with FCM.

To expand the buck-boost controller into a kilowatt power level, the LT8292 features a leaderless current sharing scheme using the ISHARE and the IGND pins, allowing higher load current and better heat management. A CLKOUT pin enables synchronizing other regulators with the LT8292.

Comparators monitoring the FB pin voltage will pull the PGOOD pin low if the output voltage varies more than ±8% (typical) from the set point, or if a fault condition is present.

See the *Block Diagram* for the best understanding of LT8292's operation.

Power Switch Control

Figure 36 shows a simplified diagram of how the four power switches, A, B, C, and D, are connected to the inductor L, the current sense resistor R_{SENSE}, the power input V_{IN}, the power output V_{OUT}, and the ground. The current sense resistor R_{SENSE} connected to the LSP and LSN pins provides inductor current information for both peak current mode control and reverse current detection in buck region, buck-boost region, and boost region. *Figure 37* shows the operation region as a function of the V_{IN}/V_{OUT} ratio. The power switches are properly controlled to smoothly transition between modes and regions. Hysteresis is added to prevent chattering between modes and regions. There are a total of three states: (1) Peak-buck current mode control in the buck region, (2) Peak-boost peak-buck current mode control in the buck-boost region, and (3) Peak-boost current mode control in the boost region. The following sections give detailed descriptions for each state with waveforms, in which the shoot-through protection dead time between switches A and B and between switches C and D are ignored for simplification.

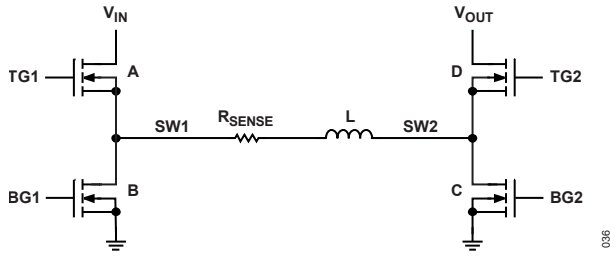


Figure 36. Simplified Diagram of the Power Switches

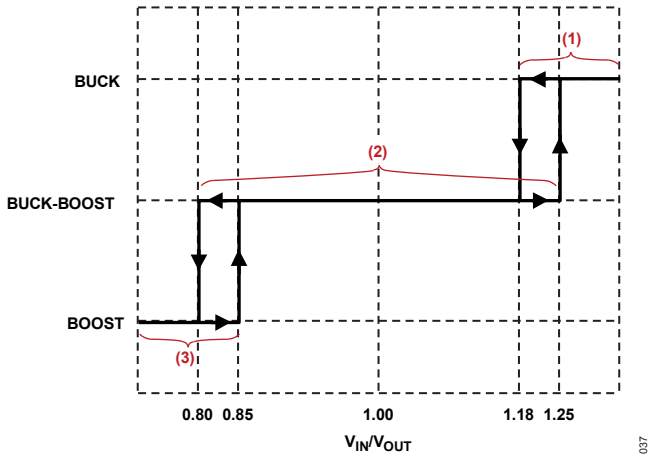


Figure 37. Operation Region vs V_{IN}/V_{OUT} Ratio

Peak-Buck in Buck Region (V_{IN} >> V_{OUT})

When V_{IN} is much higher than V_{OUT}, the LT8292 uses peak-buck current mode control in the buck region (See *Figure 38*). Switch C is always off and switch D is always on. At the beginning of every cycle, switch A is turned on and the inductor current ramps up. When the inductor current hits the peak buck current threshold commanded by V_C voltage at buck current comparator A3 during the (A+D) phase, switch A is turned off, and switch B is turned on for the rest of the cycle. Switches A and B will alternate, behaving like a typical synchronous buck regulator.

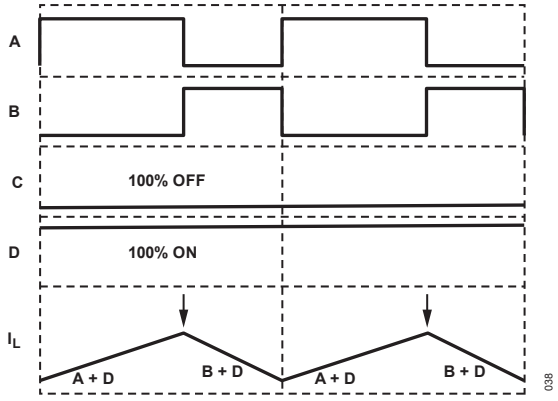


Figure 38. Peak-Buck in Buck Region (V_{IN} >> V_{OUT})

Peak-Boost Peak-Buck in Buck-Boost Region (V_{IN} ≈ V_{OUT})

When V_{IN} is equal to or slightly higher or lower than V_{OUT}, the LT8292 uses the dual edge peak-boost peak-buck current mode control in the buck-boost region (*Figure 39*, *Figure 40*, and *Figure 41*). At the beginning of every cycle, switches A and C are turned on (A+C phase). After the 10% cycle and when the inductor current hits the peak-boost current threshold commanded by V_C voltage at boost current comparator A4, switch C is turned off, and switch D is turned on for the rest of the cycle (A+D phase). Before the remaining 10% cycle and when the inductor current hits the peak buck current threshold commanded by V_C voltage at buck current comparator A3, switch A is turned off, and switch B is turned on for the rest of the cycle (B+D phase).

Switch C is always turned on for the beginning 10% cycle as a minimum duty (*Figure 40*), and switch B is always turned on for the remaining 10% cycle as a maximum duty (*Figure 41*). If the inductor current hits the peak boost current threshold before the beginning 10% cycle, the LT8292 uses only peak-buck current mode control during the (A+D) phase (*Figure 40*). Likewise, if the inductor current hits the peak buck current threshold after the remaining 10% cycle, the LT8292 uses only peak-boost current mode control during the (A+C) phase (*Figure 41*). When V_{IN} is equal to V_{OUT}, the LT8292 uses both peak boost and peak buck current mode controls within each cycle (*Figure 39*) as the inductor current firstly hits the peak boost current threshold immediately after the beginning 10% cycle and then secondly hits the peak buck current threshold just before the remaining 10% cycle. This dual edge current mode control scheme enables the 4-switch buck-boost operation to run always at its minimum switching duty ratio, leading to lower I_L ripple and improved power efficiency.

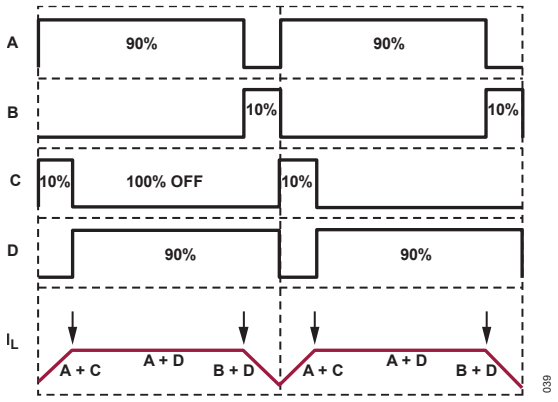


Figure 39. Peak-Boost Peak-Buck in Buck-Boost Region (V_{IN} = V_{OUT})

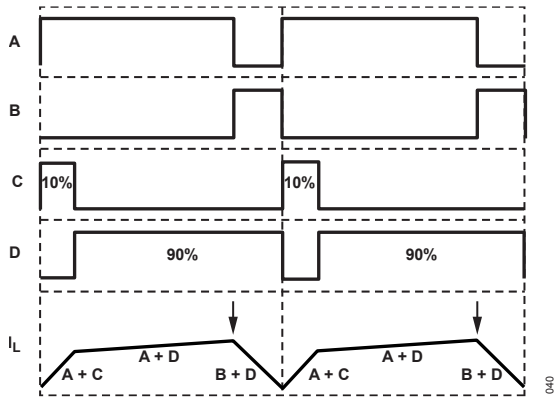


Figure 40. Peak-Boost Peak-Buck in Buck-Boost Region (V_{IN} ~> V_{OUT})

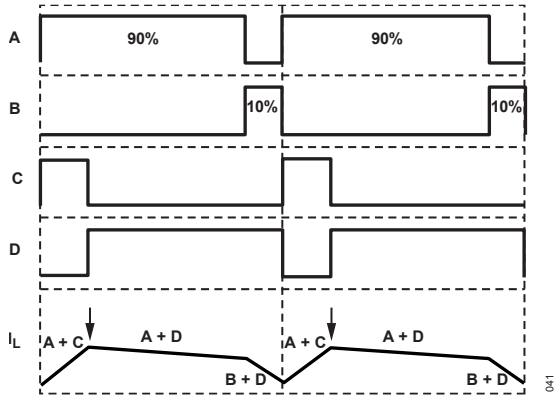


Figure 41. Peak-Boost Peak-Buck in Buck-Boost Region (V_{IN} ~< V_{OUT})

Peak-Boost in Boost Region (V_{IN} << V_{OUT})

When V_{IN} is much lower than V_{OUT}, the LT8292 uses peak-boost current mode control in the boost region (*Figure 42*). Switch A is always on, and switch B is always off. At the beginning of every cycle, switch C is turned on, and the inductor current ramps up. When the inductor current hits the peak boost current threshold commanded by V_C voltage at boost current comparator A4 during the (A+C) phase, switch C is turned off, and switch D is turned on for the rest of the cycle. Switches C and D will alternate, behaving like a typical synchronous boost regulator.

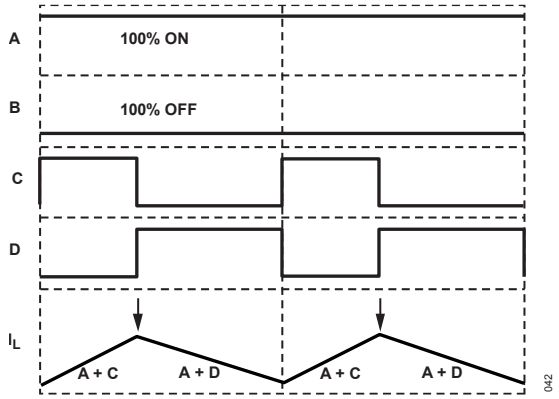


Figure 42. Peak-Boost in Boost Region (V_{IN} << V_{OUT})

Main Control Loop

The LT8292 is a fixed-frequency current mode controller. The inductor current is sensed through the inductor sense resistor between the LSP and LSN pins. The current sense voltage is gained up by amplifier A1 and added to a slope compensation ramp signal from the internal oscillator. The summing signal is then fed into the positive terminals of the buck current comparator A3 and boost current comparator A4. The negative terminals of A3 and A4 are controlled by the voltage on the V_C pin, which is the diode-OR of error amplifiers EA1 and EA2.

Depending on the state of the peak-buck peak-boost current mode control, either the buck logic or the boost logic is controlling the four power switches so that either the FB voltage is regulated to 1V or the current sense voltage between the ISP and ISN pins is regulated by the ICTRL pin during normal operation. The gains of EA1 and EA2 have been balanced to ensure a smooth transition between constant-voltage and constant-current operation with the same compensation network.

Light Load Operation

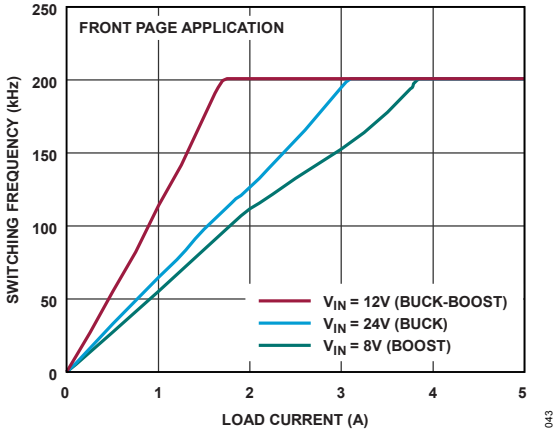


Figure 43. SW Frequency vs Load Current in Burst Mode Operation

Low Ripple Burst Mode

To enhance efficiency at light loads, the LT8292 operates in low ripple Burst Mode operation, which keeps the output capacitor charged to the desired output voltage while minimizing the input quiescent current and minimizing output voltage ripple. In Burst Mode operation, the LT8292 delivers single small pulses of current to the output capacitor, followed by sleep periods where the output power is supplied by the output capacitor. While in sleep mode, the LT8292 consumes very low (30µA typical) input quiescent current. To select low ripple Burst Mode operation, tie the SYNC/MODE pin low to the ground.

As the output load decreases, the frequency of single current pulses decreases (see *Figure 43*), and the percentage of time the LT8292 is in sleep mode increases, resulting in much higher light load efficiency than for typical converters. By maximizing the time between pulses, the converter quiescent current approaches 50µA for a typical application when there is no output load. Therefore, to optimize the quiescent current performance at light loads, the current in the feedback resistor divider must be minimized as it appears to the output as load current. In addition, all possible leakage currents from the output should also be minimized as they all add to the equivalent output load.

In Burst Mode operation, the peak inductor current limit is approximately 5mV (typical) between the LSP and LSN pins, resulting in low output voltage ripple. As the load ramps upward from zero, the switching frequency will increase but only up to the switching frequency programmed by the resistor at the R_T pin, as shown in *Figure 8*. The output load at which the LT8292 reaches the programmed frequency varies based on input voltage, output voltage, and inductor choice.

Pulse-Skipping Mode

For some applications, it is desirable for the LT8292 to operate in pulse-skipping mode (PSM), offering two major differences from the Burst Mode operation. The first difference is that the clock stays awake at all times, and all switching cycles are aligned to the clock. In this mode, much of the internal circuitry is awake at all times, increasing quiescent current to a few mA and thus achieving better transient response. The second difference is that the full switching frequency is reached at a lower output load than in the Burst Mode operation. To enable pulse-skipping mode, tie the SYNC/MODE pin with 100kΩ to GND. *Table 4* demonstrates a brief comparison between Burst Mode, pulse-skipping, and FCM.

Table 4. Comparison Between Burst Mode, Pulse-Skipping Mode, and Forced Continuous Mode Operations

Performance	Burst Mode	Pulse-skipping	FCM
Transient Response	Normal	Good	Best
V_{OUT} Ripple at Light Load	Good	Normal	Best
Efficiency at Light Load	Best	Good	Normal
Reverse Current	No	No	Yes

Forced Continuous Mode (FCM)

The LT8292 can operate in FCM for fast transient response and full-frequency operation over the entire load range. When in FCM, the oscillator operates continuously, and positive SW transitions are aligned to the clock. The negative inductor current is allowed at light loads or under large transient conditions. The LT8292 can sink current from the output and return this charge to the input in this mode, improving load step transient response (*Figure 44*). At light loads, FCM operation is less efficient than Burst Mode operation or pulse-skipping mode but may be desirable in applications where it is necessary to keep switching harmonics out of the signal band. FCM must be used if the output is required to sink current. To enable FCM, float the SYNC/MODE pin.

FCM is disabled during soft-start until the soft-start capacitor is fully charged. When FCM is disabled in these ways, the negative inductor current is not allowed, and the LT8292 operates in pulse-skipping mode.

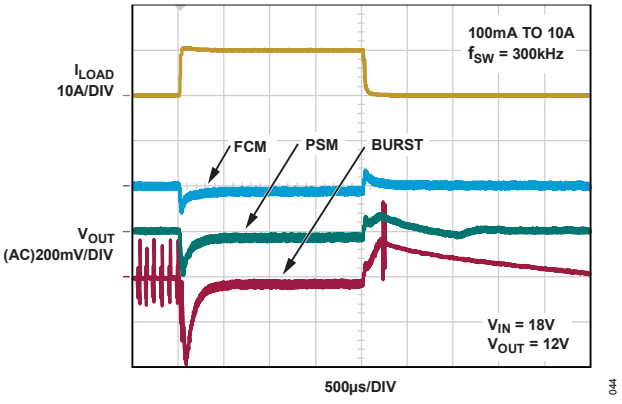


Figure 44. Load Step Transient Response with and without FCM

Internal Charge Path

Each of the two top MOSFET drivers is biased from its floating bootstrap capacitor, which is normally re-charged by $INTV_{CC}$ through the integrated bootstrap diode D1 or D2 when the top MOSFET is turned off. When the LT8292 operates exclusively in the buck or boost regions, one of the top MOSFETs is constantly on. An internal charge path, from V_{OUT} and BST2 to BST1 or from VIN and BST1 to BST2, charges the bootstrap capacitor to 4.6V so that the top MOSFET can be kept on.

Shutdown and Power-on-Reset

The LT8292 enters shutdown mode and drains less than 2µA quiescent current when the EN/UVLO pin is below its shutdown threshold (0.6V typical). Once the EN/UVLO pin is above its shutdown threshold, the LT8292 wakes up startup circuitry, generates bandgap reference, and powers up the internal $INTV_{CC}$ LDO. The $INTV_{CC}$ LDO supplies the internal control circuitry and gate drivers. Now, the LT8292 enters UVLO mode. When in UVLO mode, the part is in a power-on-reset (POR) state, waking up the entire internal control circuitry and settling to the right initial conditions. When the following conditions are met, the LT8292 is ready to exit the POR state and will enter the INIT state:

1) SS < 0.2V
2) $INTV_{CC}$ pin is charged above its rising UVLO threshold (3.6V typical) for approximately 100us.
3) EN/UVLO pin passes its rising enable threshold (1.239V typical).
4) Junction temperature is less than its thermal shutdown (170°C typical).

The LT8292 has an accurate enable threshold (typically 1.239V rising and 1.18V falling) on the EN/UVLO pin to enable the part. The accurate enable threshold allows the user to program an UVLO threshold with a resistor divider from the input supply V_{IN} to the ground. When operating in Burst Mode, the current flowing through the resistor divider can easily exceed the quiescent current consumed by the part. Therefore, the resistor divider values should be large enough to minimize its effect on the efficiency at light load conditions.

Start-Up and Fault Protection

Figure 45 shows the start-up and fault sequence for the LT8292. When the LT8292 is in the initial POR state, the SS pin is hard pulled down with a 50Ω internal resistor to ground. In a pre-biased condition, the SS pin has to be pulled below 0.2V to enter the INIT state, where the LT8292 waits for 10µs so that the SS pin can be fully discharged to the ground. The INIT state is a transition state, and the LT8292 will not be in longer than 10µs. After the 10µs in the INIT state, the LT8292 enters the UP/PRE state, and the SS pin is charged up by a 13µA pull-up current while the switching is disabled.

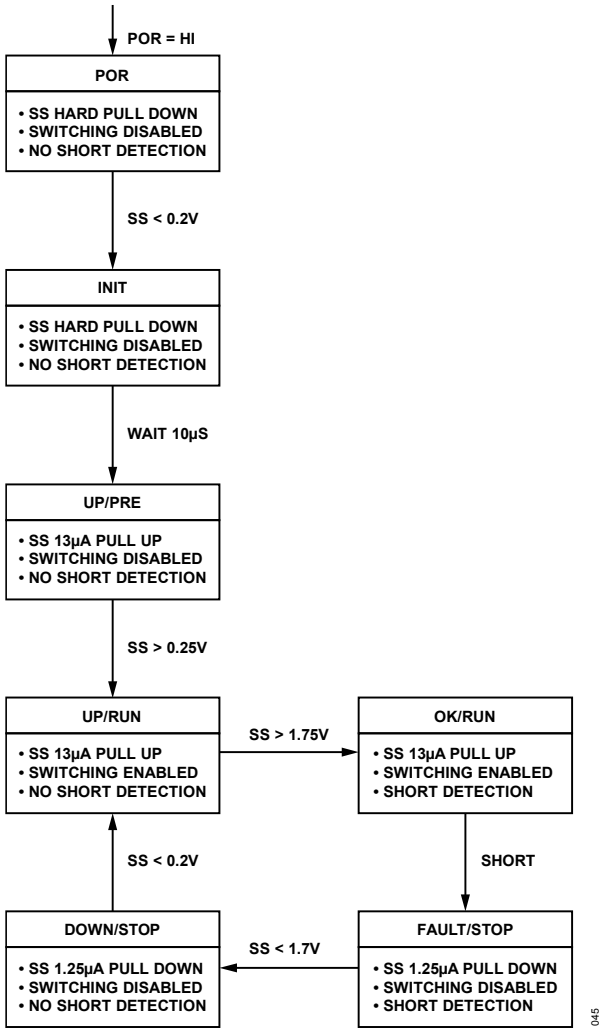


Figure 45. Start-Up and Fault Sequence

Once the SS pin is charged above 0.25V, the LT8292 enters the UP/RUN state, where the switching is enabled, and the start-up of the output voltage V_{OUT} is controlled by the voltage on the SS pin. When the SS pin voltage is less than 1V, the LT8292 regulates the FB pin voltage to the SS pin voltage instead of the 1V reference. This allows the SS pin to be used to program soft-start by connecting an external capacitor from the SS pin to the GND. The internal 13µA pull-up current charges up the capacitor, creating a voltage ramp on the SS pin. As the SS pin voltage rises linearly from 0.25V to 1V (and beyond), the V_{OUT} rises smoothly to its final regulation voltage. After passing 1V, the SS pin continues to be charged up until exceeding 1.75V, then the start-up period is finished. Before the SS pin rises above

1.75V, the control logic forbids synchronizing from the external clock and disables the Burst Mode operation, FCM, and spread spectrum frequency modulation. After the SS pin rises above 1.75V, both external frequency synchronization and operation mode selection are controlled by the SYNC/MODE pin setting.

Once the SS pin is charged above 1.75V, the LT8292 enters the OK/RUN state, where the output short detection is activated. The output short means V_{FB} < 0.25V. When the output short happens, the LT8292 enters the FAULT/STOP state, where the switching is immediately disabled, and a 1.25µA pull-down current slowly discharges the SS pin. Once the SS pin is discharged below 1.7V, the LT8292 enters the DOWN/STOP state, where the short detection is deactivated with the previous fault latched. During this period, the part forbids the Burst Mode operation, FCM, and spread spectrum frequency modulation. Once the SS pin is discharged below 0.2V, the LT8292 goes back to the UP/RUN state.

In an output short condition, the LT8292 is set to hiccup fault protection mode, where the LT8292 will hiccup between 0.2V and 1.75V and go around the UP/RUN, OK/RUN, FAULT/STOP, and DOWN/STOP states until the fault condition is cleared.

Once the FB pin voltage exceeds 8% (typical) above its 1V regulation voltage, the output overvoltage fault will be triggered, which disables the switching immediately. After the FB pin voltage drops below the overvoltage threshold, the switching will be enabled again. No soft start-up will be re-initiated in this fault case.

APPLICATIONS INFORMATION

See *Typical Application Diagram* for more details. This Applications Information section serves as a guideline for selecting external components for typical applications. The examples and equations in this section assume continuous conduction mode unless otherwise specified.

Switching Frequency Selection

The LT8292 uses a constant-frequency control scheme between 100kHz and 650kHz. The selection of the switching frequency is a tradeoff between efficiency and component size. Low-frequency operation improves efficiency by reducing MOSFET switching losses but requires larger inductor and capacitor values. For high-power applications, consider operating at lower frequencies to minimize MOSFET heating from switching losses. For low-power applications, consider operating at higher frequencies to minimize the total solution size.

In addition, the specific application also plays an important role in switching frequency selection. In a noise-sensitive system, the switching frequency is usually selected to keep the switching noise out of a sensitive frequency band.

Switching Frequency Setting

The switching frequency of the LT8292 can be set by the internal oscillator. With the SYNC/MODE pin set to the internal oscillator frequency, the switching frequency is set by a resistor from the R_T pin to the ground. *Table 5* shows R_T resistor values for common switching frequencies.

Table 5. Switching Frequency vs R_T Value (1% Resistor)

f_{OSC} (kHz)	R_T (kΩ)
100	523kΩ
200	258kΩ
300	171kΩ
350	147kΩ
400	127kΩ
500	102kΩ
600	85kΩ
650	79kΩ

Spread Spectrum Frequency Modulation

Switching regulators can be particularly troublesome for applications where EMI is a concern. To improve the EMI performance, the LT8292 implements a triangle spread spectrum frequency modulation scheme. With the SYNC/MODE pin tied to $INTV_{CC}$, the LT8292 starts to spread its switching frequency from 0% to 25% around the internal oscillator frequency.

Frequency Synchronization

The LT8292 switching frequency can be synchronized to an external clock using the SYNC/MODE pin. Driving the SYNC/MODE with a 50% duty cycle waveform is always a good choice; otherwise, maintain the duty cycle between 10% and 90%. Due to using a phase-locked loop (PLL) inside, there is no restriction between the synchronization frequency and the internal oscillator frequency. The rising edge of the synchronization clock represents the beginning of a switching cycle, turning on switches A and C or switches A and D.

Inductor Selection

The switching frequency and inductor selection are interrelated in that higher switching frequencies allow the use of smaller inductor and capacitor values. The inductor value has a direct effect on the ripple current. The highest current ripple $\Delta I_L\%$ happens in the buck region at $V_{IN(MAX)}$, and the lowest current ripple $\Delta I_L\%$ happens in the boost region at $V_{IN(MIN)}$. For any given ripple allowance set by customers, the minimum inductance can be calculated as:

$$L_{BUCK} > \frac{V_{OUT} \bullet (V_{IN(MAX)} - V_{OUT})}{f \bullet I_{OUT(MAX)} \bullet \Delta I_L\% \bullet V_{IN(MAX)}}$$

$$L_{BOOST} > \frac{V_{IN(MIN)}^2 \bullet (V_{OUT} - V_{IN(MIN)})}{f \bullet I_{OUT(MAX)} \bullet \Delta I_L\% \bullet V_{OUT}^2}$$

where:

$$\Delta I_L\% > \frac{\Delta I_L}{I_{L(AVG)}}$$

f is the switching frequency.

$V_{IN(MIN)}$ is the minimum input voltage.

$V_{IN(MAX)}$ is the maximum input voltage.

V_{OUT} is the output voltage.

$I_{OUT(MAX)}$ is the maximum output current.

Slope compensation provides stability in constant frequency current mode control by preventing subharmonic oscillations at certain duty cycles. The minimum inductance required for stability when duty cycles are larger than 50% can be calculated as:

$$L > \frac{10 \bullet V_{OUT} \bullet R_{SENSE}}{f}$$

For high efficiency, choose an inductor with low core loss, such as ferrite. Also, the inductor should have low DC resistance to reduce the I^2R losses and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a shielded inductor.

R_{SENSE} Selection and Maximum Output Current

The inductor current sense resistor (R_{SENSE}) is chosen based on the required output current. The duty cycle independent maximum current sense thresholds (50mV in peak-buck and 50mV in peak-boost) set the maximum inductor peak current in buck region, buck-boost region, and boost region. In the boost region, the lowest maximum average load current happens at $V_{IN(MIN)}$ and can be calculated as:

$$I_{OUT(MAX\_BOOST)} = \left(\frac{50mV}{R_{SENSE}} - \frac{\Delta I_{L(BOOST)}}{2}\right) \bullet \frac{V_{IN(MIN)}}{V_{OUT}}$$

where $\Delta I_{L(BOOST)}$ is the peak-to-peak inductor ripple current in the boost region and can be calculated as:

$$\Delta I_{L(BOOST)} = \frac{V_{IN(MIN)} \bullet (V_{OUT} - V_{IN(MIN)})}{f \bullet L \bullet V_{OUT}}$$

In buck region, the lowest maximum average load current happens at $V_{IN(MAX)}$ and can be calculated as:

$$I_{OUT(MAX\_BUCK)} = \left(\frac{50mV}{R_{SENSE}} - \frac{\Delta I_{L(BUCK)}}{2}\right)$$

where $\Delta_{IL(BUCK)}$ is peak-to-peak inductor ripple current in buck region and can be calculated as:

$$\Delta I_{L(BUCK)} = \frac{V_{OUT} \bullet (V_{IN(MAX)} - V_{OUT})}{f \bullet L \bullet V_{IN(MAX)}}$$

The maximum current sense R_{SENSE} in the boost region is:

$$R_{SENSE(BOOST)} = \frac{2 \bullet 50mV \bullet V_{IN(MIN)}}{2 \bullet I_{OUT(MAX)} \bullet V_{OUT} + \Delta I_{L(BOOST)} \bullet V_{IN(MIN)}}$$

The maximum current sense R_{SENSE} in the buck region is:

$$R_{SENSE(BUCK)} = \frac{2 \cdot 50mV}{2 \bullet I_{OUT(MAX)} + \Delta I_{L(BUCK)}}$$

The final R_{SENSE} value should be lower than the calculated R_{SENSE} in both buck and boost regions. A 20% to 30% margin is usually recommended. Always choose a low ESL current sense resistor.

Power MOSFET Selection

The LT8292 requires four external N-channel power MOSFETs, two for the top switches (switches A and D, shown in *Figure 36*) and two for the bottom switches (switches B and C, shown in *Figure 36*). Important parameters for the power MOSFETs are the breakdown voltage $V_{BR(DSS)}$, threshold voltage $V_{GS(TH)}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance $C_{RSS,}$ and maximum current I_{DS}(MAX).

The drive voltage is set by the 5V $INTV_{CC}$ supply. Consequently, logic-level threshold MOSFETs must be used in LT8292 applications.

To select the power MOSFETs, the power dissipated by the device must be known. For switch A, the maximum power dissipation happens in the boost region, when it remains on all the time. Its maximum power dissipation at maximum output current is given by:

$$P_{A(BOOST)} = \left(\frac{I_{OUT(MAX)} \bullet V_{OUT}}{V_{IN}}\right)^2 \bullet \rho_T \bullet R_{DS(ON)}$$

where ρT is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically 0.4%/°C, as shown in *Figure 46*. For a maximum junction temperature of 125°C, using a value of ρT = 1.5 is reasonable.

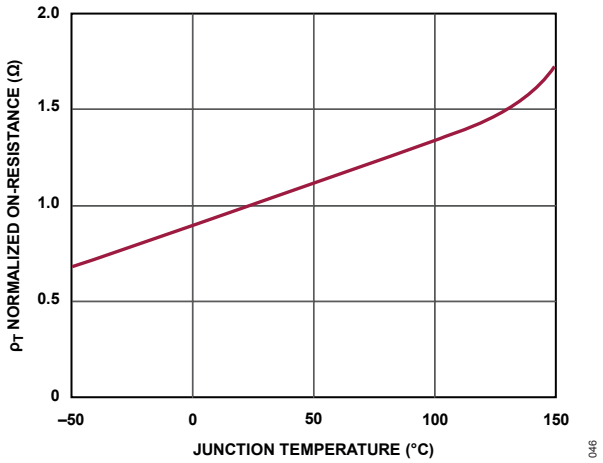


Figure 46. Normalized $R_{DS(ON)}$ vs Temperature

Switch B operates in the buck region as the synchronous rectifier. Its power dissipation at maximum output current is given by:

$$P_{B(BUCK)} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}^{2} \bullet \rho_T \bullet R_{DS(ON)}$$

Switch C operates in the boost region as the control switch. Its power dissipation at maximum current is given by:

$$P_{C(BOOST)} = \frac{(V_{OUT} - V_{IN}) \bullet V_{OUT}}{V_{IN}^{2}} \bullet I_{OUT(MAX)}^{2} \bullet \rho_T \bullet R_{DS(ON)} + k \bullet V_{OUT}^{3} \bullet \frac{I_{OUT(MAX)}}{V_{IN}} \bullet C_{RSS} \bullet f$$

where C_{RSS} is usually specified by the MOSFET manufacturers. The constant k, which accounts for the loss caused by the reverse recovery current, is inversely proportional to the gate drive current and has an empirical value of 1.7.

For switch D, the maximum power dissipation happens in the boost region, when its duty cycle is higher than 50%. Its maximum power dissipation at maximum output current is given by:

$$P_{D(BOOST)} = \frac{V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}^{2} \bullet \rho_T \bullet R_{DS(ON)}$$

For the same output voltage and current, switch A has the highest power dissipation, and switch B has the lowest power dissipation unless a short occurs at the output.

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

$$T_J = T_J + P \bullet R_{TH(JA)}$$

The junction-to-ambient thermal resistance $R_{TH(JA)}$ includes the junction-to-case thermal resistance $R_{TH(JC)}$ and the case-to-ambient thermal resistance $R_{TH(CA)}$. This value of T_J can then be compared to the original, assumed value used in the iterative calculation process.

Optional Schottky Diode (D_B, D_D) Selection

The optional Schottky diodes D_B (in parallel with switch B) and D_D (in parallel with switch D) are conducted during the dead time between the conduction of the power MOSFET switches. They are intended to prevent the body diode of synchronous switches B and D from turning on and storing charge during the dead time. In particular, D_B significantly reduces the reverse recovery current between switch B turn-off and switch A turn-on, and D_D significantly reduces the reverse recovery current between switch D turn-off and switch C turn-on. They improve converter efficiency and reduce switch voltage stress. For the diode to be effective, the inductance between it and the synchronous switch must be as small as possible, mandating that these components be placed adjacently.

C_{IN} and C_{OUT} Selection

Input and output capacitance are necessary to suppress voltage ripple caused by discontinuous current moving in and out of the regulator. A parallel combination of capacitors is typically used to achieve high capacitance and low equivalent series resistance (ESR). Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface-mount packages. Capacitors with low ESR and high ripple current ratings, such as OS-CON and POSCAP, are also available.

Ceramic capacitors should be placed near the regulator input and output to suppress high-frequency switching spikes. Ceramic capacitors of at least 1µF should also be placed from V_{IN} to GND and V_{OUT} to GND as close to the LT8292 pins as possible. Due to their excellent low ESR characteristics, ceramic capacitors can significantly reduce input ripple voltage and help reduce power loss in the higher ESR bulk capacitors. X5R or X7R dielectrics are preferred, as these materials retain their capacitance over wide voltage and temperature ranges. Many ceramic capacitors, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired operating voltage.

Input Capacitance (C_{IN})

Discontinuous input current is highest in the buck region due to switch A toggling on and off. Ensure that the C_{IN} capacitor network has low enough ESR and is sized to handle the maximum RMS current. In buck region, the input RMS current is given by:

$$I_{RMS} \approx I_{OUT(MAX)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

The formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Output Capacitance (C_{OUT})

Discontinuous current shifts from the input to the output in the boost region. Ensure that the C_{OUT} capacitor network is capable of reducing the output voltage ripple. The effects of ESR and bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage.

The maximum steady state ripple due to charging and discharging the bulk capacitance is given by:

$$\Delta V_{CAP(BOOST)} = \frac{I_{OUT(MAX)} \bullet \left(V_{OUT} - V_{IN(MIN)}\right)}{C_{OUT} \bullet V_{OUT} \bullet f}$$

$$\Delta V_{CAP(BUCK)} = \frac{V_{OUT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)}{8 \bullet L \bullet f^2 \bullet C_{OUT}}$$

The maximum steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{ESR(BOOST)} = \frac{V_{OUT} \bullet I_{OUT(MAX)}}{V_{IN(MIN)}} \cdot ESR$$

$$\Delta V_{ESR(BUCK)} = \frac{V_{OUT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)}{L \cdot f} \cdot ESR$$

Dual Input $INTV_{CC}$ Regulator

An internal P-channel low dropout (LDO) regulator produces 5V at the $INTV_{CC}$ pin from either the V_{IN} supply or V_{OUT} pins powering internal circuitry and gate drivers in the LT8292. The $INTV_{CC}$ regulator can supply a peak current of 170mA and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor. A good local bypass is necessary to supply the high transient current required by MOSFET gate drivers.

Note: The $INTV_{CC}$ LDO is designed only to supply the internal circuitry of LT8292 and can not be used as a bias supply for other external circuits. Overload or short circuit on the $INTV_{CC}$ LDO may cause permanent damage and failure.

To enable a wider V_{IN} range and more efficient operation, the internal LDO can intelligently draw current from either the V_{IN} supply pin or the V_{OUT} pin. When V_{IN} is below 5.5V, the internal LDO draws current from the higher of the two voltage pins so that the LT8292 can provide enough gate drive capability. When the V_{OUT} is regulated above 5V, the LT8292 can still securely operate with the minimum V_{IN} as low as 3V.

When V_{IN} and V_{OUT} are both above 5.5V, the internal LDO draws current from the lower of the two voltage pins so that the LT8292 can optimize efficiency across all loads. If the V_{IN} is above 5.5V but the V_{OUT} is below 5.5V, the internal LDO will then draw current from the V_{IN}, ensuring gate drive capability. *Table 6* summarizes this input selection logic of the LT8292's dual input LDO.

Higher input voltage applications with large MOSFETs being driven at higher switching frequencies may cause the maximum junction temperature rating for the LT8292 to be exceeded. The system supply current is normally dominated by the gate charge current. The total LT8292 power dissipation, in this case, is $V_{SOURCE} \cdot I_{INTVCC}$, where V_{SOURCE} is either V_{IN} or V_{OUT}, depending on the conditions described above. The junction temperature can be estimated by using the equation:

$$T_J = T_A + P_D \bullet \theta_{JA}$$

where θ_{JA} (in °C/W) is the package thermal resistance. To prevent the maximum junction temperature from being exceeded, the input supply current must be checked, operating in continuous mode at maximum V_{SOURCE}.

Table 6. Dual Input LDO's Supply Combination Logic

V_{IN}	V_{OUT}	LDO Supply Input
$V_{IN} \le 5.5V$	$V_{OUT} > V_{IN}$	V_{OUT}
	$V_{OUT} < V_{IN}$	V_{IN}
$V_{IN} \ge 5.5V$	$V_{OUT} < 5.5V$	V_{IN}
	$5.5V < V_{OUT} < V_{IN}$	V_{OUT}
	$V_{OUT} > V_{IN}$	V_{IN}

Top Gate MOSFET Driver Supply (C_{BST1}, C_{BST2})

The top MOSFET drivers, TG1 and TG2, are driven between their respective SW and BST pin voltages. The boost voltages are biased from floating bootstrap capacitors C_{BST1} and C_{BST2}, which are normally re-charged through internal bootstrap diodes D1 and D2 when the respective top MOSFET is turned off. Both capacitors are charged to the same voltage as the $INTV_{CC}$ voltage. Although the internal bootstrap diodes are capable of charging C_{BST1} and C_{BST2} in most applications, low leakage external bootstrap Schottky diodes are recommended to parallel with D1/D2 when top MOSFETs are selected with very high gate capacitance and operate at a high switching frequency. The voltage on the C_{BST1} and C_{BST2} may be measured at the maximum switching frequency during the steady-state operation. If the voltage is lower than 4.6V, the external bootstrap diodes are suggested to help D1/D2 supply top drivers. The bootstrap capacitors C_{BST1} and C_{BST2} need to store about 100 times the gate charge required by the top switches A and D. In most applications, a 0.1µF to 0.47µF, X5R or X7R dielectric capacitor is adequate.

Split Gate Driver Outputs

Voltage regulator designs often insert a small resistance between a switch driver pin and a gate pin of the power switch. This practice reduces the EMI radiation of the switching converter by slowing down the turn-on speed of the gate, in a conventional single-gate drive. However, the added gate resistance will also slow down the turn-off speed of the gate and weaken the pull-down strength of the driver, causing degraded efficiency and system reliability.

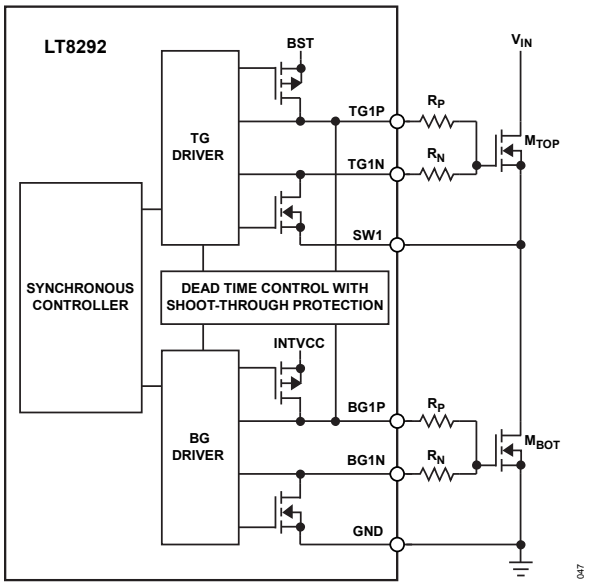


Figure 47. Split-Gate Driver of the LT8292 (Buck-Side)

To overcome this issue, the LT8292 offers split gate drive outputs, which allow weak turn-on and strong turn-off of the gate to achieve optimized efficiency and EMI performance. TGP and TGN pins are the pull-up and pull-down pins for the top power switch, respectively. BGP and BGN pins are the pull-up and pull-down pins for the bottom power switch, respectively, as shown in *Figure 47*. The pull-up and pull-down strength can be individually controlled by inserting the separate gate resistors R_P and R_N, respectively. For strong pull-down strength, R_N can be shorted so that the pull-down pins are directly connected to the gate of the power switch. If individual control of the pull-up and pull-down strength is not needed, the split pins can be shorted and used as a single-gate drive.

Dead time Programming with Shoot-Through Protection

The added external gate resistance in a conventional single-gate drive can prevent the controller from detecting the true gate voltage of the power switch, which can result in vast amounts of shoot-through current flowing between the two power switches. Thus, general controller products typically provide a relatively longer margin to their fixed dead time period. Longer dead time may result in additional loss of efficiency and make it challenging for higher-frequency operations.

The LT8292 eliminates these side effects by offering adaptive and selectable dead times from 40ns to 2ns (typical). The novel LT8292 split gate drive architecture enables the controller to always observe the true gate voltages of the power switches (see *Figure 47*), allowing it to determine better the on- and off-states of the power switches for more accurate and robust dead time control.

Buck side switching dead time can be set by a resistor from R_{DT1} pin to ground, and boost side switching dead time can be set by a resistor from RDT2 pin to ground. *Table 7* shows R_{DT1} and R_{DT2} resistor values for the selectable dead time periods. For the high power, low frequency (<200kHz) applications, either 10ns or 20ns are recommended for dead time selection. For compact, high-frequency applications (such as driving low-Q_g MOSFET or GaN FET), the 2ns dead time can be selected. The LT8292 has built-in shoot-through protection for additional system reliability, as depicted in *Figure 47*. If the controller does not detect the complete off state of the power switches, it will adaptively delay the dead time up to 100ns, regardless of the dead time selection. It is best to avoid such events, however. Thus, proper PCB layout and power MOSFET selection should be carefully considered.

For the applications requiring additional reliability or with a more complicated, larger PCB layout, the 40ns dead time can be selected. With the proper design of the gate resistance, all the selected dead times in LT8292 will be unlikely to vary over the use of different values of gate resistor, making it easy to achieve both an optimized efficiency and EMI.

Table 7. Dead Time Period vs R_{DT} value

R_{DT1}/R_{DT2}	Dead Time Periods
51kΩ	2ns
82kΩ	10ns
130kΩ	20ns
Connect to $INTV_{CC}$	40ns

Programming V_{IN} UVLO

A resistor divider from V_{IN} to the EN/UVLO pin implements V_{IN} UVLO. The EN/UVLO enable rising threshold is set at 1.239V (typical), and the falling threshold is set at 1.184V (typical) with 55mV hysteresis. The programmable UVLO thresholds are:

$$V_{IN(UVLO+)} = 1.239V \bullet \frac{R1 + R2}{R2}$$

$$V_{IN(UVLO-)} = 1.184V \bullet \frac{R1 + R2}{R2}$$

Due to the internal logic design, LT8292 requires V_{IN} to be above 5.5V before EN/UVLO crosses the rising threshold of 1.239V. It is recommended to use a resistor divider ratio of at least R1 > 4 • R2. DO NOT connect the EN/UVLO pin directly to the V_{IN}.

To implement proper LT8292 shutdown, EN/UVLO must be turned off with a time constant of τ > 10µs. *Figure 48* shows the implementation of a capacitor to set the EN/UVLO time constant τ. τ can be calculated by using the equation:

$$\tau = C1 \bullet \frac{R1 \bullet R2}{R1 + R2}$$

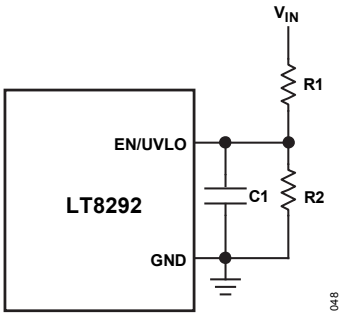


Figure 48. V_{IN} UVLO

Figure 49 shows the implementation of external shut-down control while still using the UVLO function. When the n-channel metal-oxide-semiconductor (NMOS) is turned on, and the RC network on the EN/UVLO pin allows proper LT8292 shutdown with less than 0.7µA of quiescent current. Use the following equation to ensure τ > 10µs for proper shutdown:

$$\tau = C1 \bullet R3$$

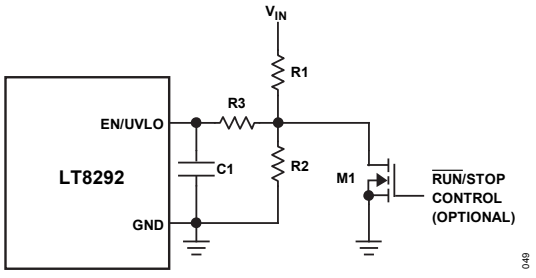


Figure 49. V_{IN} UVLO with external shut-down control

Programming Input or Output Current Limit

The input or output current limit can be programmed by placing an appropriate value current sense resistor, R_{IS}, in the input or output power path. The voltage drop across R_{IS} is (Kelvin) sensed by the ISP and ISN pins. The ICTRL pin should be tied to a voltage higher than 1.35V to get the full-scale 50mV (typical) threshold across the sense resistor. The ICTRL pin can be used to reduce the current threshold to zero, although relative accuracy decreases with the decreasing sense threshold. When the ICTRL pin voltage is between 0.3V and 1.15V, the current limit is:

$$I_{IS(MAX)} = \frac{V_{ICTRL} - 0.25V}{20 \bullet R_{IS}}$$

When V_{ICTRL} is between 1.15V and 1.35V, the current limit varies with V_{ICTRL} but departs from the equation above by an increasing amount as V_{ICTRL} increases. Ultimately, when V_{iCTRL} is larger than 1.35V, the current limit no longer varies. The typical V_{ISP}-V_{ISN} threshold vs V_{ICTRL} is listed in *Table 8*.

Table 8. V_{ISP} – V_{ISN} Threshold vs V_{ICTRL}

V_{ICTRL} (V)	V_{ISP} – V_{ISN} (mV)
1.15	45
1.20	47.2
1.25	49
1.30	49.8
1.35	50

When V_{CTRL} is larger than 1.35V, the current threshold is regulated to:

$$I_{IS(MAX)} = \frac{50mV}{R_{IS}}$$

The ICTRL pin should not be left open (tie to $INTV_{CC}$ if not used). The ICTRL pin can also be used in conjunction with a thermistor to provide overtemperature protection for the output load. The presence of a time varying differential voltage ripple signal across the ISP and ISN pins at the switching frequency is expected. If the current sense resistor R_{IS} is placed between the power input and input bulk capacitor (*Figure 50*), or between the output bulk capacitor and system output (*Figure 52*), a filter is typically unnecessary. If the R_{IS} is placed between the input bulk capacitor and the input decoupling capacitor (*Figure 51*), or between the output decoupling capacitor and the output bulk capacitor (*Figure 53*), a low-pass filter formed by R_F and C_F is recommended to reduce the current ripple and stabilize the current loop. Since the bias currents of the ISP and ISN pins are mismatched, some offset is introduced by R_F. To minimize the offset, do not use very large value R_F (normally $R_F << 1k\Omega$). If the input or output current limit is not used, the ISP and ISN pins should be shorted to V_{IN}, V_{OUT}, or ground.

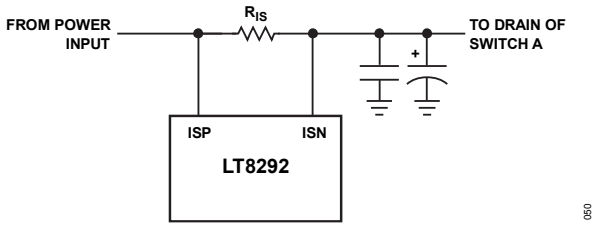


Figure 50. Programming Input Current Limit

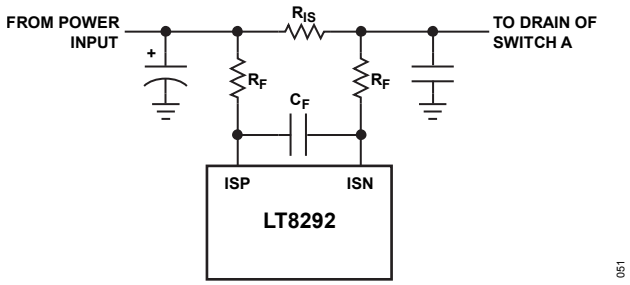


Figure 51. Programming Input Current Limit

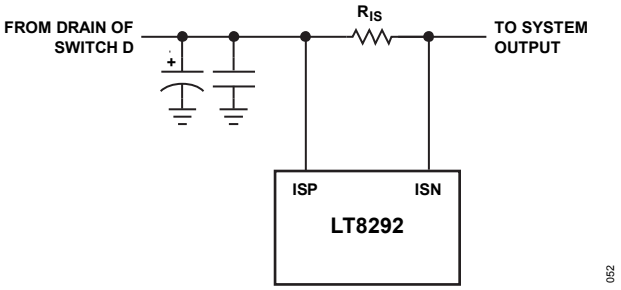


Figure 52. Programming Output Current Limit

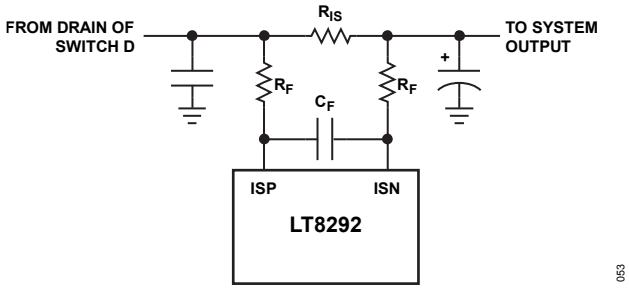


Figure 53. Programming Output Current Limit

Paralleling Multiple Regulators

Leaderless Current Sharing (ISHARE and IGND)

The LT8292 provides leaderless current sharing among multiple LT8292s in parallel, enabling higher load current and better heat management by using the ISHARE and IGND pins. Each LT8292 regulates the average output current, eliminating the need for a leader controller. To enable paralleling, connect the ISHARE pins of all the LT8292s together, and kelvin all IGND pins to a common ground as shown in *Figure 54*.

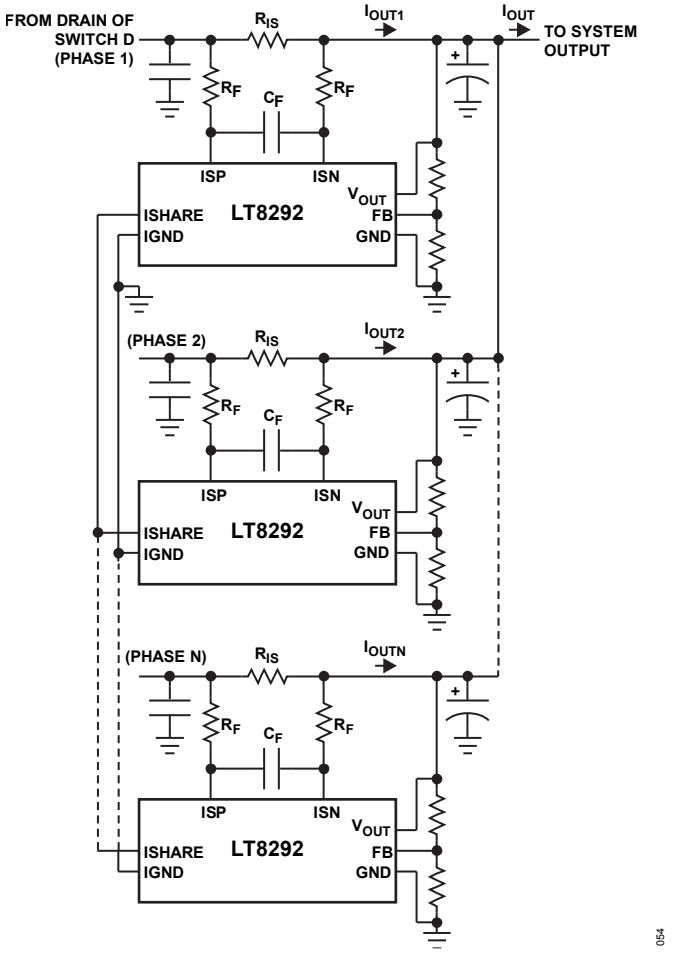


Figure 54. ISHARE and IGND Connection for LT8292s in Parallel

To regulate each LT8292's output current to the average output current, make the current sense resistor (R_{IS}) values equal in the output power paths of all the LT8292s (see *Figure 54*). The voltage drop across the R_{IS} represents the output current, I_{OUT}, and is (Kelvin) sensed by the ISP and ISN pins. When the LT8292 is enabled, and the PGOOD is high, each LT8292's I_{OUT} is autonomously regulated to the average output as:

$$I_{OUT1} = I_{OUT2} = I_{OUTN} = \sum_{n=1}^{N} \frac{I_{OUTn}}{N}$$

where, I_{OUTN} is the output current of the N^{th} phase.

A low-pass filter formed by R_F and C_F (*Figure 54*) is recommended to optimize the current loop response and stability. To stabilize the parallel system, the R_F and C_F values should be selected so that the outer current (I_{OUTN}) loop is formed slower than the inner voltage (V_{OUT}) loop, which is set by the V_C pin. (See the *Loop Compensation* in the *Applications Information* section for more details.) For a typical voltage regulator application, the 50Ω resistors (R_F) and a 10µF capacitor (C_F) are adequate and can be a good starting point. The Typical application diagram (*Figure 57*) demonstrates a good parallel design example.

In practical implementations, however, any mismatch in R_F possibly will affect the current sharing accuracy, such that:

$$\%I_{SHARE\_ERROR} = \frac{20\mu A \bullet \Delta R_F}{\left(\sum_{n=1}^{N} \frac{I_{OUTn}}{N}\right) \bullet R_{IS}}$$

where $\%I_{SHARE\_ERROR}$ is the percentage of the current sharing error, and ΔR_F is the mismatch of the R_F (in Ω). The bias currents of the ISP and ISN pins are 20µA (typical) in LT8292. To further improve the current sharing accuracy, it is recommended to choose the resistors (R_F) with tolerances lower than 2%, or to use the relatively smaller value if the lower tolerance resistor is not available. A resistor value of less than 50Ω is mostly recommended.

Phase Synchronization

The LT8292 provides a digital clock output pin CLKOUT that enables synchronizing one or more LT8292 ICs in parallel. The CLKOUT pin provides a 180° out-of-phase clock signal at the switching frequency set by the internal oscillator or the external frequency synchronization using the SYNC/MODE pin, and the duty cycle is fixed at 50%. See the design example in the Typical application diagram (*Figure 57*).

Programming Output Voltage and Thresholds

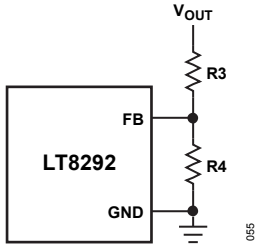


Figure 55. Feedback Resistor Connection

The LT8292 has a voltage feedback pin FB that can be used to program a constant-voltage output. The output voltage can be set by selecting the values of R3 and R4 (*Figure 55*) according to the following equation:

$$V_{OUT} = 1.0V \bullet \frac{R3 + R4}{R4}$$

In addition, the FB pin also sets the output overvoltage threshold, PGOOD upper and lower thresholds, and output short thresholds. For an application with small output capacitors, the output voltage may overshoot a lot during a load transient event. Once the FB pin hits its overvoltage threshold of 1.08V, the LT8292 stops switching by turning off TG1, BG1, TG2, and BG2. The output overvoltage threshold can be calculated as:

$$V_{OUT(OVP)} = 1.08V \bullet \frac{R3 + R4}{R4}$$

To provide the output short-circuit detection and protection, the output short threshold can be calculated as:

$$V_{OUT(SHORT)} = 0.25V \bullet \frac{R3 + R4}{R4}$$

Power Good (PGOOD) Pin

The LT8292 provides an open-drain status pin, PGOOD, which is pulled low when V_{FB} exceeds ±8% of the 1V regulation voltage. The PGOOD pin can be pulled up by an external resistor to $INTV_{CC}$ or an external voltage source of up to 6V.

Soft-Start and Short-Circuit Protection

As shown in *Figure 45* and explained in the *Theory of Operation* section, the SS pin can be used to program the output voltage soft-start by connecting an external capacitor from the SS pin to the ground. The internal 13µA pull-up current charges up the capacitor, creating a voltage ramp on the SS pin. As the SS pin voltage rises linearly from 0.25V to 1V (and beyond), the output voltage rises smoothly into its final voltage regulation. The soft-start time can be calculated as:

$$t_{SS} = 1V \bullet \frac{C_{SS}}{13\mu A}$$

Ensure that the C_{SS} is at least five to ten times larger than the compensation capacitor on the V_C pin for a well-controlled output voltage soft-start. A 0.1µF ceramic capacitor is a good starting point.

The SS pin is also used as a fault timer. Once an output short-circuit fault is detected, the LT8292 enters a low-duty cycle auto-retry (hiccup) operation. In this scenario, the switching is immediately disabled, and a 1.25µA pull-down current source is activated to discharge the SS pin. After the SS pin is discharged below 0.2V, the 13µA pull-up current charges the SS pin up again. If the output short-circuit condition has not been removed when the SS pin reaches 1.75V, the 1.25µA pull-down current turns on again, initiating a new hiccup cycle. This will continue until the fault is removed. Once the output short-circuit condition is removed, the output will have a smooth short-circuit recovery due to a soft-start.

Loop Compensation

The LT8292 uses an internal transconductance error amplifier, the output of which, V_C, compensates the control loop. The external inductor, output capacitor, and compensation resistor and capacitor determine the loop stability.

The inductor and output capacitor are chosen based on performance, size, and cost. The compensation resistor and capacitor on the V_C pin are set to optimize control loop response and stability. For a typical voltage regulator application, a 10nF compensation capacitor on the V_C pin is adequate, and a series resistor should always be used to increase the slew rate on the V_C pin to maintain tighter output voltage regulation during fast transients on the input supply of the converter.

Efficiency Considerations

The power efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what limits efficiency and which change would produce the most improvement. Although all dissipative elements in circuits produce losses, four main sources account for most of the losses in LT8292 circuits:

1. DC I^2R losses. These arise from the resistances of the MOSFETs, sensing resistor, inductor, and PC board traces and cause the efficiency to drop at high output currents.
2. Transition loss. This loss arises from the brief amount of time switch A or switch C spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength, and MOSFET capacitance, among other factors.
3. $INTV_{CC}$ current. This is the sum of the MOSFET driver and control currents.
4. C_{IN} and C_{OUT} loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator in the buck region, and the output capacitor has the difficult job of filtering the large RMS output current in the boost region. Both C_{IN} and C_{OUT} must have low ESR to minimize the AC I^2R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.
5. Other losses. Body diodes of switch B and switch D, or optional Schottky diodes D_B and D_D, are responsible for conduction losses during dead time and light load conduction periods. Inductor core loss occurs predominantly at light loads. Switch A causes reverse recovery current loss in the buck region, and switch C causes reverse recovery current loss in the boost region.
6. When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If you make a change and the input current decreases, then the efficiency has increased. If there is no change in the input current, then there is no change in efficiency.

PC Board Layout Checklist

The basic PC board layout requires a dedicated ground plane layer. For high currents, a multilayer board provides heat sinking for power components.

- The ground plane layer should not have traces and should be as close as possible to the layer with power MOSFETs.
- Place C_{IN}, switch A, switch B, and D_B in one compact area. Place C_{OUT}, switch C, switch D, and D_D in one compact area.
- Connect the components to the ground plane using immediate vias. Use several large vias for each power component.
- Use planes for V_{IN} and V_{OUT} to maintain good voltage filtering and to keep power losses low.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to any DC net (V_{IN} or GND).
- Separate the signal and power grounds. All small-signal components should return to the exposed GND pad from the bottom, which is then tied to the power GND close to the sources of switch B and switch C.
- Place all power switches close to the controller. Keep the power GND, BG, TG, and SW traces short.
- Keep the high dV/dT SW1, SW2, BST1, BST2, TG1 and TG2 nodes away from sensitive small-signal nodes.
- The path formed by switch A, switch B, D_B, and the C_{IN} capacitor should have short leads and PCB trace lengths. The path formed by switch C, switch D, D_D, and the C_{OUT} capacitor should also have short leads and PCB trace lengths.

- The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor.
- Connect the top driver boost capacitor C_{BST1} closely to the BST1 and SW1 pins. Connect the top driver boost capacitor C_{BST2} closely to the BST2 and SW2 pins.
- Connect the input capacitors C_{IN} and output capacitors C_{OUT} closely to the power MOSFETs. These capacitors carry the MOSFET AC current.
- Route LSP and LSN trace together with minimum PCB trace spacing. Avoid sense lines passing through noisy areas, such as switch nodes. The filter capacitor between LSP and LSN should be as close as possible to the IC. Ensure accurate, current sensing with Kelvin connections at the R_{SENSE} resistor. A low ESL sense resistor is recommended. LSP trace and SW1 trace should be two separate traces. Do not share traces.
- Connect the V_C pin compensation network close to the IC, between the V_C and the signal ground. The capacitor helps to filter the effects of PCB noise and output ripple voltage from the compensation loop.
- Connect the $INTV_{CC}$ bypass capacitor, C_{INTVCC}, close to the IC, between the $INTV_{CC}$ and the power ground. This capacitor carries the MOSFET drivers' current peaks. An additional 1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ pin and power ground can help improve noise performance substantially.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8390/LT8390A	60V Synchronous 4-Switch Buck-Boost Controller with Spread Spectrum	V_{IN}: 4V to 60V, V_{OUT}: 1V to 60V, ±1.5% Voltage Accuracy, ±3% Current Accuracy, TSSOP-28, and 4mm × 5mm QFN-28
LT8392	60V Synchronous 4-Switch Buck-Boost Controller with Spread Spectrum	V_{IN}: 3V to 60V, V_{OUT}: 1V to 60V, ±1.5% Voltage Accuracy, ±4% Current Accuracy, TSSOP-28, and 4mm × 5mm QFN-28
LT3790	60V Synchronous 4-Switch Buck-Boost Controller	V_{IN}: 4.7V to 60V, V_{OUT}: 1.2V to 60V, ±2% Voltage Accuracy, ±6% Current Accuracy, and TSSOP-38
LT8705	80V Synchronous 4-Switch Buck-Boost Controller	V_{IN}: 2.8V to 80V, V_{OUT}: 1.3V to 80V, Regulates V_{OUT}, I_{OUT}, V_{IN}, I_{IN}, 5mm × 7mm QFN-38 and Modified TSSOP-38 for High Voltage
LTC3789	38V Synchronous 4-Switch Buck-Boost Controller	V_{IN}: 4V to 38V, V_{OUT}: 0.8V to 38V, Regulates V_{OUT}, I_{OUT}, or IIN, 5mm × 5mm QFN-32 and SSOP-24
LTC3780	36V Synchronous 4-Switch Buck-Boost Controller	V_{IN}: 4V to 36V, V_{OUT}: 0.8V to 30V, Regulates V_{OUT}, 4mm × 5mm QFN-28 and SSOP-28

TYPICAL APPLICATIONS

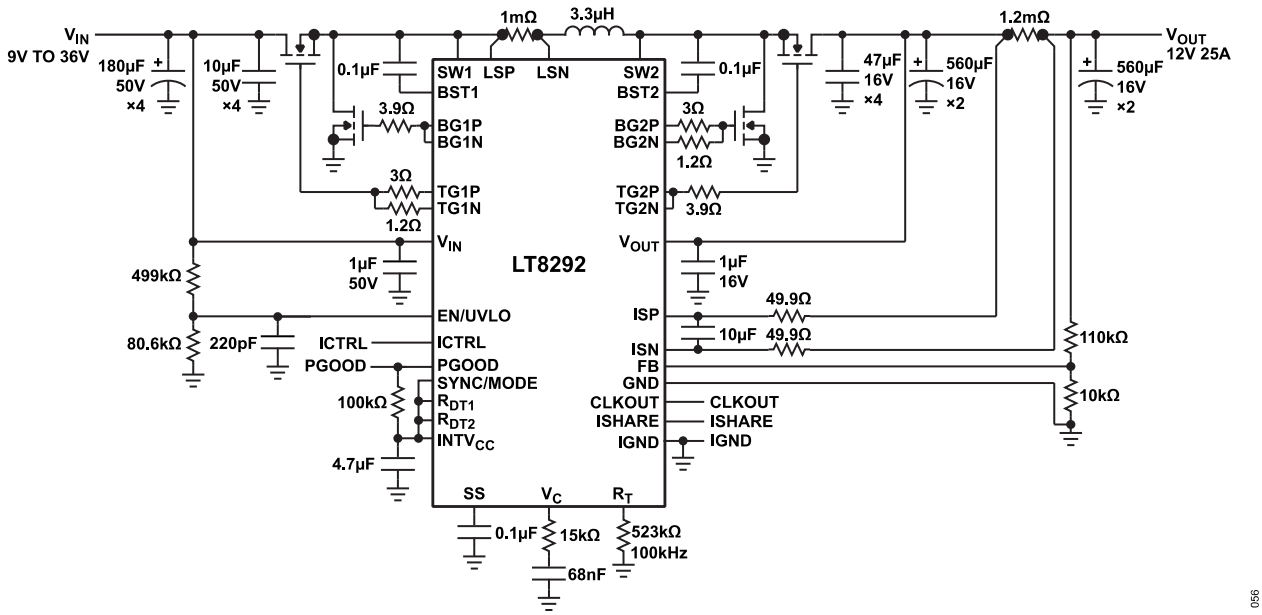


Figure 56. 300W (12V, 25A) Parallelable Buck-Boost Voltage Regulator

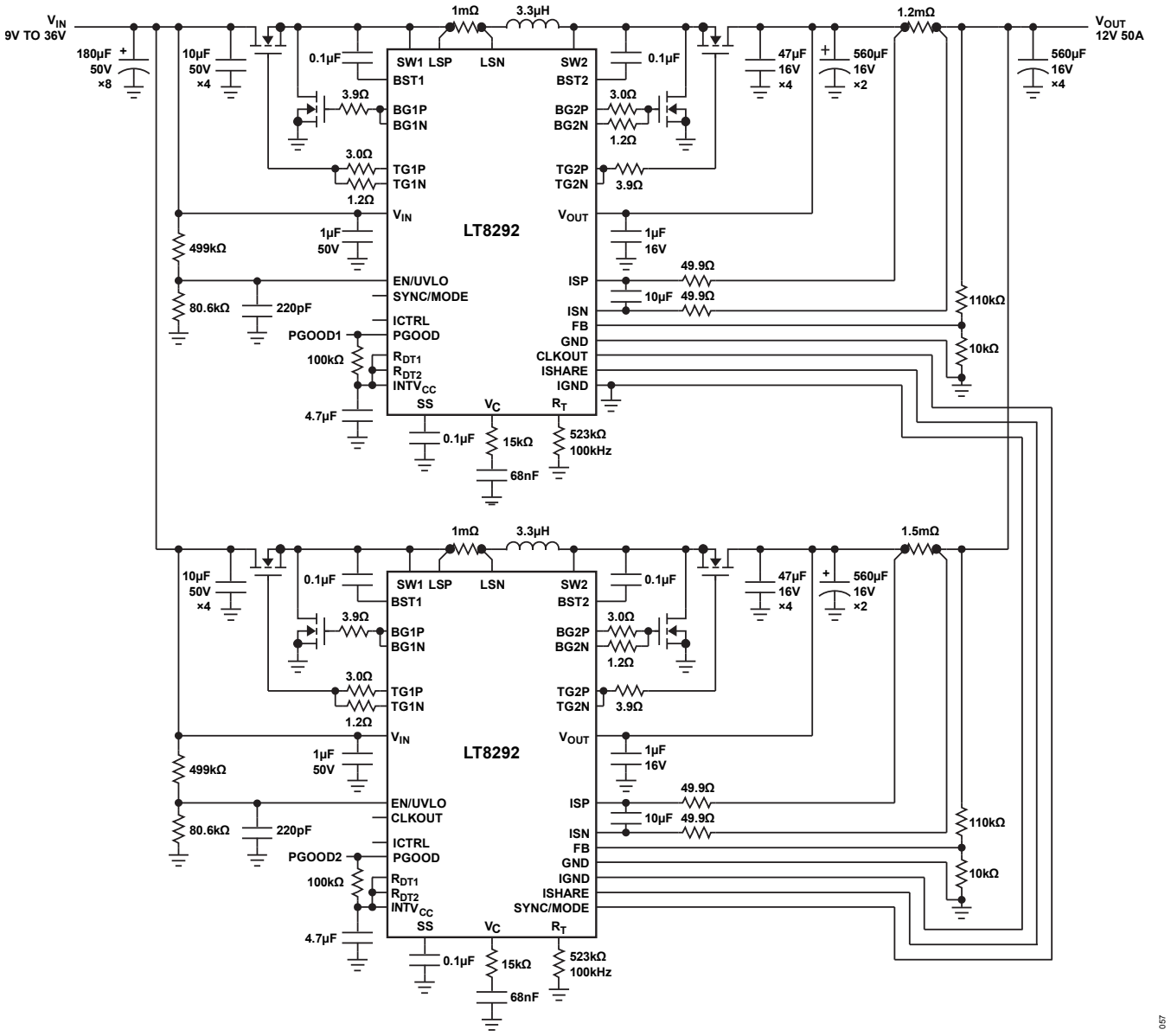


Figure 57. 600W (12V, 50A) 2-Phase Parallel Buck-Boost Voltage Regulator System with 180° Phase Shift using CLKOUT

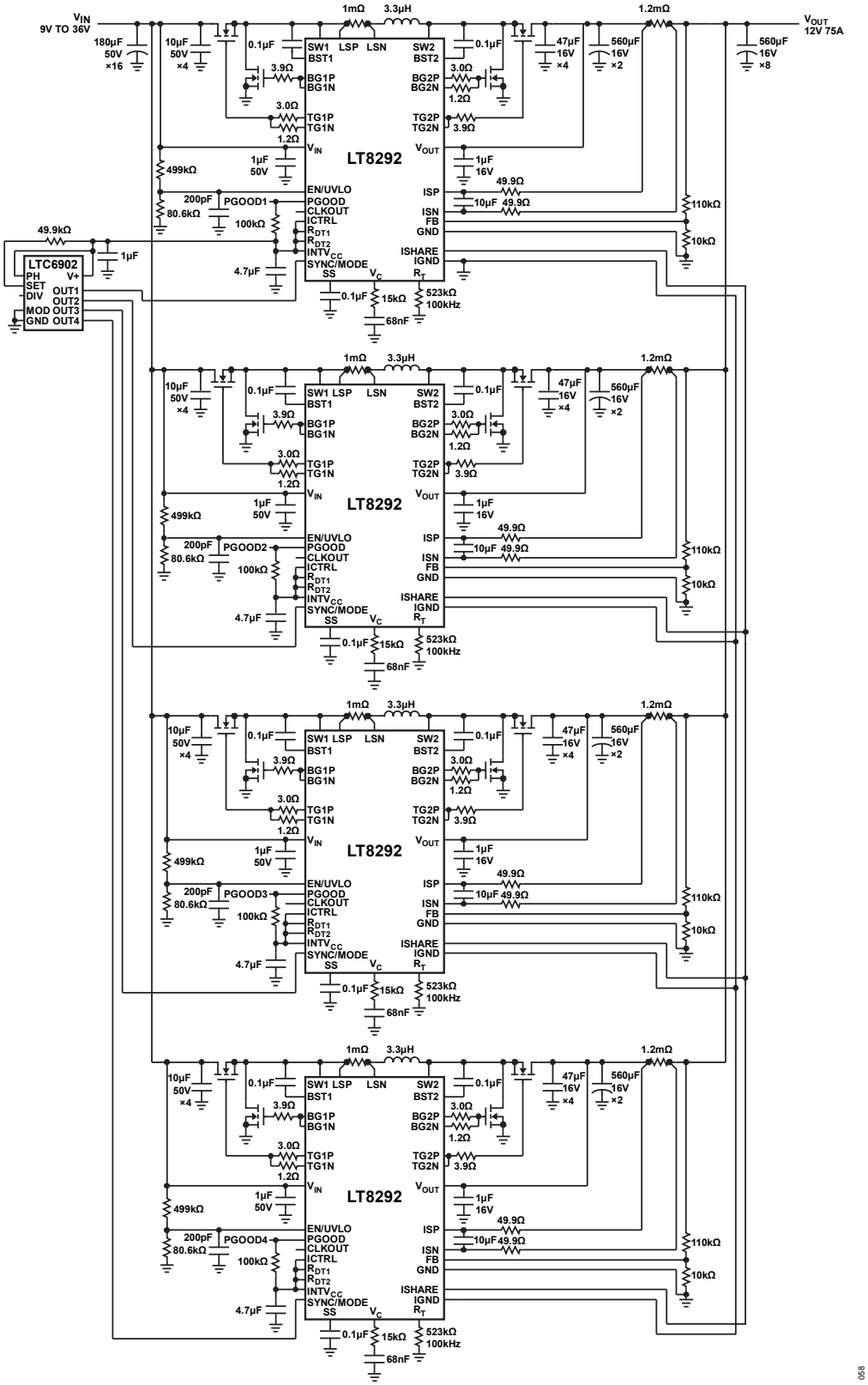
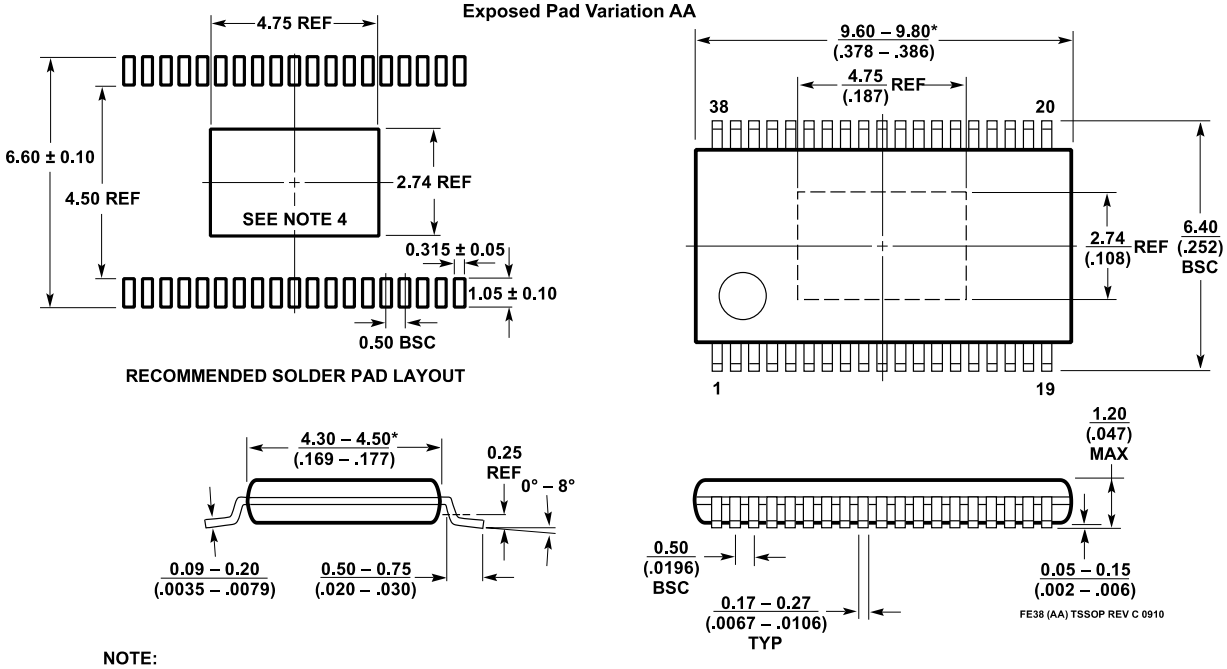


Figure 58. 1.2kW (12V, 100A) 4-Phase Parallel Buck-Boost Voltage Regulator System with 90° Phase Shift using LTC6902

OUTLINE DIMENSIONS

FE Package
38-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG#05-08-1772 Rev C)
Exposed Pad Variation AA



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

ORDERING GUIDE

Table 9. Ordering Guide

LEAD-FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8292AFE#PBF	LT8292AFE#TRPBF	LT8292FE	38-Lead Plastic TSSOP	–40°C to 125°C
AUTOMOTIVE PRODUCTS*				
LT8292AFE#WPBF	LT8292AFE#WTRPBF	LT8292FE	38-Lead Plastic TSSOP	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges.

*Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only automotive-grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability report for this model.

Mouser Electronics

Authorized Distributor

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