ANALOG DEVICES

Evaluation Board User Guide

EVAL-LTC7893-AZ

High Frequency Step-Up Controller with GaN FETs

General Description

The evaluation circuit EVAL-LTC7893-AZ is a single output synchronous step-up converter that drives GaN field effect transistors (FETs). The EVAL-LTC7893-AZ evaluation board features 100V GaN FETs.

The EVAL-LTC7893-AZ features the LTC®7893: a low quiescent current, high frequency (programmable fixed frequency from 100kHz up to 3MHz), step-up DC/DC synchronous controller, with a dedicated driver feature for GaN FETs, which can also be used to drive logic-level silicon FETs.

The EVAL-LTC7893-AZ operates over an input voltage range from 8V to 36V and produces a 48V output with load current up to 18A (without heatsink). A mode selector allows the EVAL-LTC7893-AZ to operate in forced continuous operation, pulse-skipping or Burst Mode® operation during light loads. The EVAL-LTC7893-AZ is set to 500kHz switching frequency, which results in a small and efficient circuit.

The performance summary table summarizes the performance of the evaluation circuit at room temperature. The evaluation circuit can be easily modified for different applications. The LTC7893 is housed in a 28-lead (4mm × 5mm), side-wettable QFN package. Refer to the data sheet in conjunction with this EVAL-LTC7893-AZ evaluation circuit user guide.

Design files for this circuit board are available at *www.analog.com*.

Performance Summary (T_A = 25°C)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	See *Figure 8*		8		36	V
Output Voltage, V_{OUT}	V_{IN} = 8V–36V		46.9	48.3	49.8	V
Output Voltage Ripple, $V_{OUT(AC)}$	V_{IN} = 12V, I_{OUT} = 5.5A			500		mV_{P-P}
Maximum Load, I_{OUT}	Maximum Component Temperature <100°C	V_{IN} = 8V			3.5	A
		V_{IN} = 12V			5.5	A
		V_{IN} = 24V			11	A
		V_{IN} = 36V			18	A
Run Rising Threshold, RUN				7.6		V
Run Falling Threshold, RUN				7.0		V
Input Current	FCM, V_{IN} = 12V, I_{OUT} = 0A			180		mA
	Burst Mode, V_{IN} = 12V, I_{OUT} = 0A			1		mA
Typical Switching Frequency	JP2 = DISABLE SS (SSFM OFF)			500		kHz
	JP2 = ENABLE SS (SSFM ON)		500		650	kHz
Efficiency	V_{IN} = 12V, V_{OUT} = 48V, I_{OUT1} = 5.5A			96.6		%
	V_{IN} = 24V, V_{OUT} = 48V, I_{OUT2} = 11A			98.2		%

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Quick Start Procedure

The EVAL-LTC7893-AZ evaluation circuit is easy to set up to evaluate the performance of the LTC7893 when used with GaN FETs. See *Figure 1* for proper measurement equipment setup, and follow the procedure below:

1. With power off, connect the input power supply to V_{IN} and GND.
2. Connect the output load between V_{OUT} and GND.
3. Enable the input power supply. Increase the V_{IN} to 12V. Make sure the RUN switch is set to the ON position. NOTE: Make sure that the input voltage is always within the specified range.
4. Check for the proper output voltages and verify that V_{OUT} = 48.3V.
5. Once the proper output voltage is established, adjust the input voltage and load current within the operating range and measure the output voltage regulation, ripple voltage, efficiency, and other parameters.
   NOTE: When measuring the input or output voltage ripple, take care to avoid a long ground lead on the oscilloscope probe. Measure the input or output voltage ripple by touching the probe tip directly across the V_{IN} or V_{OUT} and GND terminals or directly across the relevant capacitor. See *Figure 2* for the proper probing technique.

Adjusting the Output Voltage

The output voltage of the LTC7893 can be set from a range of 1.2V to 100V using a feedback resistor divider. The programmed output voltage of 48V can be changed by updating the values of R1 and R2. Refer to the Setting the Output Voltage section in the data sheet for calculating the V_{FB} resistor divider values for the desired output voltage. The corresponding power components may need to be changed to meet the desired output voltage.

Setting the Switching Frequency

Selecting the switching frequency is a trade-off between efficiency and component size. For optimal performance, a switching frequency of 500kHz is chosen. R13 programs the desired switching frequency. The switching frequency is set using FREQ and PLLIN/SPREAD pins. Refer to the Setting the Operating Frequency section in the LTC7893 data sheet for details.

RUN Control (RUN, S1)

The RUN turret of the evaluation circuit serve as an external on/off control for the controller. The EVAL-LTC7893-AZ includes a resistive voltage divider (R8 and R11) connected between V_{IN} and GND to turn on the device at the required input voltage. Turn the switch (S1) to the ON position to connect the RUN pin to the center of this resistor divider. The EVAL-LTC7893-AZ connects the run pin to a resistor divider set to turn on the LTC7893 at ~7.6V. The threshold can be adjusted by changing the resistor divider. See *Table 3* to configure S1.

Soft-Start Input (SS)

The LTC7893's SS pin can program an external soft-start function to allow V_{OUT} to ramp up over V_{IN}. The adjustable soft-start function is used to limit the inrush current during startup. The soft-start time is adjusted by changing the value of C5. Refer to the Soft-Start section in the data sheet.

Mode Selection (MODE, JP1)

The EVAL-LTC7893-AZ provides a jumper (JP1) to allow the LTC7893 to operate in either forced continuous, pulse skipping, or burst modes at lighter loads. Refer to the LTC7893 data sheet for more details on the modes of operation. Table 1 shows the mode selection JP1 settings that can be used to configure the desired mode of operation.

Spread Spectrum, Phase-Locked Loop, and External Frequency Synchronization (PLLIN/SPREAD, JP2)

The LTC7893 features spread spectrum mode operation to improve EMI. This mode varies the switching frequency within the typical boundaries of the frequency set by the FREQ pin and +20% typical. Spread spectrum operation is enabled by tying the PLLIN/SPREAD pin to $INTV_{CC}$. The EVAL-LTC7893-AZ includes a jumper (JP2) to conveniently enable or disable the spread spectrum operation. See Table 2 to configure JP2.

The LTC7893 also features a phase-locked loop to synchronize the internal oscillator to an external clock source. EVAL-LTC7893-AZ provides a SYNC turret to connect the external clock source to synchronize with the device switching. Keep the jumper (JP2) in the external sync position when the external clock signal is applied. Refer to the LTC7893 data sheet for more details about external clock synchronization.

Open-Drain PGOOD Output (PGOOD)

EVAL-LTC7893-AZ provides a PGOOD turret to monitor the status of the PGOOD output. PGOOD is high when the V_{FB} voltage is within ±10% of the 1.2V reference. PGOOD is pulled low when the V_{FB} voltage is not within 1.2V ±10% or the RUN pin voltage is low (shutdown). The voltage on the PGOOD pins should not exceed 6V.

$EXTV_{CC}$ Linear Regulator

The $EXTV_{CC}$ pin allows the $INTV_{CC}$ power to be derived from a high efficiency external source. On EVAL-LTC7893-AZ, the $EXTV_{CC}$ pin is connected to GND. The $EXTV_{CC}$ turret can be used to connect an external power supply to source the $EXTV_{CC}$ LDO. When using an external power supply on the $EXTV_{CC}$ turret, make sure to disconnect the GND connection to the $EXTV_{CC}$ pin by removing R6. Populate R4 with a 0Ω resistor.

Thermal Performance

The EVAL-LTC7893-AZ features excellent thermal performance. The component temperatures of EVAL-LTC7893-AZ with a 12V input and 5.5A load are shown in Figure 7. The six-layer PCB layout features solid copper planes that provide adequate heat spreading across the whole board. For input voltages lower than 36V, the output current must be derated to keep the maximum component temperature under 100°C. See Figure 8 for maximum output current vs. input voltage.

Heatsink

The EVAL-LTC7893-AZ features space for a heatsink to extend the power and thermal capabilities significantly. The board is designed for the Wakefield-Vette 567-45AB heatsink and is to be used in conjunction with thermal pads and Wurth Elektronik 9774010243R spacers. The spacers should be soldered onto P1, P2, P3, and P4, and a thermal pad placed between the heatsink and the GaN FETs. Properly screw in the heatsink to fully extend the power capabilities of the board.

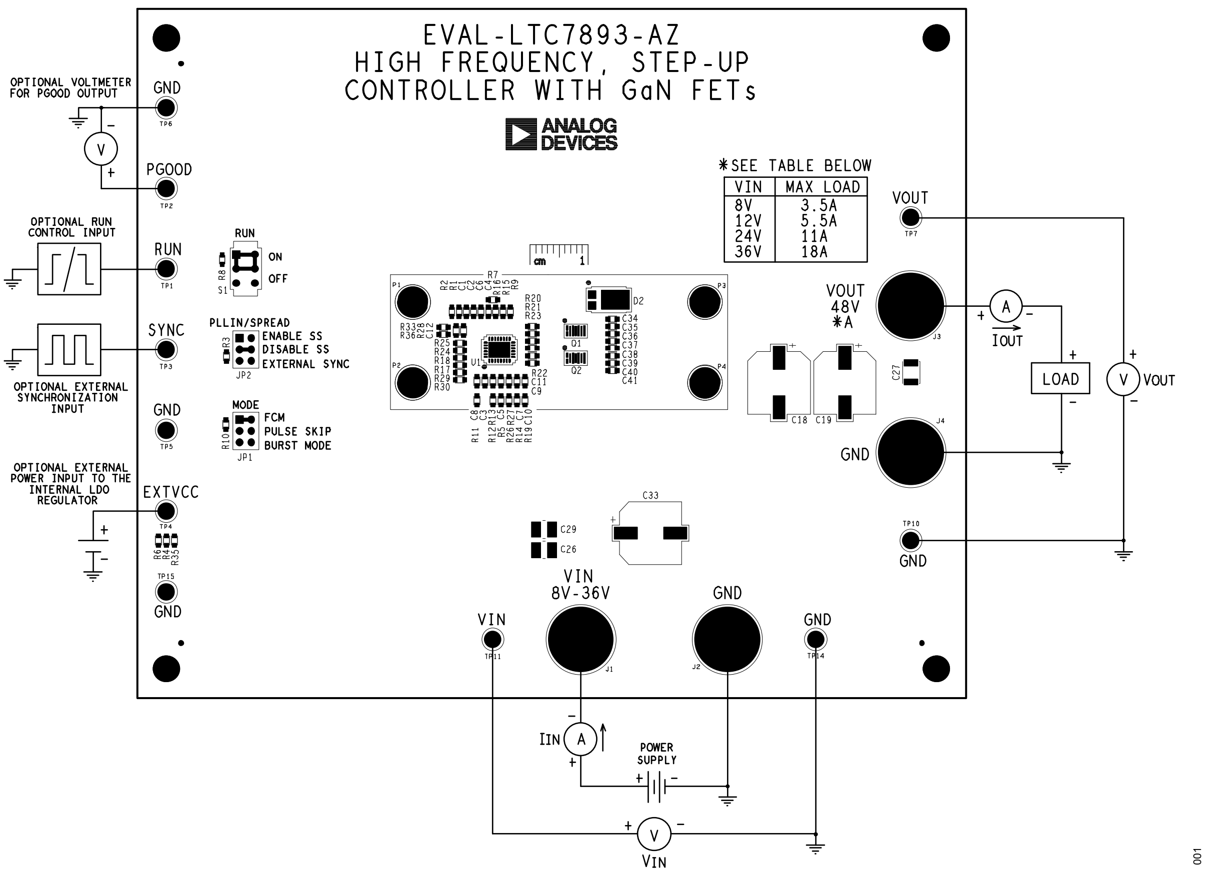


Figure 1. EVAL-LTC7893-AZ Board Connections

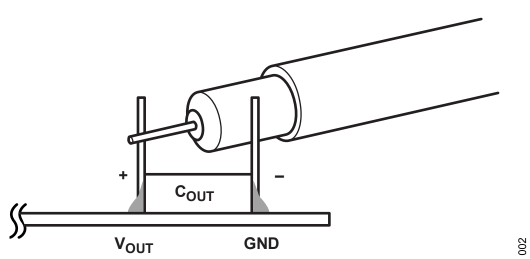


Figure 2. EVAL-LTC7893-AZ Ripple Measurement

Table 1. MODE Selection Jumper (JP1) Settings

SHUNT POSITION	MODE PIN	MODE
1-2*	Connected to $INTV_{CC}$	FCM mode of operation
3-4	Connected to $INTV_{CC}$ with a 100kΩ	Pulse-Skipping mode of operation
5-6	Connected to GND	Burst mode of operation

**Default position*

Table 2. PLLIN/SPREAD Jumper (JP2) Settings

SHUNT POSITION	PLLIN/SPREAD PIN	DESCRIPTION
1-2	Connected to $INTV_{CC}$	Enable SS
3-4*	Connected to GND	Disable SS
5-6	Connected to the center node of R3 and C3	External SYNC input

**Default position*

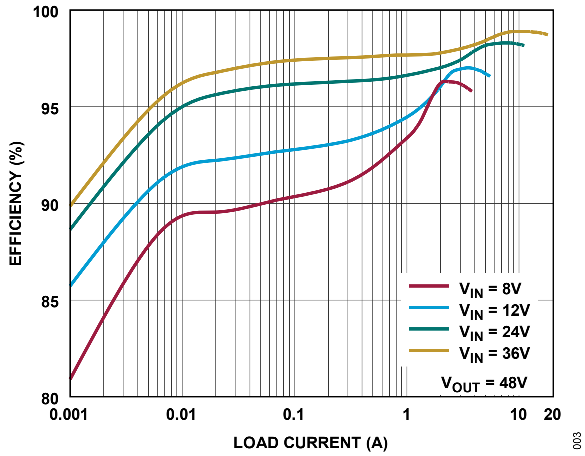
Table 3. RUN Switch (S1) Settings

SWITCH POSITION	RUN PIN	CONTROLLER
ON*	Connected to the center node of the resistor-divider R8 and R11	Programmed to startup at the desired input voltage level
OFF	Connected to GND	Disabled

**Default position*

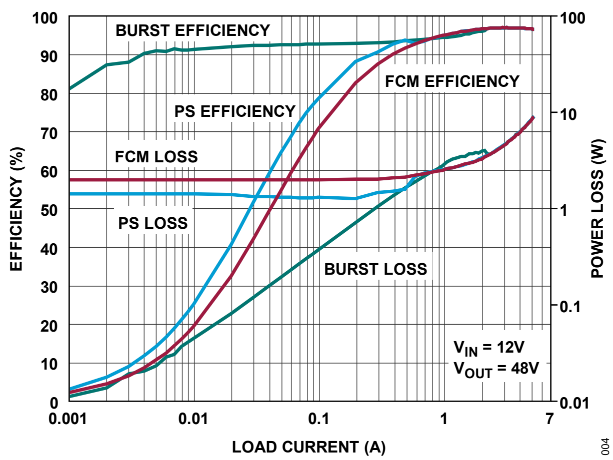
Performance

(T_A = +25°C, unless otherwise noted.)



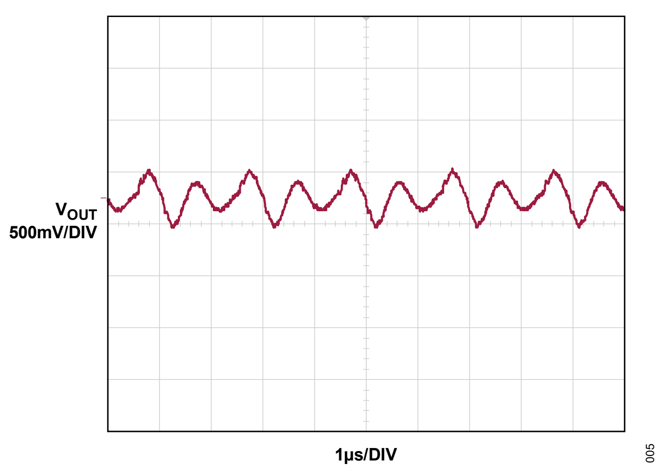
V_{OUT} = 48V, f_{SW} = 500kHz, Burst Mode

Figure 3. Efficiency vs. Load Current



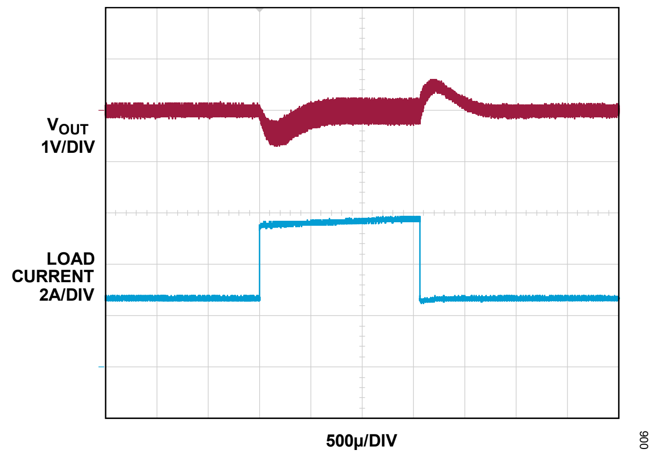
V_{IN} = 12V, V_{OUT} = 48V, f_{sw} = 500kHz

Figure 4. Efficiency and Power Loss vs. Load Current



V_{IN} = 12V, V_{OUT} = 48V, I_{OUT} = 5.5A (20MHz BW)

Figure 5. Output Voltage Ripple



V_{IN} = 12V, V_{OUT} = 48V, I_{OUT} = 2.7A-5.5A-2.7A

Figure 6. Load Transient Response

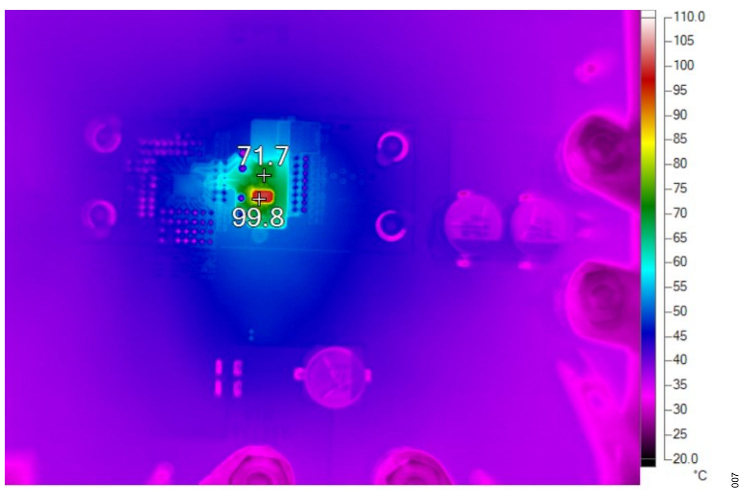


Figure 7. Typical Thermal Performance with a 12V Input, 48V Output, 5.5A Load, 500kHz Switching Frequency (Conditions: T_A = 25°C, No Forced Airflow)

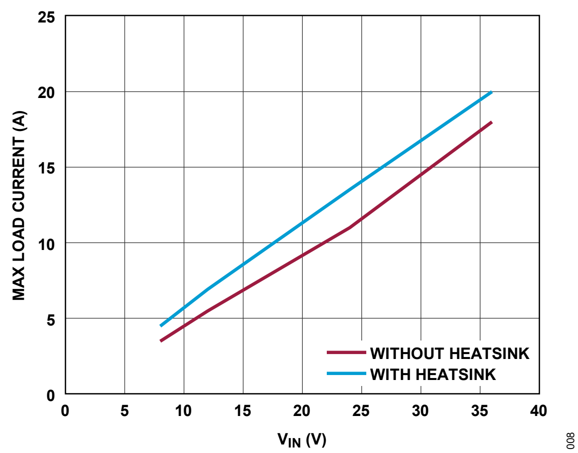
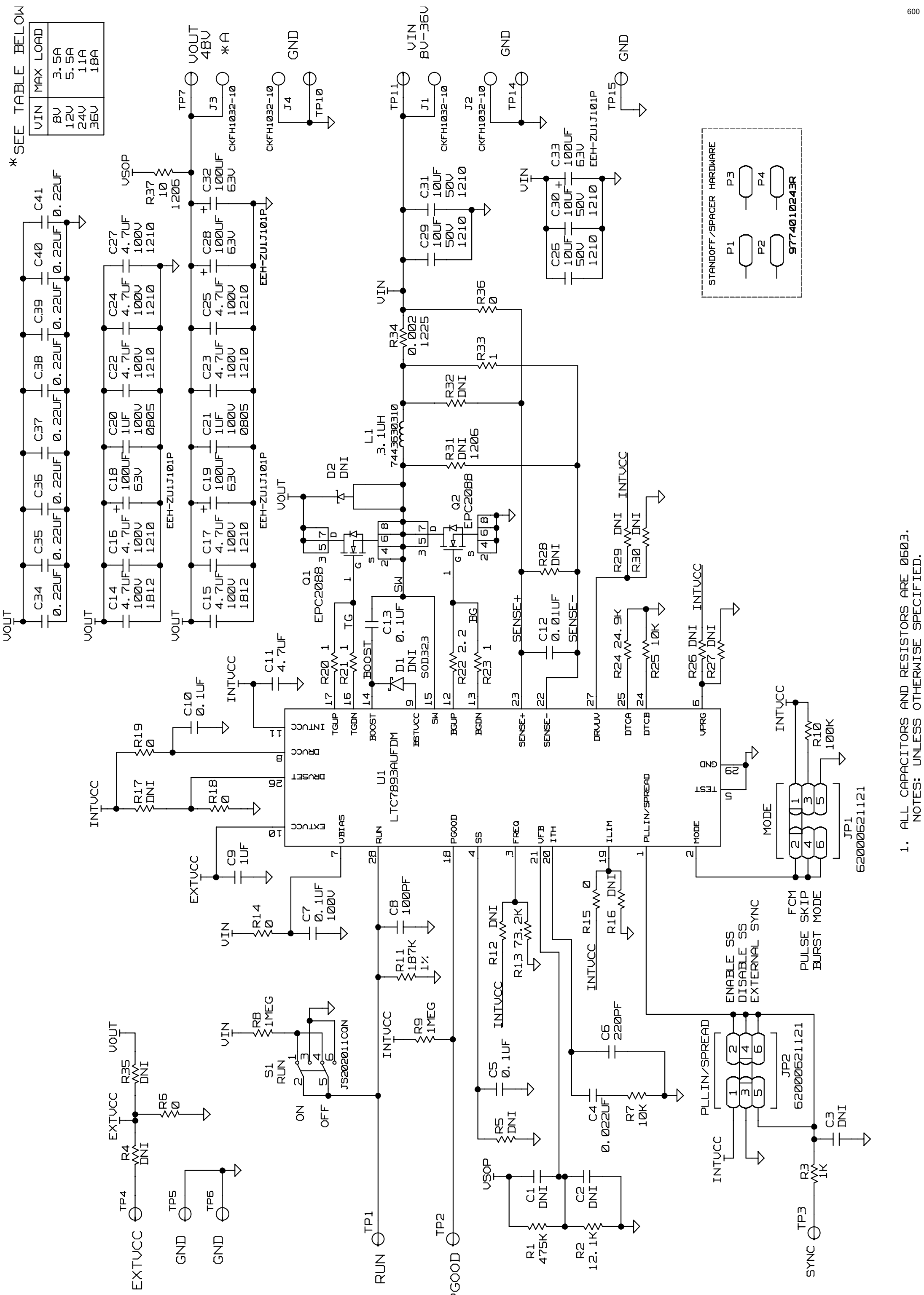


Figure 8. Maximum Output Current vs. Input Voltage (Conditions: T_A = 25°C, No Forced Airflow, Components temperature rise less than 100°C)

Schematic


*SEE TABLE BELOW
VIN | MAX LOAD
8V | 3.5A
12V | 5.5A
24V | 11A
36V | 18A
VOUT 48V *A
VIN 8V-36V
GND
U1 LTC7893AUFDM
L1 3.1UH 744363031
Q1 EPC2088
Q2 EPC2088
STANDOFF/SPACER HARDWARE
9774010243R
JP1 62000621121
JP2 62000621121
MODE
FCM
PULSE SKIP
BURST MODE
ENABLE SS
DISABLE SS
EXTERNAL SYNC
EXTVCC
RUN
PGOOD
SYNC
NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL CAPACITORS AND RESISTORS ARE 0603.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	09/24	Initial release	—

Notes