Evaluating the AD4050/AD4052 Compact, Low Power, 12-Bit/16-Bit, 2 MSPS Easy Drive SAR ADCs

FEATURES

- Full featured evaluation boards for the AD4050 and AD4052 with a USB power solution
- Single differential channel and common-mode input available through SMA connectors
- Out of the box evaluation experience with the SDP-K1
- PC software (ACE plugin) for control and data analysis of the time and frequency domains
- Compatible with other Arduino form factor controller boards

EQUIPMENT NEEDED

- PC with Windows 7 or later operating system
- SDP-K1 controller board and accompanying USB cable
- Precision signal generator (see the Evaluation Board Hardware section)

SOFTWARE NEEDED

- ACE evaluation software
- AD4050/AD4052 ACE plugin from the plugin manager (see the Software Installation Procedure section)

EVALUATION BOARD KIT CONTENTS

- EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ evaluation board

USEFUL LINKS AND RESOURCES

- AD4050 product page
- AD4052 product page
- EVAL-AD4050-ARDZ product page
- EVAL-AD4052-ARDZ product page
- ACE Installer

GENERAL DESCRIPTION

The EVAL-AD4050-ARDZ and EVAL-AD4052-ARDZ evaluation boards enable quick and easy evaluation of the performance and features of the AD4050 or the AD4052, respectively. The AD4050 and AD4052 are compact, low power, 12-bit or 16-bit (respectively) Easy Drive successive approximation register (SAR) analog-to-digital converters (ADCs).

The primary controller board for the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ is the SDP-K1. The EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ conform to the Arduino® Uno Shield mechanical and electrical standards to interface with the SDP-K1, in addition to various software development kits from other manufacturers.

The AD4050/AD4052 evaluation solutions include the AD4050/AD4052 industrial input and output (IIO) firmware application drivers for device configuration and ADC data capture and the AD4050/AD4052 ACE plugin graphical user interface (GUI) for performance evaluation.

EVALUATION BOARD PHOTOGRAPH

Figure 1. EVAL-AD4052-ARDZ Evaluation Board Photograph

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REVISION HISTORY

8/2024—Rev. 0 to Rev. A

Added EVAL-AD4050 (Universal) 1

5/2024—Revision 0: Initial Version

QUICK START GUIDE

The AD4050/AD4052 ACE plugin is the evaluation GUI that interfaces with the firmware on the SDP-K1 controller board to communicate with the connected EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ evaluation board. The ACE software must be installed prior to installing and running the AD4050/AD4052 ACE plugin. See the Software Installation Procedure section for instructions on downloading the ACE software and the AD4050/AD4052 ACE plugin.

HARDWARE SETUP

This section details how to set up the AD4050/AD4052 and SDP-K1 boards for use with the AD4050/AD4052 ACE plugin. Refer to the Evaluation Board Hardware section for detailed descriptions of the on-board circuit blocks and for descriptions of all jumpers referenced in this section.

To set up the hardware, complete the following steps:

- Disconnect both the evaluation board and the SDP-K1 from all power sources before connecting them together.
- The EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ connect to the SDP-K1 via the Arduino Uno compatible headers (P1 to P4). Plug the headers on the bottom side of the evaluation board to the corresponding headers on the top side of the SDP-K1 (see Figure 2).

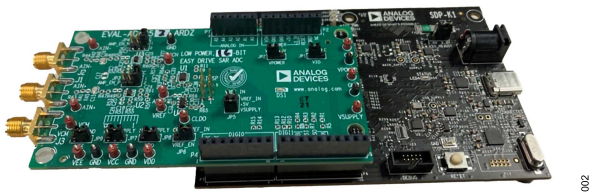

Figure 2. EVAL-AD4052-ARDZ and SDP-K1 Connections

The SDP-K1 supports both 3.3 V and 1.8 V logic levels, and the logic level is selected with the VIO_ADJUST jumper. Although the AD4050/AD4052 ADCs are compatible with either logic level, the AD4050/AD4052 ACE plugin requires that VIO_ADJUST be set to 3.3 V.

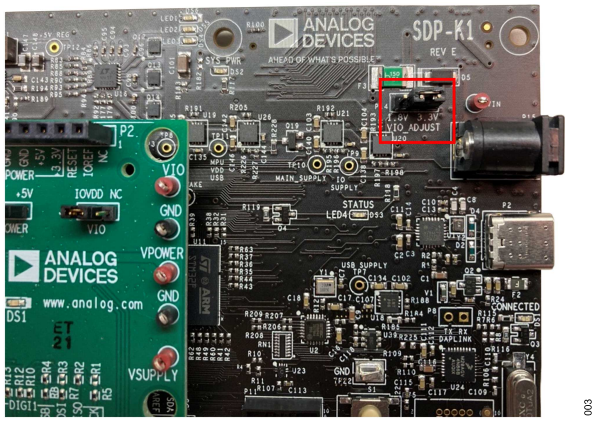

Figure 3. VIO_ADJUST Jumper on SDP-K1 Board

After the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ are connected to the SDP-K1 board and the VIO_ADJUST jumper is in the desired location, power can be applied to the SDP-K1. The SDP-K1 accepts power from either the USB cable and port from the PC or from a separate switched-mode DC power supply (7 V to 12 V, see the SDP-K1 User Guide for more information). The DS1 light-emitting diode (LED) illuminates when the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ are receiving power from the SDP-K1 and is generating the +3.3 V rail to the on-board AD4050/AD4052 and its companion circuitry.

When powering from the USB, perform the following steps:

- Ensure the JP2 jumper on the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ is set to the +5 V position. This position connects the evaluation board power management circuitry to the +5 V pin on the Arduino Uno power header.
- Connect the SDP-K1 to the PC with a USB cable. After a few seconds, the SYS_PWR LED on the SDP-K1 illuminates to indicate the SDP-K1 is receiving power from the USB.

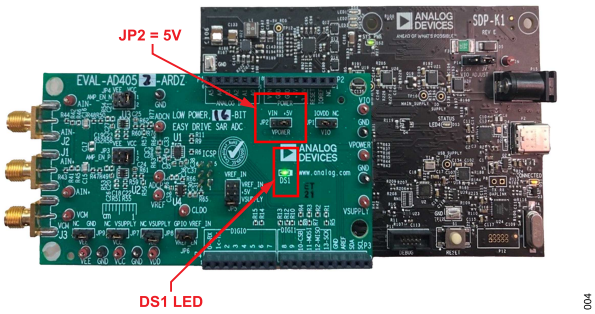

Figure 4. EVAL-AD4052-ARDZ on USB Power

When powering from an external power supply, perform the following steps:

- Ensure the JP2 jumper on the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ is set to the VIN position. This position connects the evaluation board power management circuitry to the VIN pin on the Arduino Uno power header.
- Plug the external power supply into the DC jack (P15) on the SDP-K1. The SYS_PWR LED on the SDP-K1 illuminates to indicate the SDP-K1 is receiving power from the external power supply.
- After the external power supply is connected, connect the SDP-K1 to the PC with a USB cable.

QUICK START GUIDE

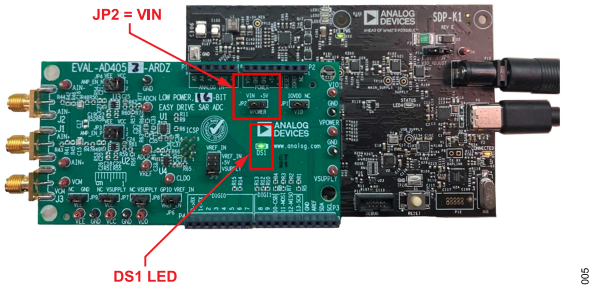

Figure 5. EVAL-AD4052-ARDZ on DC Jack Power

Before launching the AD4050/AD4052 ACE plugin, it is recommended to connect a precision signal source or signal generator to the analog input Subminiature Version A (SMA) connectors to drive the AD4050/AD4052 inputs into their specified operating ranges. See the Analog Front End (AFE) section for more information.

If no signal generator is available, a jumper cable between the VREF and VCM test points can be used to bias the AD4050/AD4052 analog inputs to VREF. This is preferred over connecting the amplifier inputs to GND, because the amplifier VEE rails are connected to GND by default.

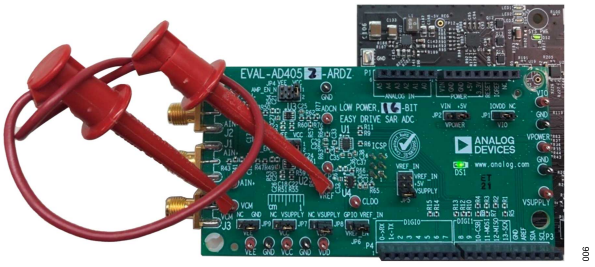

Figure 6. Biasing the EVAL-AD4052-ARDZ Inputs Without Signal Generator Hardware for Software Validation

EVALUATION BOARD HARDWARE

HARDWARE OVERVIEW

The EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ include the AD4050/AD4052 with companion circuitry for an out of the box evaluation experience. The EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ also include several prototyping options for the analog and digital circuitry on board, as described in the following sections.

Figure 7 shows a simplified block diagram of the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ. Figure 8 and Figure 9 show the location of the primary circuit blocks on the board. The factory-default circuitry includes the following:

- AD4050BCPZ/AD4052BCPZ: the 14-lead LFCSP model of the AD4050/AD4052
- The low-noise, low-power MAX6070 voltage reference provides a 2.5 V reference voltage for the AD4050/AD4052
- Two low-power, rail-to-rail input and output MAX44260 operational amplifiers (op amps) buffer the signal generator's output to the AD4050/AD4052 analog inputs
- The AD7118 regulates the SDP-K1 input power source down to a 3.3 V rail to power the AD4050/AD4052 and other analog components

These companion components were selected to simplify evaluation and achieve typical performance characteristics of the AD4050/AD4052 and are not necessarily applicable to all system designs and use cases.

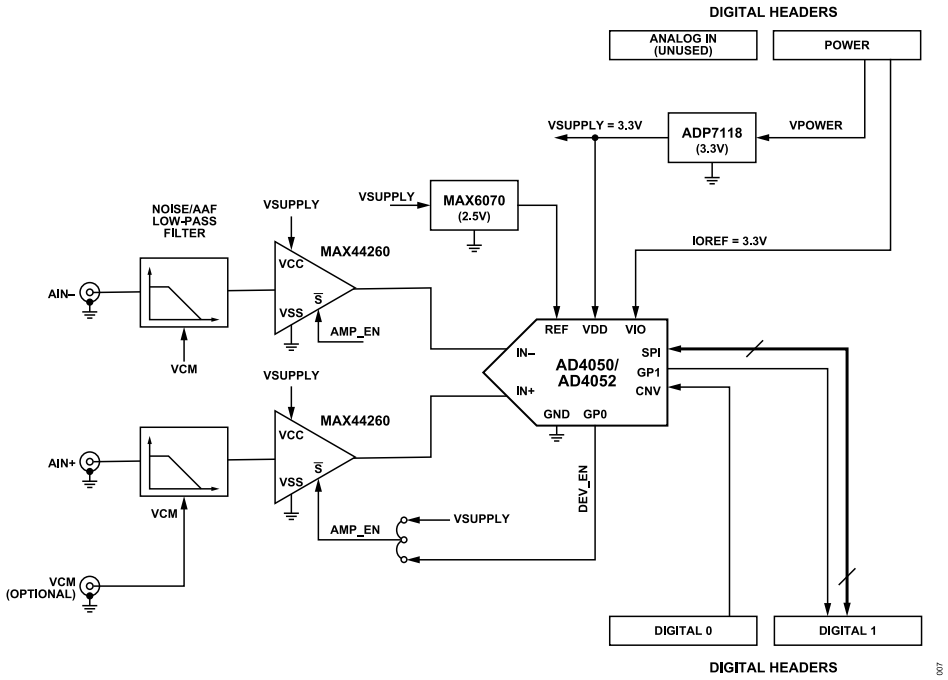

Figure 7. EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ Simplified Block Diagram

EVALUATION BOARD HARDWARE

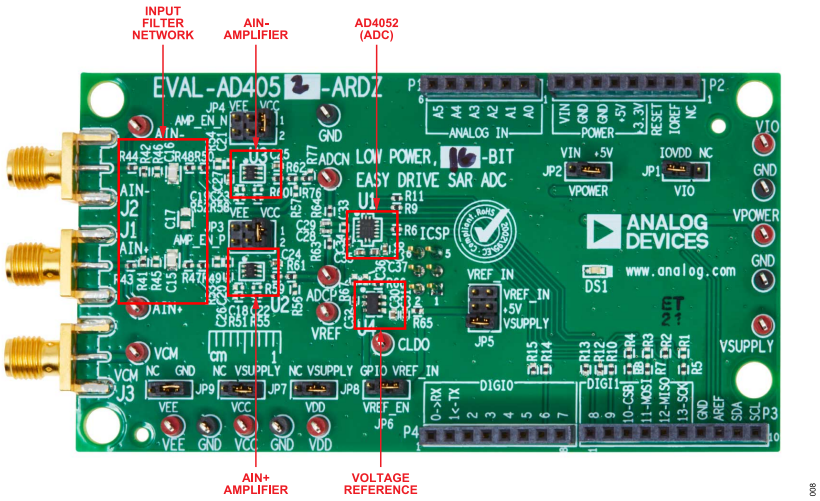

Figure 8. EVAL-AD4052-ARDZ Evaluation Board Circuitry Locations Top Side

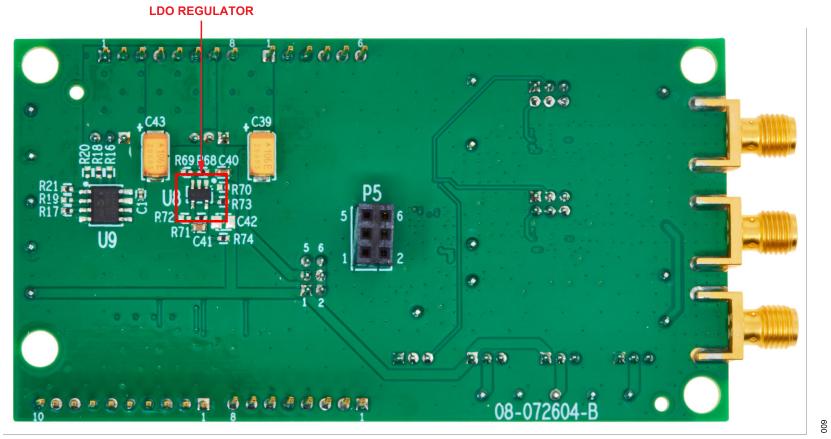

Figure 9. EVAL-AD4052-ARDZ Evaluation Board Circuitry Locations Bottom Side

EVALUATION BOARD HARDWARE

CONNECTORS AND SOCKETS

The connectors and sockets on the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ are outlined in Table 1.

Table 1. On-Board Connectors

Connector	Function
AIN−	Negative analog input (SMA)
AIN+	Positive analog input (SMA)
VCM	Common-mode input (SMA)
P1 to P4	Arduino Uno headers

DIGITAL INTERFACE CONNECTIONS

The AD4050/AD4052 digital interface includes an SPI for reading and writing data, a CNV input for initiating conversions, and two GPIOs with multiple functions. The AD4050/AD4052 digital interface signals are transmitted between the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ and the controller board via the Arduino Uno digital headers (P3 and P4). The digital pin function assignment conforms to the Arduino Uno standard. The digital headers and signals are primarily on page 3 of both the EVAL-AD4050-ARDZ schematics PDF and the EVAL-AD4052-ARDZ schematics PDF. Table 2 details the digital signal names, default and secondary functions, and digital header pin assignments.

The EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ include an electrically erasable programmable read-only memory (EEPROM) (U9) used by the AD4050/AD4052 ACE plugin to identify and connect to the board. The controller board communicates with the EEPROM via the inter-integrated circuit (I^2C) pins on the Arduino Uno header.

Note the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ include the ICSP header (P5) to conform to the Arduino Uno mechanical specification only. The pins on this header are not routed out as signals to the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ.

Table 2. Digital Header Connections

Signal Name	Function	Header Pin	Arduino Pin Name	Pull-Up/Pull-Down
CNV	ADC convert-start trigger.	P4 Pin 7	D6/PWM	100 kΩ pull-down (R15)
GP1	ADC GPIO 1. Functions as the data ready (RDYb) signal from the AD4052 by default.	P3 Pin 1	D8	100 kΩ pull-down (R13)
GP0	ADC GPIO 0. No function by default. Can optionally be configured as the AD4052 DEV_EN timer output to power-cycle the front-end amplifiers with custom firmware (see JP3 and JP4).	P3 Pin 2	D9/PWM	100 kΩ pull-down (R12)
CSB	SPI chip-select.	P3 Pin 3	D10/PWM/CSB	100 kΩ pull-up (R4)
SDI	SPI serial data in (MOSI).	P3 Pin 4	D11/PWM/MOSI	DNI pull-up (R3)
SDO	SPI serial data out (MISO).	P3 Pin 5	D12/MISO	100 kΩ pull-up (R2)
SCLK	SPI serial clock.	P3 Pin 6	D13/SCK	DNI pull-up (R1)
SDA_ARD	I^2C serial data. Used to read board ID data from the EEPROM.	P3 Pin 9	SDA	
SCL_ARD	I^2C serial clock. Used to read board ID data from the EEPROM.	P3 Pin 10	SCL	

EVALUATION BOARD HARDWARE

POWER SUPPLIES

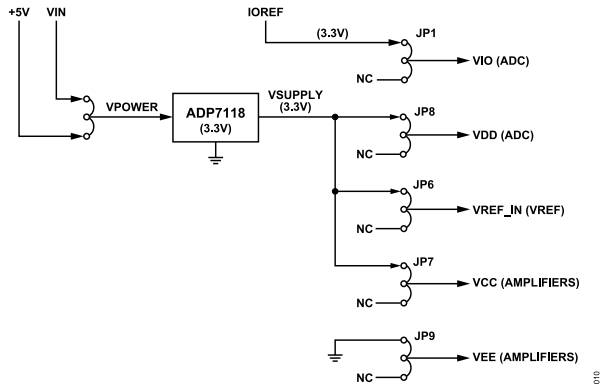

Figure 10. EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ Power Tree

Figure 10 shows the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ power tree. In factory default configuration, the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ analog circuitry is powered by an on-board 3.3 V supply and the AD4050/AD4052 I/O logic voltage is supplied directly from the controller board's IOREF voltage (for example, the SDP-K1's 3.3 V IOREF supply). The on-board ADP7118 LDO regulator (U8) regulates the controller board power into a low-noise 3.3 V rail to supply the AD4050/AD4052, the voltage reference, and the op amps. The power circuitry is located on page 3 of the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ schematic PDF.

The controller board (SDP-K1, for example) provides the input power for the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ through the Arduino Uno power header (P2 on the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ). The JP2 jumper selects between the +5 V or VIN as the input source of the ADP7118 that supplies the 3.3 V analog rail. By default, +5 V is selected, as 5 V has enough headroom for the ADP7118 to generate a regulated 3.3 V output. The SDP-K1 can generate the 5 V supply from either an external switched-mode DC supply or from the USB port (see the SDP-K1 user guide). The EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ supply current demand in the default configuration is low enough to be powered off the USB port without an additional supply.

The AD4050/AD4052 digital I/O logic supplies (VIO) are sourced directly from the IOREF voltage from the controller board via P2. This ensures the AD4050/AD4052 digital interfaces operate on the same logic levels as the controller board. The AD4050/AD4052 support 3.3 V logic. By default, the JP1 jumper connects the VIO supply on the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ to the IOREF supply from the controller board.

Table 3 lists the power domains present on the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ as named in the schematic. Each power rail can be measured or driven with external supplies via the test points labeled in the table. See the Hardware and Link Options section for details on how to configure the jumpers to supply the rails with external supplies. Refer to the data sheets for each relevant product when providing power externally.

Table 3. EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ Power Domains

Power Rail	Function	Test Point Name	Default Nominal Voltage (V)
+5 V	5 V power source from the P2 header.	N/A	5
VIN	VIN power source from the P2 header, generated by optional DC jack on SDP-K1.	N/A	7 to 12
IOREF	Controller board I/O logic supply.	N/A	3.3
GND	Power ground.	GND	0
VPOWER	Primary power input from the P2 header. Sourced from either +5 V or VIN.	VPOWER	5
VSUPPLY	Primary analog supply generated by on-board ADP7118. Distributed to analog component supply pins.	VSUPPLY	3.3
VCC	Amplifier positive supply rail.	VCC	3.3 (VSUPPLY)
VEE	Amplifier negative supply rail.	VEE	0 (GND)
VREF_IN	Voltage reference supply input.	N/A	3.3 (VSUPPLY)
VDD	AD4050/AD4052 analog input, sourced from VSUPPLY via JP8.	VDD	3.3 (VSUPPLY)
CLDO	AD4050/AD4052 internal LDO regulator output. By default, the AD4050/AD4052 generates this supply with an internal LDO regulator.	CLDO	1.8
VIO	AD4050/AD4052 digital logic supply.	VIO	3.3 (IOREF)

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VOLTAGE REFERENCE CIRCUIT

In the factory default configuration, the on board MAX6070 (U4) provides a 2.5 V reference voltage (VREF) to the AD4050/AD4052 REF input. The VREF sets the input range of the AD4050/AD4052, as described in the AD4050 and AD4052 data sheets. By default, the MAX6070 is powered by the 3.3 V analog rail. A 2.2 µF VREF decoupling capacitor (C34) is located next to the AD4050/AD4052 REF pin to ensure a stable 2.5 V VREF voltage during the conversion time of the SAR ADC core.

ANALOG FRONT END (AFE)

The AFE components provide signal conditioning between the signal generator outputs and the AD4050/AD4052 analog inputs (IN+ and IN− pins). In the factory default configuration, the AFE consists of the following components:

- SMA connectors for the positive and negative inputs (J1 and J2, respectively)
- SMA connector for an optional common-mode voltage (VCM) source (J3)
- Passive filter network for signal generator noise and/or anti-aliasing filtering (see Figure 11)
- MAX44260 op amps in 6-lead SC70 footprint configured as unity-gain buffers by default (see Figure 12)
- RC kickback filter at the AD4050/AD4052 inputs

The Analog Inputs section provides instructions for interfacing the signal generator and the SMA inputs on the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ.

By default, the amplifiers are configured as unity-gain buffers, but optional passive components are included in the design to support noninverting with gain, single-pole active filter, and Sallen-Key filter configurations.

By default, all amplifiers are powered with a single supply with VEE connected to GND and VCC supplied by VSUPPLY = 3.3 V. See the Power Supplies section for more details.

The shutdown pins on the AFE amplifiers can optionally be routed to the GP0 pin on the AD4050/AD4052 via JP3 and JP4 jumpers. This allows performance and power measurements using the DEV_EN control signal from the AD4050/AD4052 to power-cycle the amplifiers in between conversions. See the AD4050 and AD4052 data sheets for more information on the DEV_EN control signal for dynamic power cycling of the AFE.

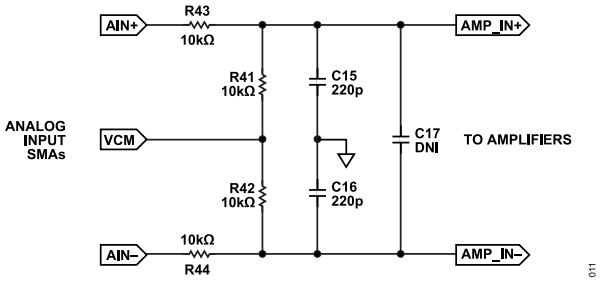

Figure 11. Signal and Common-Mode Inputs and Input Filter

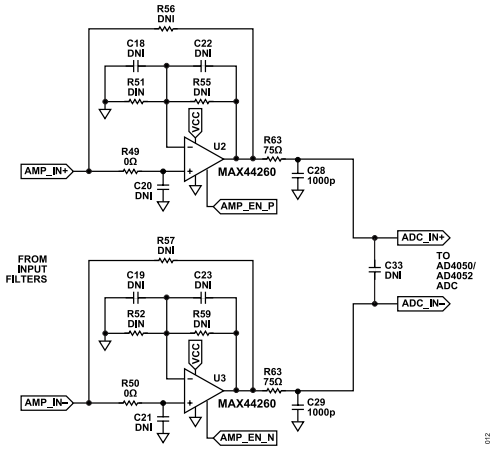

Figure 12. Default Amplifier Circuit Simplified Schematics

Analog Inputs

This section provides guidance for driving the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ with a precision signal generator for ADC performance evaluation.

The AD4050/AD4052 input range is set by the VREF voltage. In the factory default configuration, the on board MAX6070 generates a 2.5 V VREF (see Voltage Reference Circuit section). Therefore, the AD4050/AD4052 input is 0 V to 2.5 V on either input (IN+ and IN−) for a resulting maximum differential input swing of 2.5 V peak and 5 V p-p.

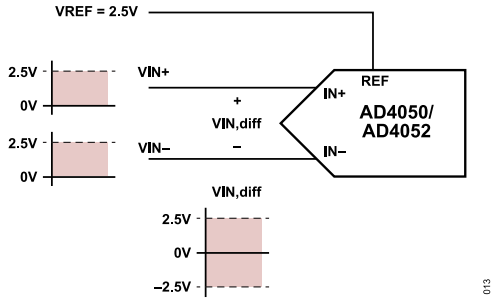

Figure 13. AD4050/AD4052 Input Range

By default, the MAX44260 amplifiers driving the AD4050/AD4052 analog inputs are configured as unity-gain buffers, so the signal on their noninverting inputs must also be limited to 0 V to 2.5 V. When

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populating optional feedback networks for larger gain, the input signal must be limited such that the output swings of the amplifier stay within the AD4050/AD4052 input range.

The following provides some examples for hooking up different types of signal generators to the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ. All of these examples ignore the output impedance of the signal generator:

- For signal generators with bipolar, differential output swings (signals that go below GND), the VCM input provides a means to apply the necessary DC offset to satisfy the input range specification of the MAX44260 amplifiers. Figure 14 gives an example with a 2.5 V VREF and amplifiers in unity-gain configuration. The signal source (VS) is 5 V peak or 10 V p-p and VCM is 2.5 V DC.
- For signal generators with floating, differential outputs, the VCM input provides a means to apply the necessary DC offset to satisfy the input range specification of the MAX44260 amplifiers. Figure 15 gives an example with a 2.5 V VREF and amplifiers in unity-gain configuration. The differential input swing (VIN,diff) is 5 V peak or 10 V p-p and VCM is 1.25 V DC.
- For signal generators with differential outputs that provide their own DC offset, the VCM input can be left disconnected. In the factory default configuration, the R41 and R42 resistors that are used with the VCM input will attenuate the differential input signal by half. It is recommended to disconnect R41 and R42 when using these types of signal generators, as shown in Figure 16. VIN,diff is 2.5 V peak or 5 V p-p, and VCM is 1.25 V DC.

Note that any noise generated by the signal generator will propagate through the AFE circuit and appear at the AD4050/AD4052 analog inputs. If the noise of the signal generator is large enough, performance metrics like SNR, RMS noise, and others will be affected. If the noise signal is common to both the positive and negative inputs, then the AD4050/AD4052 will reject some portion of it depending on the bandwidth of the device. If the noise signal is differential (or when operating the board with a single-ended signal generator), the noise will couple directly into the ADC samples.

By default, the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ are populated with a single-pole RC low-pass filter set to a bandwidth of ~140 kHz to assist with anti-aliasing and noise filtering. The RC filter components can be modified based on the input signal bandwidth and noise targets for the evaluation or prototyping system.

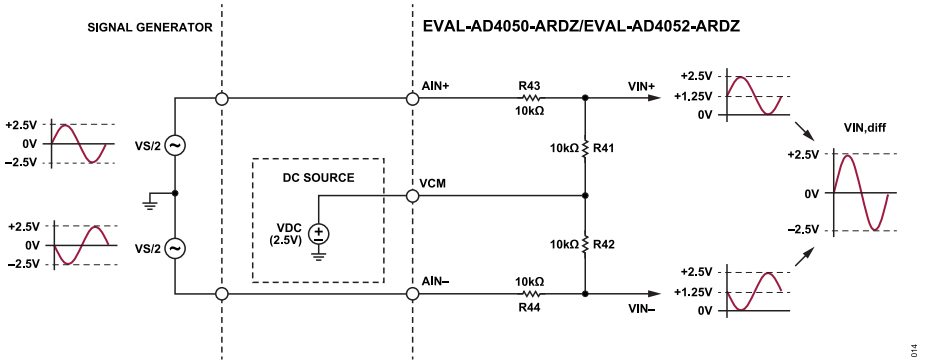

Figure 14. Bipolar Differential Signal Generator Example

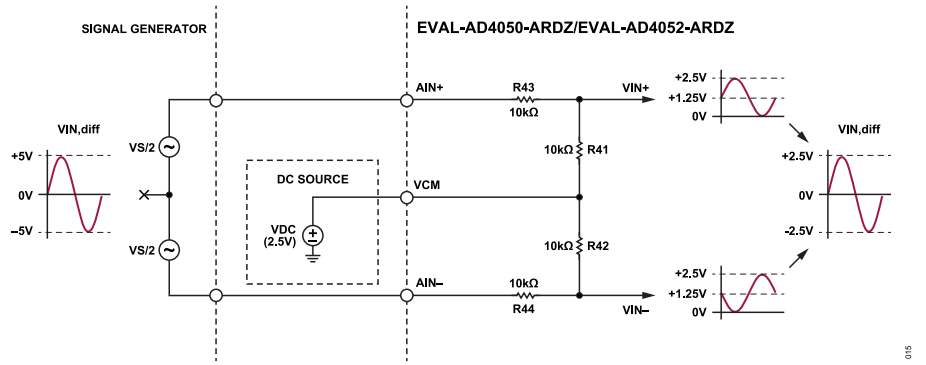

Figure 15. Floating Differential Signal Generator Example

EVALUATION BOARD HARDWARE

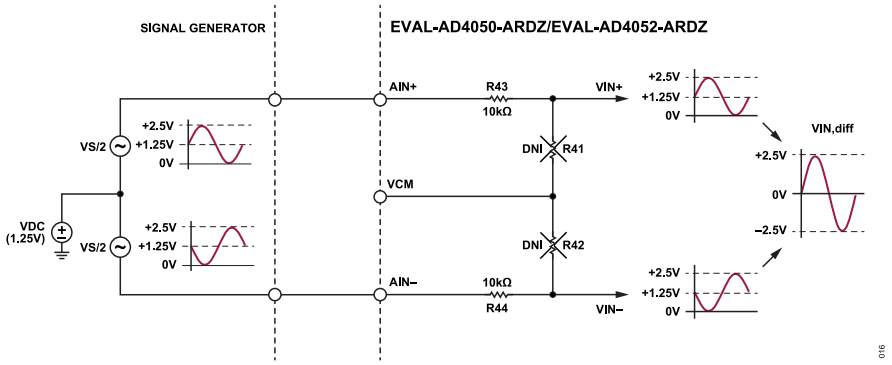

Figure 16. Biased Differential Signal Generator Example

EVALUATION BOARD HARDWARE

HARDWARE AND LINK OPTIONS

Table 4 details each of the optional jumper and link options present on the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ with a brief description of the default and secondary positions and functions.

Table 4. Jumper and Link Options and Descriptions

Jumper Reference Designator	Description	Default Position/Function	Secondary Position/Function(s)
JP1	VIO Source Selection	1: VIO supplied by the IOREF supply of the controller board.	3: No connect. Place the jumper in this position if supplying VIO by an external supply.
JP2	VPOWER Source Selection	3: VPOWER supplied by the +5 V supply of the controller board.	1: VPOWER supplied by the VIN supply of the controller board.
JP3	AIN+ Amplifier Shutdown Selection	1 to 2: Shutdown pin tied high to enable amplifier.	3 to 4: Shutdown pin driven by AD4050/AD4052 DEV_EN signal on GP0. Allows prototyping with dynamic power scaling. 5 to 6: Shutdown pin tied low to disable amplifier.
JP4	AIN− Amplifier Shutdown Selection	1 to 2: Shutdown pin tied high to enable amplifier.	3 to 4: Shutdown pin driven by AD4050/AD4052 DEV_EN signal on GP0. Allows prototyping with dynamic power scaling. 5 to 6: Shutdown pin tied low to disable amplifier.
JP5	VREF_IN Source Selection	1 to 2: VREF_IN supplied by VSUPPLY.	3 to 4: VREF_IN supplied by +5 V. Allows prototyping with different voltage references up to 3.3 V. 5 to 6: No connect. Place the jumper in this position if powering VREF_IN from an external supply.
JP6	VREF Shutdown Selection	1: Shutdown pin tied high to enable voltage reference.	3: Shutdown pin connected to GPIO signal. Allows prototyping of dynamic power scaling of voltage reference during long periods without ADC activity.
JP7	VCC Source Selection	1: VCC supplied by VSUPPLY.	3: No connect. Place the jumper in this position if powering VCC from an external supply.
JP8	VDD Source Selection	1: VDD supplied by VSUPPLY.	3: No connect. Place the jumper in this position if powering VDD from an external supply.
JP9	VEE Source Selection	1: VEE tied to GND.	3: No connect. Place the jumper in this position if powering VEE from an external supply.

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION PROCEDURE

Download the ACE evaluation software from the EVAL-AD4050-ARDZ or the EVAL-AD4052-ARDZ evaluation kit page. Install the software on a PC before using the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ kit. Download the AD4050/AD4052 ACE plugin from the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ product page or from the ACE plugin manager.

Perform the following steps to complete the installation process:

1. Install the ACE evaluation software.
2. Install the AD4050/AD4052 plugin. The ACE Quickstart page shows the plugin installation guide.

INSTALLING THE ACE EVALUATION SOFTWARE

To install the ACE evaluation software, take the following steps:

1. Download the ACE software to a Windows-based PC.
2. Double click the **ACEInstall.exe** file to begin the installation. By default, the ACE software is saved to the following location: **C:\Program Files (x86)\Analog Devices\ACE**.
3. A dialog box opens asking for permission to allow the program to make changes to the PC. Click **Yes** to start the installation process.
4. In the **ACE Setup** window, click **Next >** to continue the installation.

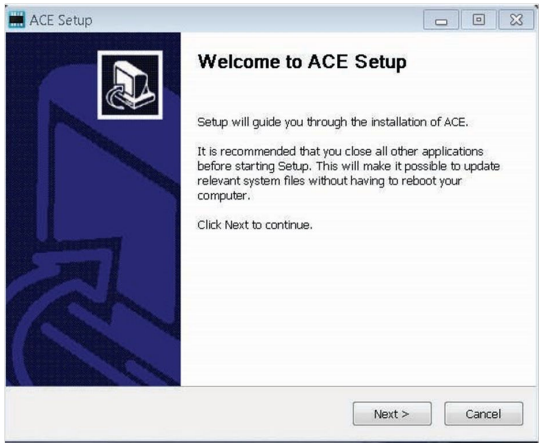

Figure 17. Evaluation Software Installation Confirmation

5. Read the software license agreement and click **I Agree**.
6. Click **Browse...** to choose the installation location and then click **Next >**.

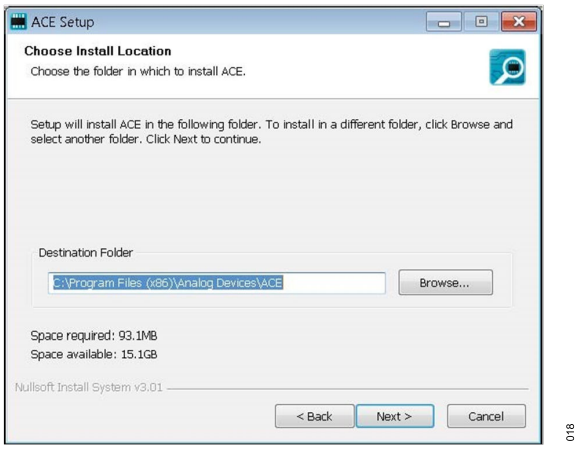

Figure 18. Choose Installation Location Window

7. The ACE software components to install are preselected. Click **Install** and wait for installation to complete.

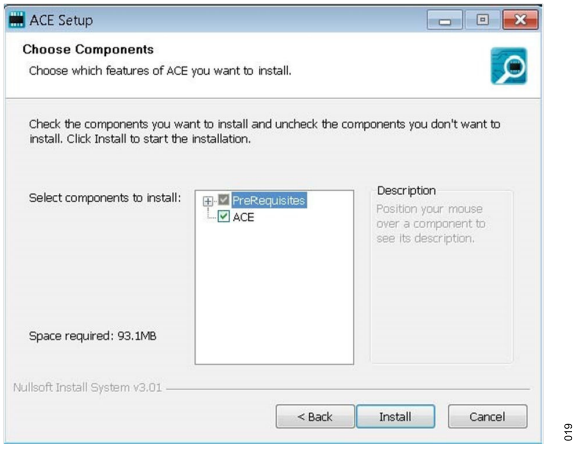

Figure 19. Choose ACE Installation Components Window

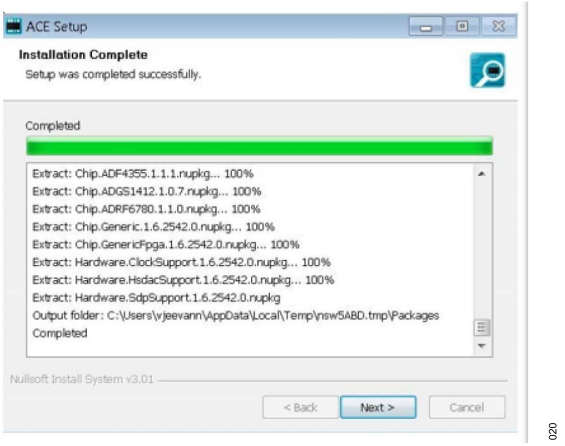

Figure 20. ACE Installation Progress Window

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INSTALLING THE AD4050/AD4052 ACE PLUGIN

1. Download and install the ACE software tool from the ACE download page, as per the Installing the ACE Evaluation Software section. If ACE is already installed, make sure you have the latest version by using **Check For Updates** option in the ACE sidebar, as shown in Figure 21.

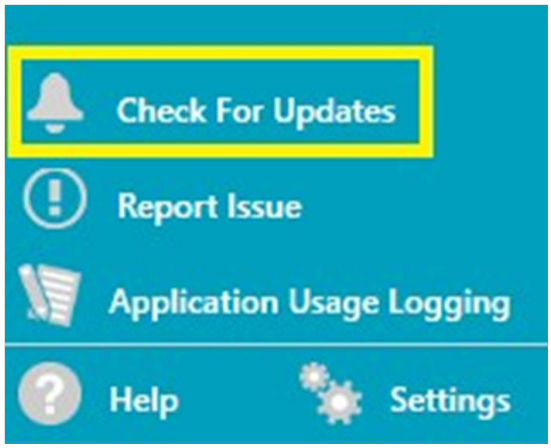

Figure 21. Check for Updates in the ACE Sidebar

2. Run the **ACE** software. Select **Plugin Manager** from the ACE sidebar to install the board plugin that supports the product evaluation board, and select **Available Packages**, as shown in Figure 22. You can use the search field to help filter the list of boards to find the relevant one. An ACE quick start guide is available at ACE Quickstart - Using ACE and Installing Plugins.

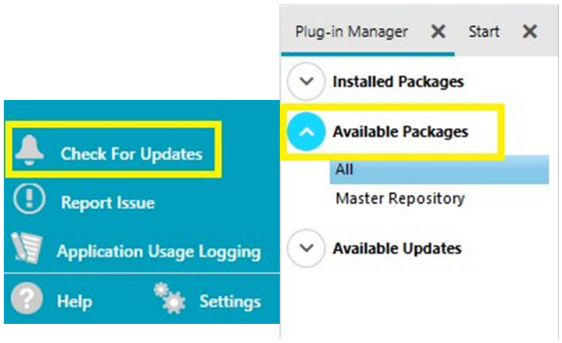

Figure 22. Plugin Manager Option in the ACESidebar

LAUNCHING THE SOFTWARE

To start the ACE evaluation software, open the Windows **Start** menu and click **Analog Devices > ACE**. The software window continues loading until the software recognizes the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ. When the software recognizes the board, a firmware loading prompt will appear (see Figure 23). Click **OK** and ACE will begin loading the generic tinyiiod firmware onto the SDP-K1. (Note that after connecting to the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ, the ACE plugin will need to load an AD4050/AD4052 specific firmware build, as described in the Board View and Firmware Selection section).

After several seconds, the firmware will be flashed onto the SDP-K1, and the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ icon will appear under **Attached Hardware**. Double-click on the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ icon to launch the AD4050/AD4052 ACE plugin.

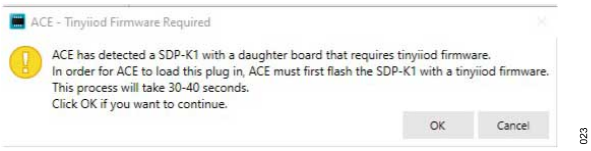

Figure 23. ACE Firmware Loading Prompt (Press OK)

BOARD VIEW AND FIRMWARE SELECTION

After connecting to the EVAL-AD4050-ARDZ/EVAL-AD4052-ARDZ board, ACE loads the AD4050/AD4052 plugin board view (see Figure 24). The **Firmware Config Wizard** tab includes a dropdown menu for selecting between the available firmware builds. One of these firmware options must be loaded onto the SDP-K1 via the **Firmware Config Wizard** before proceeding to the AD4050/AD4052 chip view and data capture and analysis tools.

Each firmware build corresponds to a different AD4050/AD4052 operating mode. See the AD4050/AD4052 plugin markdown documentation for a list of the firmware builds with corresponding functionality.

To load the firmware onto the SDP-K1, select it from the **Firmware Config Wizard** dropdown list and press **Apply**. While the firmware is loading, ACE may appear unresponsive. After a few seconds, ACE will finish flashing the SDP-K1 with the specific AD4050/AD4052 firmware, and the rest of the plugin functionality will become available.

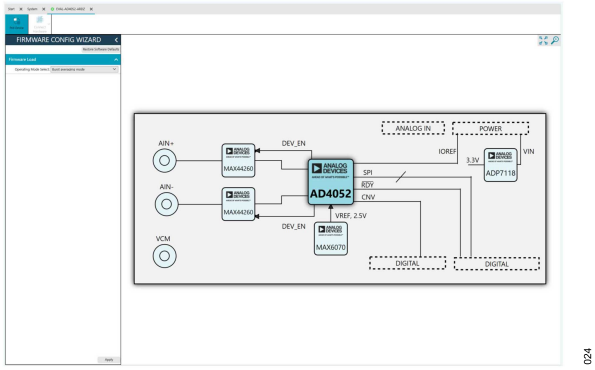

Figure 24. AD4052 Plugin Board View

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CHIP VIEW

Hover over the AD4050/AD4052 symbol in the **Board View** and double click to enter the **Chip View** (see Figure 25).

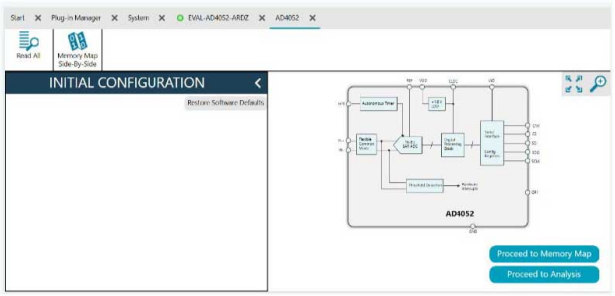

Figure 25. AD4052 Plugin Chip View

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ANALYSIS VIEW

Click **Proceed to Analysis** to navigate to the **AD4050/AD4052 Analysis** window. From here, choose the type of analysis to be performed by selecting the **Waveform** tab, the **Histogram** tab, or the **FFT** tab. Select options for **Run Once** or **Run Continuous** to begin capturing data that will appear in the **Results** section and the **Waveform** plot window. Select channel results are displayed in the **Displayed Channels** section (default is display all).

Waveform Tab

The **Waveform** tab displays data in the form of time vs. discrete data values with the results, as shown in Figure 26.

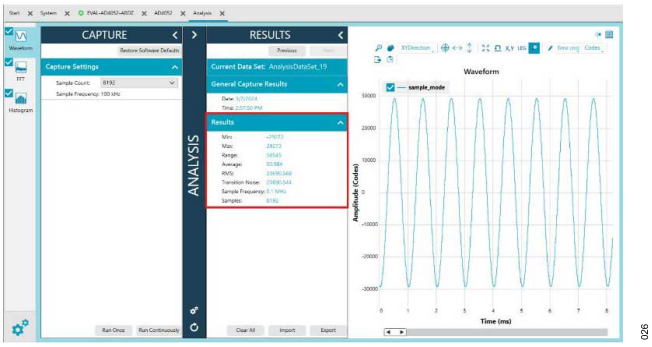

Figure 26. Waveform Tab

The **Waveform** graph shows each successive sample of the AD4050/AD4052 output. The user can zoom in on and pan over the **Waveform** graph using the embedded waveform tool bar located above the graph. Select the channels to display in the **Display Channels** section.

Under the **Display Units** pull-down menu, select **Codes** above the **Waveform** graph to select whether the **Waveform** graph displays in units of **Codes**, **Hex**, or **Volts**. The axis controls are dynamic.

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Histogram Tab

The **Histogram** tab contains the histogram graph and the **Results** pane, as shown in Figure 27.

The **Results** pane displays the information related to the DC performance.

The **Histogram** graph displays the number of hits per code within the sampled data. Use this graph for DC analysis as it indicates the noise performance of the device.

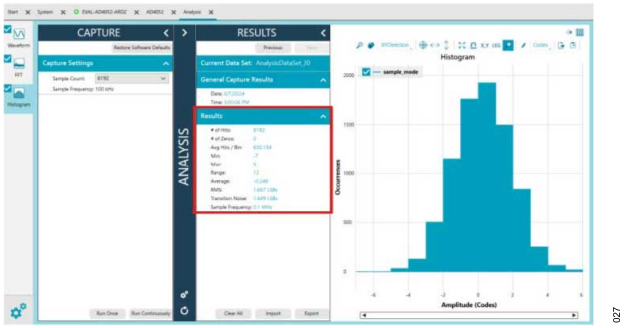

Figure 27. Histogram Tab

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FFT Tab

The **FFT** tab displays fast Fourier transform (FFT) information for the last batch of samples gathered (see Figure 28).

When performing an FFT analysis, the **RESULTS** pane shows the noise and distortion performance of the AD4050/AD4052. The signal-to-noise ratio (**SNR**) and other noise performance measurements, such as the signal-to-noise-and-distortion (**SINAD**), **Dynamic Range**, noise density (**Noise/Hz**), and peak harmonic or spurious noise (**SFDR**), are shown in the **RESULTS** pane. The total harmonic disturbance (**THD**) measurements, as well as the major harmonics contributing to the THD performance, are shown also.

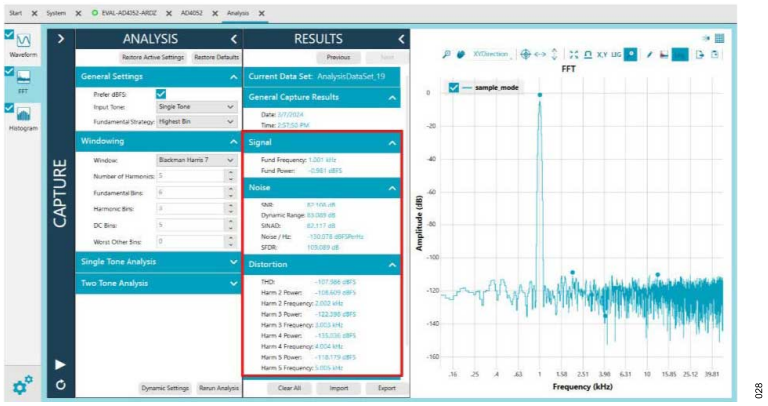

Figure 28. FFT Tab

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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EVAL-AD4050-ARDZ