Data Sheet

ADPL62092

Low-Power, Supervisory Circuit with Manual Reset and Watchdog Timer in 5-Lead SOT23

FEATURES

- Low Supply Current: 5µA (typ), 6.8µA (max) at 3.6V Over Temperature (T_A = +125°C)
- Factory-Set Reset Threshold Options from 1V to 5V in 50mV/100mV Increments
- Watchdog Timer Capability
- Manual Reset Input
- Guaranteed Reset Valid to V_{CC} ≥ 1V
- Open-Drain Reset Output
- Power Supply Transient Immunity
- -40°C to +125°C Operating Temperature Range

APPLICATIONS

- Portable/Battery-Powered Equipment or Instrumentation
- Smartphones
- MP3 Players/e-Reader Tablets
- Glucose and Patient Monitors

GENERAL DESCRIPTION

The ADPL62092 is a supervisory circuit that monitors voltages from 1.1V to 5V using a factory-set reset threshold. It offers a watchdog timer and manual reset capability.

The ADPL62092 features an open-drain, active-low reset output. The reset output asserts and remains asserted for the reset timeout period after the monitored voltage exceeds its threshold.

The ADPL62092 is available in 5-pin SOT23 package. It can operate over the -40°C to +125°C temperature range.

SIMPLIFIED APPLICATION DIAGRAM

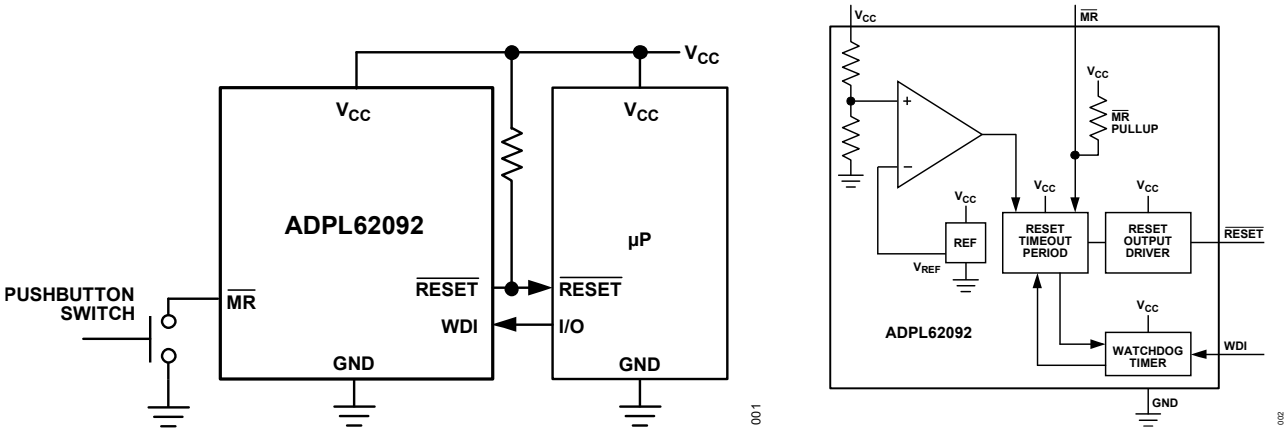

Figure 1. (a) Typical Application Circuit and (b) Functional Block Diagram

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REVISION HISTORY

11/2024 - Rev 0: Initial Release

SPECIFICATIONS

Table 1. Electrical Characteristics

(V_{CC} = 1V to 5.5V, C1 = 0.1µF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.[1])

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	[2]	1.0		5.5	V
V_{CC} Undervoltage Lockout	V_{CCUVLO}	[3]			0.9	V
Supply Current	I_{CC}	V_{CC} = 5.5V, no load with WDI input		8	10	µA
		V_{CC} = 3.6V, no load with WDI input		5	6.8	µA
Threshold Voltage	V_{TH}	T_A = -40°C to +125°C	V_{TH} + 3.0%	V_{TH}	V_{TH} + 3.0%	V
Reset Threshold Hysteresis	V_{HYST}	V_{CC} rising		5		$\%V_{TH}$
Reset Threshold Tempco	ΔV_{TH}/°C			30		ppm/°C
$\overline{\text{RESET}}$ OUTPUT						
Output Low	V_{OL}	V_{CC} = $V_{TH(MIN)}$, V_{TH} > 4.25V, I_{SINK} = 10mA			0.4	V
		V_{CC} = $V_{TH(MIN)}$, V_{TH} > 2.5V, I_{SINK} = 3.2mA			0.4	V
		V_{CC} = $V_{TH(MIN)}$, V_{TH} > 1.67V, I_{SINK} = 1mA			0.4	V
		V_{CC} = $V_{TH(MIN)}$, V_{TH} > 1V, I_{SINK} = 100µA			0.4	V
		V_{TH} > 0.9V, V_{CC} falling, I_{SINK} = 15µA			0.4	V
High Impulse Leakage		Reset not asserted		0.2	1	µA
MANUAL RESET INPUT ($\overline{\text{MR}}$)						
$\overline{\text{MR}}$ Input High Voltage	V_{IH}		0.7 x V_{CC}			V
$\overline{\text{MR}}$ Input Low Voltage	V_{IL}				0.3 x V_{CC}	V
$\overline{\text{MR}}$ Pull-up Resistance			25	50	80	kΩ
WATCHDOG INPUT (WDI)						
WDI Input High Voltage	V_{WDI-IH}		0.8 x V_{CC}			V
WDI Input Low Voltage	V_{WDI-IL}				0.3 x V_{CC}	V
WDI Input Current	I_{WDI}		-1		+1	µA

(V_{CC} = 1V to 5.5V, C1 = 0.1µF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.[1])

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING						
Reset Timeout Period	t_{RP}			30		µs
		V_{CC1} = 1.1V x V_{TH}	t_{RP} - 33%	t_{RP}	t_{RP} + 33%	ms
$\overline{MR}$ Minimum Pulse Width	t_{MPW}		1			µs
$\overline{MR}$ Glitch Rejection	t_{EGR}			100		ns
$\overline{MR}$ to Reset Delay				200		ns
V_{CC} to Reset Delay	t_{RD}	V_{CC} falling at 10mV/µs from (V_{TH} + 100mV) to (V_{TH} - 100mV)		30		µs
WDI Minimum Pulse Width			100			ns
Watchdog Timeout Period	t_{WD}	V_{CC1} = 1.1V x V_{TH}	t_{WD} - 33%	t_{WD}	t_{WD} + 33%	ms

1 Production testing done at T_A = +25°C only. Overtemperature limits are guaranteed by design and are not production tested.

2 Reset is guaranteed down to V_{CC} = 1V.

3 Guaranteed by design.

Timing Diagrams

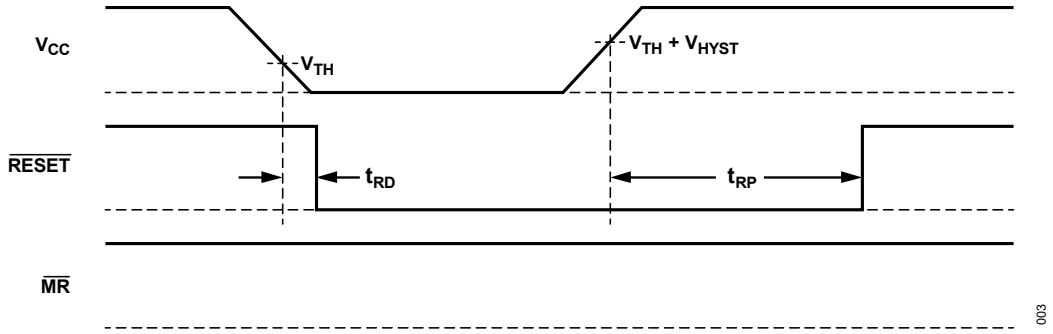

Figure 2. Reset Timing Diagram

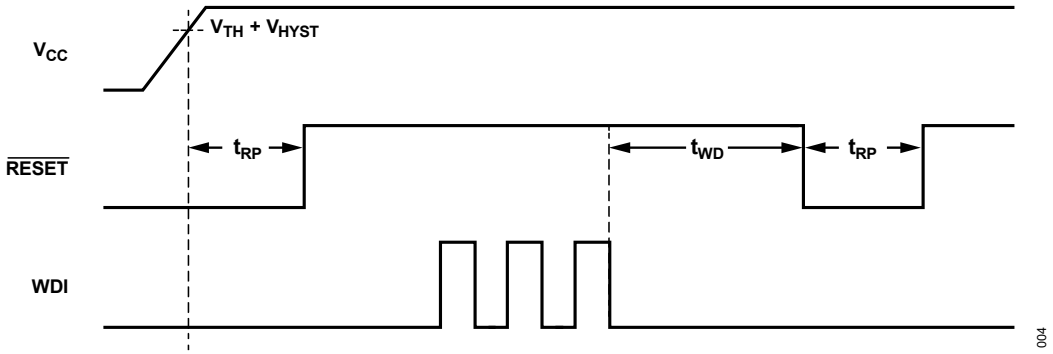

Figure 3. Watchdog Input Timing Diagram

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C, unless otherwise specified.)

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
V_{CC}	-0.3V to +6V
$\overline{RESET}$	-0.3V to +6V
$\overline{MR}$, WDI Input	-0.3V to (V_{CC} + 0.3)V
Input/Output Current (all pins)	20mA
Continuous Power Dissipation (T_A = +70°C) (derate 3.9mW/°C above +70°C)	313mW
Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

PACKAGE INFORMATION

Table 3. Package Information

5 SOT23	
Package Code	U5+2
Outline Number	*21-0057*
Land Pattern Number	*90-0174*
Thermal Resistance, Multi-Layer Board:	
Junction-to-Ambient (θ_{JA})	255.9°C/W
Junction-to-Case (θ_{JC})	81°C/W

For the latest package outline information and land patterns (footprints), go to *Package Index*. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *Thermal Characterization of IC Packages*.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

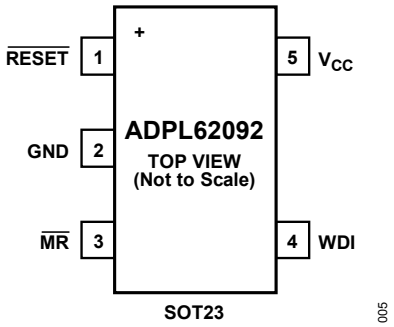

Figure 4. Pin Configuration

Pin Descriptions

Table 4. Pin Descriptions

PIN	NAME	DESCRIPTION
1	$\overline{\text{RESET}}$	Active-Low, Open-Drain Reset Output. $\overline{\text{RESET}}$ changes from high impedance to active low when V_{CC} drops below the detector threshold (V_{TH}), or $\overline{\text{MR}}$ is pulled low, or the watchdog triggers a reset. $\overline{\text{RESET}}$ remains low for the reset timeout period after V_{CC} exceeds the reset threshold and $\overline{\text{MR}}$ is high, or the watchdog triggers a reset.
2	GND	Ground
3	$\overline{\text{MR}}$	Active-Low, Manual Reset Input. Drive low to force a reset. Reset remains active as long as $\overline{\text{MR}}$ is low and for the reset timeout period (if applicable) after $\overline{\text{MR}}$ is driven high. $\overline{\text{MR}}$ has an internal pull-up resistor connected to V_{CC}, which can be left unconnected if it is not used.
4	WDI	Watchdog Input. If WDI remains high or low for the duration of the watchdog timeout period, the internal watchdog timer expires and triggers a reset. The internal watchdog timer clears whenever a reset asserts, or WDI sees a rising or falling edge. To disable the watchdog feature, leave WDI unconnected or three-state the driver connected to WDI.
5	V_{CC}	Supply Voltage and Input for the Reset Threshold Monitor. Connect a 0.1µF capacitor from V_{CC} to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

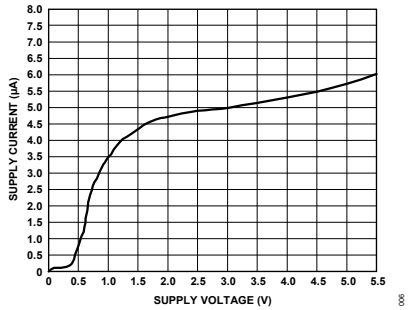

Figure 5. Supply Current vs. Supply Voltage

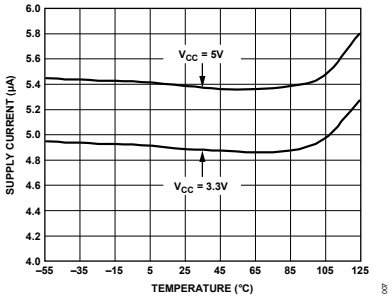

Figure 6. Supply Current vs. Temperature

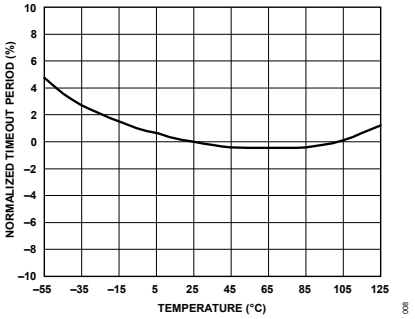

Figure 7. Normalized Timeout Period vs. Temperature

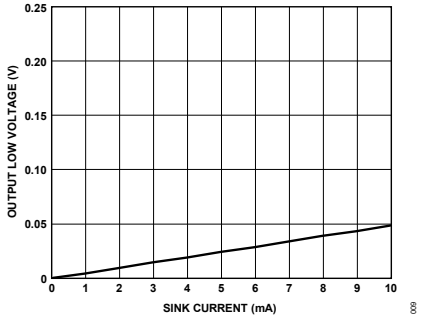

Figure 8. Output Low Voltage vs. Sink Current

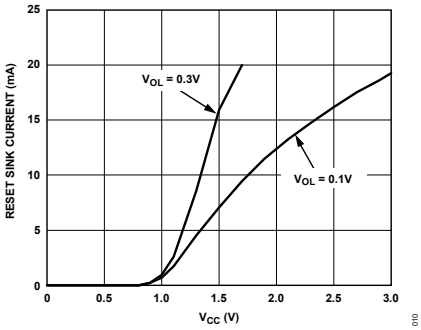

Figure 9. Reset Sink Capability vs. V_{CC}

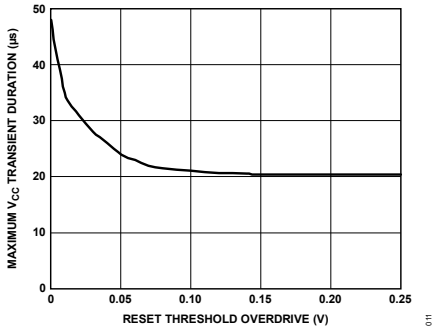

Figure 10. Maximum V_{CC} Transient Duration vs. Reset Threshold Overdrive

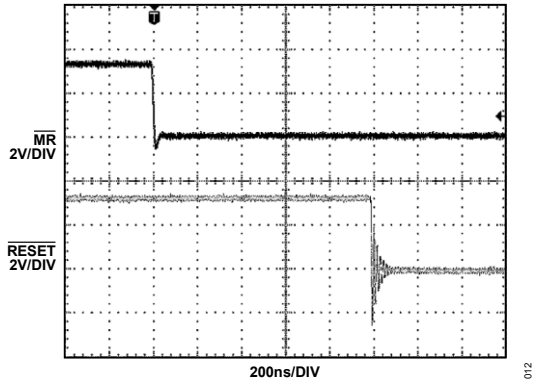

Figure 11. $\overline{MR}$ to $\overline{RESET}$ Output Delay

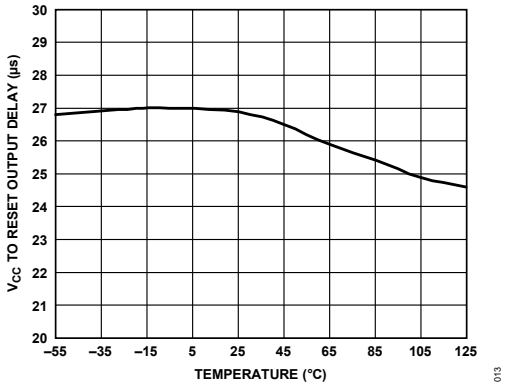

Figure 12. V_{CC} to Reset Output Delay vs. Temperature

THEORY OF OPERATION

The ADPL62092 is a supervisory circuit that monitors voltages from 1.1V to 5V using a factory-set reset threshold. It includes a watchdog timer and manual reset capability.

The ADPL62092 features an open-drain, active-low reset output. The reset output asserts and remains asserted for the reset timeout period after the monitored voltage exceeds its threshold.

Supply and Monitored Input (V_{CC})

The ADPL62092 operates with a V_{CC} supply voltage from 1.0V to 5.5V. V_{CC} has a rising threshold of $V_{TH} + V_{HYST}$ and a falling threshold of V_{TH}. When V_{CC} rises above $V_{TH} + V_{HYST}$ and $\overline{MR}$ is high, $\overline{RESET}$ goes high after the reset timeout period (t_{RP}). When V_{CC} falls below V_{TH}, $\overline{RESET}$ goes low after a fixed delay (t_{RD}). See *Figure 2*. It is recommended to place a 0.1µF decoupling capacitor as close as possible to the device between the V_{CC} pin and GND pin.

Manual Reset Input ($\overline{MR}$)

Many microprocessor (µP)-based products require manual reset capability to allow the operator, a test technician, or external logic circuit to initiate a reset. A logic-low on $\overline{MR}$ asserts reset. The reset remains asserted while $\overline{MR}$ is low, and for the reset active timeout period (t_{RP}) or delay (t_{ON}) after $\overline{MR}$ returns high. This input has an internal 50kΩ pull-up resistor, so it can be left unconnected if it is not used. $\overline{MR}$ can be driven with TTL or CMOS logic levels, or with open-drain/collector outputs. For manual operation, connect a normally open momentary switch from $\overline{MR}$ to GND; external debouncing circuitry is not required. If $\overline{MR}$ is driven from long cables or if the device is used in a noisy environment, connect a 0.1µF capacitor from $\overline{MR}$ to ground to provide additional noise immunity.

Watchdog Timer

The ADPL62092 features a watchdog timer that monitors µP activity through the WDI input. A rising or falling edge on WDI within the watchdog timeout period (t_{WDI}) indicates normal µP operation. The reset asserts for the reset timeout period if WDI remains high or low for longer than the watchdog timeout period. If it is not used, WDI can be left unconnected.

During normal operating mode, the supervisor asserts the reset output if the µP does not present WDI with a valid transition (high to low or low to high) within the watchdog timeout period. When the reset timeout period ends and the reset output deasserts, the watchdog timer continuous to monitor WDI. See *Figure 3*.

APPLICATIONS INFORMATION

Interfacing to µP with Bidirectional Reset Pins

Since $\overline{\text{RESET}}$ on the ADPL62092 is open drain, this device can interface easily with µPs that have bidirectional reset pins. Connecting the device's $\overline{\text{RESET}}$ output directly to the µP's $\overline{\text{RESET}}$ input with a single pull-up resistor allows either device to assert reset (*Figure 13*).

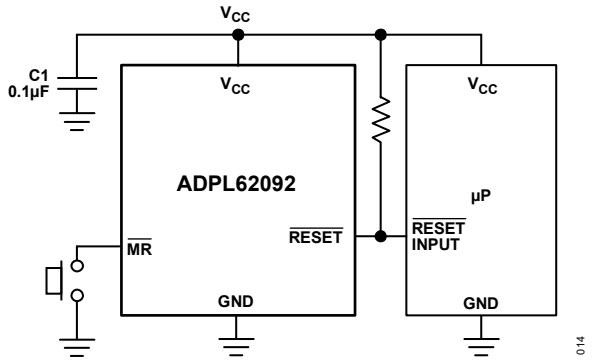

Figure 13.Interfacing to µP with Bidirectional Reset Pins

Negative-Going V_{cc} Transients

The ADPL62092 is relatively immune to short-duration, negative-going V_{CC} transient (glitches). *Figure 10* indicates the typical transient pulse width and amplitude required to trigger a reset. The reset threshold overdrive specifies how far the pulse falls below the actual reset threshold, and the maximum transient duration specifies the width of the pulse as it crosses the reset threshold. If a pulse occurs in the region above the curve, a reset triggers. If a pulse occurs in the region below the curve, a reset does not trigger. It is recommended to place a 0.1µF decoupling capacitor as close as possible to the device between the V_{CC} and GND pins.

ORDERING GUIDE

Table 5. Ordering Guide

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE	TOP MARK
ADPL62092UK16AKA+T	-40°C to +125°C	5 SOT23	AMKM
ADPL62092UK26OOA+T	-40°C to +125°C	5 SOT23	AMKN
ADPL62092UK28BGA+T	-40°C to +125°C	5 SOT23	AMKO
ADPL62092UK29OMA+T	-40°C to +125°C	5 SOT23	AMKP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape-and-reel package.

SELECTOR GUIDE

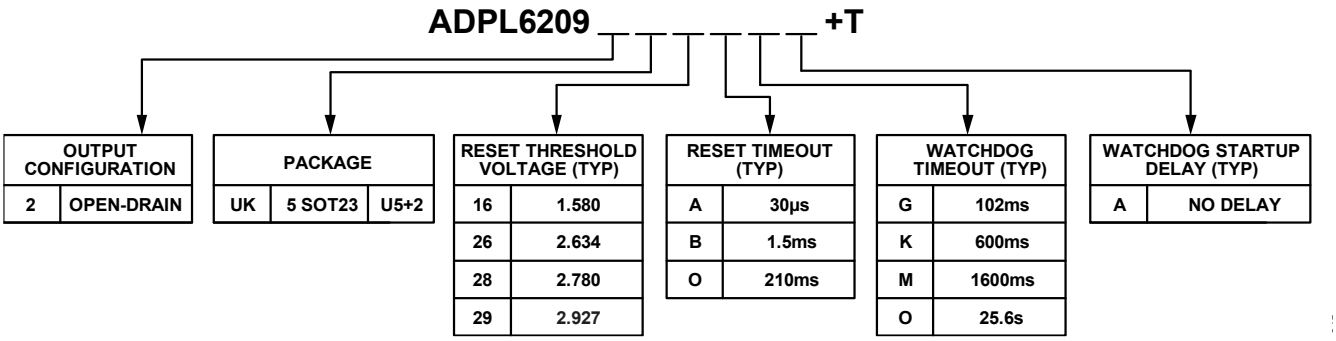

Figure 14. Selector Guide

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

ADPL62092UK28BGA+T ADPL62092UK29OMA+T ADPL62092UK26OOA+T ADPL62092UK16AKA+T