ADPL62083

Low-Power, Supervisory Circuit in 3-Lead SOT23

FEATURES

- Low Supply Current: 5µA (typ), 6.8µA (max) at 3.6V Over Temperature (+125°C)
- Factory-Set Reset Threshold Options from 1.02V to 4.8V in 50mV/100mV Increments
- Guaranteed Reset Valid to V_{CC} ≥ 1V
- Open-Drain Reset Output
- Power-Supply Transient Immunity
- -40°C to +125°C Operating Temperature Range

APPLICATIONS

- Portable/Battery-Powered and Industrial Equipment
- e-Readers/Tablets
- Smartphones

GENERAL DESCRIPTION

The ADPL62083 is a supervisory circuit that monitors voltages from 1.02V to 4.8V using a factory-set reset threshold.

The ADPL62083 features an open-drain, active-low reset output. The reset output asserts and remains asserted for the reset timeout period after the monitored voltage exceeds its threshold.

The ADPL62083 is available in 3-lead SOT23 package. It operates over the -40°C to +125°C temperature range.

SIMPLIFIED APPLICATION DIAGRAM

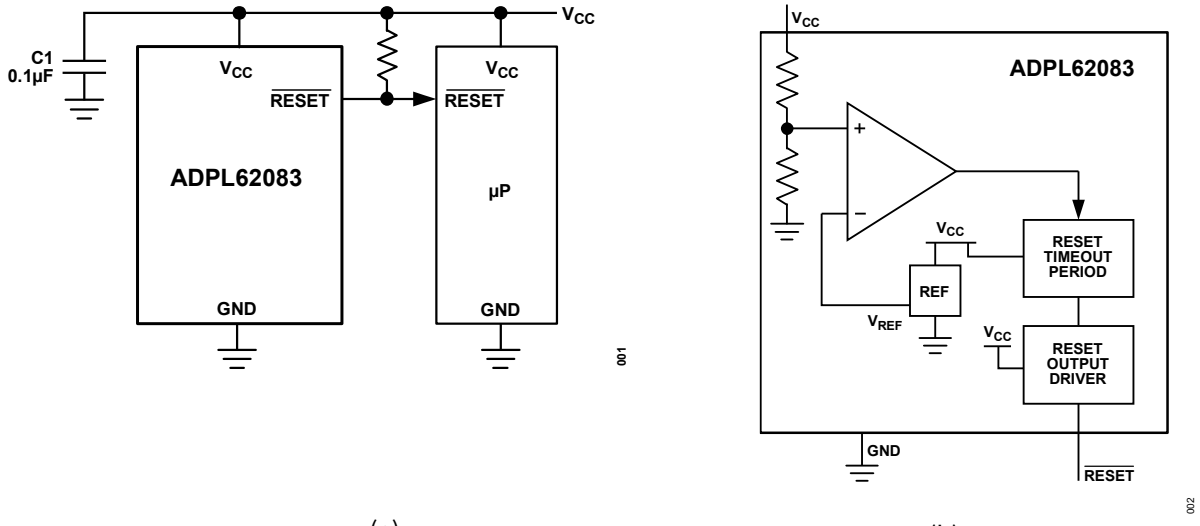

Figure 1. (a) Typical Application Circuit and (b) Functional Block Diagram

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REVISION HISTORY

11/2024 - Rev 0: Initial Release

SPECIFICATIONS

Table 1. Electrical Characteristics

(V_{CC} = 1V to 5.5V, C1 = 0.1µF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.[1])

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	[2]	1.0		5.5	V
V_{CC} Undervoltage Lockout	V_{CCUVLO}	[3]			0.9	V
Supply Current	I_{CC}	V_{CC} = 5.5V, no load		7	10	µA
		V_{CC} = 3.6V, $\overline{RESET}$ no load		5	6.8	µA
Threshold Voltage	V_{TH}	T_A = -40°C to +125°C	V_{TH} – 3.0%		V_{TH} + 3.0%	V
Reset Threshold Hysteresis	V_{HYST}	V_{CC} rising		5		$\%V_{TH}$
Reset Threshold Tempco	$\Delta V_{TH}/°C$			30		ppm/°C
$\overline{RESET}$ OUTPUT						
Output Low[3]	V_{OL}	$V_{CC} = V_{TH(MIN)}$, V_{TH} > 4.25V, I_{SINK} = 10mA			0.4	V
Output Low[3]	V_{OL}	$V_{CC} = V_{TH(MIN)}$, V_{TH} > 2.5V, I_{SINK} = 3.2mA			0.4	V
		$V_{CC} = V_{TH(MIN)}$, V_{TH} > 1.67V, I_{SINK} = 1mA			0.4	V
		$V_{CC} = V_{TH(MIN)}$, V_{TH} > 1V, I_{SINK} = 100µA			0.4	V
		V_{CC} ≥ 0.95V, I_{SINK} = 80µA			0.4	V
		V_{CC} > 0.9V, V_{CC} falling, I_{SINK} = 15µA			0.4	V
High-Impedance Input Leakage Current		Reset not asserted		0.2	1	µA
TIMING						
Reset Timeout Period	t_{RP}	V_{CC1} = 1.1V x V_{TH}	t_{RP} – 50%	t_{RP}	t_{RP} + 50%	ms
V_{CC} to Reset Delay	t_{RD}	V_{CC} falling at 10mV/µs from (V_{TH} + 100mV) to (V_{TH} – 100mV)		30		µs

1 Production testing done at T_A = +25°C only. Overtemperature limits are guaranteed by design and are not production tested.

2 Reset is guaranteed down to V_{CC} = 1V.

3 Guaranteed by design, not production tested.

Timing Diagrams

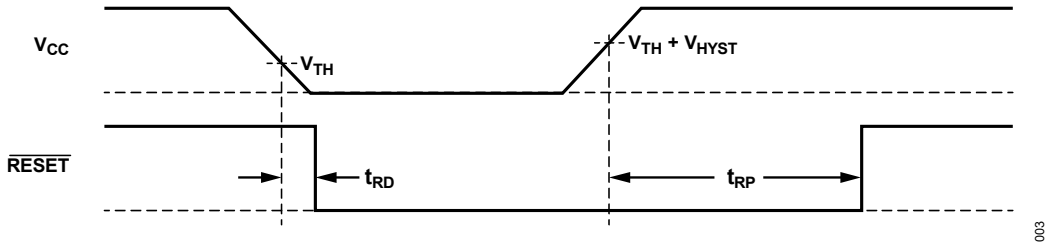

Figure 2. Reset Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
V_{CC}	-0.3V to +6V
$\overline{RESET}$	-0.3V to +6V
Input/Output Current (all pins)	20mA
Continuous Power Dissipation (T_A = +70°C) (derate 2.9mW/°C above T_A = +70°C)	235mW
Operating Temperature	-40°C to +125°C
Storage Temperature	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature	+300°C
Soldering Temperature	+260°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

PACKAGE INFORMATION

Table 3. Package Information

3 SOT23	
Package Code	U3+2
Outline Number	*21-0051*
Land Pattern Number	*90-0179*
Thermal Resistance, Multi-Layer Board:	
Junction-to-Ambient (θ_{JA})	340°C/W
Junction-to-Case (θ_{JC})	115°C/W

For the latest package outline information and land patterns (footprints), go to the *Package Index*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *Thermal Characterization of IC Packages*.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

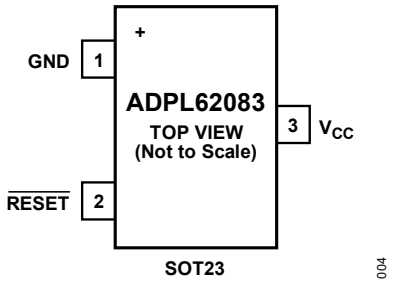

Figure 3. Pin Configuration

Pin Descriptions

Table 4. Pin Descriptions

PIN	NAME	DESCRIPTION
1	GND	Ground
2	RESET	Active-Low, Open-Drain Reset Output. RESET changes from high impedance to active low when VCC drops below the detector threshold (VTH). RESET remains low for the reset timeout period after VCC exceeds the reset threshold.
3	VCC	Supply Voltage and Input for the Reset Threshold Monitor. It is recommended to place a 0.1µF decoupling capacitor as close as possible to the device between the VCC and GND pins.

TYPICAL PERFORMANCE CHARACTERISTICS

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

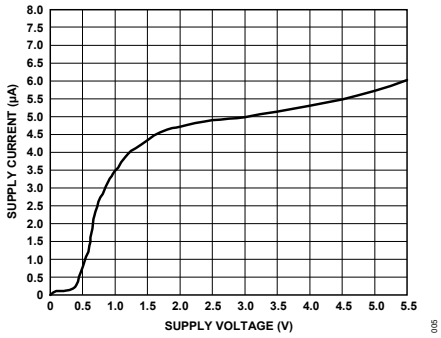

Figure 4. Supply Current vs. Supply Voltage

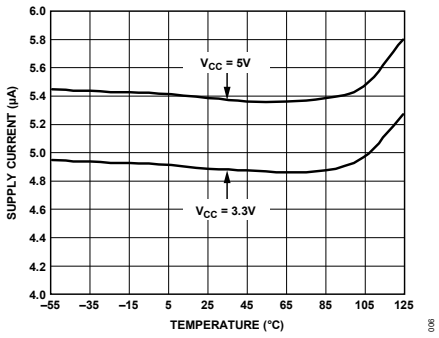

Figure 5. Supply Current vs. Temperature

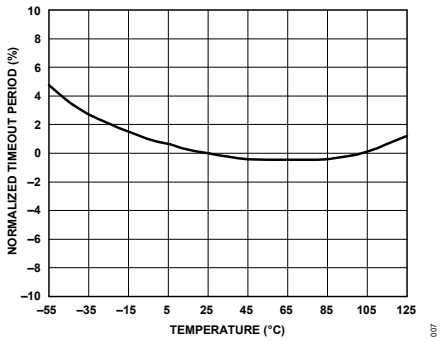

Figure 6. Normalized Timeout Period vs. Temperature

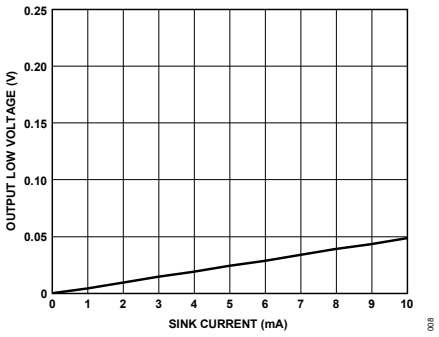

Figure 7. Output Low Voltage vs. Sink Current

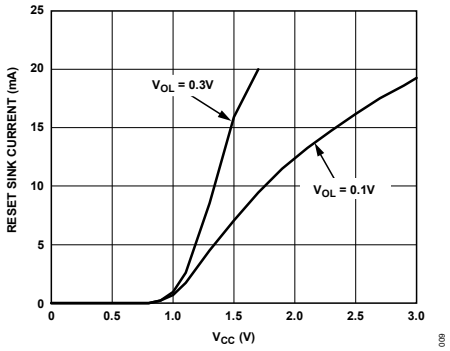

Figure 8. Reset Sink Capability vs. V_{CC}

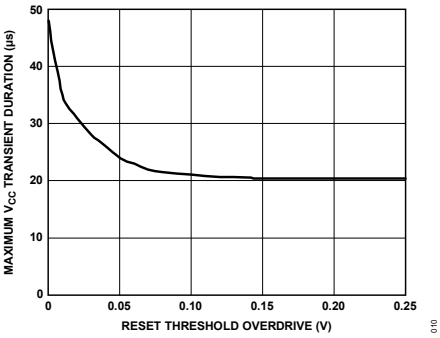

Figure 9. Maximum V_{CC} Transient Duration vs. Reset Threshold Overdrive

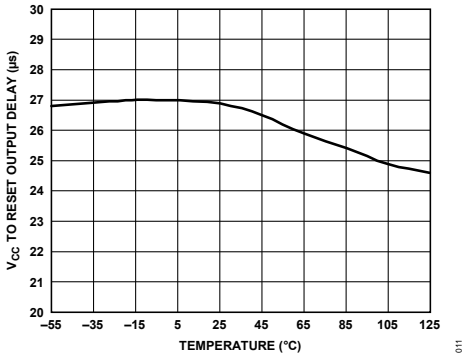

Figure 10. V_{CC} to Reset Output Delay vs. Temperature

THEORY OF OPERATION

The ADPL62083 monitors voltages from 1.1V to 5.0V. It features an open-drain, active-low reset output. The reset output asserts and remains asserted for the reset timeout period after the monitored voltage exceeds its threshold.

Supply and Monitored Input (V_{CC})

The ADPL62083 operates with a V_{CC} supply from 1.0V to 5.5V. V_{CC} has a rising threshold of $V_{TH} + V_{HYST}$ and a falling threshold of V_{TH}. When V_{CC} rises above $V_{TH} + V_{HYST}$, $\overline{RESET}$ goes high after the reset timeout period (t_{RP}). See *Figure 2*. When V_{CC} falls V_{TH}, $\overline{RESET}$ goes low after a fixed delay (t_{RD}). It is recommended to place a 0.1µF decoupling capacitor as close as possible to the device between the V_{CC} and GND pins.

APPLICATIONS INFORMATION

Interfacing to µP with Bidirectional Reset Pins

Since $\overline{RESET}$ on the ADPL62083 is open drain, it interfaces easily with microprocessors (µP) that have bidirectional reset pins. Connecting the device's $\overline{RESET}$ output directly to the µP's $\overline{RESET}$ input with a single pull-up resistor allows either device to assert a reset (*Figure 11*).

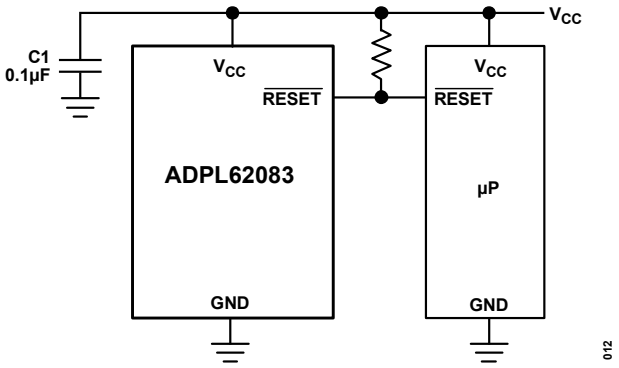

Figure 11. Interfacing to µP with Bidirectional Reset Pins

Negative-Going V_{CC} Transients ESD Protection

The ADPL62083 is relatively immune to short-duration, negative-going V_{CC} transients (glitches). *Figure 9* indicates the typical transient pulse width and amplitude required to trigger a reset. The reset threshold overdrive specifies how far the pulse falls below the actual reset threshold, and the maximum transient duration specifies the width of the pulse as it crosses the reset threshold. If a pulse occurs in the region above the curve, a reset triggers. If a pulse occurs in the region below the curve, a reset does not trigger. It is recommended to place a 0.1µF decoupling capacitor as close as possible to the device between the V_{CC} and GND pins.

ORDERING GUIDE

Table 5. Ordering Guide

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE	TOP MARK
ADPL62083UR16N+T	-40°C to +125°C	3 SOT23	FZYI
ADPL62083UR29H+T	-40°C to +125°C	3 SOT23	FZYJ
ADPL62083UR30O+T	-40°C to +125°C	3 SOT23	FZYM
ADPL62083UR31O+T	-40°C to +125°C	3 SOT23	FZYK
ADPL62083UR44Q+T	-40°C to +125°C	3 SOT23	FZYL

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

SELECTOR GUIDE

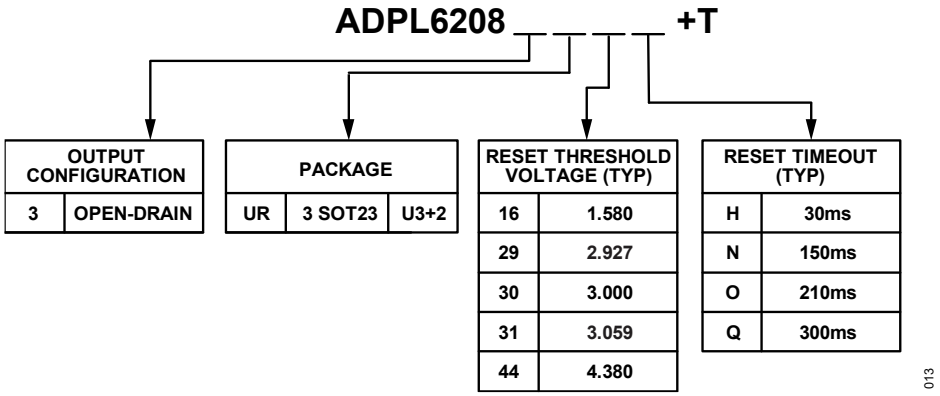

Figure 12. Selector Guide

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

ADPL62083UR44Q+T ADPL62083UR31O+T ADPL62083UR30O+T ADPL62083UR16N+T ADPL62083UR29H+T