1 GHz to 8 GHz, Low Noise Amplifier with Integrated Temperature Sensor and Enable and Disable Function

FEATURES

- Single positive supply: 5 V and I_{DQ} of 90 mA nominal
- RBIAS drain current adjustment pin
- Integrated temperature sensor
- Integrated enable and disable function
- Gain: 20 dB typical from 3 GHz to 4.5 GHz
- OIP3: 35.5 dBm typical from 1 GHz to 4.5 GHz
- Noise figure: 1 dB typical from 3 GHz to 6 GHz
- Extended operating temperature range: −55°C to +125°C
- RoHS-compliant, 3 mm × 3 mm, 16-lead LFCSP

APPLICATIONS

- Telecommunications
- Test instrumentation
- Military

GENERAL DESCRIPTION

The ADL8108 is a highly integrated, 1 GHz to 8 GHz, low noise amplifier (LNA). On-chip features include input and output AC coupling capacitors, an integrated bias inductor, an integrated temperature sensor, and an enable or disable pin (VPD).

Typical gain, output power 1 dB compression (OP1dB), third-order intercept point (OIP3), second-order intercept point (OIP2), and noise figure are 20 dB, 22 dBm, 35.5, 42 dBm, and 1 dB, respectively, from 3 GHz to 4.5 GHz. The nominal operating current (I_{DQ}), which can be adjusted, is 90 mA operating from a 5 V supply voltage (V_{DD}). Operation at 3 V is also supported.

The ADL8108 is fabricated on a pseudomorphic high electron mobility transistor (pHEMT) process. This device is housed in an RoHS-compliant, 3 mm x 3 mm, 16-lead LFCSP package and is specified for operation over an extended temperature range of −55°C to +125°C.

FUNCTIONAL BLOCK DIAGRAM

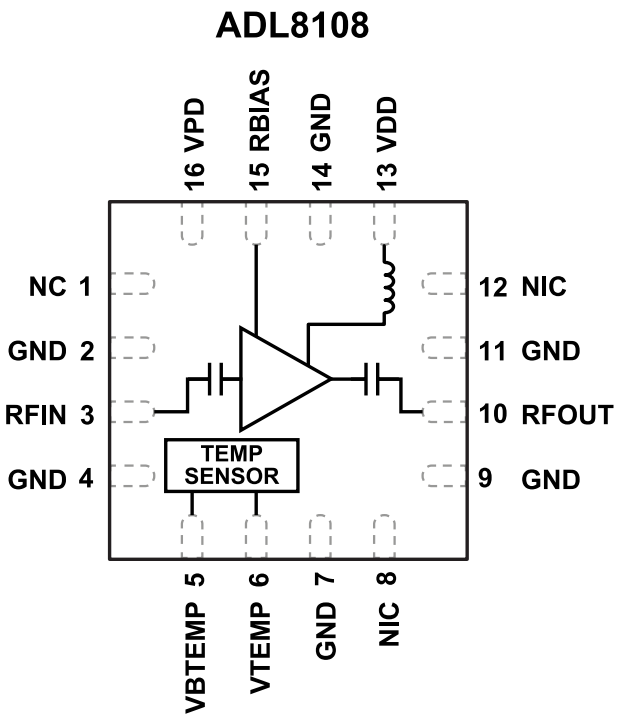

Figure 1. Functional Block Diagram

DOCUMENT FEEDBACK
TECHNICAL SUPPORT

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REVISION HISTORY

10/2024—Revision 0: Initial Version

SPECIFICATIONS

1 GHz TO 3 GHz FREQUENCY RANGE

V_{DD} = 5 V, I_{DQ} = 90 mA, bias resistance (R_{BIAS}) = 1270 Ω, VPD voltage (V_{PD}) = 0 V, and T_{CASE} = 25°C, unless otherwise noted.

Table 1. 1 GHz to 3 GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	1		3	GHz	
GAIN	20.5	22.5		dB	
Gain Variation over Temperature		0.006		dB/°C	
NOISE FIGURE		1.2		dB	
RETURN LOSS					
Input (S11)		11		dB	
Output (S22)		14.5		dB	
OUTPUT					
OP1dB	20	22		dBm	
Saturated Power (P_{SAT})		23		dBm	
OIP3		35.5		dBm	Measurement taken at output power (P_{OUT}) per tone = 8 dBm
OIP2		42		dBm	Measurement taken at P_{OUT} per tone = 8 dBm
POWER ADDED EFFICIENCY (PAE)		40.5		%	Measured at P_{SAT}

3 GHz TO 4.5 GHz FREQUENCY RANGE

V_{DD} = 5 V, I_{DQ} = 90 mA, R_{BIAS} = 1270 Ω, V_{PD} = 0 V, and T_{CASE} = 25°C, unless otherwise noted.

Table 2. 3 GHz to 4.5 GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	3		4.5	GHz	
GAIN	18	20		dB	
Gain Variation over Temperature		0.006		dB/°C	
NOISE FIGURE		1		dB	
RETURN LOSS					
Input		9.5		dB	
Output		13		dB	
OUTPUT					
OP1dB	20	22		dBm	
P_{SAT}		23		dBm	
OIP3		35.5		dBm	Measurement taken at P_{OUT} per tone = 8 dBm
OIP2		42		dBm	Measurement taken at P_{OUT} per tone = 8 dBm
PAE		37		%	Measured at P_{SAT}

SPECIFICATIONS

4.5 GHz TO 6 GHz FREQUENCY RANGE

V_{DD} = 5 V, I_{DQ} = 90 mA, R_{BIAS} = 1270 Ω, V_{PD} = 0 V, and T_{CASE} = 25°C, unless otherwise noted.

Table 3. 4.5 GHz to 6 GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	4.5		6	GHz	
GAIN	16	18.5		dB	
Gain Variation over Temperature		0.007		dB/°C	
NOISE FIGURE		1		dB	
RETURN LOSS					
Input		9.5		dB	
Output		13		dB	
OUTPUT					
OP1dB	18.5	21		dBm	
P_{SAT}		23		dBm	
OIP3		35		dBm	Measurement taken at P_{OUT} per tone = 8 dBm
OIP2		48		dBm	Measurement taken at P_{OUT} per tone = 8 dBm
PAE		33.5		%	Measured at P_{SAT}

6 GHz TO 8 GHz FREQUENCY RANGE

V_{DD} = 5 V, I_{DQ} = 90 mA, R_{BIAS} = 1270 Ω, V_{PD} = 0 V, and T_{CASE} = 25°C, unless otherwise noted.

Table 4. 6 GHz to 8 GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	6		8	GHz	
GAIN		16.5		dB	
Gain Variation over Temperature		0.008		dB/°C	
NOISE FIGURE		1.5		dB	
RETURN LOSS					
Input		10.5		dB	
Output		14.5		dB	
OUTPUT					
OP1dB		19.5		dBm	
P_{SAT}		21.5		dBm	
OIP3		34		dBm	Measurement taken at P_{OUT} per tone = 8 dBm
OIP2		50		dBm	Measurement taken at P_{OUT} per tone = 8 dBm
PAE		26.5		%	Measured at P_{SAT}

SPECIFICATIONS

DC SPECIFICATIONS

Table 5. DC Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT					
I_{DQ}		90		mA	V_{PD} = 0V
		10		mA	V_{PD} = 5 V
Amplifier Current (I_{DQ_AMP})		86.9		mA	
RBIAS Current (I_{RBIAS})		3.1		mA	
SUPPLY VOLTAGE					
V_{DD}	3	5	5.5	V	

Table 6. Logic Control (V_{PD})

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL CONTROL INPUT					
Low, Amplifier On State	0		0.3	V	
High, Amplifier Off State	1.9		V_{DD}	V	
VPD Input Current (I_{PD})		1		mA	V_{PD} = 5 V
SWITCHING TIME					
Amplifier On State Time		15		ns	50% of the V_{PD} falling edge to the output envelope at 90%
Amplifier Off State Time		10		ns	50% of the V_{PD} rising edge to the output envelope at 10%

Table 7. Temperature Sensor

Parameter	Min	Typ	Max	Unit
VTEMP Voltage (V_{TEMP}) Output Voltage (V_{OUT}), T_{CASE} = 25°C		2.45		V
V_{TEMP} Temperature Coefficient, T_{CASE} = −55°C to +125°C		3.4		mV/°C
VBTEMP Voltage (V_{BTEMP}) Input Current		2		mA

ABSOLUTE MAXIMUM RATINGS

Table 8. Absolute Maximum Ratings

Parameter	Rating
V_{DD}	7 V
V_{PD}	V_{DD}
RF Input Power Survivability (RFIN)	27 dBm
Continuous Power Dissipation (P_{DISS}), T_{CASE} = 85°C (Derate 20.8 mW/°C Above 85°C)	1.88 W
Temperature	
Storage Range	−65°C to +150°C
Operating Range	−55°C to +125°C
Nominal Channel (T_{CASE} = 85°C, V_{DD} = 5 V, I_{DQ} = 90 mA, Input Power (P_{IN}) = Off)	107°C
Maximum Channel	175°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Overall Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JC} is the channel to case thermal resistance.

Table 9. Thermal Resistance[1]

Package Type	θ_{JC}	Unit
CP-16-35		
Quiescent, T_{CASE} = 25°C	40	°C/W
Worst Case[2], T_{CASE} = 85°C	48	°C/W

1 Thermal resistance varies with operating conditions.

2 Across all specified operating conditions

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADL8108

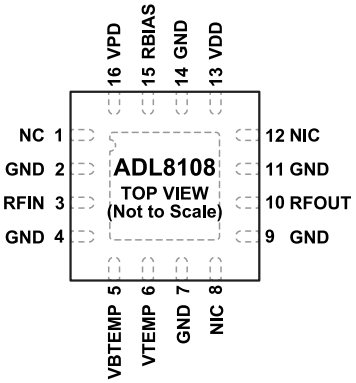
Table 10. ADL8108, 16-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±250	1A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NO CONNECT. THE NC PIN CAN BE SOLDERED TO A PCB PAD, BUT THIS PIN MUST BE LEFT OPEN.
2. NIC = NO INTERNAL CONNECTION. THE NIC PINS ARE NOT CONNECTED INTERNALLY. FOR NORMAL OPERATION, CONNECT THE NIC PINS TO GROUND.
3. GROUND PADDLE. CONNECT THE GROUD PADDLE TO A GROUND PLANE WHICH HAS A LOW ELECTRICAL AND THERMAL IMPEDANCE.

Figure 2. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	No Connect. The NC pin can be soldered to a PCB pad, but this pin must be left open.
2, 4, 7, 9, 11, 14	GND	Ground. Connect the GND pins to a ground plane that has low electrical and thermal impedance. See Figure 3 for the interface schematic.
3	RFIN	RF Input. RFIN is AC-coupled and matched to 50 Ω. See Figure 4 for the interface schematic.
5	VBTEMP	Bias Voltage for the Temperature Sensor. See Figure 5 for the interface schematic.
6	VTEMP	Temperature Sensor Output Voltage. See Figure 5 for the interface schematic.
8, 12	NIC	No Internal Connection. The NIC pins are not connected internally. For normal operation, connect the NIC pins to ground.
10	RFOUT	RF Output. The RFOUT pin is AC-coupled and matched to 50 Ω. See Figure 6 for the interface schematic.
13	VDD	Drain Bias. Connect the VDD pin to the supply voltage. See Figure 6 for the interface schematic.
15	RBIAS	Bias Setting Resistor. Connect a resistor between RBIAS and VDD to set the quiescent drain current. See the typical application circuit (see Figure 96) and Table 12 to Table 15 for more details. See Figure 7 for the interface schematic.
16	VPD	Power-Down Control. To enable the ADL8108, connect the VPD pin to the ground. To disable the ADL8108, connect the VPD pin to the VDD pin. See Figure 8 for the interface schematic.
	GROUND PADDLE	Ground Paddle. Connect the ground paddle to a ground plane which has a low electrical and thermal impedance.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

Figure 3. GND Interface Schematic

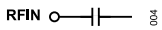


Figure 4. RFIN Interface Schematic

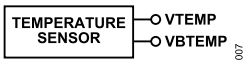


Figure 5. VTEMP and VBTEMP Interface Schematic

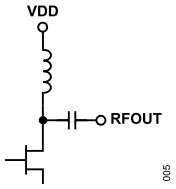


Figure 6. RFOUT and VDD Interface Schematic

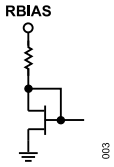


Figure 7. RBIAS Interface Schematic

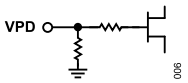


Figure 8. VPD Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

AMPLIFIER ON STATE (V_{PD} = 0 V)

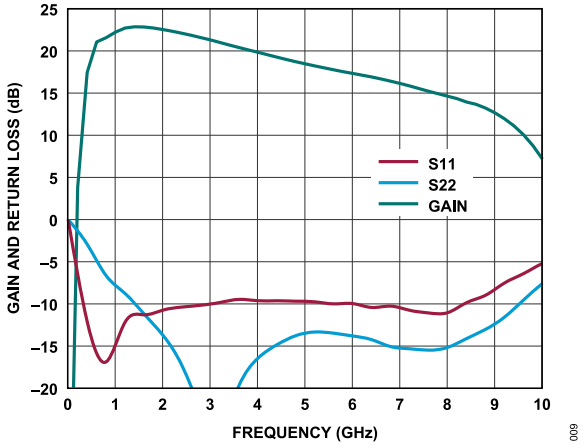


Figure 9. Broadband Gain and Return Loss vs. Frequency, 10 MHz to 10 GHz, V_{DD} = 5 V, I_{DQ} = 90 mA

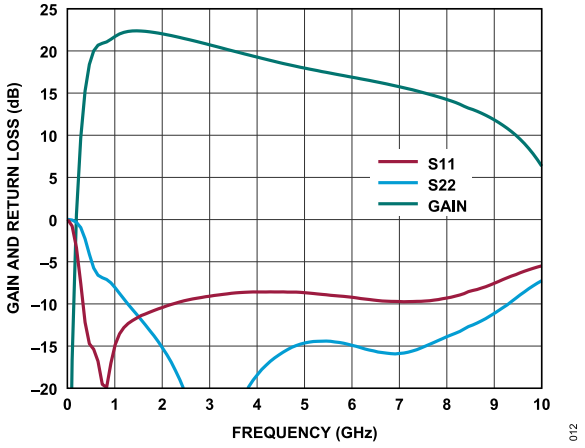


Figure 12. Broadband Gain and Return Loss vs. Frequency, 10 MHz to 10 GHz, V_{DD} = 3 V, I_{DQ} = 60 mA

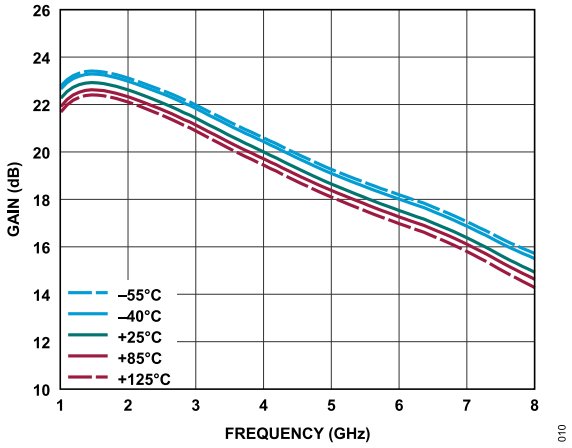


Figure 10. Gain vs. Frequency for Various Temperatures, 1 GHz to 8 GHz, V_{DD} = 5 V, I_{DQ} = 90 mA

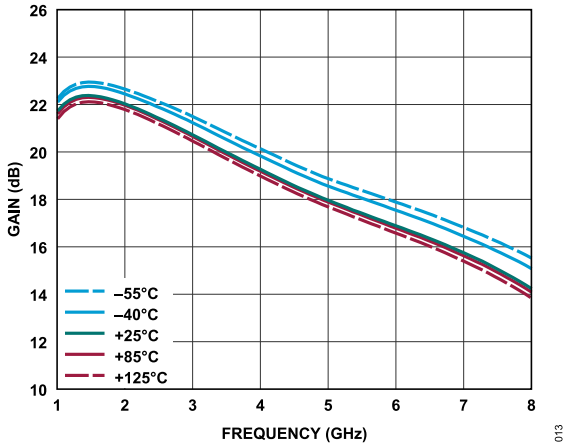


Figure 13. Gain vs. Frequency for Various Temperatures, 1 GHz to 8 GHz, V_{DD} = 3 V, I_{DQ} = 60 mA

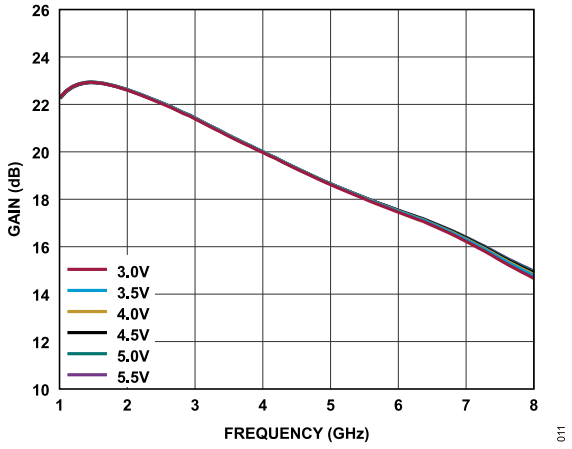


Figure 11. Gain vs. Frequency for Various Supply Voltages, 1 GHz to 8 GHz, I_{DQ} = 90 mA

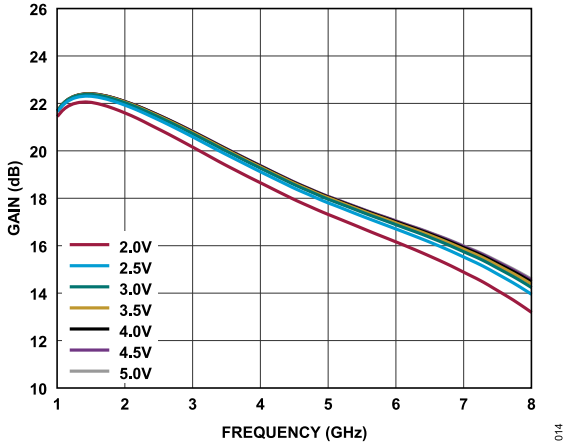


Figure 14. Gain vs. Frequency for Various Supply Voltages, 1 GHz to 8 GHz, I_{DQ} = 60 mA

TYPICAL PERFORMANCE CHARACTERISTICS

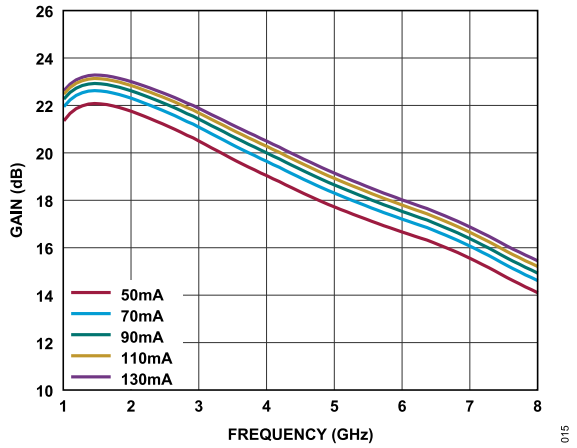


Figure 15. Gain vs. Frequency for Various I_{DQ} Values, 1 GHz to 8 GHz, V_{DD} = 5 V

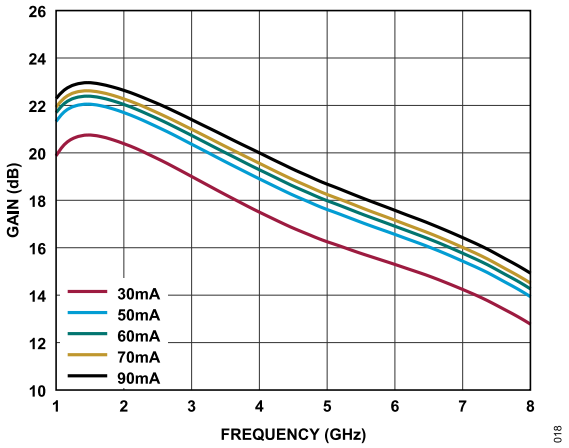


Figure 18. Gain vs. Frequency for Various I_{DQ} Values, 1 GHz to 8 GHz, V_{DD} = 3 V

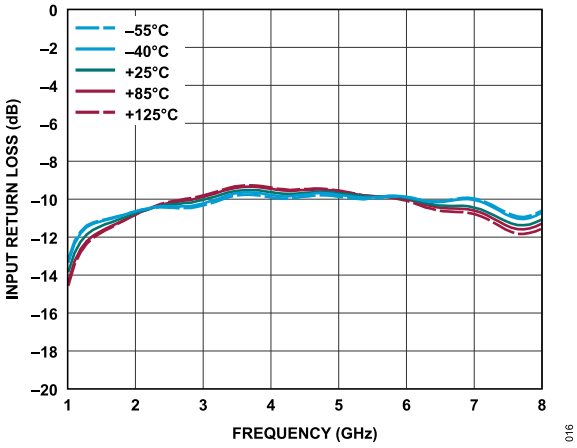


Figure 16. Input Return Loss vs. Frequency for Various Temperatures, 1 GHz to 8 GHz, V_{DD} = 5 V, I_{DQ} = 90 mA, R_{BIAS} = 1270 Ω

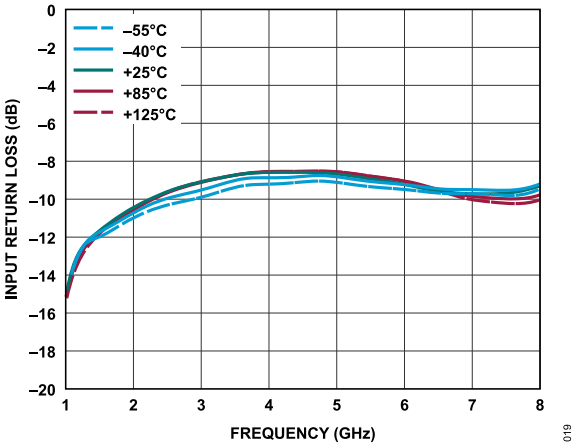


Figure 19. Input Return Loss vs. Frequency for Various Temperatures, 1 GHz to 8 GHz, V_{DD} = 3 V, I_{DQ} = 60 mA, R_{BIAS} = 698 Ω

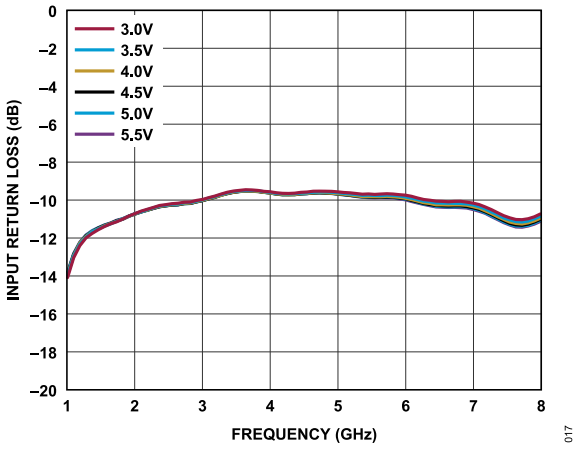


Figure 17. Input Return Loss vs. Frequency for Various Supply Voltages, 1 GHz to 8 GHz, I_{DQ} = 90 mA

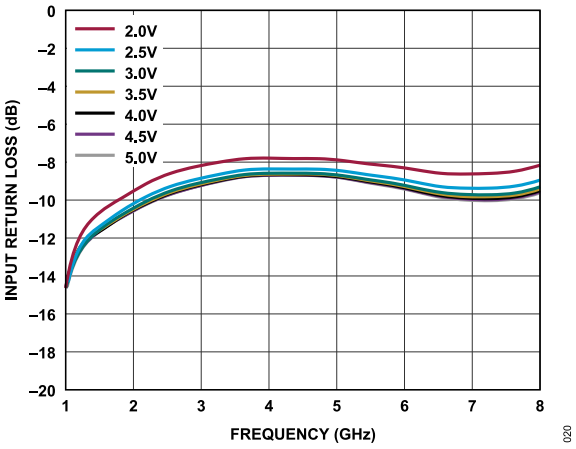


Figure 20. Input Return Loss vs. Frequency for Various Supply Voltages, 1 GHz to 8 GHz, I_{DQ} = 60 mA

TYPICAL PERFORMANCE CHARACTERISTICS

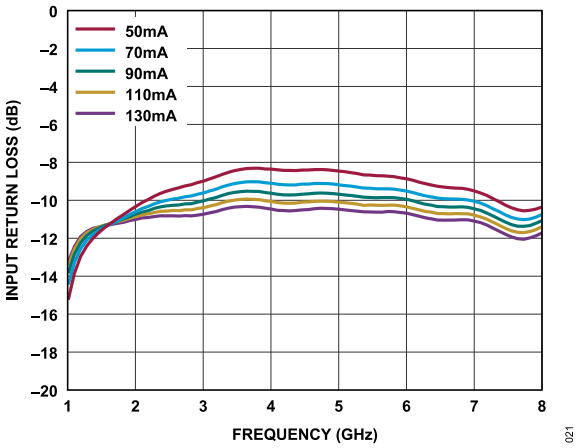


Figure 21. Input Return Loss vs. Frequency for Various I_{DQ} Values, 1 GHz to 8 GHz, V_{DD} = 5 V

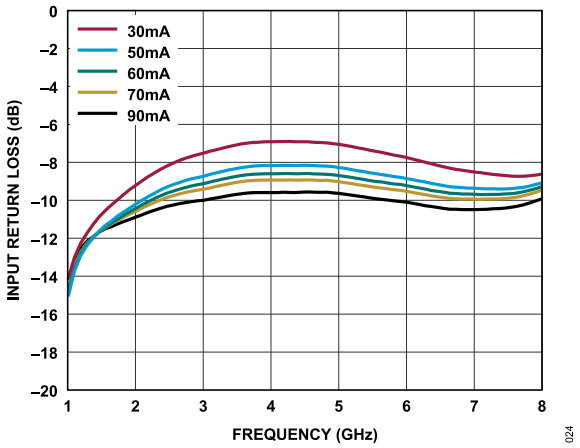


Figure 24. Input Return Loss vs. Frequency for Various I_{DQ} Values, 1 GHz to 8 GHz, V_{DD} = 3 V

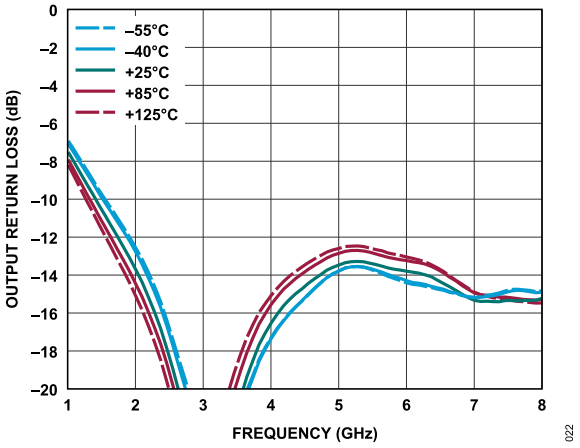


Figure 22. Output Return Loss vs. Frequency for Various Temperatures, 1 GHz to 8 GHz, V_{DD} = 5 V, I_{DQ} = 90 mA, R_{BIAS} = 1270 Ω

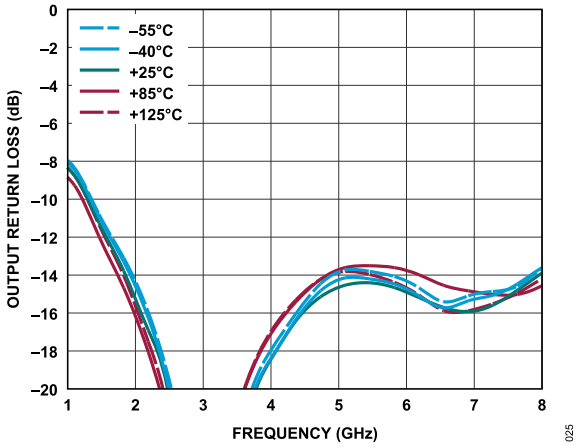


Figure 25. Output Return Loss vs. Frequency for Various Temperatures, 1 GHz to 8 GHz, V_{DD} = 3 V, I_{DQ} = 60 mA, R_{BIAS} = 698 Ω

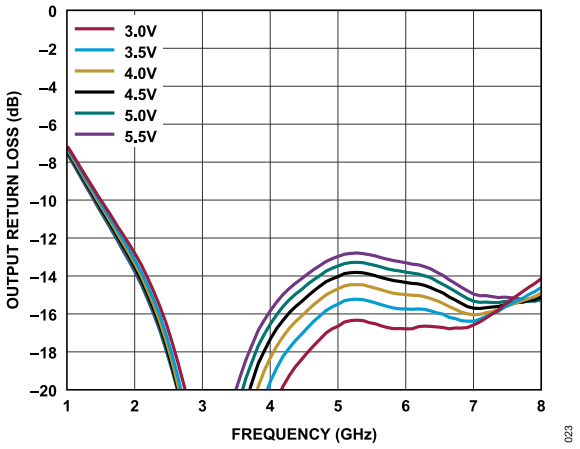


Figure 23. Output Return Loss vs Frequency for Various Supply Voltages, 1 GHz to 8 GHz, I_{DQ} = 90 mA

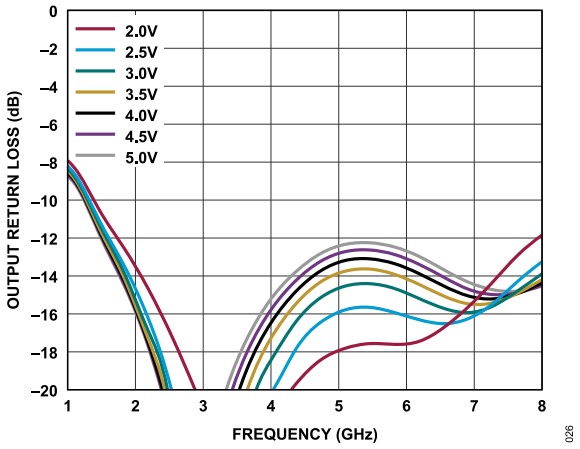


Figure 26. Output Return Loss vs. Frequency for Various Supply Voltages, 1 GHz to 8 GHz, I_{DQ} = 60 mA

TYPICAL PERFORMANCE CHARACTERISTICS

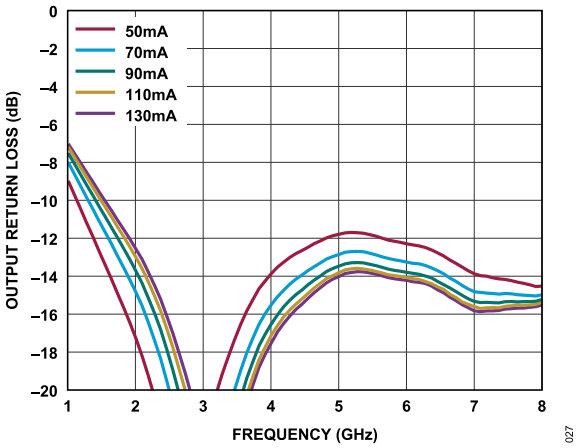


Figure 27. Output Return Loss vs. Frequency for Various I_{DQ} Values, 1 GHz to 8 GHz, V_{DD} = 5 V

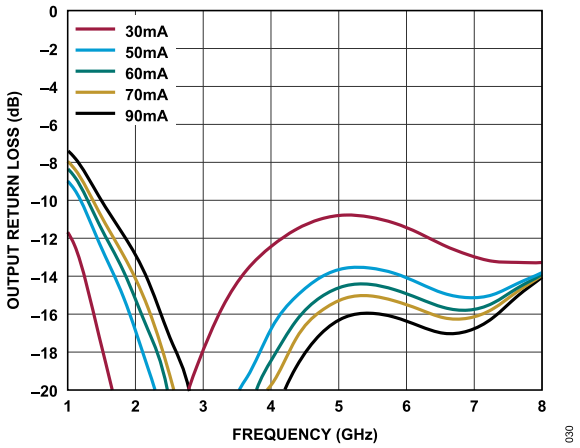


Figure 30. Output Return Loss vs. Frequency for Various I_{DQ} Values, 1 GHz to 8 GHz, and V_{DD} = 3 V

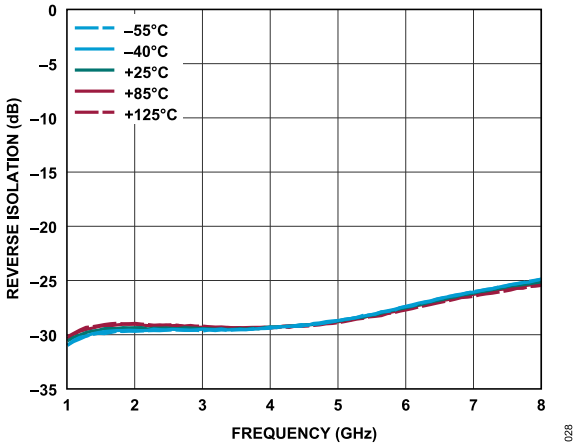


Figure 28. Reverse Isolation vs. Frequency for Various Temperatures, 1 GHz to 8 GHz, V_{DD} = 5 V, I_{DQ} = 90 mA, R_{BIAS} = 1270 Ω

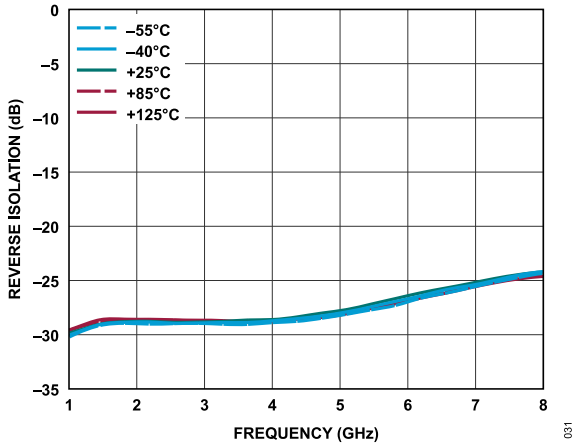


Figure 31. Reverse Isolation vs. Frequency for Various Temperatures, 1 GHz to 8 GHz, V_{DD} = 3 V, I_{DQ} = 60 mA, R_{BIAS} = 698 Ω

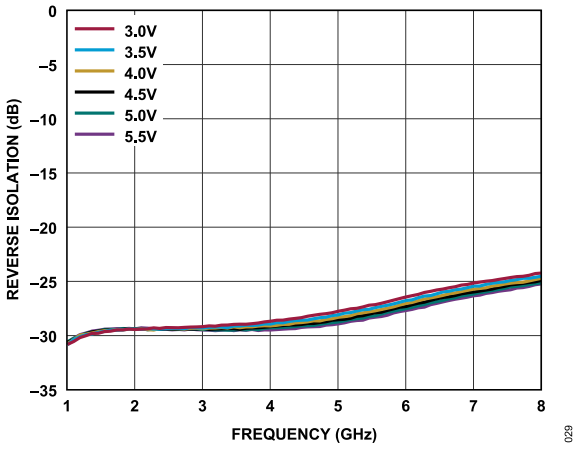


Figure 29. Reverse Isolation vs. Frequency for Various Supply Voltages, 1 GHz to 8 GHz, I_{DQ} = 90 mA

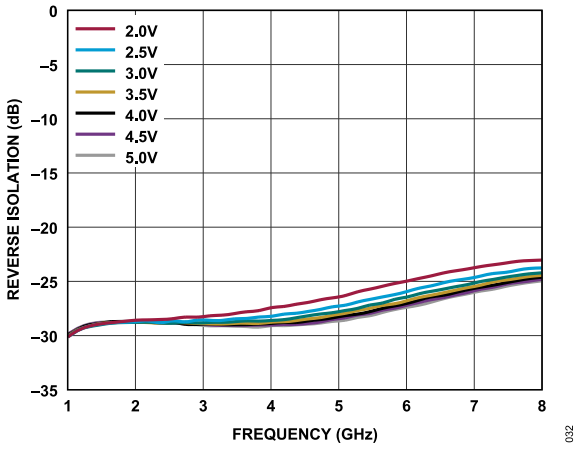


Figure 32. Reverse Isolation vs. Frequency for Various Supply Voltages, 1 GHz to 8 GHz, I_{DQ} = 60 mA

TYPICAL PERFORMANCE CHARACTERISTICS

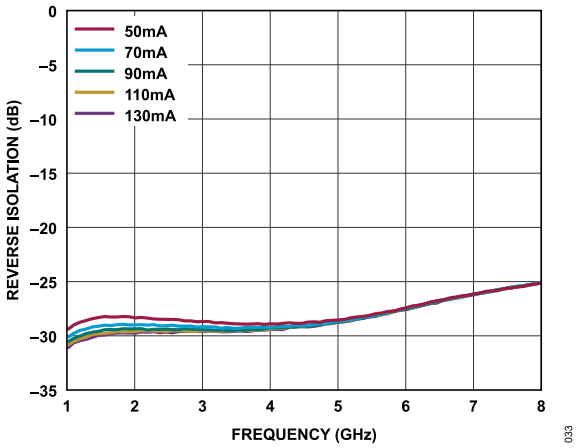


Figure 33. Reverse Isolation vs. Frequency for Various I_{DQ} Values, 1 GHz to 8 GHz, V_{DD} = 5 V

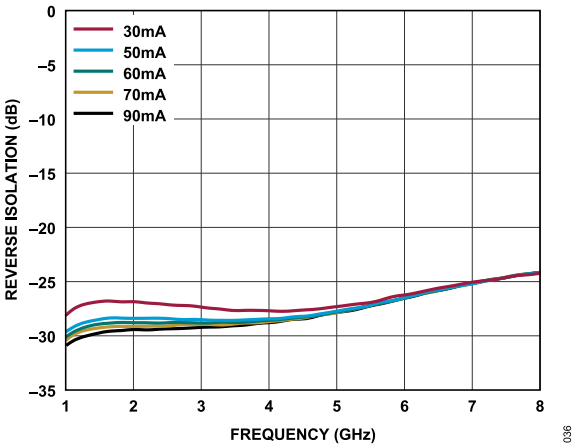


Figure 36. Reverse Isolation vs. Frequency for Various I_{DQ} Values, 1 GHz to 8 GHz, V_{DD} = 3 V

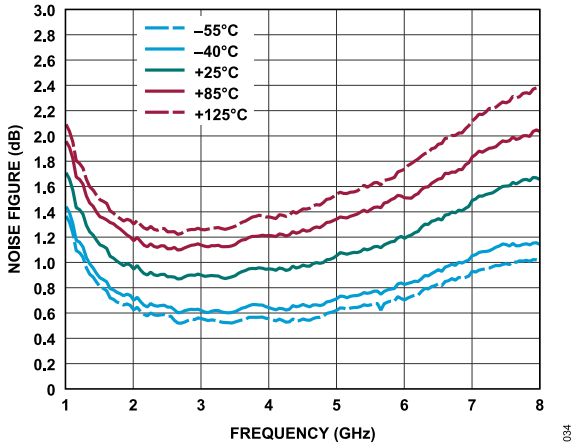


Figure 34. Noise Figure vs. Frequency for Various Temperatures, 1 GHz to 8 GHz, V_{DD} = 5 V, I_{DQ} = 90 mA, R_{BIAS} = 1270 Ω

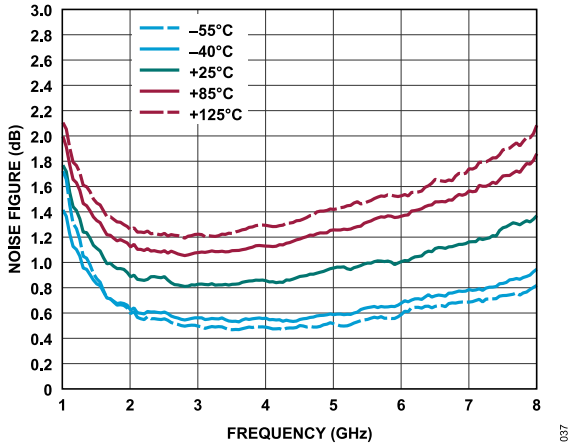


Figure 37. Noise Figure vs. Frequency for Various Temperatures, 1 GHz to 8 GHz, V_{DD} = 3 V, I_{DQ} = 60 mA, R_{BIAS} = 698 Ω

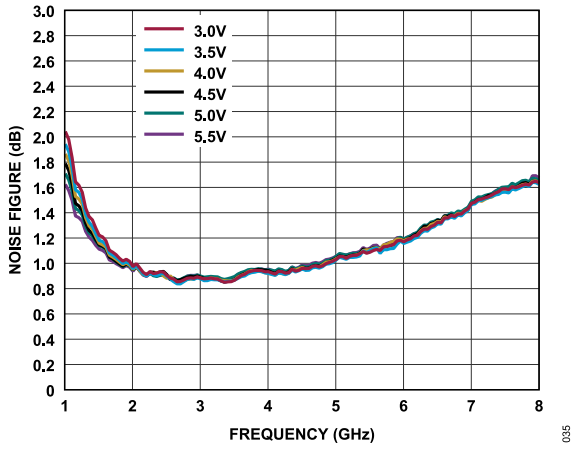


Figure 35. Noise Figure vs. Frequency for Various Supply Voltages, 1 GHz to 8 GHz, I_{DQ} = 90 mA

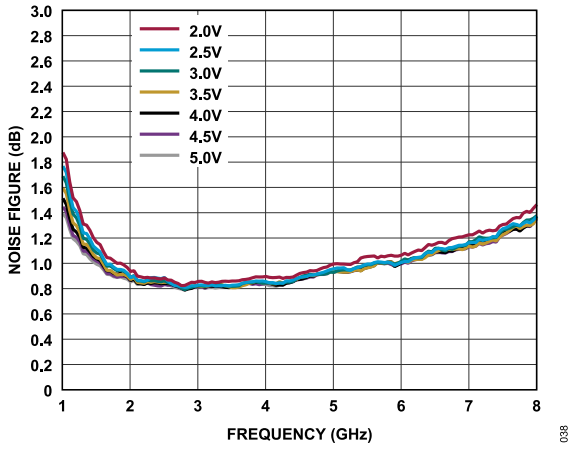


Figure 38. Noise Figure vs. Frequency for Various Supply Voltages, 1 GHz to 8 GHz, I_{DQ} = 60 mA

TYPICAL PERFORMANCE CHARACTERISTICS

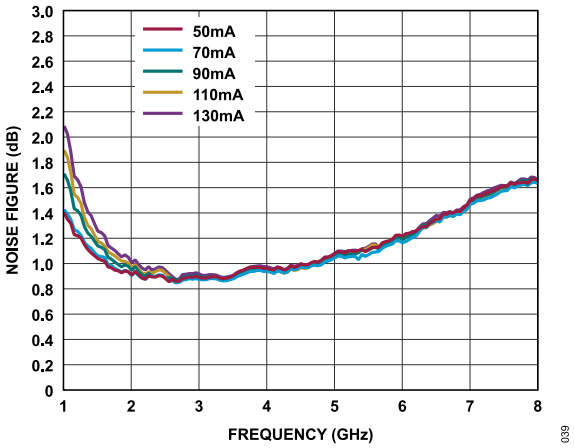


Figure 39. Noise Figure vs. Frequency for Various I_{DQ} Values, 1 GHz to 8 GHz, V_{DD} = 5 V

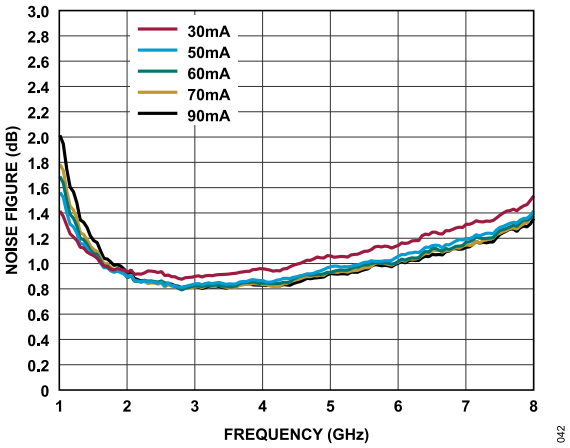


Figure 42. Noise Figure vs. Frequency for Various I_{DQ} Values, 1 GHz to 8 GHz, V_{DD} = 3 V

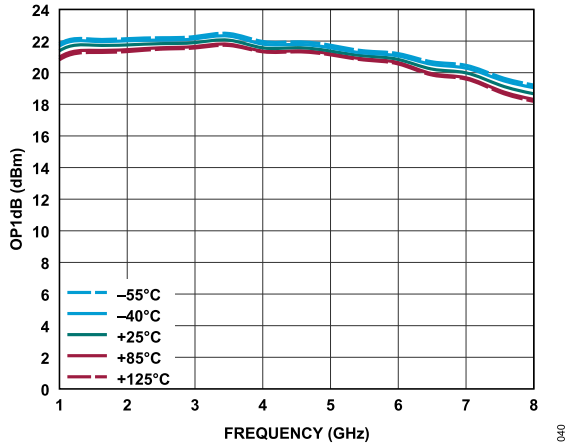


Figure 40. OP1dB vs. Frequency for Various Temperatures, 1 GHz to 8 GHz, V_{DD} = 5 V, I_{DQ} = 90 mA, R_{BIAS} = 1270 Ω

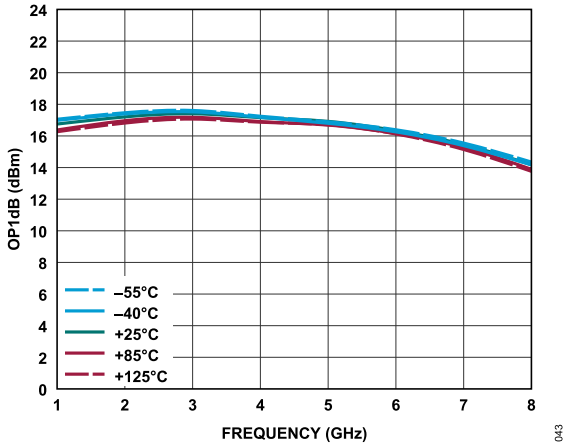


Figure 43. OP1dB vs. Frequency for Various Temperatures, 1 GHz to 8 GHz, V_{DD} = 3 V, I_{DQ} = 60 mA, R_{BIAS} = 698 Ω

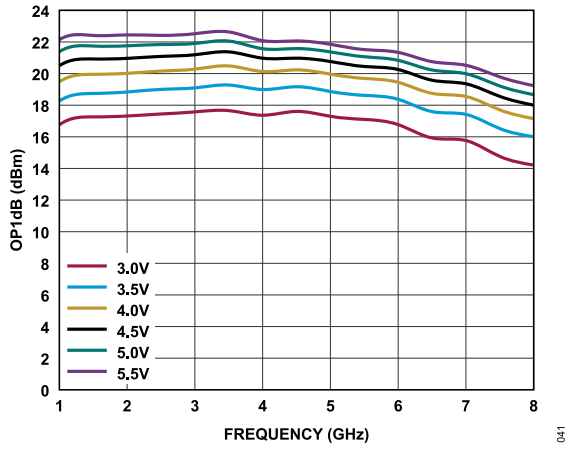


Figure 41. OP1dB vs. Frequency for Various Supply Voltages, 1 GHz to 8 GHz, I_{DQ} = 90 mA

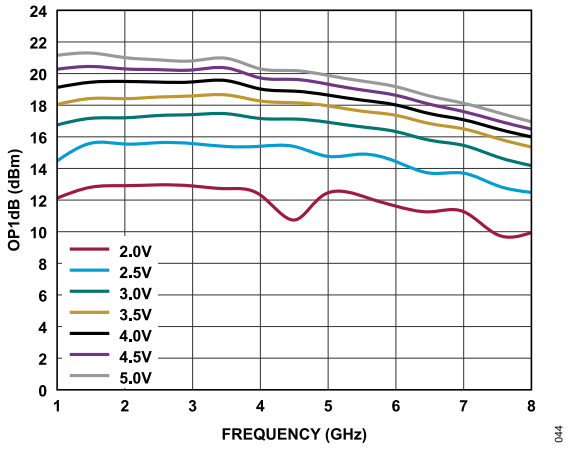


Figure 44. OP1dB vs. Frequency for Various Supply Voltages, 1 GHz to 8 GHz, I_{DQ} = 60 mA

TYPICAL PERFORMANCE CHARACTERISTICS

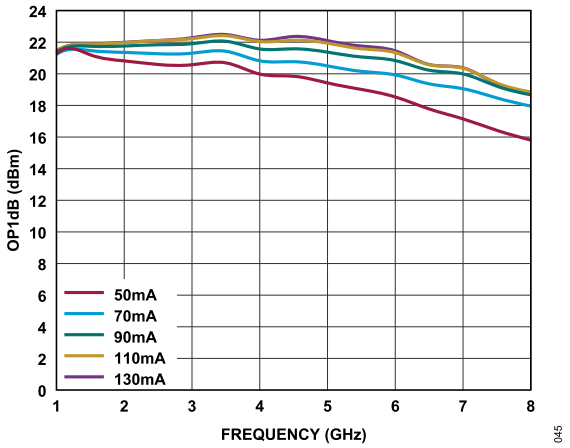


Figure 45. OP1dB vs. Frequency for Various I_{DQ} Values, 1 GHz to 8 GHz, V_{DD} = 5 V

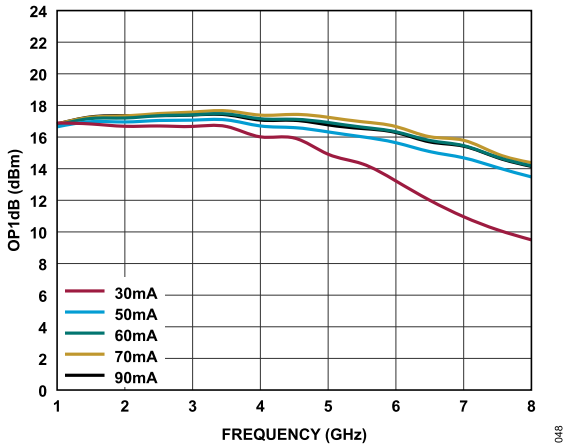


Figure 48. OP1dB vs. Frequency for Various I_{DQ} Values, 1 GHz to 8 GHz, V_{DD} = 3 V

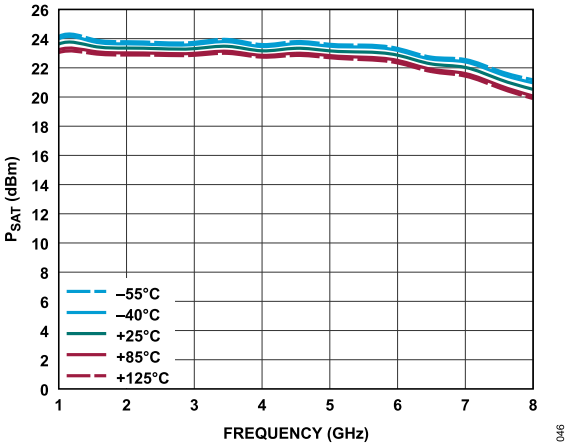


Figure 46. P_{SAT} vs. Frequency for Various Temperatures, 1 GHz to 8 GHz, V_{DD} = 5 V, I_{DQ} = 90 mA

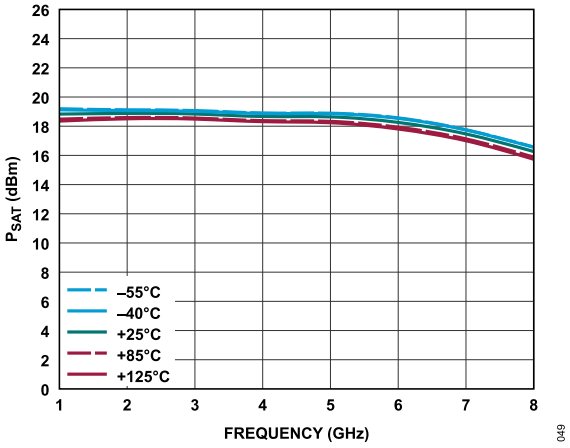


Figure 49. P_{SAT} vs. Frequency for Various Temperatures, 1 GHz to 8 GHz, V_{DD} = 3 V, I_{DQ} = 60 mA, R_{BIAS} = 698 Ω

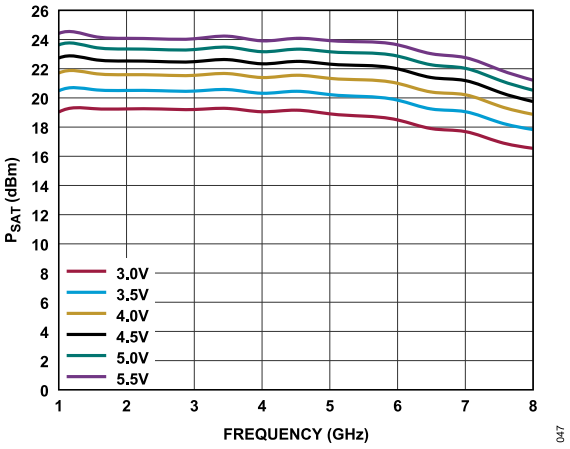


Figure 47. P_{SAT} vs. Frequency for Various Supply Voltages, 1 GHz to 8 GHz, I_{DQ} = 90 mA

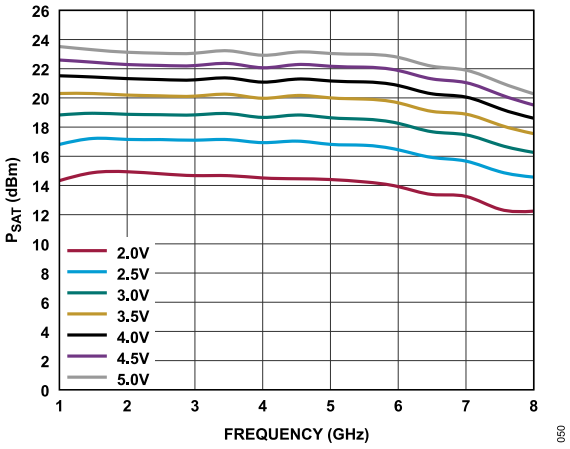


Figure 50. P_{SAT} vs. Frequency for Various Supply Voltages, 1 GHz to 8 GHz, I_{DQ} = 60 mA

TYPICAL PERFORMANCE CHARACTERISTICS

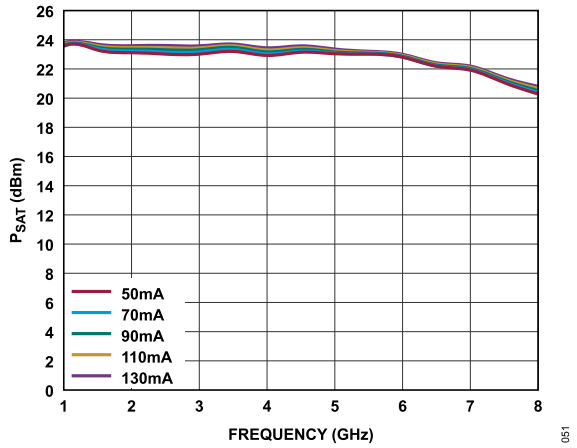


Figure 51. P_{SAT} vs. Frequency for Various I_{DQ} Values, 1 GHz to 8 GHz, V_{DD} = 5 V

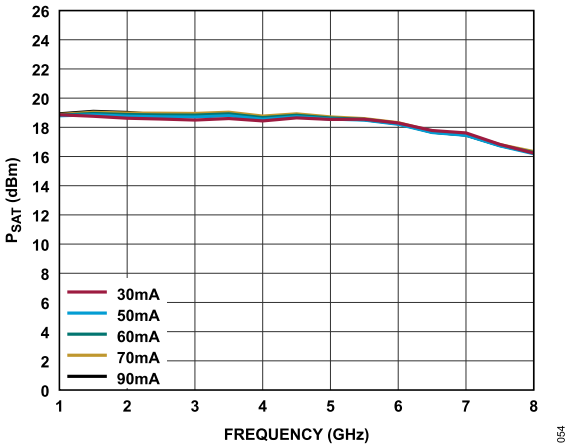


Figure 54. P_{SAT} vs. Frequency for Various I_{DQ} Values, 1 GHz to 8 GHz, V_{DD} = 3 V

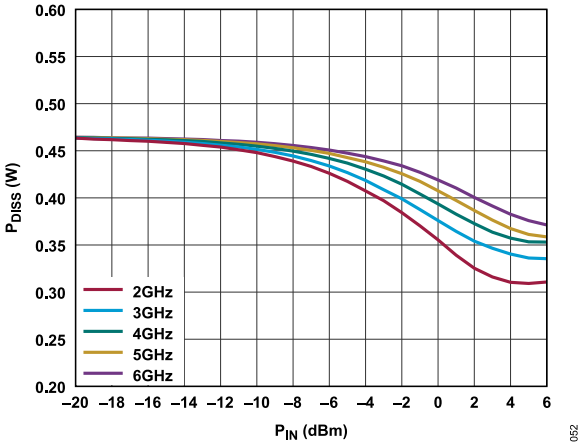


Figure 52. P_{DISS} vs. P_{IN} at T_{CASE} = 85°C, V_{DD} = 5 V, R_{BIAS} = 1270 Ω

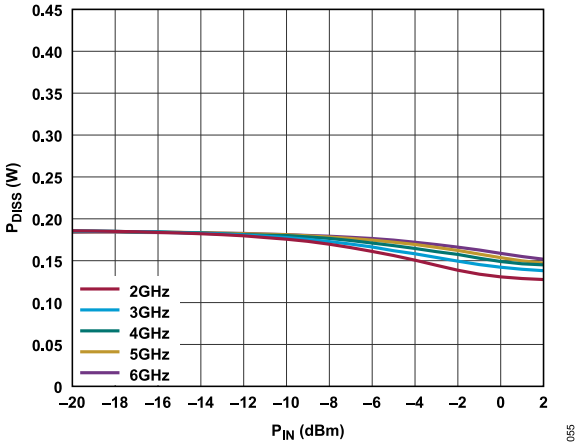


Figure 55. P_{DISS} vs. P_{IN} at T_{CASE} = 85°C, V_{DD} = 3 V, R_{BIAS} = 698 Ω

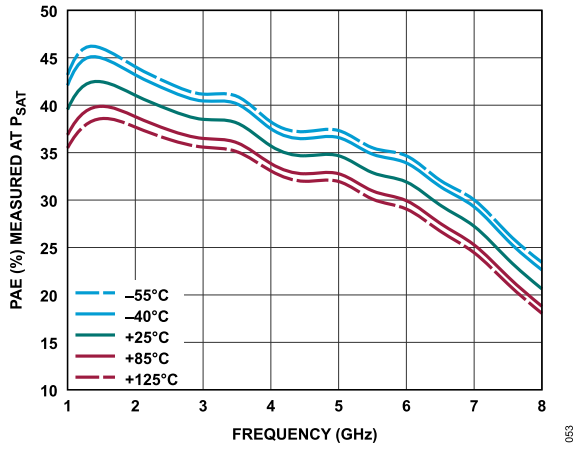


Figure 53. PAE vs. Frequency for Various Temperatures, 1 GHz to 8 GHz, V_{DD} = 5 V, I_{DQ} = 90 mA, R_{BIAS} = 1270 Ω

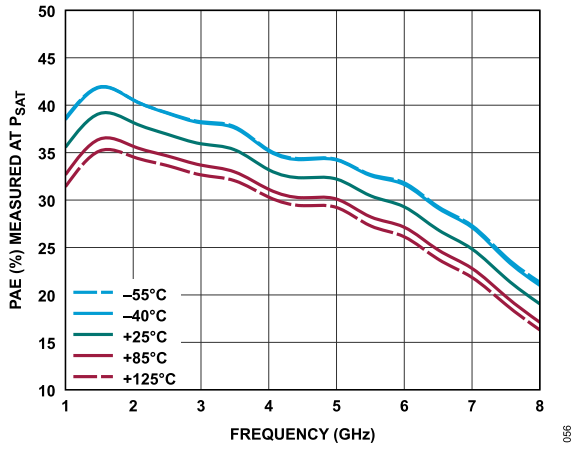


Figure 56. PAE Measured at P_{SAT} vs. Frequency for Various Temperatures, 1 GHz to 8 GHz, V_{DD} = 3 V, I_{DQ} = 60 mA, R_{BIAS} = 698 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

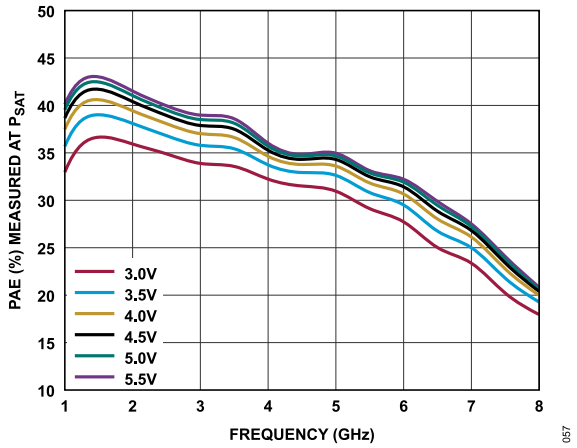


Figure 57. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages, 1 GHz to 8 GHz, I_{DQ} = 90 mA

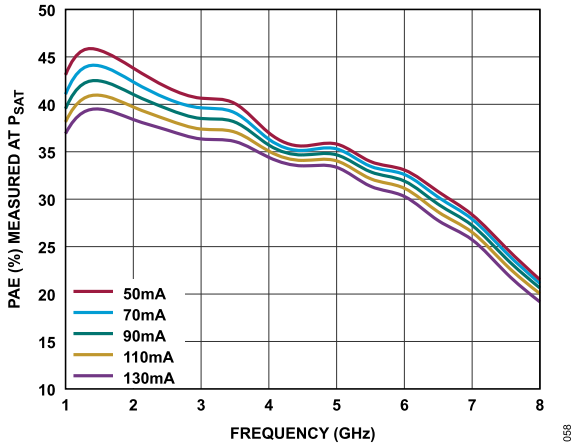


Figure 58. PAE Measured at P_{SAT} vs. Frequency for Various I_{DQ} Values, 1 GHz to 8 GHz, V_{DD} = 5 V

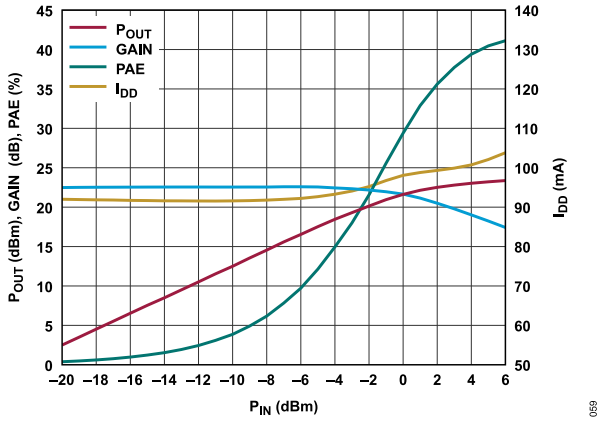


Figure 59. P_{OUT}, Gain, PAE and Drain Current (I_{DD}) vs. P_{IN}, Power Compression at 2 GHz, V_{DD} = 5 V, R_{BIAS} = 1270 Ω

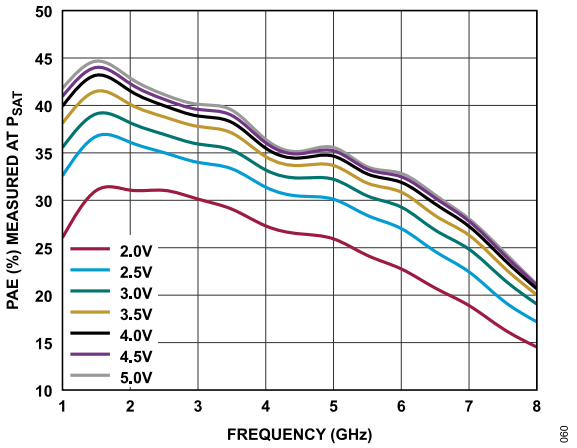


Figure 60. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages, 1 GHz to 8 GHz, I_{DQ} = 60 mA

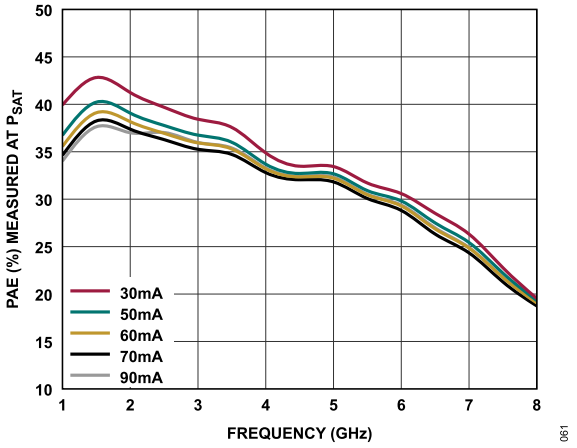


Figure 61. PAE Measured at P_{SAT} vs. Frequency for Various I_{DQ} Values, 1 GHz to 8 GHz, V_{DD} = 3 V

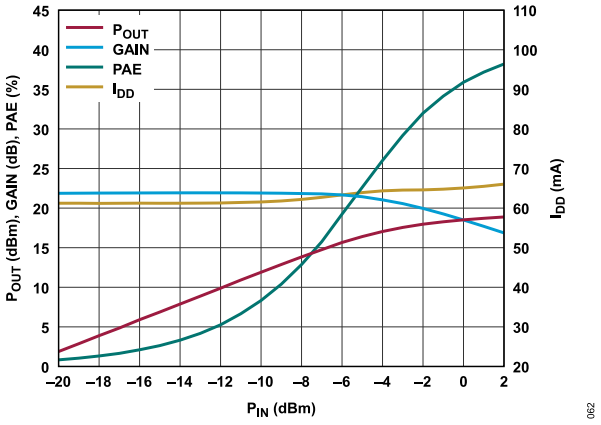


Figure 62. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 2 GHz, V_{DD} = 3 V, R_{BIAS} = 698 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

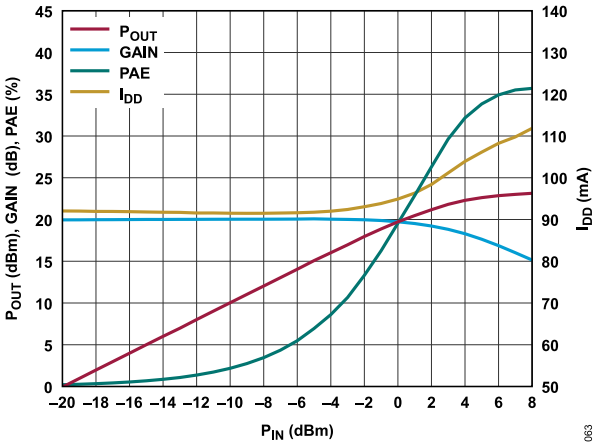


Figure 63. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 4 GHz, V_{DD} = 5 V, R_{BIAS} = 1270 Ω

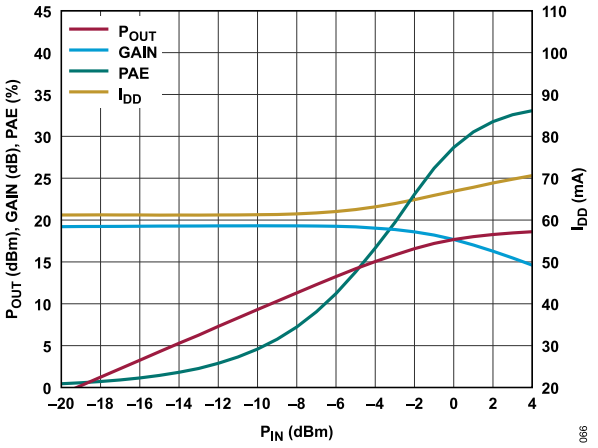


Figure 66. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 4 GHz, V_{DD} = 3 V, R_{BIAS} = 698 Ω

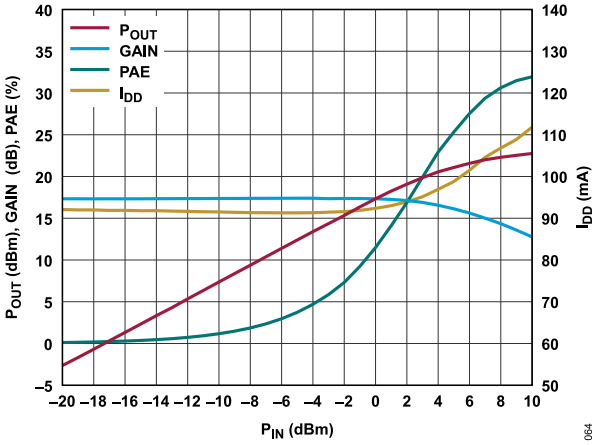


Figure 64. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 6 GHz, V_{DD} = 5 V, R_{BIAS} = 1270 Ω

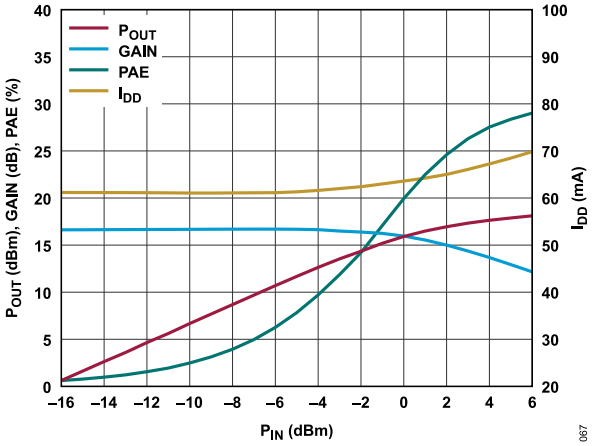


Figure 67. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 6 GHz, V_{DD} = 3 V, R_{BIAS} = 698 Ω

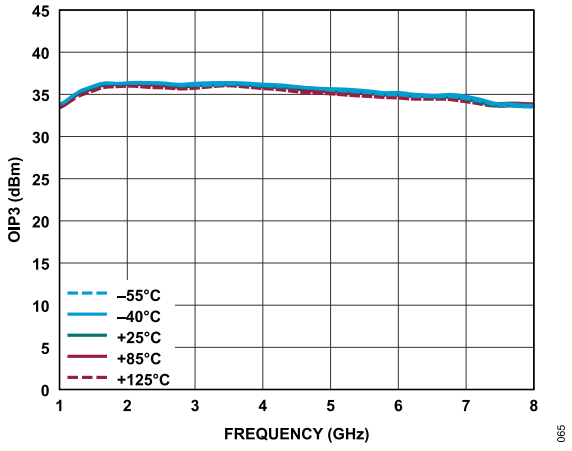


Figure 65. OIP3 vs. Frequency for Various Temperatures, 1 GHz to 8 GHz, V_{DD} = 5V, I_{DQ} = 90 mA, R_{BIAS} = 1270 Ω, P_{OUT} per Tone = 8 dBm

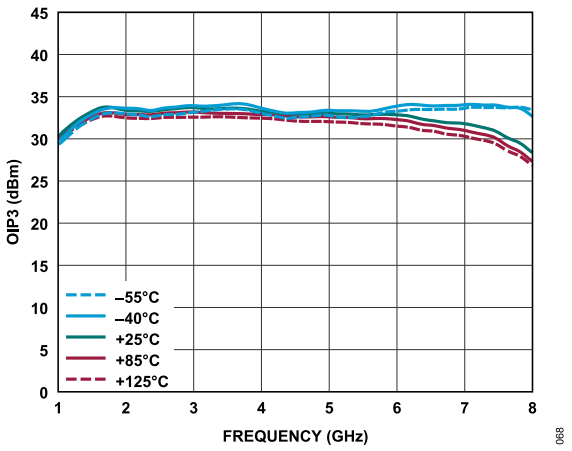


Figure 68. OIP3 vs. Frequency for Various Temperatures, 1 GHz to 8 GHz, V_{DD} = 3 V, I_{DQ} = 60 mA, R_{BIAS} = 698 Ω, P_{OUT} per Tone = 4 dBm

TYPICAL PERFORMANCE CHARACTERISTICS

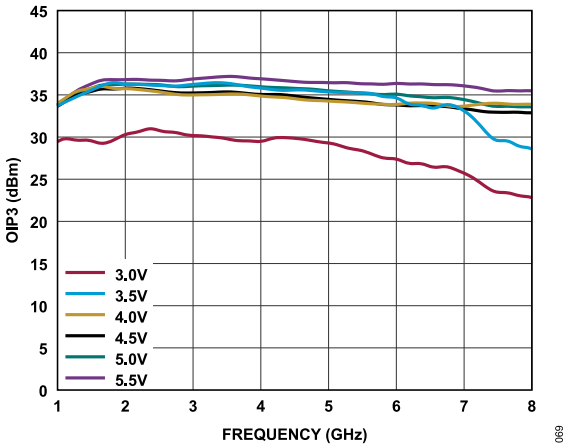


Figure 69. OIP3 vs. Frequency for Various Supply Voltages, I_{DQ} = 90 mA, P_{OUT} per Tone = 8 dBm

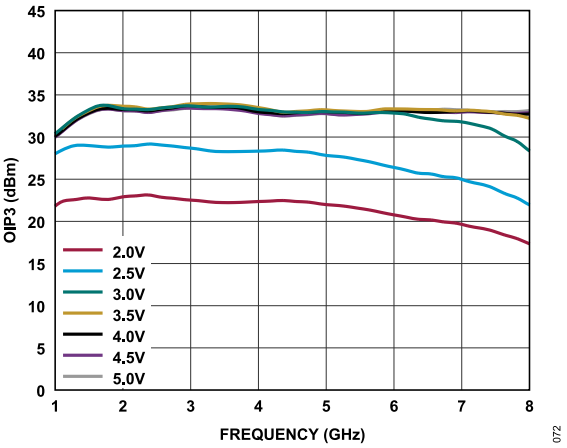


Figure 72. OIP3 vs. Frequency for Various Supply Voltages, I_{DQ} = 60 mA, P_{OUT} per Tone = 4 dBm

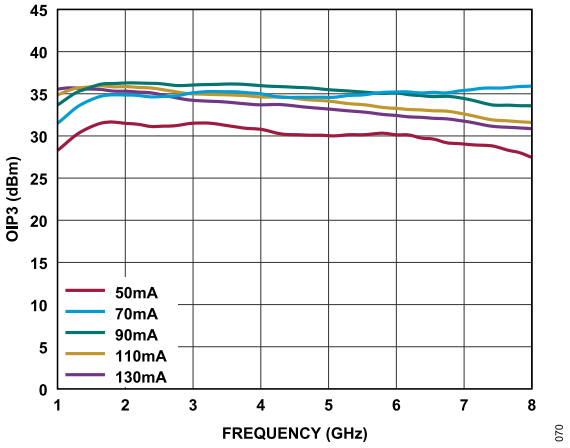


Figure 70. OIP3 vs. Frequency for Various I_{DQ} Values, V_{DD} = 5 V, P_{OUT} per Tone = 8 dBm

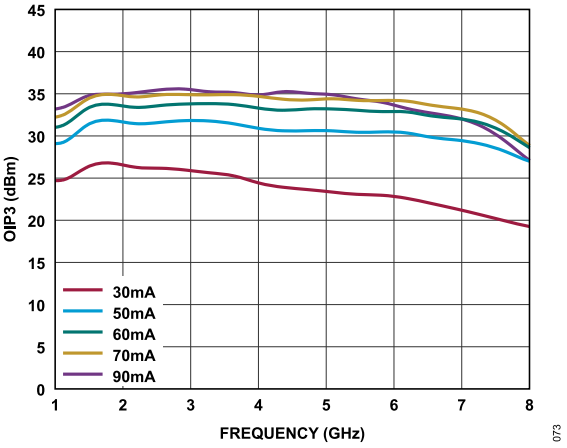


Figure 73. OIP3 vs. Frequency for Various I_{DQ} Values, V_{DD} = 3 V, P_{OUT} per Tone = 4 dBm

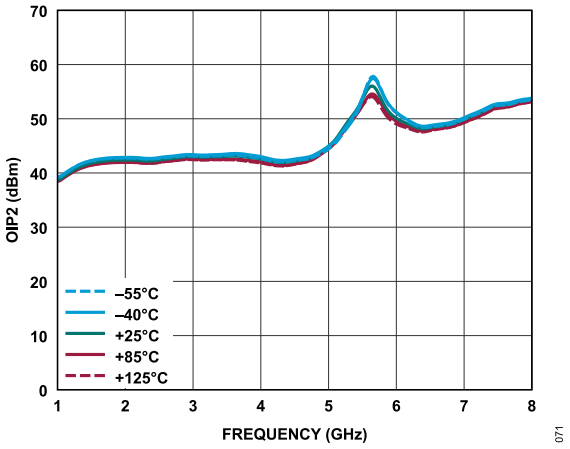


Figure 71. OIP2 vs. Frequency for Various Temperatures, 1 GHz to 8 GHz, V_{DD} = 5 V, I_{DQ} = 90 mA, R_{BIAS} = 1270 Ω, P_{OUT} per Tone = 8 dBm

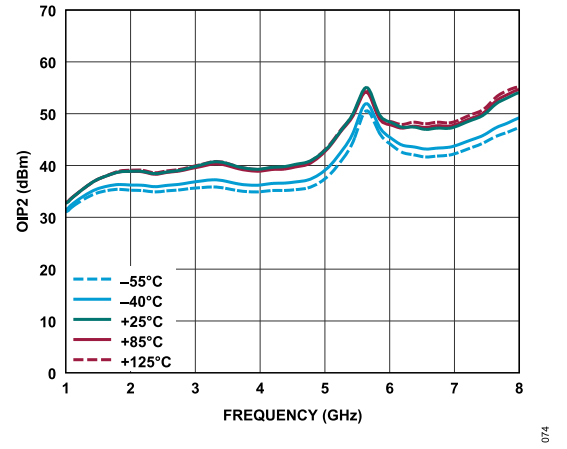


Figure 74. OIP2 vs. Frequency for Various Temperatures, 1 GHz to 8 GHz, V_{DD} = 3 V, I_{DQ} = 60 mA, R_{BIAS} = 698 Ω, P_{OUT} per Tone = 4 dBm

TYPICAL PERFORMANCE CHARACTERISTICS

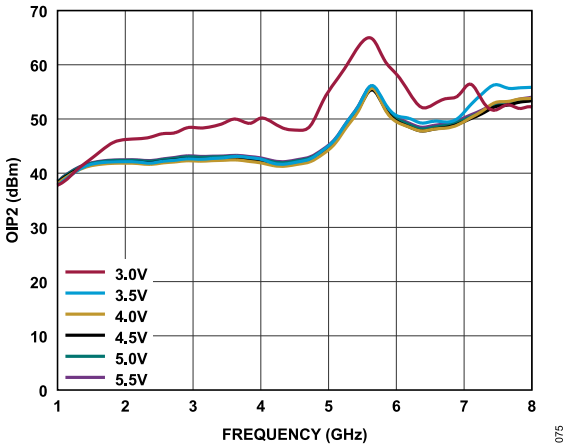


Figure 75. OIP2 vs. Frequency for Various Supply Voltages, I_{DQ} = 90 mA, P_{OUT} per Tone = 8 dBm

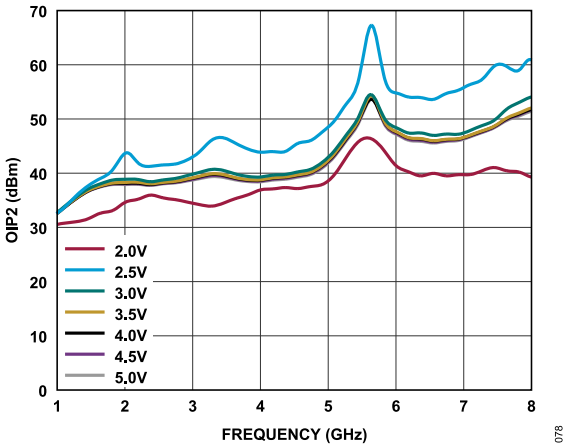


Figure 78. OIP2 vs. Frequency for Various Supply Voltages, I_{DQ} = 60 mA, P_{OUT} per Tone = 4 dBm

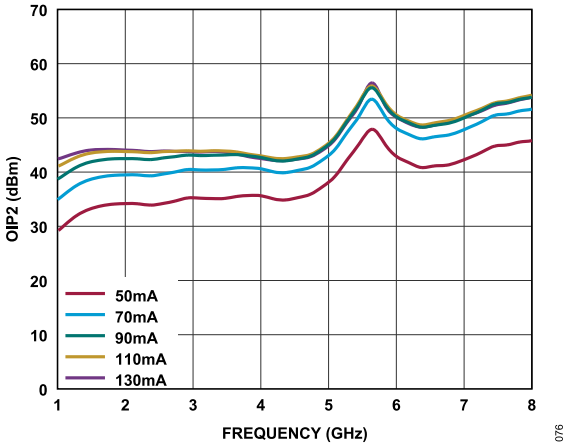


Figure 76. OIP2 vs. Frequency for Various I_{DQ} Values, V_{DD} = 5 V, P_{OUT} per Tone = 8 dBm

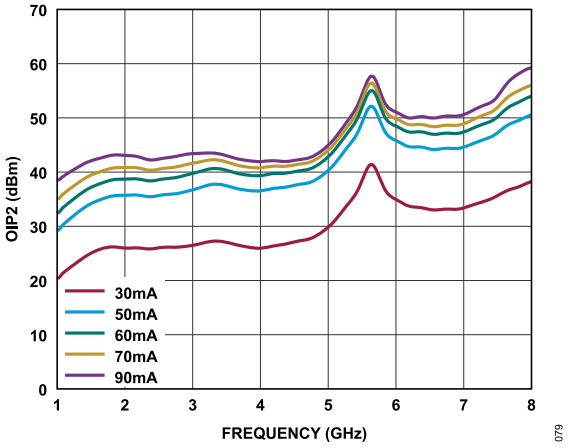


Figure 79. OIP2 vs. Frequency for Various I_{DQ} Values, V_{DD} = 3 V, P_{OUT} per Tone = 4 dBm

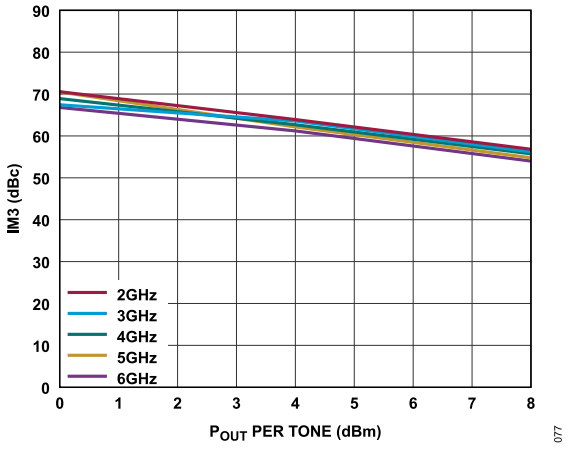


Figure 77. Output IM3 vs P_{OUT} per Tone for Various Frequencies, V_{DD} = 5 V, R_{BIAS} = 1270 Ω

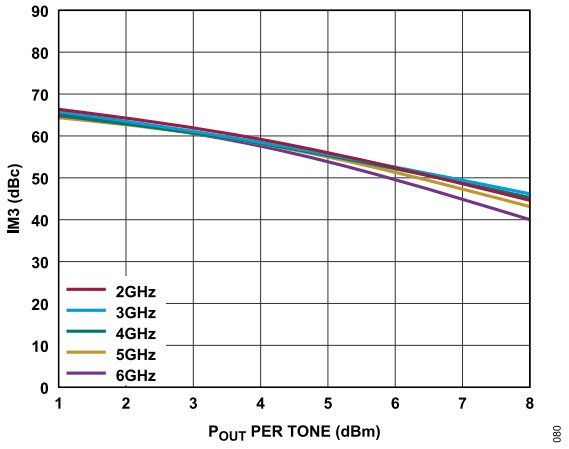


Figure 80. Output IM3 vs P_{OUT} per Tone for Various Frequencies, V_{DD} = 3 V, R_{BIAS} = 698 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

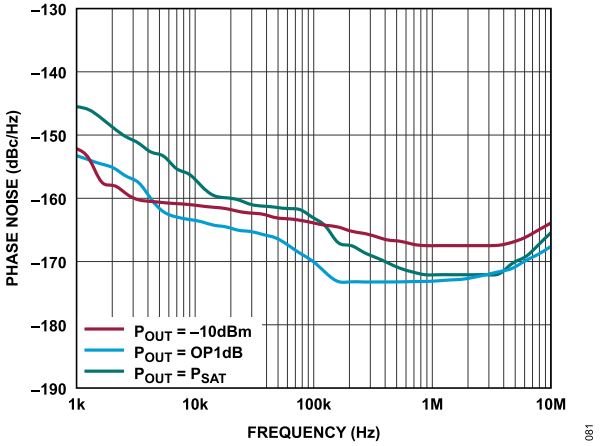


Figure 81. Phase Noise vs. Frequency at 3 GHz for Various P_{OUT} Values, V_{DD} = 5 V, I_{DQ} = 90 mA, R_{BIAS} = 1270 Ω

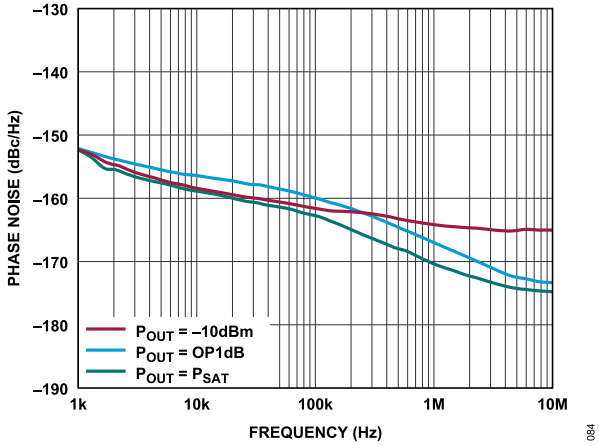


Figure 84. Phase Noise vs. Frequency at 5.5 GHz for Various P_{OUT} Values, V_{DD} = 5 V, I_{DQ} = 90 mA, R_{BIAS} = 1270 Ω

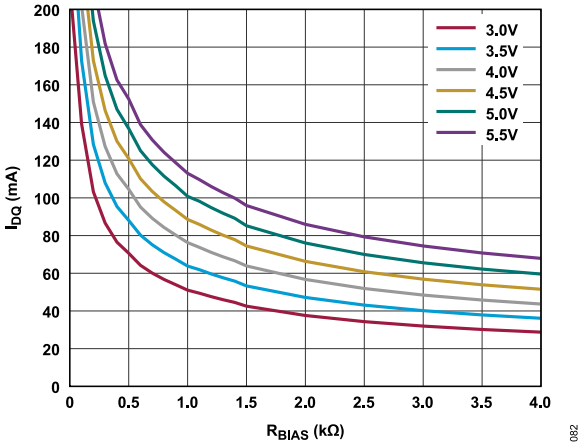


Figure 82. I_{DQ} vs. R_{BIAS} Values for Various Supply Voltages, 0 Ω to 4 kΩ

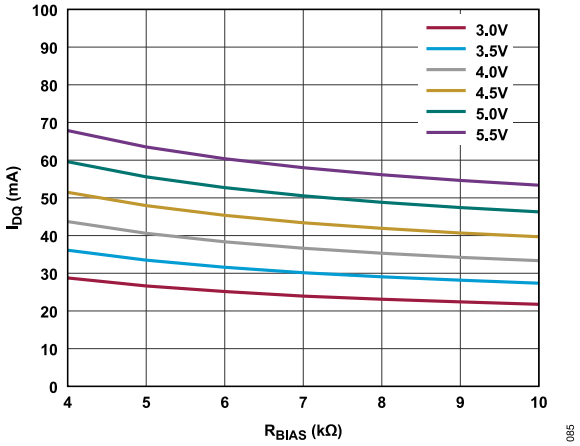


Figure 85. I_{DQ} vs. R_{BIAS} Values for Various Supply Voltages, 5 kΩ to 10 kΩ

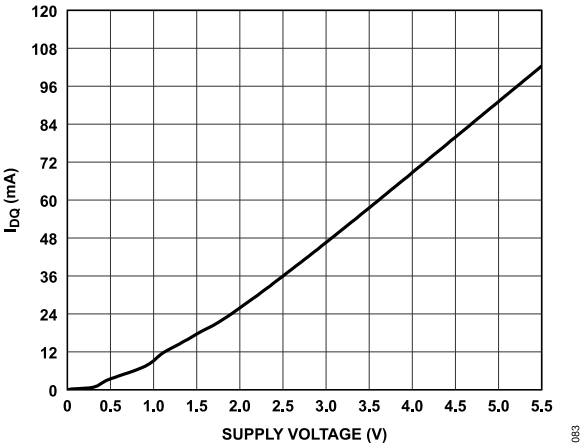


Figure 83. I_{DQ} vs. Supply Voltage, R_{BIAS} = 1270 Ω

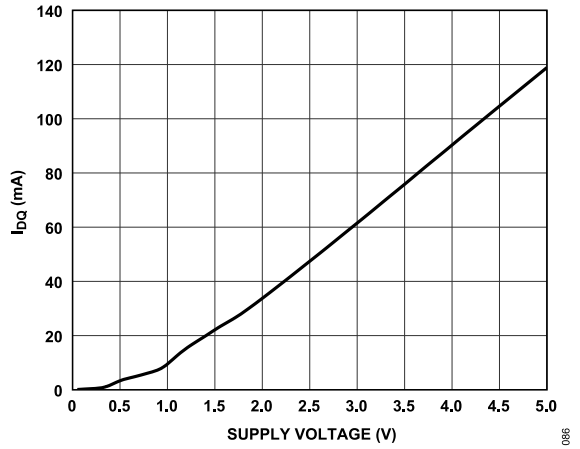


Figure 86. I_{DQ} vs. Supply Voltage, R_{BIAS} = 698 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

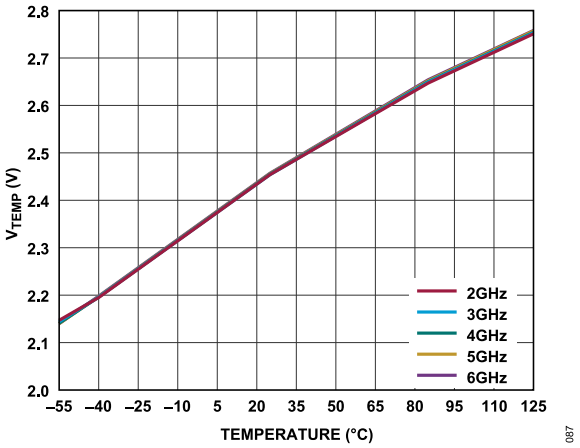


Figure 87. V_{TEMP} vs. Temperature for Various Frequencies, P_{OUT} = 20 dBm, V_{DD} = 5 V, I_{DQ} = 90 mA, R_{BIAS} = 1270 Ω

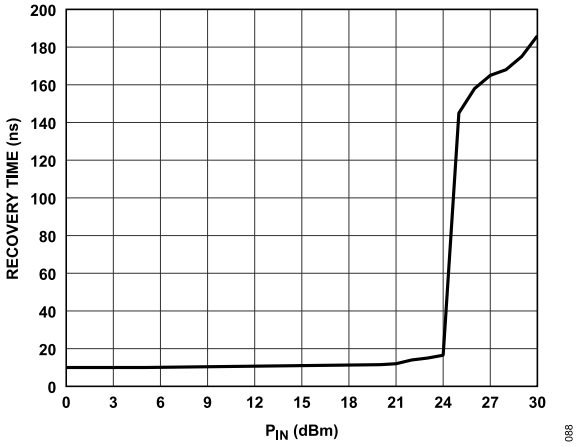


Figure 88. Overdrive Recovery Time vs. P_{IN} at 6 GHz, Recovery to Within 90% of Small Signal Gain Value, V_{DD} = 5 V, I_{DQ} = 90 mA, R_{BIAS} = 1270 Ω

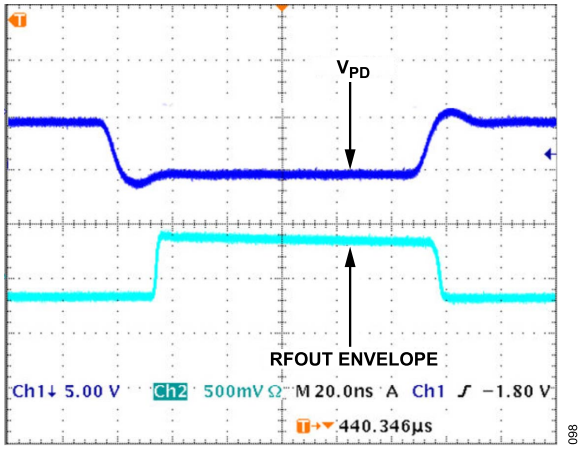


Figure 89. On and/or Off Response of the RFOUT Envelope Timing When the VPD Pin Is Toggled

TYPICAL PERFORMANCE CHARACTERISTICS

AMPLIFIER OFF STATE (V_{PD} = V_{DD})

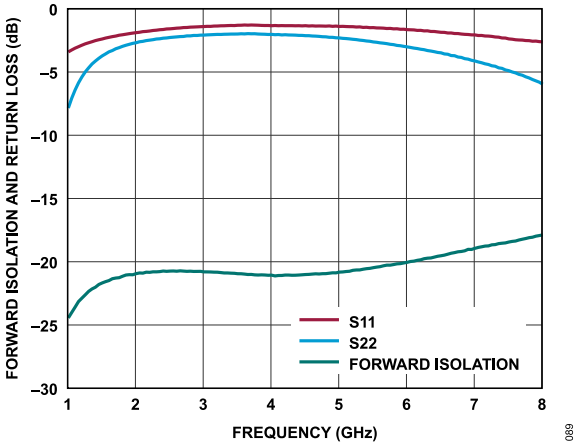


Figure 90. Forward Isolation and Return Loss vs. Frequency, 1 GHz to 8 GHz, V_{DD} = 5 V

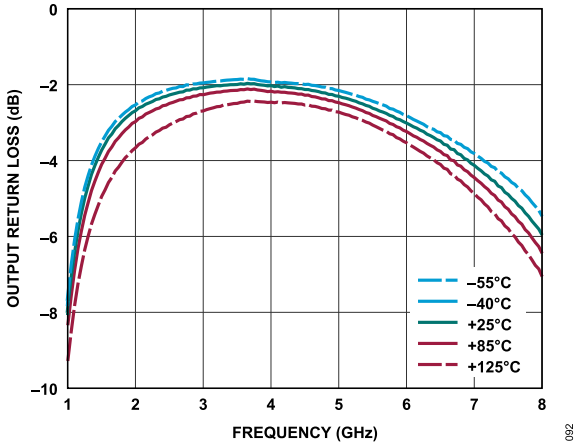


Figure 93. Output Return Loss vs. Frequency for Various Temperatures, 1 GHz to 8 GHz, V_{DD} = 5 V

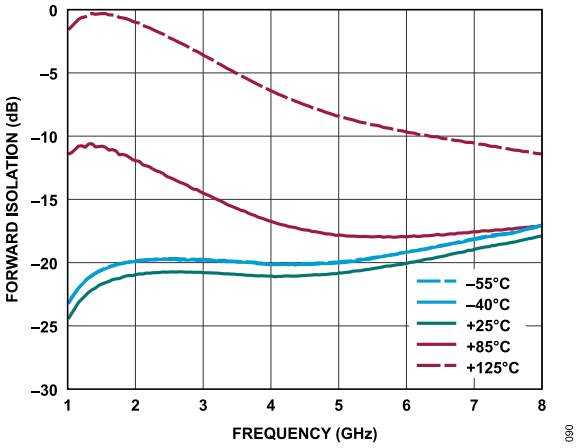


Figure 91. Forward Isolation vs. Frequency for Various Temperatures, 1 GHz to 8 GHz, V_{DD} = 5 V

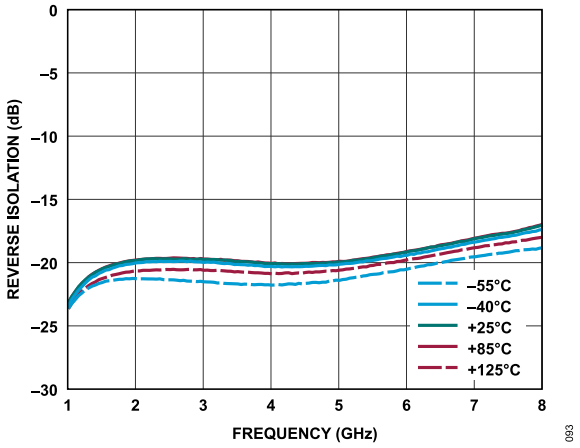


Figure 94. Reverse Isolation vs. Frequency for Various Temperatures, 1 GHz to 8 GHz, V_{DD} = 5 V

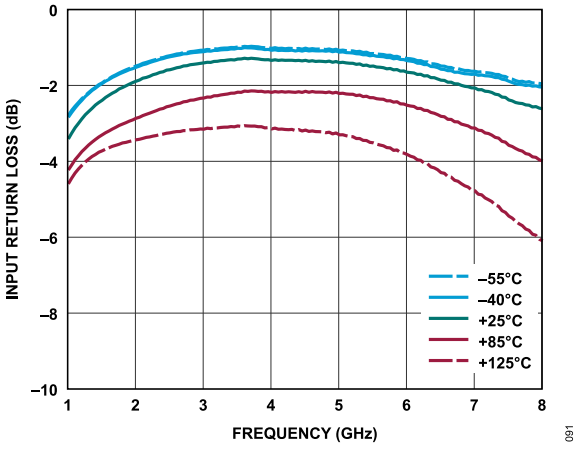


Figure 92. Input Return Loss vs. Frequency for Various Temperatures, 1 GHz to 8 GHz, V_{DD} = 5 V

THEORY OF OPERATION

The ADL8108 is a wideband LNA with integrated AC-coupling capacitors, a bias inductor, a temperature sensor, and an enable or disable function. Figure 95 shows the simplified architecture of the ADL8108.

The ADL8108 has AC-coupled, single-ended input and output ports with impedances that are nominally equal to 50 Ω over the 1 GHz to 8 GHz frequency range. No external matching components are required. To adjust the quiescent current, connect an external resistor between the RBIAS and VDD pins.

The ADL8108 contains an integrated temperature sensor. The temperature sensor is biased using the VBTEMP pin. The voltage that is proportional to the device temperature can be measured on the VTEMP pin.

The ADL8108 also has an enable or disable function. By pulling the VPD pin low or high, the ADL8108 can be enabled or disabled, respectively.

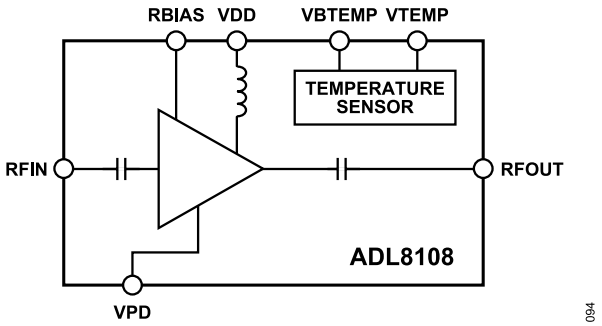


Figure 95. Simplified Architecture

APPLICATIONS INFORMATION

The basic connections for operating the ADL8108 over the specified frequency range are shown in Figure 96 . No external biasing inductor is required, which allows the 5 V supply to be connected to the VDD pin. It is recommended to use 100 pF and 1000 pF power-supply decoupling capacitors. The power-supply decoupling capacitors shown in Figure 96 represent the configuration used to characterize and qualify the ADL8108.

To set I_{DQ}, connect a resistor (R2) between the RBIAS and VDD pins. A default value of 1270 Ω is recommended, which results in a nominal I_{DQ} of 90 mA. Table 12 shows how I_{DQ} and I_{DQ_AMP} vary vs. R_{BIAS}. The RBIAS pin also draws a current that varies with the value of R_{BIAS} (see Table 12). Do not leave the RBIAS pin open.

The VTEMP pin provides an output voltage that is proportional to the die temperature. The VTEMP pin has a high output resistance that must be buffered using an op-amp. To activate the temperature sensor, connect the VBTEMP pin to V_{DD}. If the temperature sensor is not used, the VBTEMP and VTEMP pins can be grounded or left open.

The VPD pin provides a convenient method to power down the ADL8108. To disable the amplifier, connect the VPD pin to a supply. To enable the amplifier, connect the VPD pin to ground.

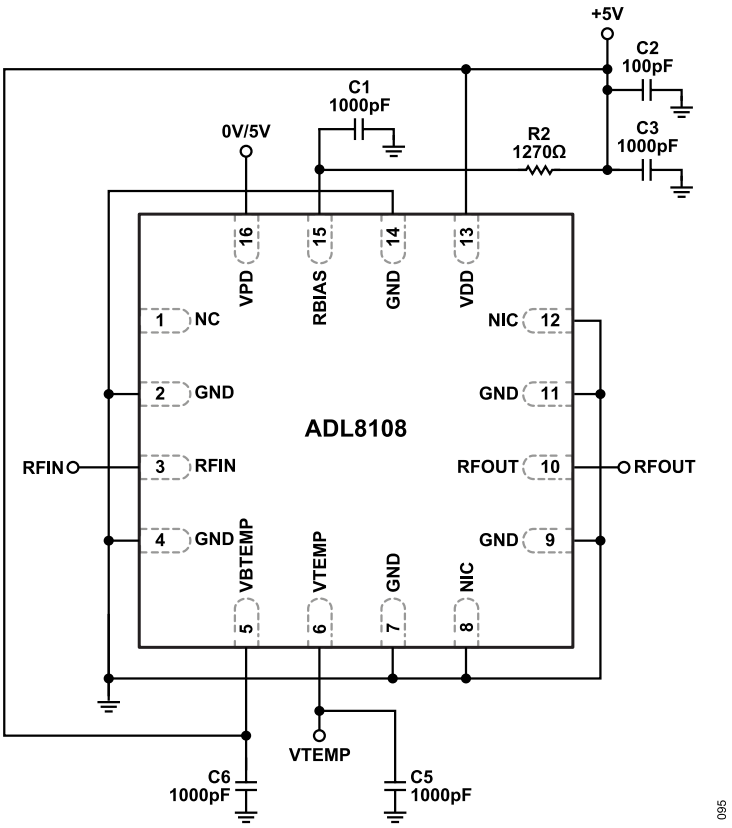


Figure 96. Typical Application Circuit

APPLICATIONS INFORMATION

RECOMMENDED BIAS SEQUENCING

Correct sequencing of the DC and RF power is required to safely operate the ADL8108. During power up, apply VDD before the RF power is applied to RFIN, and during power off, remove the RF power from RFIN before VDD is powered off.

Table 12. Recommended Bias Resistor Values for V_{DD} = 5 V

R_{BIAS} (Ω)	I_{DQ} (mA)	I_{DQ_AMP} (mA)	I_{RBIAS} (mA)
6810	50	49.4	0.6
2394	70	68.3	1.7
1270	90	86.9	3.1
795	110	105.4	4.6
545	130	123.7	6.3

Table 13. Recommended Bias Resistor Values for V_{DD} = 3 V

R_{BIAS} (Ω)	I_{DQ} (mA)	I_{DQ_AMP} (mA)	I_{RBIAS} (mA)
3570	30	29.4	0.6
1050	50	48.1	1.9
698	60	57.3	2.7
511	70	66.6	3.4
296	90	84.9	5.1

Table 14. Recommended Bias Resistor Values for Various Supply Voltages, I_{DQ} = 90 mA

R_{BIAS} (Ω)	V_{DD} (V)	I_{DQ_AMP} (mA)	I_{RBIAS} (mA)
296	3.0	84.9	5.1
471	3.5	85.5	4.5
678	4.0	86.0	4.0
940	4.5	86.5	3.5
1270	5.0	87.0	3.0
1705	5.5	87.4	2.6

Table 15. Recommended Bias Resistor Values for Various Supply Voltages, I_{DQ} = 60 mA

R_{BIAS} (Ω)	V_{DD} (V)	I_{DQ_AMP} (mA)	I_{RBIAS} (mA)
182	2.0	56.2	3.8
406	2.5	56.8	3.2
698	3.0	57.3	2.7
1120	3.5	57.8	2.2
1695	4.0	58.2	1.8
2516	4.5	58.6	1.4
3758	5.0	58.9	1.1

RECOMMENDED POWER MANAGEMENT CIRCUIT

Figure 97 shows a recommended power management circuit for the ADL8108. The LT8607 step-down regulator is used to step down a 12 V rail to 5.5 V, which is then applied to the LT3042 low dropout (LDO) linear regulator to generate a low noise 5 V output. While the circuit shown in Figure 97 has an input voltage of 12 V, the input range to the LT8607 can be as high as 42 V.

The 5.5 V regulator output (V_{REG}) of the LT8607 is set by the R4A and R5A resistors according to the following equation:

$$R5A = R4A/((V_{REG}/0.778\ V) - 1) \quad (1)$$

The switching frequency (f_{SW}) is set to 2 MHz by the 18.2 kΩ resistor (R2A) on the RT pin of the LT8607. The LT8607 data sheet provides a table of resistor values that can be used to select other switching frequencies ranging from 0.2 MHz to 2.200 MHz.

V_{OUT} of the LT3042 is set by the R3B resistor connected to the SET pin, according to the following equation:

$$R3B = V_{OUT}/100\,\mu A \quad (2)$$

The resistors on the PGFB pins of the LT3042 are chosen to trigger the power-good (PG) signal when the output reaches 90% of its target voltage of 5 V. The PG open-collector output is pulled up to the 5 V output to give users a convenient 0 V or 5 V output voltage.

The LT8607 can source a maximum current of 750 mA, and the LT3042 can source a maximum current of 200 mA. If the power supply voltage is developed as a bus supply to serve multiple components, higher current devices can be used. The LT8608 and LT8609 step-down regulators can source a maximum current of 1.5 A and 3 A, respectively, and these devices are pin-compatible with the LT8607. The LT3045 linear regulator, which is pin-compatible with the LT3042, can source a maximum current up to 500 mA.

Table 16. Recommended Resistor Values to Set to Various LT3042 and LT8607 Output Voltages

LT3042 LDO V_{OUT} and Power Good Threshold				LT8607 V_{REG}		
V_{OUT} (V)	R3B (kΩ)	R5B (kΩ)	R6B (kΩ)	Recommended V_{REG} (V)	R4A (MΩ)	R5A (kΩ)
2.0	20	453	90.9	2.5	1	453
3.0	30.1	453	56.2	3.5	1	287
3.3	33.2	453	51.1	3.8	1	255
4.0	40.2	453	41.2	4.5	1	210
5.0	49.9	453	32.4	5.5	1	165

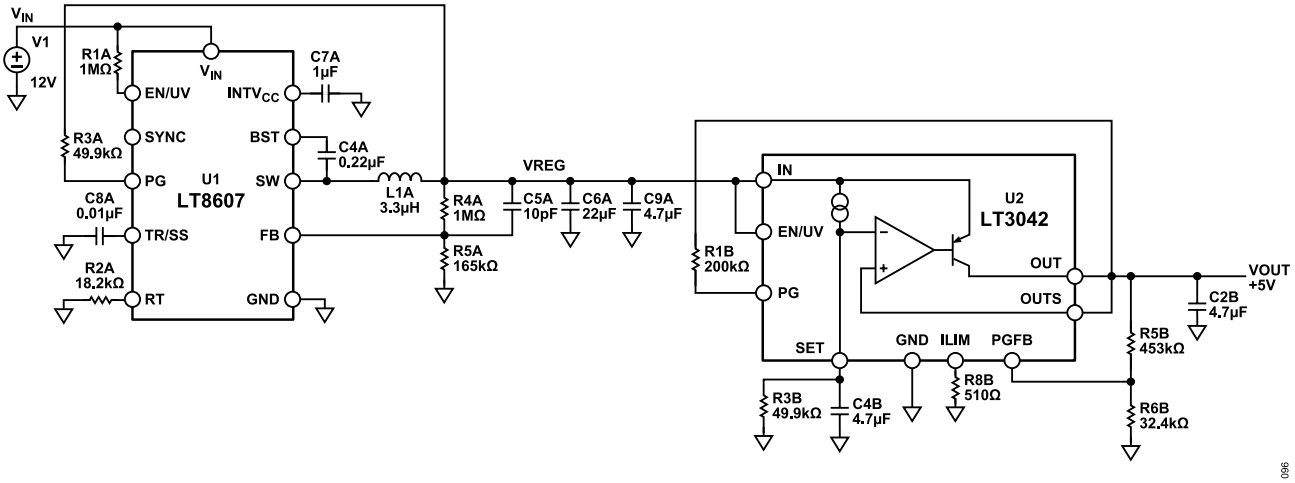
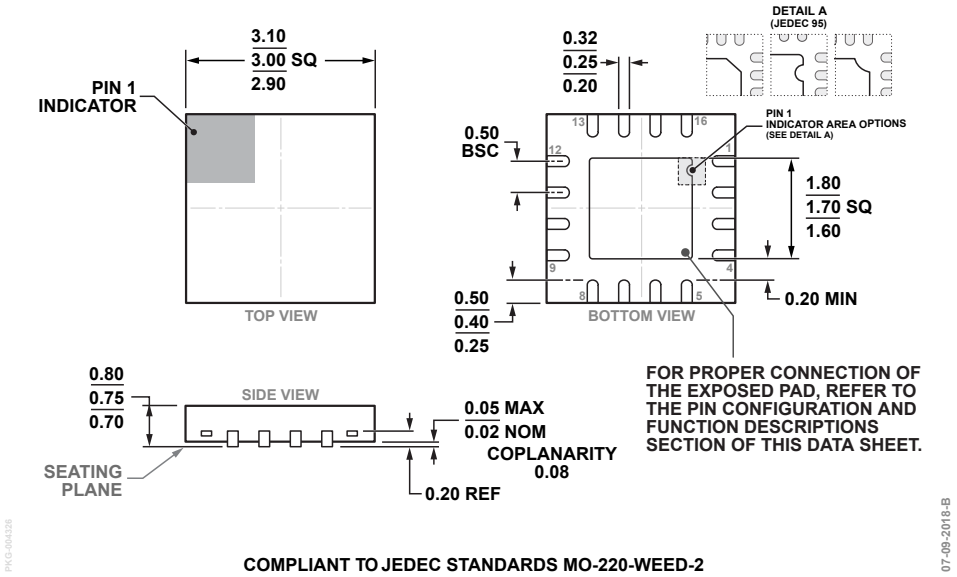


Figure 97. Recommended Power Management Circuit

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-2

Figure 98. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-35)
Dimensions Shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Packing Quantity	Package Option
ADL8108ACPZN	−55°C to +125°C	16-Lead LFCSP, 3 mm × 3 mm × 0.75 mm	Tape, 1	CP-16-35
ADL8108ACPZN-R7	−55°C to +125°C	16-Lead LFCSP, 3 mm × 3 mm × 0.75 mm	Reel, 1500	CP-16-35

[1] Z = RoHS Compliant Part.

[2] The lead finish of the ADL8108ACPZN and ADL8108ACPZN-R7 is nickel palladium gold

EVALUATION BOARDS

Model[1]	Description
ADL8108-EVALZ	Evaluation Board

[1] Z = RoHS Compliant Part.

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ADL8108ACPZN ADL8108ACPZN-R7