10-Channel Precision Synchronizer

FEATURES

- 10 BSYNC channels
- Precise BSYNC time alignment (<5 ps)
- Enables clock synchronization in large distribution networks
- Independent programmable BSYNC channel delay
- Precise path delay compensation of each BSYNC channel using bidirectional loopback capability
- Flexible physical interface supports PCB trace or cable connections with DC or AC coupling
- Each BSYNC channel supports gapped periodic clocking
- Integrated TDC
- Integrated temperature sensor

APPLICATIONS

- 5G timing transport high precision synchronization
- Phased array radar
- Automatic test equipment (ATE) pin electronics
- JESD204B/JESD204C support for analog-to-digital converter (ADC) and digital-to-analog converter (DAC) clocking

FUNCTIONAL BLOCK DIAGRAM

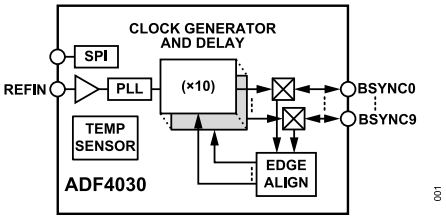

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADF4030 provides for 10 bidirectional synchronized clock (BSYNC) channels and accepts a reference clock input (REFIN) signal as a frequency reference for generating an output clock on any BSYNC channels that are configured as an output. The hallmark feature of the ADF4030 is the ability to time align the clock edges of any one or more BSYNC channels to <5 ps (at the device pins) with respect to the BSYNC channel selected as the reference BSYNC channel.

The ADF4030 is well adapted for multiple connections with other ADF4030 devices for synchronizing clock signals in a system. Each BSYNC is bidirectional, allowing for reversing the direction of the clock signal to measure the propagation delay of the transmission medium. Round trip constructions that use replica paths are also supported. The bidirectional nature of the round trip delay measurement greatly reduces the error in determining the propagation delay through the BSYNC transmission medium as compared to using a replica path. This feature makes the ADF4030 capable to time align the clock edges of BSYNC channels across multiple ADF4030 devices, independent of the tree or cascade architecture in which the ADF4030 system is designed. The benefits of bidirectional clocking extend to devices other than the ADF4030 (assuming those devices support bidirectional clock exchanges).

The output divider block associated with each BYSNC channel has an optional pseudorandom binary sequence (PRBS) generator for producing gapped periodic clock signals that supports JESD204B and JESD204BC operation.

The ADF4030 may be used as a standalone differential time-to-digital converter (TDC) to measure the difference in time between clocks arriving at the inputs.

The RMS jitter of one ADF4030 BSYNC clock is 4.3 ps typical.

The ADF4030 is available in a 48-lead, 7 mm × 7 mm, land grid array [LGA] package and operates over the −40°C to +105°C ambient temperature range.

Throughout the data sheet, the letter x is used to mean any integer. For example, in BSYNCx, x refers to any channel from Channel 0 to Channel 9.

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REVISION HISTORY

10/2024—Revision 0: Initial Version

SPECIFICATIONS

The minimum and maximum values apply for the full range of supply voltage and operating temperature variations. Typical values apply for VDD18x = 1.8 V, VDD33x = 3.3 V, and T_A = 25°C, unless otherwise noted.

Table 1. Specifications

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
OPERATING TEMPERATURE					
Ambient Temperature	−40	+25	+105	°C	$T_J \leq 125$ °C
Die Temperature			125	°C	
SUPPLY VOLTAGE					
VDD18x	1.71	1.8	1.89	V	
VDD33x	3.15	3.3	3.45	V	
SUPPLY CURRENT					
VDD33_PLL		102	121	mA	
VDD33_TDC		15	19	mA	
VDD18_DIG and VDD18_TDC		30	37	mA	$f_{CORECLK}$[1] = 125 MHz, f_{BSYNC}[2] = 200 MHz
VDD33_BSx					
BSYNCx Receiver Disabled[3]		0.2	180	µA	Transmitter path (driver and delay lines) powered down [4]
		6.1	8	mA	Transmitter path (driver and delay lines) powered down and AC-coupled biasing[5]
		22.3	27	mA	Transmitter driver powered down and delay lines powered up[6]
		27.3	33	mA	Transmitter driver powered up and idle and delay lines powered up[7]
		54.3	65	mA	Transmitter driver powered up and enabled and delay lines powered up[8]
		60.6	72	mA	Transmitter driver powered up and enabled, delay lines powered up, and 20 mA driver[9]
BSYNCx Receiver Enabled[10]		16.4	20	mA	Transmitter path (driver and delay lines) powered down[11]
		22.5	28	mA	Transmitter path (driver and delay lines) powered down and AC-coupled biasing[5]
		38.6	47	mA	Transmitter driver powered down and delay lines powered up[6])
		43.6	53	mA	Transmitter driver powered up and idle and delay lines powered up[7]
		70.6	84	mA	Transmitter driver powered up and enabled and delay lines powered up[8]
		76.9	92	mA	Transmitter driver powered up and enabled, delay lines powered up, and 20 mA driver[9]
TOTAL POWER DISSIPATION					
Configuration 1		2.3	2.9	W	REFIN = 100 MHz, BSYNC0 to BSYNC9 transmit nongapped 100 MHz with driver current at 14 mA
Configuration 2		2.1	2.7	W	REFIN = 100 MHz, nine BSYNCx transmit nongapped 100 MHz with driver current at 14 mA and one BSYNCx receives 100 MHz
Configuration 3		0.5	0.7	W	REFIN = 100 MHz, BSYNC0 to BSYNC9 receive 100 MHz
Configuration 4		1.4	1.8	W	REFIN = 100 MHz, one BSYNCx transmits nongapped 100 MHz with driver current at 14 mA, one BSYNCx receives 100 MHz, and all others set to transmit with driver disabled

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
POWER DOWN CURRENT					PD_ALL = 1
1.8 V Supplies		2	500	µA	I_{VDD18_DIG} + I_{VDD18_TDC}
3.3 V Supplies		0.2	2.5	mA	I_{VDD33_BS0} + I_{VDD33_BS1} + … + I_{VDD33_BS9} + I_{VDD33_PLL} + I_{VDD33_TDC}
REFERENCE CLOCK INPUT					
Differential Mode					
Input Frequency	10		250	MHz	
Differential Input Voltage	160	350	1000	mV p-p	Can accommodate single ended inputs via AC grounding of unused inputs and 100 Ω resistor connected to GND, and instantaneous voltage on each pin must not exceed VDD33_PLL
Minimum Input Slew Rate		500		V/µs	
Common-Mode Internally Generated Input Voltage		1.85		V	Provided for information only; AC coupling is recommended
Differential Input Resistance		3		kΩ	
Differential Input Capacitance		1		pF	
Minimum Duty Cycle		40		%	
Maximum Duty Cycle		60		%	
Concept Peak Detector					
Minimum Input Signal Detected (REF_OK Bit = 1)		100		mV p-p	
Maximum Input Signal Not Detected (REF_OK Bit = 0)		80		mV p-p	
PHASE-LOCKED LOOP (PLL)					
Phase/Frequency Detector (PFD)	10		20	MHz	
Minimum Charge Pump Current		360		µA	2-bit resolution
Maximum Charge Pump Current		630		µA	2-bit resolution
Voltage-Controlled Oscillator (VCO)					
Frequency Range	2375		2625	MHz	2500 MHz ± 5%
BYSNC					
Frequency	0.65		200	MHz	
BSYNC Transmit					
Rise Time and Fall Time (20% to 80%)		80		ps	100 Ω terminations for BSYNC transmit
Duty Cycle	45	50	55	%	
Differential Output Voltage Swing	290	350	410	mV p-p	14 mA driver current and 100 Ω termination at destination
	410	500	590	mV p-p	20 mA driver current and 100 Ω termination at destination
Common-Mode Output Voltage	0.43	0.5	0.57	V	RCM = 1 and 14 mA driver current
	0.66	0.8	0.94	V	RCM = 51 and 14 mA driver current
	0.98	1.2	1.42	V	RCM = 62 and 14 mA driver current
	0.68	0.8	0.92	V	RCM = 21 and 20 mA driver current
	1.0	1.2	1.4	V	RCM = 52 and 20 mA driver current
Common-Mode Difference			15	mV	Voltage difference between output pins and output driver static
RMS Jitter One Channel		4.3		ps	Between 100 Hz and 30 MHz
BSYNC Receive					
Instantaneous BSYNC Pin Voltage	0		1.9	V	Instantaneous voltage on each pin must not fall under 0 V or exceed 1.9 V
Differential Input Voltage	200	330	1000	mV p-p	
Minimum Input Slew Rate		500		V/µs	Minimum limit imposed for TDC performance

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
Common-Mode Internally Generated Input Voltage		0.84		V	
Input Common-Mode Range (V_{CMI})	300		1600	mV	DC coupling supported
Differential Input Resistance		640		kΩ	External differential termination
Differential Input Capacitance		1		pF	External differential termination
Duty Cycle	48	50	52	%	187 MHz < f_{BSYNC} ≤ 200 MHz
	45	50	55	%	f_{BSYNC} ≤ 187 MHz. See the Maximum BSYNC Frequency Reduction vs. Duty Cycle section if duty cycle is outside 45% to 55% range
BSYNC ALIGNMENT					AVGEXP ≥ 12, t_{RISE} < 300 ps or Δt_{RISE} < 100 ps, V_{CMI} = 0.35 V to 1 V or ΔV_{CMI} < 75 mV[1][2]
Maximum BSYNC Alignment Error		± 5		ps	At the ADF4030 pin level, nongapped periodic clocks or gapped periodic clocks with TDC time difference > 350 ps
		± 17		ps	At the ADF4030 pin level, gapped periodic clocks with TDC time difference < 350 ps
REFIN to BSYNC Temperature Coefficient		+160		fs/°C	Independent of REFIN drift with temperature
BSYNC to BSYNC Temperature Coefficient		± 30		fs/°C	Independent of REFIN drift with temperature
Fine Delay Step Size		1.4		ps	Least significant bit of Bits[5:0], ADEL_x, Register 0x84 to Register 0x8D
Intermediate Delay Step Size		50		ps	1/8 of f_{VCO} = 2.5 GHz period and least significant bit of Bits[15:0], DELTA_NDEL_COAR, Register 0x18 and Register 0x19
TDC					t_{RISE} < 300 ps or Δt_{RISE} < 100 ps and V_{CMI} = 0.35 V to 1 V or ΔV_{CMI} < 75 mV
TDC Resolution		21		µ°	24 Bits
TDC Accuracy		± 3.6		ps	Nongapped periodic clocks or gapped periodic clocks with TDC time difference > 350 ps
		± 15.6		ps	Gapped periodic clocks with (TDC input) TDC time difference < 350 ps
TEMPERATURE MEASUREMENT SYSTEM					
Output Resolution		1		°C	
Conversion Time		42.5		µs	17 cycles at ADCCLK = 1/400 kHz
SDO, SDIO, IRQB, MUXOUT1, and MUXOUT2 OUTPUT					
SDO High-Z Leakage			±1	µA	
Output Voltage High	VDD18_DIG − 0.3V			V	1.8 V logic, load current = 1 mA
	VDD33_TDC − 0.3V			V	3.3 V logic, load current = 1 mA
Output Voltage Low			0.4	V	1.8 V or 3.3 V logic, load current = 1 mA
IRQB Open Drain Mode					IRQB_OPENDRAIN bit set to 1 and external 1 kΩ pull-up resistor set to 1.8 V or 3.3 V function of CMOS_OV bit
Output High Leakage			1	µA	IRQB pin pulled to 3.3 V
Output Voltage Low			0.4	V	When external 1 kΩ pull-up resistor to 3.3 V
Maximum Supported Sink Current			5	mA	

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
ADDR0, ADDR1, ADDR2, ADDR3, $\overline{CS}$, SCLK, and SDIO INPUT					
Input Voltage High	1.2			V	1.8 V or 3.3 V logic
Input Voltage Low			0.6	V	1.8 V or 3.3 V logic
Input Current			±1	µA	For both high and low input voltages

[1] Digital core clock frequency.

[2] BSYNC frequency.

[3] Channel not selected as TDC source or target.

[4] PD_TX_PATH_x = 1.

[5] PD_TX_PATH_x = 1, AC_COUPLEDx = 1.

[6] PD_TX_PATH_x = 0, PD_DRV_x = 1.

[7] PD_TX_PATH_x = 0, PD_DRV_x = 0, EN_DRVx = 0.

[8] PD_TX_PATH_x = 0, PD_DRV_x = 0, EN_DRVx = 1.

[9] PD_TX_PATH_x = 0, PD_DRV_x = 0, EN_DRVx = 1, BOOSTx = 1.

[10] Channel selected as TDC source or target.

[11] PD_TX_PATH_x = 1.

[12] ΔV_{CMI} is difference between the BSYNC channels

SPECIFICATIONS

SERIAL INTERFACE TIMING CHARACTERISTICS

Table 2. Serial Interface Timing Characteristics

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
SCLK Frequency			75	MHz	
SCLK Pulse High (t_{HIGH})	6			ns	All timing specifications measured at the output high range (VIH) = 1.2 V levels
SCLK Pulse Low (t_{LOW})	6			ns	
SDIO Setup Time (t_{DS})	4			ns	
SDIO Hold Time (t_{DH})	2			ns	
SCLK Fall Edge to SDIO Valid Prop Delay (t_{ACCESS_SDIO})	6			ns	
SCLK Fall Edge to SDO Valid Prop Delay (t_{ACCESS_SDO})	6			ns	
$\overline{CS}$ Rising Edge to SDIO High-Z (t_Z)	6			ns	
$\overline{CS}$ Falling Edge to SCLK Rise Setup Time (t_S)	2			ns	
SCLK Rising Edge to $\overline{CS}$ Rise Hold Time (t_H)	3			ns	

Address bits A[14], A[13], and A[8] are always 0. A[12:9] map to the ADDR3, ADDR2, ADDR1, and ADDR0 pins, respectively. A[7:0] represent the register addresses in Figure 2, Figure 3, and Figure 4.

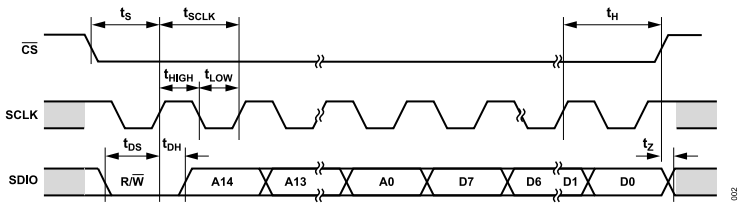

Figure 2. Write Timing Diagram

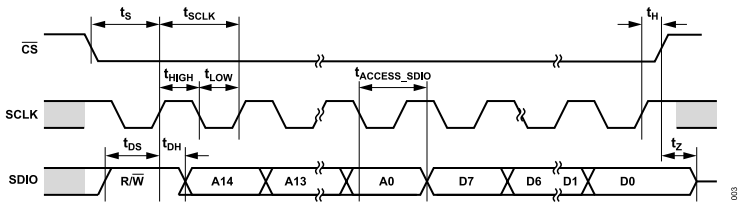

Figure 3. 3-Wire Read Timing Diagram

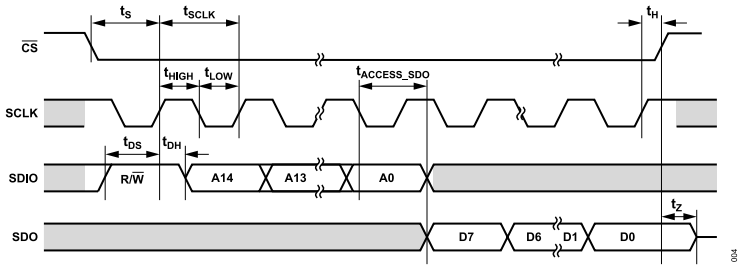

Figure 4. 4-Wire Read Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings

Parameter	Rating
VDD33_BS0, VDD33_BS1, VDD33_BS2, VDD33_BS3, VDD33_BS4, VDD33_BS5, VDD33_BS6, VDD33_BS7, VDD33_BS8, VDD33_BS9, VDD33_TDC, and VDD33_PLL to GND	−0.3 V to +3.6 V
VDD18_DIG, VDD18_TDC to GND	−0.3 V to +2.0 V
REFIN+, REFIN−	−0.675 V to VDD33_PLL + 0.675 V
REFIN+ to REFIN−	−1.35 V to +1.35 V
BSYNC0+, BSYNC0−, BSYNC1+, BSYNC1−, BSYNC2+, BSYNC2−, BSYNC3+, BSYNC3−, BSYNC4+, BSYNC4−, BSYNC5+, BSYNC5−, BSYNC6+, BSYNC6−, BSYNC7+, BSYNC7−, BSYNC8+, BSYNC8−, BSYNC9+, and BSYNC9− Inputs	−0.3 V to Maximum (+0.3 V, VDD_BSx − 0.8 V)
BSYNCx+ to BSYNCx− (x = 0, 1, …, 9)	−1.35 V to +1.35 V
Voltage on all other pins	−0.3 V to VDD33_PLL + 0.3 V
Temperature	
Operating Junction Range[1]	−40 °C to +125°C
Junction	150°C
Storage Range	−55 °C to +150°C
Peak[2]	260 °C

[1] Device is guaranteed to meet the specified performance limits over the full operating junction temperature range.

[2] Analog Devices, Inc., recommends that reflow profiles used in soldering RoHS-compliant devices conform to J-STD-020D.1 from JEDEC. Refer to JEDEC for the latest revision of this standard.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

TRANSISTOR COUNT

The transistor counts for the ADF4030 are 312642 (CMOS) and 7771 (bipolar).

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the junction to ambient thermal resistance measured in a natural convection JEDEC environment.

$\theta_{JC\text{-}TOP}$ and $\theta_{JC\text{-}BOTTOM}$ are the JEDEC thermal resistances of the junction-to-top of case and junction-to-bottom of case, respectively.

θ_{JB} is the junction-to-board JEDEC thermal resistance.

Ψ_{JT} is the junction-to-top of case JEDEC thermal characterization parameter.

Ψ_{JB} is the junction-to-board JEDEC thermal characterization parameter.

Table 4. Thermal Resistance

Package Type	θ_{JA}	$\theta_{JC\text{-}TOP}$	$\theta_{JC\text{-}BOTTOM}$	θ_{JB}	Ψ_{JT}	Ψ_{JB}	Unit
CC-48-10[1]	42.2	22.0	21.3	28.6	1.8	28.0	°C/W

[1] Test Condition: thermal impedance simulated values are based on use of a 6-layer PCB with the thermal impedance paddle soldered to a ground plane.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only. Human body model (HBM) per ANSI/ESDA/JEDEC JS-001. Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADF4030

Table 5. ADF4030, 48-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM	3500	2
CDM	1250	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

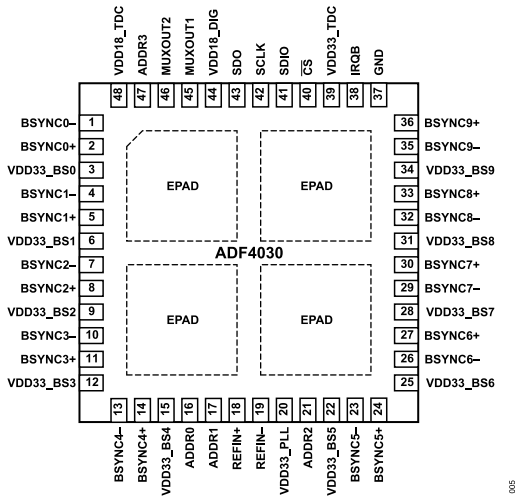

Figure 5. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Pin Name	Pin Type[1]	Description
1	BSYNC0–	I/O	Complementary Bidirectional Clock, Channel 0.
2	BSYNC0+	I/O	Normal Bidirectional Clock, Channel 0.
3	VDD33_BS0	Power	3.3 V Supply to BSYNC Channel 0.
4	BSYNC1–	I/O	Complementary Bidirectional Clock, Channel 1.
5	BSYNC1+	I/O	Normal Bidirectional Clock, Channel 1.
6	VDD33_BS1	Power	3.3 V Supply to BSYNC Channel 1.
7	BSYNC2–	I/O	Complementary Bidirectional Clock, Channel 2.
8	BSYNC2+	I/O	Normal Bidirectional Clock, Channel 2.
9	VDD33_BS2	Power	3.3 V Supply to BSYNC Channel 2.
10	BSYNC3–	I/O	Complementary Bidirectional Clock, Channel 3.
11	BSYNC3+	I/O	Normal Bidirectional Clock, Channel 3.
12	VDD33_BS3	Power	3.3 V Supply to BSYNC Channel 3.
13	BSYNC4–	I/O	Complementary Bidirectional Clock, Channel 4.
14	BSYNC4+	I/O	Normal Bidirectional Clock, Channel 4.
15	VDD33_BS4	Power	3.3 V Supply to BSYNC Channel 4.
16	ADDR0	I	Bit 0 of Serial Port Interface (SPI) Extended Address. Floating 1.8 V or 3.3 V CMOS input with no internal pull-up or pull-down resistors. Tie ADDR0 to GND, 1.8 V, or 3.3 V to define the Bit A[9] in the SPI instruction word (see Figure 48).
17	ADDR1	I	Bit 1 of SPI Extended Address. Floating 1.8 V or 3.3 V CMOS input with no internal pull-up or pull-down resistors. Tie ADDR1 to GND, 1.8 V, or 3.3 V to define the Bit A[10] in the SPI instruction word (see Figure 48).
18	REFIN+	I	Normal Reference Clock Input.
19	REFIN–	I	Complementary Reference Clock Input.
20	VDD33_PLL	Power	3.3 V Supply to PLL.
21	ADDR2	I	Bit 2 of SPI Extended Address. Floating 1.8 V or 3.3 V CMOS input with no internal pull-up or pull-down resistors. Tie ADDR2 to GND, 1.8 V, or 3.3 V to define the Bit A[11] in the SPI instruction word (see Figure 48).
22	VDD33_BS5	Power	3.3 V Supply to BSYNC Channel 5.
23	BSYNC5–	I/O	Complementary Bidirectional Clock, Channel 5.
24	BSYNC5+	I/O	Normal Bidirectional Clock, Channel 5.
25	VDD33_BS6	Power	3.3 V Supply to BSYNC Channel 6.
26	BSYNC6–	I/O	Complementary Bidirectional Clock, Channel 6.
27	BSYNC6+	I/O	Normal Bidirectional Clock, Channel 6.
28	VDD33_BS7	Power	3.3 V Supply to BSYNC Channel 7.
29	BSYNC7–	I/O	Complementary Bidirectional Clock, Channel 7.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions (Continued)

Pin No.	Pin Name	Pin Type[1]	Description
30	BSYNC7+	I/O	Normal bidirectional clock, Channel 7.
31	VDD33_BS8	Power	3.3 V Supply to BSYNC Channel 8.
32	BSYNC8–	I/O	Complementary Bidirectional Clock, Channel 8.
33	BSYNC8+	I/O	Normal Bidirectional clock, Channel 8.
34	VDD33_BS9	Power	3.3 V Supply to BSYNC Channel 9.
35	BSYNC9–	I/O	Complementary Bidirectional Clock, Channel 9.
36	BSYNC9+	I/O	Normal Bidirectional Clock, Channel 9.
37	GND	Power	Ground Connection.
38	IRQB	O	Interrupt Request. Programmable output mode and selectable internal interrupt source.
39	VDD33_TDC	Power	3.3 V Supply to Differential TDC.
40	$\overline{CS}$	I	Serial Port Chip Select. 1.8 V or 3.3 V compatible CMOS input.
41	SDIO	I/O	Serial Data Input/Output. 1.8 V or 3.3 V compatible CMOS input. 1.8 V or 3.3 V programmable serial CMOS output. Bidirectional for 3-wire SPI mode. Input only for 4-wire SPI mode.
42	SCLK	I	Serial Port Clock. 1.8 V or 3.3 V compatible CMOS input.
43	SDO	O	Optional Serial Data Output. 1.8 V or 3.3 V programmable serial CMOS output. High-z for 3-wire SPI mode. Output only for 4-wire SPI mode. When $\overline{CS}$ is deasserted, SDO returns to high impedance. Optionally, attach a resistor of >200 kΩ to prevent a floating output.
44	VDD18_DIG	Power	1.8 V Supply to Digital Core.
45	MUXOUT1	O	Access to Various Internal Test Points (programmable).
46	MUXOUT2	O	Access to Various Internal Test Points (programmable).
47	ADDR3	I	Bit 3 of SPI Extended Address. Floating 1.8 V or 3.3 V CMOS input with no internal pull-up or pull-down resistors. Tie ADDR3 to GND, 1.8 V, or 3.3 V to define the Bit A[12] in the SPI instruction word (see Figure 48).
48	VDD18_TDC	Power	1.8 V Supply to Differential TDC.
	EPAD	Power	Primary Ground Connection.

[1] I/O is input/output, I is input, and O is output.

TYPICAL PERFORMANCE CHARACTERISTICS

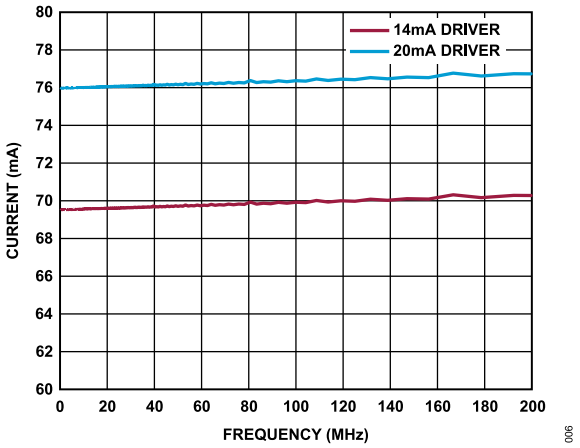

Figure 6. VDD33_Bx Current vs. Output Frequency, BSYNCx Channel Transmits Clock and BSYNCx Receiver Enabled

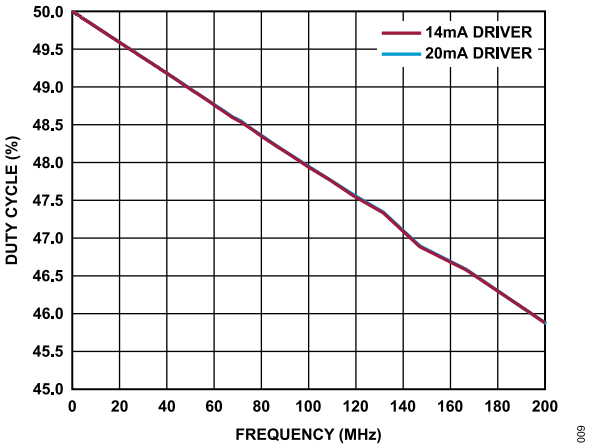

Figure 9. BSYNC Positive Duty Cycle vs. Output Frequency for Odd ODIV Values, BSYNC Channel Transmits Clock

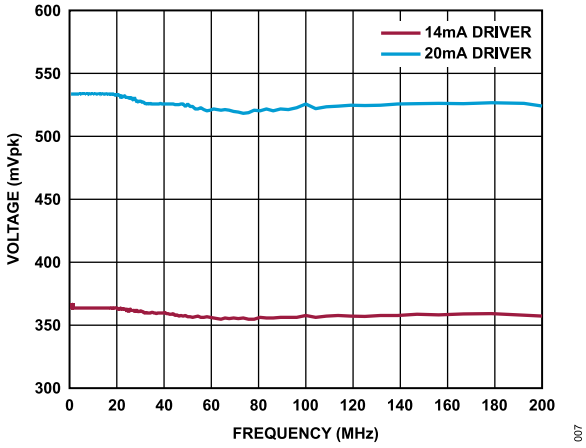

Figure 7. BSYNC Differential Voltage Swing vs. Output Frequency, BSYNC Channel Transmits Clock

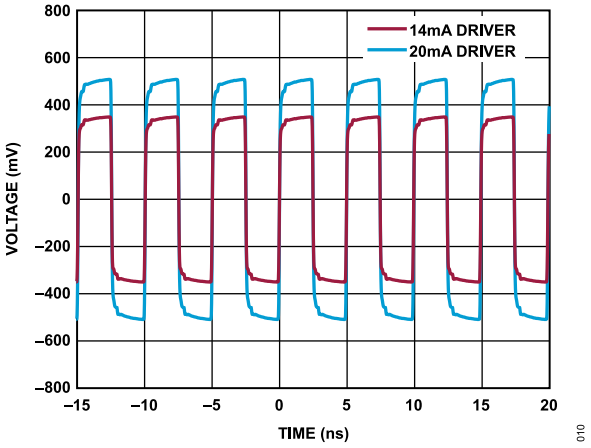

Figure 10. BSYNC Output Waveform, Differential, 200 MHz

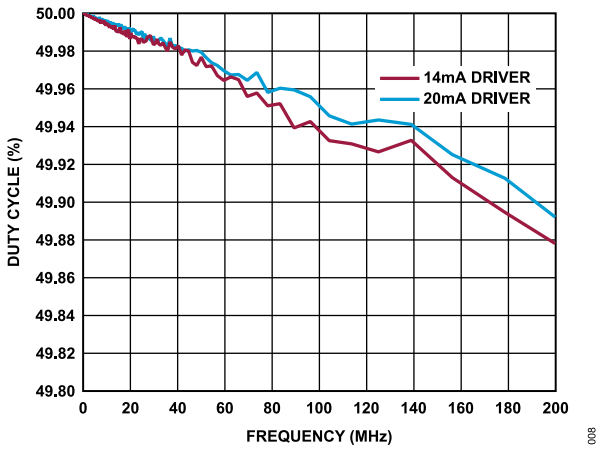

Figure 8. BSYNC Positive Duty Cycle vs. Output Frequency for Even ODIV Values, BSYNC Channel Transmits Clock

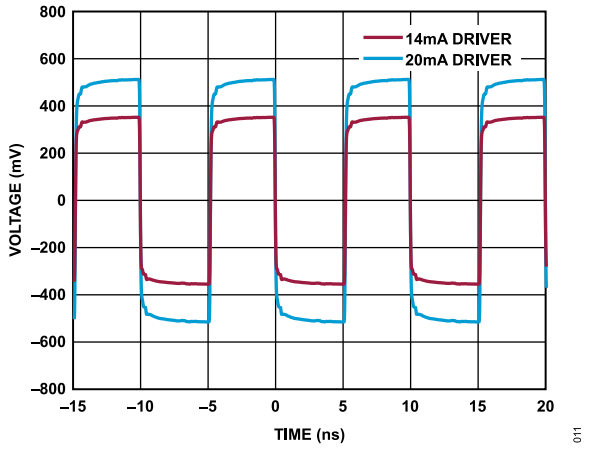

Figure 11. BSYNC Output Waveform, Differential, 100 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

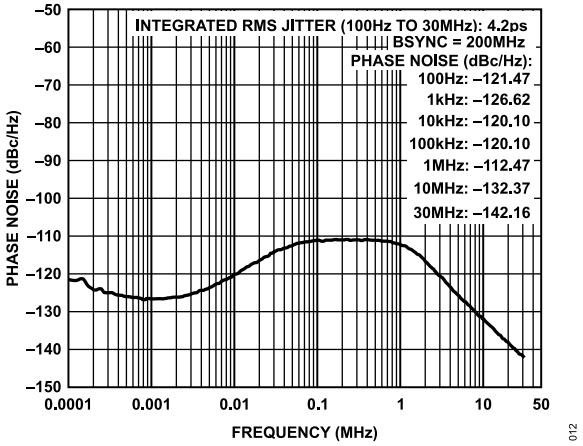

Figure 12. BSYNC Output Absolute Phase Noise, 200 MHz

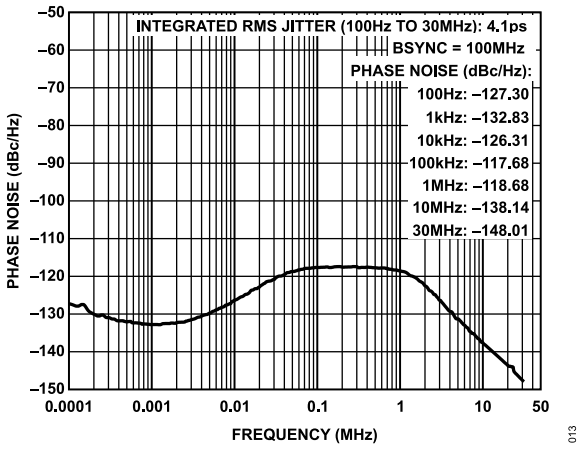

Figure 13. BSYNC Output Absolute Phase Noise, 100 MHz

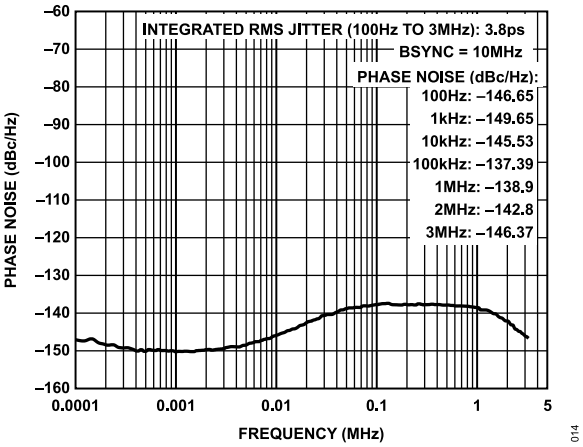

Figure 14. BSYNC Output Absolute Phase Noise, 10 MHz

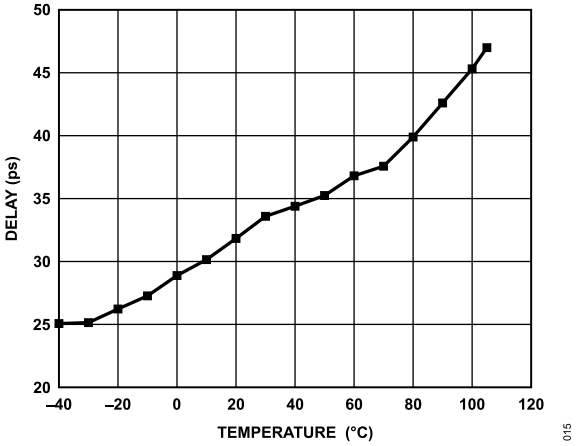

Figure 15. REFIN to BSYNC Propagation Delay over Temperature Range

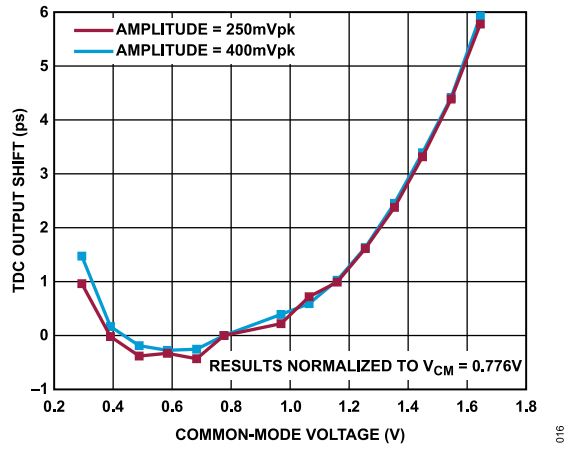

Figure 16. TDC Output Shift vs. Incoming BSYNC Common-Mode Voltage for Various Amplitudes

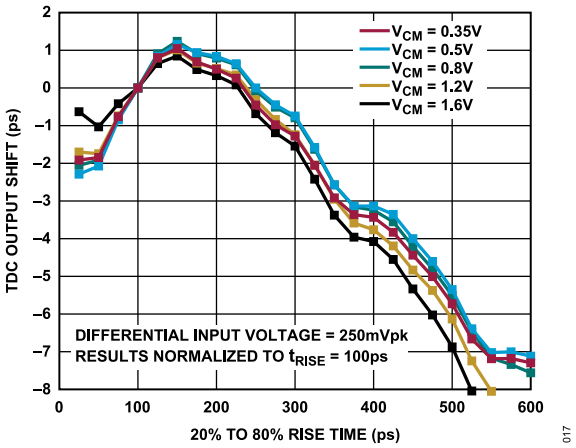

Figure 17. TDC Output Shift vs. Incoming BSYNC Time Rise for Various Common-Mode Voltages

DEVICE INITIALIZATION

Upon the initial power up of the ADF4030, the device undergoes an internal power-on reset (POR) sequence that forces the SPI registers to the default values and puts the device into a known initial state. Two other register resetting methods exist. The first is to set Bit 7 and Bit 0, SOFT_RESET, in Register 0x00 to 1 at any time (these bits clear automatically), which forces all SPI registers, except Register 0x00, to the default values. The second is to set Bit 0, SOFTRESET_CHIP, in Register 0xFF to 1 at any time (this bit clears automatically), which resets all SPI registers to their default values (equivalent to power cycling the device in terms of the register map). Note that writing to Register 0x00 is always considered a broadcast operation, and when SOFT_RESET bits are set to 1, all ADF4030 devices on the SPI bus are reset. See the SPI Broadcast Mode section for more details.

The recommended device initialization procedure after power up follows in Figure 18.

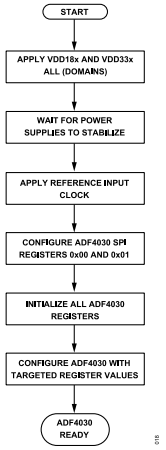

Figure 18. ADF4030 Programming Sequence After Power Up

After power up, apply the reference input clock. Without this clock, the PLL calibration procedure does not work. Then, configure the serial port using Register 0x00 and Register 0x01, which requires ADDR bits in the instruction word to be equal to 0000 (see the SPI Operation section). Using the SPI streaming mode, (0x01[7] cleared to 0, the default) with the address ascension set to decrement (0x00[5] = 0x00[2] = 0, the default), is recommended for the ADF4030 registers to be written in the shortest amount of time.

All the ADF4030 registers must then be written with their initial values, meaning all registers are written with zero values except the registers shown in Table 7. The registers in Table 7 are initialized with the values shown. Write the registers in the recommended streaming mode, including the zero valued registers, starting from Address 0x72 and ending with Address 0x10 (see the PLL section for the reasons behind this approach). If the streaming mode cannot be accommodated, initialize one register at a time starting from Address 0x72 and ending with Address 0x10.

In the targeted register values, ensure Bit 6, PLL_CAL_EN, Register 0x5A is set to 1. Then, configure the ADF4030 with the targeted register values following the approach as follows: with the SPI in streaming mode and the address ascension set to decrement, write all registers from Address 0x72 to Address 0x10. Or, initialize one register at a time, starting from Address 0x72 and ending with Address 0x10.

Table 7. Registers with Nonzero Values Initialized After Power Up

Address	Data
0x6A	0x0A
0x69	0x0A
0x66	0x80
0x64	0x1E
0x63	0x1E
0x62	0x4C
0x61	0x01
0x60	0x2B
0x5F	0x5D
0x5E	0x32
0x5D	0x10
0x5C	0x1E
0x5B	0xC9
0x5A	0x17
0x59	0x49
0x58	0x53
0x57	0x45
0x56	0x7D
0x55	0x01
0x54	0x90
0x53	0x19
0x52	0xE9
0x50	0xE9
0x4E	0xE9
0x4C	0xE9
0x4A	0xE9
0x48	0xE9
0x46	0xE9
0x44	0xE9
0x42	0xE9
0x40	0xE9
0x3C	0xFF
0x3B	0xFC
0x37	0x02
0x35	0x05
0x34	0x24
0x33	0x1D
0x32	0x1D
0x31	0x45
0x16	0x06
0x11	0x1F
0x10	0x1F

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In this document, register addresses use 8-bit hexadecimal notation (for example, Register 0x3F) even though the SPI communication pads this address with Bit 14, Bit 13, and Bit 8 that are always 0 and with Bits[12:9] that represent the state of ADDR3, ADDR2, ADDR1 and ADDR0 pins, respectively. See the SPI Instruction Word section for details.

DEVICE OVERVIEW

The block diagram in Figure 19 reveals further detail regarding the functionality of the ADF4030. The primary function of the ADF4030 is to deliver up to 10 independent output clock signals via BSYNC channels with 5 ps clock edge alignment (relative to the reference BSYNC). Any BSYNC channel may be designated as the reference BSYNC. The device pins associated with the reference BSYNC constitute a reference timing plane. The ADF4030 can achieve 5 ps clock edge alignment on any (or all) of the other active BSYNC channels relative to the reference BSYNC (assuming the other active BSYNC channels generate the same frequency as the reference BSYNC).

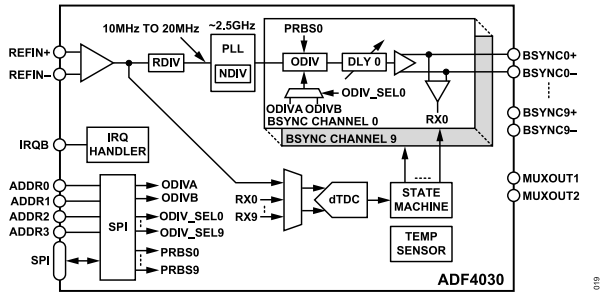

Figure 19. Detailed Block Diagram

As shown in Figure 19, the frequency of a BSYNC channel derives from an external frequency source applied at the REFIN input. The REFIN signal passes through a divider (RDIV) that drives the input of an integrated PLL. The value of RDIV (1 to 31) is user programmable via Register 0x57[4:0]. The PLL multiplies the divided REFIN signal via a feedback divider (NDIV) to produce a common frequency (f_{VCO}) that applies to the input to each of the BSYNC channels. The value of NDIV (8 to 255) is user programmable via Register 0x56[7:0]. The value of f_{VCO} depends on f_{REFIN}, RDIV, and NDIV per Equation 1.

$$f_{VCO} = \frac{f_{REFIN}}{RDIV} \times NDIV \quad (1)$$

where:
f_{VCO} must be in the range of 2.5 GHz ±5%.
f_{REFIN}/RDIV must be in the range of 10 MHz to 20 MHz.

Each BSYNC channel has an output divider (ODIV) that divides f_{VCO} to yield a desired BSYNC output frequency. Although each BSYNC channel has a dedicated output divider, the divide value for all BSYNC channels is constrained to one of two values, ODIVA (10 to 4095) or ODIVB (10 to 4095). The 12-bit ODIVA value is programmable via Register 0x54[3:0] and Register 0x53[7:0] (LSB). The 12-bit ODIVB value is programmable via Register 0x55[7:0] and Register 0x54[7:4] (LSB). The user selects which of the two values is in effect on a per BSYNC channel basis per Table 8 through bits ODIV_SELx. Register 0x3F[7] corresponds to ODIV_SEL0 in Figure 19.

Table 8. ODIV Selection

		ODIV_SELx	
BSYNCx	Address	Bit D7 = 0	Bit D7 = 1
0	0x3F	ODIVA	ODIVB
1	0x41	ODIVA	ODIVB
2	0x43	ODIVA	ODIVB
3	0x45	ODIVA	ODIVB
4	0x47	ODIVA	ODIVB
5	0x49	ODIVA	ODIVB
6	0x4B	ODIVA	ODIVB
7	0x4D	ODIVA	ODIVB
8	0x4F	ODIVA	ODIVB
9	0x51	ODIVA	ODIVB

The output frequency of a BSYNC channel is determined per Equation 2.

$$f_{BSYNC} = \frac{f_{REFIN}}{RDIV} \times \frac{NDIV}{ODIVx} \quad (2)$$

where ODIVx is either ODIVA or ODIVB dependant on the ODIV value selection per Table 8.

The ability to choose between two ODIV values is useful in applications requiring one or more BSYNC channels to generate an output frequency other than the frequency associated with ODIVA. For example, in applications that require some BSYNC channels to generate a frequency equal to f_{REFIN}, the user can choose ODIVB = NDIV/RDIV (under the constraint that NDIV/RDIV is an integer). This approach makes the ADF4030 act as a fanout buffer of REFIN clock on BSYNC channels using ODIVB.

After power up and device initialization, the state of the ODIV divider on each BSYNC channel is random. Each ODIV may have a different value, meaning the phase offset between BSYNC channels is random.

Note that the ADF4030 does not support alignment capability for ODIVB. The intended purpose of ODIVB is to provide an alternate BSYNC output frequency only, without regard to phase alignment, like fanning out the REFIN clock.

REFERENCE CLOCK INPUT (REFIN)

The typical use case for the ADF4030 is to generate multiple output clock signals (via the BSYNC channels) and to provide for high precision time alignment of those output clock signals as part of a synchronized clock system. Generation of the BSYNC output clocks requires the external application of a reference input clock signal via the REFIN pins. The REFIN pins connect to a differential receiver that is intended to receive a differential clock signal from a low voltage differential signaling (LVDS) or current-mode logic

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(CML) driver using AC coupling capacitors (C_1 and C_2) and a 100 Ω resistive termination (see Figure 20). Locate the resistor and coupling capacitors near the REFIN pins (at the far end of the transmission line originating from the external driver).

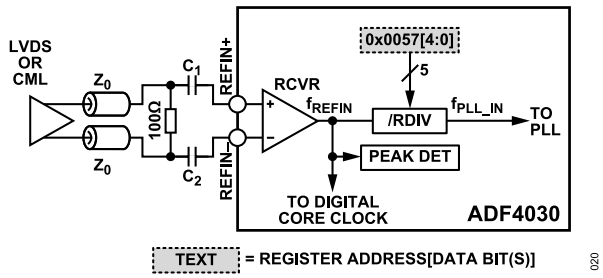

Figure 20. REFIN Diagram

If a single-ended clock source is used, drive only the upper transmission line in Figure 20. Use a 50 Ω resistor connected to GND as the resistor termination, and connect C_2 to ground as well (see Figure 21).

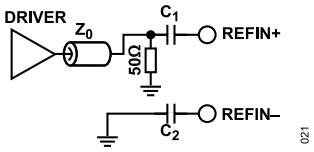

Figure 21. Reference Input Single-Ended Diagram

The output of the REFIN receiver drives a programmable divider. The value of Register 0x57[4:0] constitutes RDIV (a value of 0 is treated as if RDIV = 1). The reference divider ensures that the input frequency supplied to the PLL (f_{PLL_IN}) ranges from 10 MHz to 20 MHz, which is a requirement that must be met.

The ADF4030 has a peak detector that monitors the output signal level of the REFIN receiver. The status of the peak detector is available via Bit 6, REF_OK, in Register 0x8F. Logic 1 indicates the input signal level is sufficient for normal operation, while Logic 0 indicates the input signal is missing or the level is too low for reliable operation.

PLL

The PLL consists of a PFD, a charge pump, a loop filter, a VCO, and the feedback divider, NDIV. Some details of the PLL characteristics that have been discussed in the Device Overview section and are not discussed in this section.

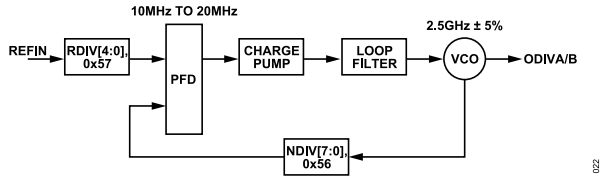

Figure 22. PLL Block Diagram

The charge pump currents are set through Bits[6:5], CP_I, in Register 0x57. Four choices are available from 360 µA to 630 µA. Initialize these, Bits[6:5], after power up at 10, making the pump current 540 µA.

To calibrate the VCO, first apply the reference input clock. Then, complete the following steps:

1. Set Bit 6, PLL_CAL_EN, in Register 0x5A to 1 to enable automatic VCO band calibration.
2. Set Bits[4:0], RDIV, in Register 0x57 to initialize the RDIV reference clock divider.
3. Set Bits[7:0], NDIV, in Register 0x56 to initialize the NDIV feedback divider.

Initializing Register 0x56 starts the VCO calibration. This is why in the Device Initialization section, the recommendation is to write registers in descending order, from Address 0x72 to Address 0x10. The PLL calibration is started simply by initializing the ADF4030 registers in the descending order.

After initiating the calibration, monitor Bit 0, CAL_BUSY, in Register 0xBA. It is equal to 1 for the duration of the calibration. Then, once CAL_BUSY becomes 0 to indicate that the calibration has ended, monitor Bit 0, PLL_LD, in Register 0x90. It becomes 1 when the PLL lock detector indicates the PLL is locked. After the PLL locks, the BSYNC related delay adjustments can be started. See the Applications Information section for details.

DIGITAL CORE CLOCK

The ADF4030 relies on a digital core clock as shown in Figure 23. The digital core clock provides timing to the following internal functions:

- TDC state machine (see the TDC Core section)
- Temperature sensor (see the Temperature Measurement System section)

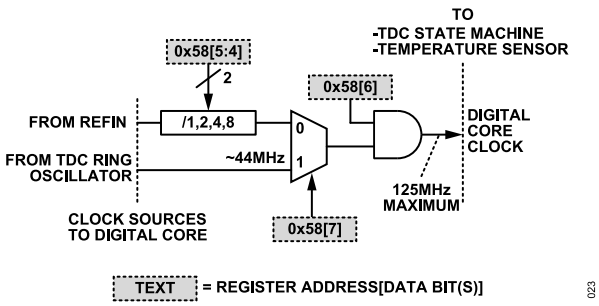

Figure 23. Digital Core Clock Diagram

Enable the digital core clock by setting Bit 6, EN_DIGCLK, in Register 0x58 to 1. Note that when EN_DIGCLK is cleared to 0, no core clock exists, meaning the functions that rely on the core clock are inactive.

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The following two options are available as a frequency source for the digital core clock, selected via Bit 7, SEL_DIGCLK, in Register 0x58.

- The clock signal originating at the REFIN pins (SEL_DIGCLK = 0, default)
- The free running ring oscillator in the TDC (SEL_DIGCLK = 1)

For a typical application that uses the REFIN clock to generate BSYNC output clock signals (via the PLL), the REFIN clock is the preferred frequency source for the digital core clock, because the frequency of the REFIN clock is known and is presumed to be reasonably precise and stable over temperature. Precise knowledge of the digital core clock frequency translates to an accurate time base for those functions that rely on the digital core clock. When the REFIN frequency is greater than 125 MHz, Bits[5:4], CORE_CLK_DIV, in Register 0x58 must be programmed to divide the REFIN frequency by $2^{CORE\_CLK\_DIV}$ to less than 125 MHz.

For applications that use the ADF4030 as a stand alone TDC (that is, applications that do not generate BSYNC clocks), the presence of a REFIN clock is optional. Therefore, to ensure the presence of a digital core clock, the ADF4030 allows a TDC ring oscillator to be selected as the clock source for the digital core clock (≈ 44 MHz). The ring oscillator frequency is typically not as well controlled as a REFIN frequency source, hence the approximate value of 44 MHz.

Because the source of the digital core clock is selectable via Bit SEL_DIGCLK, the frequency of the digital core clock ($f_{CORECLK}$) depends on the state of SEL_DIGCLK. As such, $f_{CORECLK}$ has two possible values per Equation 3.

$$f_{CORECLK} = \begin{cases} \frac{f_{REFIN}}{2^{CORE\ CLK\ DIV}}, \text{for SEL\_DIGCLK=0} \\ \frac{f_{RO}}{16}, \text{for SEL\_DIGCLK=1} \end{cases} \quad (3)$$

where:
f_{RO} is the TDC ring oscillator frequency (≈ 700 MHz).
f_{REFIN} is the frequency of the clock applied to the REFIN pins.
CORE_CLK_DIV is 0, 1, 2, or 3.

The digital core clock period ($t_{CORECLK}$), per Equation 4, constitutes the internal time base for the TDC state machine and the temperature sensor.

$$t_{CORECLK} = \frac{1}{f_{CORECLK}} \quad (4)$$

CMOS OUTPUT PIN LOGIC HIGH CONTROL

The CMOS logic pins of the ADF4030 are typically powered by a 1.8 V source. Therefore, pins associated with CMOS logic outputs have a logic high level associated with a 1.8 V supply. However, the output pins allow for the selection between a logic high source of 1.8 V or 3.3 V. The pins listed below are those with selectable output high logic levels.

- SDO
- SDIO
- IRQB
- MUXOUT1
- MUXOUT2

When Bit 7, CMOS_OV, in Register 0x5C is cleared to 0 (default), the pins use the 1.8 V supply as a logic high source. Conversely, when CMOS_OV bit is set to 1, the pins use the 3.3 V supply as a logic high source.

The $\overline{CS}$ and SCLK SPI input pins accept 1.8 V and 3.3 V CMOS compatible signals, independent of the state of CMOS_OV bit. The same is true for the SDIO pin when the SDIO acts as an input. When SDIO acts as an output, CMOS_OV pin determines the logic of the output signal. This allows a controller to manage the ADF4030 SPI communication using any 1.8 V or 3.3 V CMOS signals. See the SPI Operation section for more details.

BSYNC CHANNELS

The ADF4030 has 10 independent BSYNC channels. Figure 24 is a template for all BSYNC channels.

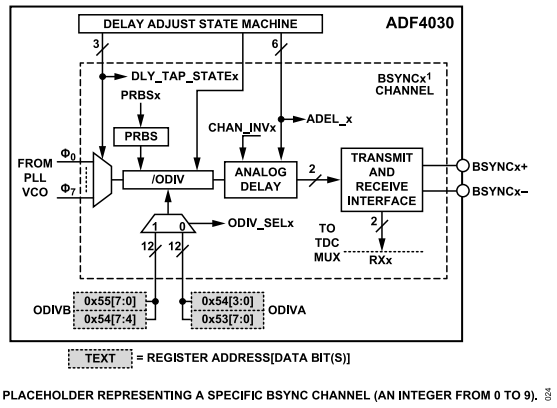

Figure 24. BSYNC Channel Diagram

Each BSYNC channel is composed of the following elements:

- A programmable ODIV divider
- An adjustable analog delay stage
- A transmit and receive interface to a BSYNC pin pair

The purpose of the ODIV divider is twofold. First, the ODIV divider reduces the PLL VCO frequency for use by the transmit section of the BSYNC channel (see the Device Overview section for details). Second, the ODIV divider of each BSYNC channel has access to the 8-phase output of the PLL VCO. Each BSYNC channel can independently select a specific phase output from the VCO that provides the ability to shift the BSYNC output signal in steps of ~50 ps ($(1/f_{VCO})/8$, where f_{VCO} ≈ 2.5 GHz). The 50 ps step capability constitutes the intermediate resolution portion of the time offset capability of the ADF4030 that allows for time alignment between BSYNC channels. The ODIV divider can provide a gapped clock

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output via the PRBS block (see the Gapped Periodic BSYNC Clock section).

The analog delay block provides an adjustable delay in ~1.4 ps steps by means of a 6-bit control word (offering a range between 0 ps and ~88 ps). The 1.4 ps step capability constitutes the fine resolution portion of the time offset capability of the ADF4030 that allows for time alignment between BSYNC channels. The analog delay block allows the user to invert the transmit signal via a control bit, CHAN_INVx (CHAN_INVx = 1 inverts the transmit signal). The 10 independent CHAN_INVx control bits reside in Register 0x15[5:0], CHAN_INV9 to CHAN_INV4, and Register 0x14[7:4], CHAN_INV3 to CHAN_INV0.

The transmit and receive interface provides each BSYNC channel with the ability to transmit and/or receive clock signals over a BSYNC pin pair (see the Transmit and Receive Interface section).

Transmit and Receive Interface

The PLL, ODIV divider, and analog delay elements of a BSYNC channel provide a transmit clock signal at the output of the analog delay block. Figure 25 is a template for all the BSYNC channels.

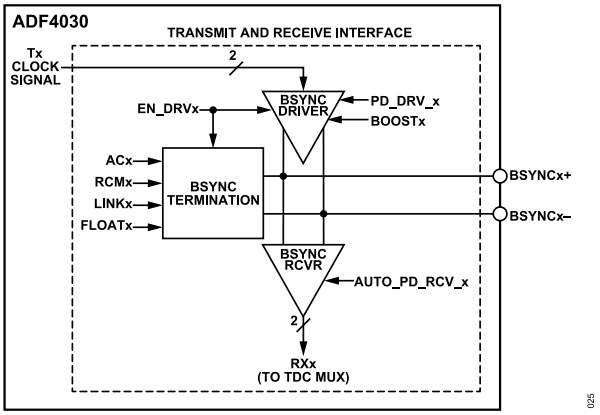

Figure 25. Transmit and Receive Interface Diagram

A current steering circuit delivers the transmit clock signal to the BSYNC pin pair. A BSYNC receiver is attached to the BSYNC pins to transfer the signal on the BSYNC pins to RXx that routes to the TDC multiplexer (mux). The termination block allows for configuration of the BSYNC pin pair to accommodate various signal loading and biasing conditions.

The BSYNC driver and BSYNC receiver can be powered down via a combination of bits within the register map (see the Programmable Power Down Options section for details).

The components within the BSYNC termination block are shared by the BSYNC driver and BSYNC receiver. Because the transmit and receive interface can be configured to transmit only, receive only, or transmit and receive simultaneously, the BSYNC termination block must adapt accordingly. Hence, the EN_DRVx input to the BSYNC termination block (see the BSYNC Terminations section for details).

EN_DRVx is a bit that enables the output of the driver and also controls the behavior of the BSYNC driver and BSYNC terminations. There are 10 independent EN_DRVx control bits that reside in Bits[1:0], EN_DRV9 and EN_DRV8, of Register 0x13 and Bits[7:0], EN_DRV7 to EN_DRV0, of Register 0x12.

BSYNC Driver

Each of the 10 BSYNC channels has a dedicated output driver stage (see Figure 26). Figure 26 is a template for all 10 BSYNC drivers.

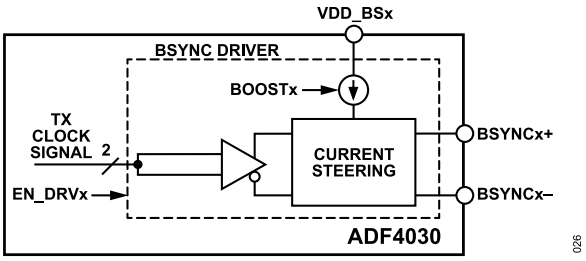

Figure 26. BSYNC Driver Diagram

The BSYNC driver receives the transmit (TX) clock signal from the BSYNC channel analog delay. The transmit clock signal feeds a differential amplifier that drives a current steering circuit into the BSYNCx pin pair.

The BSYNC drivers are enabled on a per channel basis via an EN_DRVx control bit (see the Transmit and Receive Interface section). EN_DRVx = 0 by default. Therefore, in order to actively drive the BSYNC pins, set EN_DRVx = 1.

The current source that supplies the current steering circuit has two programmable values, selectable on a per channel basis via the BOOSTx control bit. When BOOSTx = 0 or 1, the source current is 14 mA or 20 mA, respectively. The 10 BOOSTx bits reside in Bit 6 of the odd register addresses from 0x3F to 0x51.

BSYNC Receiver

Each BSYNC channel has a dedicated BSYNC receiver block (see Figure 27). Figure 27 is a template for all BSYNC channels.

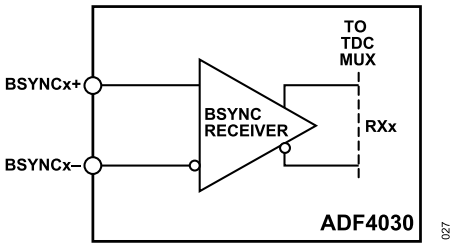

Figure 27. BSYNC Receiver Diagram

The input to the BSYNC receiver permanently connects to the BSYNC pins. The output of the BSYNC receiver routes to the TDC mux. Although the BSYNC receiver remains physically connected

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to the BSYNC pins, the receiver can be powered down (see the Programmable Power Down Options section) to save power.

BSYNC Terminations

The BSYNC terminations block provides the components necessary to terminate the BSYNC pins for various transmit and receive configurations. Figure 28 is a template for all 10 BSYNC terminations blocks.

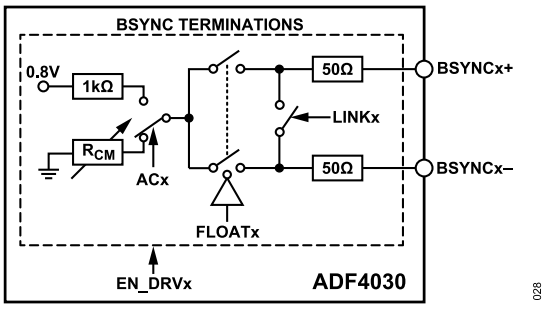

Figure 28. BSYNC Terminations Diagram

Because the BSYNC terminations block provides both transmit and receive terminations using shared hardware, the resistor (R_{CM}) and the switches depend on the state of the EN_DRVx control bit (see the Transmit and Receive Interface section).

Regarding the FLOATx and LINKx controls, when the FLOATx control = 0, the FLOATx switches are closed and when the FLOATx control = 1 the FLOATx switches are open. When the LINKx control = 0, the LINKx switch is open, and when the LINKx control = 1, the LINKx switch is closed.

The BSYNC channels are bidirectional interfaces, so switching a BSYNC channel between transmit and receive modes may be necessary. Furthermore, the required termination while transmitting may not be the same as the required termination for receiving only (that is, when not transmitting but receiving an external signal). As such, the FLOATx and LINKx controls depend on whether the BSYNC channel is in transmit mode or in receive only mode. To accommodate the differentiation between transmit and receive terminations, the register map supports a pair of float bits, FLOAT_TXx and FLOAT_RXx, and a pair of LINKx bits, LINK_TXx and LINK_RXx.

The ACx control derives from the EN_DRVx bit and the AC_COUPLEDx bit. The AC_COUPLEDx bit is only meaningful when ENDRVx = 0.

When ENDRVx = 1, the switch associated with the ACx control is in the position shown in Figure 28, regardless of the state of the AC COUPLEDx bit.

The FLOAT_RXx, FLOAT_TXx, LINK_RXx, LINK_TXx, and AC_COUPLEDx bits reside in Bits[5:1] of the even registers addresses from 0x40 to 0x52.

Transmit Configurations

The various transmit configurations in Figure 29 depend on the FLOAT_TXx bits and LINK_TXx bits per Table 9, under the assumption that EN_DRVx = 1.

Table 9. Transmit Configurations

FLOAT_TXx	LINK_TXx	Transmit Configuration	Required Terminations Outside ADF4030	Required Terminations at Receiver
0	0	Voltage driver (default)	None	100 Ω
1	0	Current driver (unterminated)	100 Ω	50 Ω to ground
1	1	Current driver (terminated)	None	50 Ω to ground

When FLOAT_TXx = 0, the LINK_TXx may be either 0 or 1. Use LINK_TXx default value of 0 for simplicity. The BSYNC transmit configuration is voltage driver.

When FLOAT_TXx = 1 and LINK_TXx = 0, the BSYNC transmit configuration is current driver, unterminated. The configuration requires an external termination, so use the current driver terminated option (FLOAT_TXx = 1 and LINK_TXx = 1) that has the termination available internally.

The voltage driver mode provides inside the ADF4030 a 100 Ω differential termination across the BSYNC pins with a programmable R_{CM} resistor connected between ground and the midpoint of the differential termination. The R_{CM} resistor establishes the common-mode voltage (V_{CM}) of the BSYNC output signal. The user programs the value of the R_{CM} resistor via RCMx (see Figure 26), a 6-bit code from 0 to 63. The 10 RCMx values (one per BSYNC channel) reside in the odd register addresses from 0x3F to 0x51. The value of RCMx relates to the value of the R_{CM} resistor per Equation 5 .

$$R_{CM} = \frac{700}{73.5 - RCMx} \quad \Omega \tag{5}$$

When the BSYNCx pins connect to an external load through DC blocking capacitors or the external load is purely differential (that is, no common-mode load), the DC current delivered by the BSYNC driver only flows through the termination shown for the BSYNC differential voltage driver configuration as shown in Figure 29. Therefore, the BSYNC driver produces a V_{CM} that relates to R_{CM} per Equation 6.

$$V_{CM} = I_{DRV} \times (26.5\ \Omega + R_{CM}) \tag{6}$$

where:
I_{DRV} is the BSYNCx driver current (14 mA or 20 mA per the BSYNC Driver section).
R_{CM} is per Equation 5.

Note that Equation 6 common-mode is not valid when the BSYNCx pins are DC-coupled to an external grounded load because the load diverts DC current from the internal termination. The recom-

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mendation is to use a differential 100 Ω termination at the receiver in DC-coupled connections. See Figure 30. In AC-coupled connections, make sure the receiver internally generates a common-mode voltage and has differential 100 Ω termination. See Figure 31 and Figure 35.

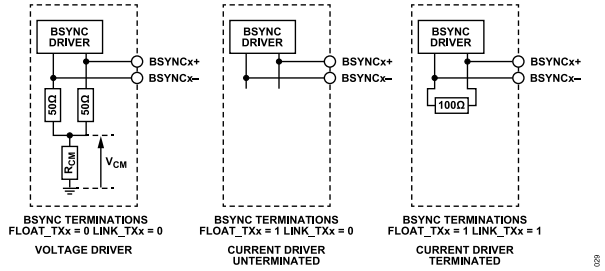

Figure 29. BSYNC Transmit Configurations Diagram

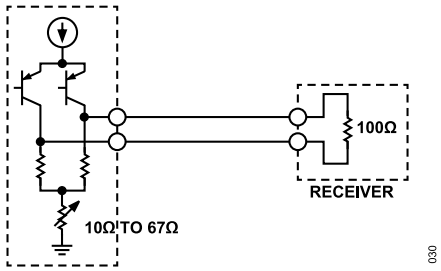

Figure 30. Differential Voltage Driver, DC-Coupled, 100 Ω Termination at Receiver

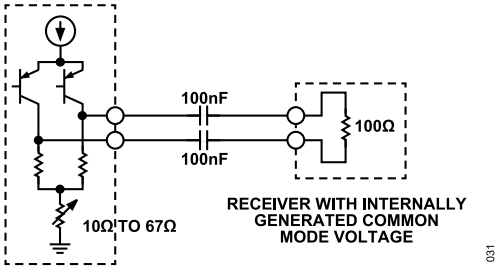

Figure 31. Differential Voltage Driver, AC-Coupled, 100 Ω Termination at Receiver

The current driver terminated mode provides an internal 100 Ω differential load to establish the signal level, but the mode relies on DC coupling the BSYNC pins to an external resistive path to ground to establish the common-mode voltage. See Figure 32. If an AC-coupled approach is necessary, configure the ADF4030 BSYNC transmitter in voltage driver mode, as presented in Figure 31.

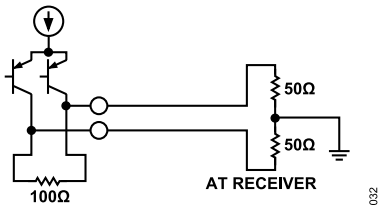

Figure 32. Differential Current Driver, Terminated, DC-Coupled 50 Ω to Ground Terminations at Receiver

Receive Configurations

The various receive configurations in Figure 33 depend on the state of the FLOAT_RXx, LINK_RXx, and AC_COUPLEDx bits that determine the BSYNC receive configuration per Table 10. The configuration external termination requiring FLOAT_RXx = 1, LINK_RXx = 0, and AC_COUPLEDx = 0 is not recommended. Use the following configuration because it requires no external termination: internal 100 Ω FLOAT_RXx = 1, LINK_RXx = 1, and AC_COUPLEDx = 0.

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Table 10. Receive Configurations

FLOAT_RXx	LINK_RXx	AC_COUPLEDx	Receive Configuration	Remarks
1	1	0	Internal 100 Ω (default)	Use for incoming DC-coupled clocks
1	0	0	External termination required	Not recommended
1	x	1	AC-coupled termination	Place AC coupling capacitors outside ADF4030
0	x	0	Grounded common mode	Supports incoming DC-coupled high speed current steering logic (HCSL) clocks
0	x	1	Not valid	

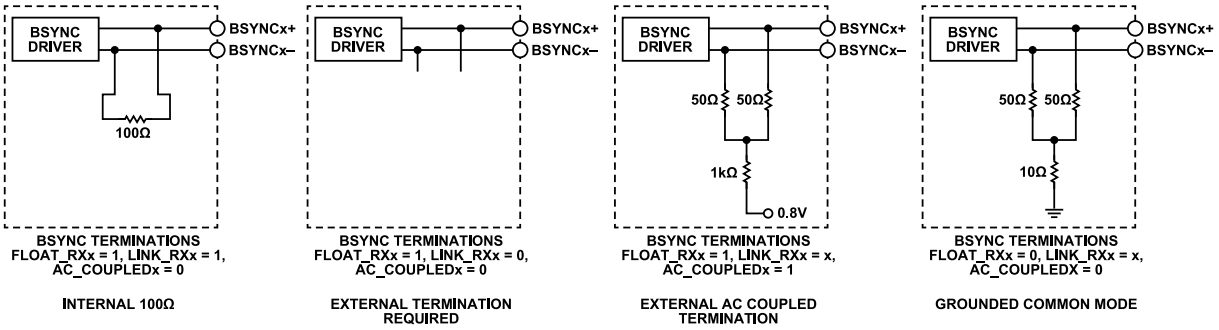

Figure 33. BSYNC Receive Configurations Diagram

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Termination Examples

This section presents several recommended schematics when the ADF4030 BSYNC channels are interfaced with any of the following:

- BSYNC channels of another ADF4030 (Figure 34 and Figure 35)
- The AD9084/AD9088 SYSREF pins (Figure 36 and Figure 37)
- An LVDS receiver (Figure 38 and Figure 39)
- Instruments that have 50 Ω and 1 MΩ input impedance (Figure 40 and Figure 41)

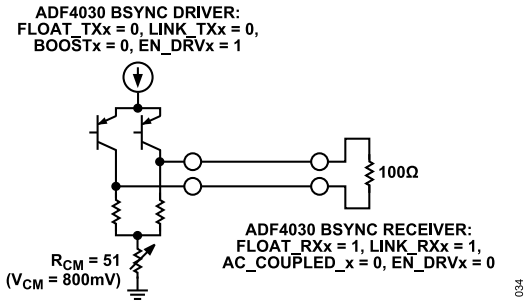

Figure 34. ADF4030 to ADF4030 DC-Coupled Connection

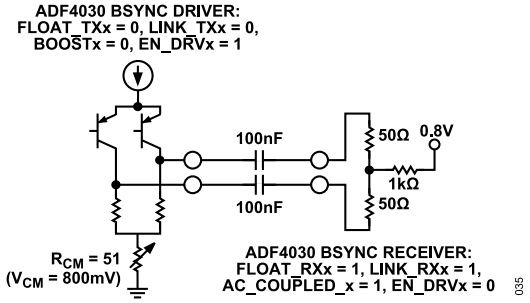

Figure 35. ADF4030 to ADF4030 AC-Coupled Connection

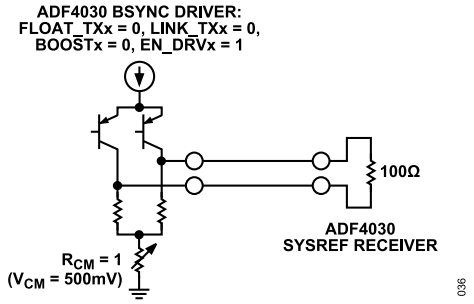

Figure 36. ADF4030 BSYNC to AD9084/AD9088 SYSREF Connection

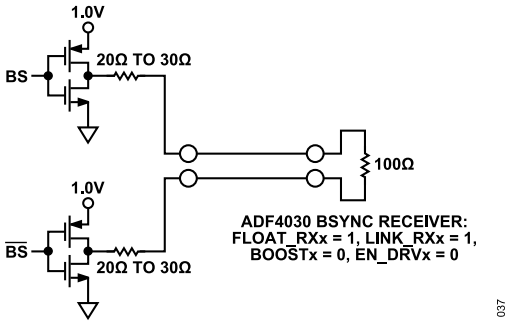

Figure 37. AD9084/AD9088 SYSREF to ADF4030 BSYNC Connection

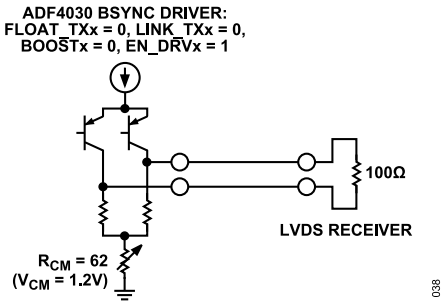

Figure 38. ADF4030 BSYNC to LVDS Receiver Connection

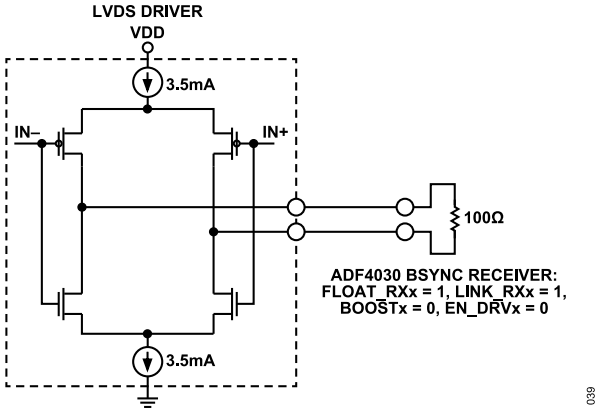

Figure 39. LVDS Driver to ADF4030 BSYNC Receiver Connection

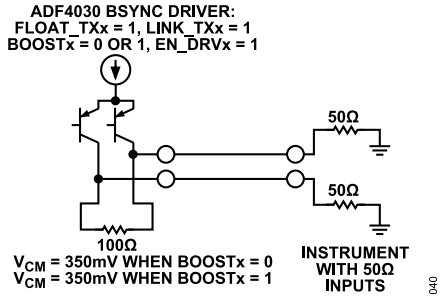

Figure 40. ADF4030 BSYNC Driver to 50 Ω Instrument Connection

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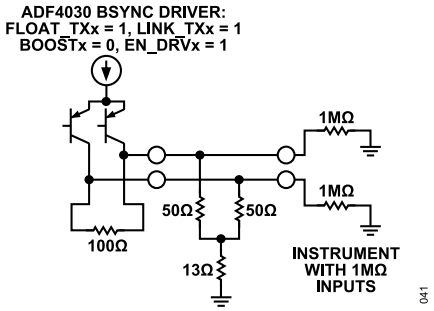

Figure 41. ADF4030 Driver to 1 MΩ Instrument Connection

Gapped Periodic BSYNC Clock

Each of the 10 BSYNC channels has a dedicated PRBS generator that enables the ODIV divider to output a gapped periodic clock (GPC) signal. The PRBS generator produces a pseudorandom sequence of ones and zeros at the same rate as the ODIV divider output clock signal. When the PRBS state is one, the ODIV divider output clock pulse for that period appears in the GPC signal. Conversely, when the PRBS state is zero, the GPC signal is zero for that period of the ODIV divider (that is, the GPC signal exhibits a one period gap resulting from the absence of a normal output pulse from the ODIV divider).

The GPC operation can be enabled independently on a per channel basis via the 10 PRBSx bits. The PRBSx bits reside in Register 0x14[3:0] and Register 0x13[7:2], where PRBSx = 1 means GPC operation is in effect on the associated BSYNC channel.

A GPC spreads out the spectral content of the underlying BSYNC frequency (f_{BSYNC}) that would normally exhibit frequency spurs at harmonics of the BSYNC frequency (that is, at $n \times f_{BSYNC}$, where n is an integer). Instead, the harmonic spurs are transformed into broadened spectral humps with reduced amplitude. Each of the 10 PRBS generators rely on a 17-bit linear feedback shift register that yields a pseudorandom sequence length of $2^{17} - 1$ (that is, 131,071 cycles of f_{BSYNC}).

Each of the 10 PRBS generators has a unique seed value that causes all 10 PRBS sequences to be offset from one another in time. Assuming all BSYNC channels assigned for GPC operation have the associated PRBS generators enabled at the same time (via the aforementioned register bits), the unique seed values ensure against any two BSYNC channels generating the same PRBS sequence simultaneously.

The PRBS setting should be consistent (on or off) during the alignment procedure, independent of using the BSYNC channel to transmit or receive clocks.

DIFFERENTIAL TIME-TO-DIGITAL CONVERTER (DTDC)

TDC Core

A differential time-to-digital converter (dTDC) is the core component that enables the high precision time alignment capability of the ADF4030. In this document, dTDC and TDC are used interchangeably for convenience. The TDC has two clock inputs and measures the difference in time between the clock edges arriving at the two inputs, source clock (SRC) and target clock (TGT), in Figure 42.

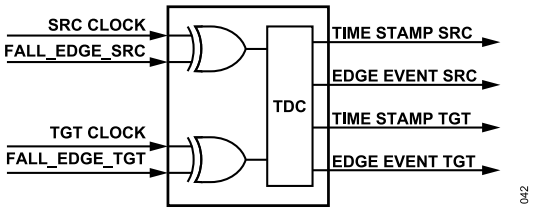

Figure 42. TDC Core Diagram

The TDC monitors the edges of the SRC and TGT clocks, identifies the clock edges, and associates time stamps to both positive and negative edges by simultaneously sampling both clocks. If a gapped periodic clock is input to the TDC, always set it as the TGT clock and use a nongapped periodic clock as the SRC clock. Never provide a gapped periodic clock as the SRC clock.

It may be useful to observe an inverted version of the input signal to the TDC. Signal inversion is done via the FALL_EDGE_SRC and FALL_EDGE_TGT Bits[7:6] in the Register 0x15 (see the TDC Input Clock Edge Selection section), giving the user independent control of the edge inversion for the SRC and/or TGT input clocks.

TDC Postprocessor

The TDC postprocessor block captures the source (SRC) and target (TGT) edge events and the associated time stamps as the edge events are output by the TDC (Figure 43). The postprocessor block has the following four functions:

- Captures the difference in edge timing between the SRC and TGT clocks to ascertain the time difference or synchronization, known as TIMEDIFF sample. The edge polarity (rising or falling) of each input is controlled by respectively Bits[7:6], FALL_EDGE_SRC and FALL_EDGE_TGT, in Register 0x15.
- Captures the time difference between successive edges of the SRC to measure the period. The SRC clock edge produces a period sample.
- Averages a large number (AVG) of the individual TIMEDIFF samples and period samples to suppress the quantization noise to a level that supports precision time alignment on a scale of picoseconds. See the TDC Time Stamp Averaging section for more details.
- After accumulating an AVG number of samples, the postprocessor calculates the phase difference between the SRC and TGT

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clock by dividing the average TIMEDIFF sample by the average period sample.

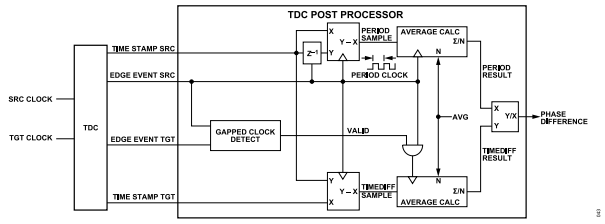

Figure 43. TDC Postprocessor Diagram

In order for the samples to be meaningful, the frequency of the SRC and TGT clocks must be identical. Otherwise, the edges of the two clocks drift apart over time, causing the sync sample values to diverge.

TDC Time Stamp Averaging

The averaging of many TDC time stamps enables the ADF4030 to resolve differential edge timing to below 1 ps, even though the measurement uncertainty associated with the instantaneous TDC time stamps is around $t_{TDC} \approx 86$ ps.

Averaging a number (AVG) of measurement samples yields the measurement uncertainty (σ_{MEAS}) associated with an averaged TDC measurement as defined in the following equation:

$$\sigma_{MEAS} = \frac{t_{TDC}}{\sqrt{AVG}} \quad (7)$$

The user sets the value of AVG via a 4-bit integer (AVGEXP) in Register 0x16[3:0]. The relationship between AVGEXP and AVG is given by Equation 8.

$$AVG = 64 \times 2^{AVGEXP} \quad (8)$$

A summary of the relationship between AVGEXP, AVG, and σ_{MEAS} is presented in Table 11.

Table 11. TDC Measurement Averaging

		σ_{MEAS} (ps rms)[1]	
AVGEXP	AVG	Typ	Max
0	64	Not supported	Not supported
1	128	Not supported	Not supported
2	256	Not supported	Not supported
3	512	3.789	6.031
4	1024	2.679	4.264
5	2048	1.894	3.015
6	4096	1.340	2.132
7	8192	0.947	1.508
8	16384	0.670	1.066
9	32768	0.474	0.754
10	65536	0.335	0.533
11	131072	0.237	0.377
12	262144	0.167	0.267
13	524288	0.118	0.188
14[2]	1048576	0.084	0.133
15[3]	2097152	0.059	0.094

[1] The tabulated values of σ_{MEAS} are based on t_{TDC} = 86 ps, which varies with temperature.

[2] AVGEXP = 14 requires $f_{BSYNC} \geq 1$ MHz for gapped periodic clocks.

[3] AVGEXP = 15 requires $f_{BSYNC} \geq 1$ MHz for nongapped periodic clocks and $f_{BSYNC} \geq 2$ MHz for gapped periodic clocks.

In Table 11, the σ_{MEAS} column is the statistical spread of repeated measurements. For example, with AVGEXP = 10, the TDC exhibits a 1σ measurement error probability of ±335 fs rms. Table 11 serves as a guide to the theoretical limits of a TDC measurement rather than a performance specification. Arbitrarily choosing AVGEXP = 15 to obtain σ_{MEAS} = 59 fs rms only means that the TDC exhibits a 1σ measurement repeatability of 59 fs rms given ideal input signals. For example, a real-world measurement may include an accuracy error of 3 ps, in which case choosing AVGEXP = 12 (σ_{MEAS} = 0.167 ps rms) may be sufficient for making the measurement.

The presence of cycle-to-cycle jitter on the TDC input signals may increase the value of σ_{MEAS}. The averaging applied by the TDC postprocessor suppresses random cycle-to-cycle jitter in like manner to the TDC quantization noise suppression. Therefore, cycle-to-cycle jitter with an RMS magnitude equal to 86 ps increases σ_{MEAS} by a factor of $\sqrt{2}$.

In the presence of a gapped clock (see the Gapped Periodic BSYNC Clock section) the TDC postprocessor must modify the averaging process. The gapped clock detect block in Figure 43 looks for a divergence in the number of rising edge events of the SRC clock relative to the TGT clock. The TIMEDIFF samples coincide with the rising edges of the gapped clock (which occur, on average, at half the rate of the period clock). In order to average the number of samples given in Table 11 when a gapped clock is present, the time required to complete the measurement doubles relative to the nongapped clock case.

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Because the presence of a gapped clock signal affects how the TDC postprocessor calculates phase error (refer to Figure 43), the user must ensure that the processor averages a sufficient number of time stamp samples to guarantee a valid phase error result. Therefore, when a TDC measurement involves a gapped clock signal, the value of AVGEXP (see Equation 8) must be programmed with a value of 6 or more. Additionally, a gapped periodic clock degrades the σ_{MEAS}, especially for $f_{BSYNC} \leq 80$ MHz.

TDC Results

The TDC postprocessor divides the TIMEDIFF result by the period result that constitutes the phase difference as a fraction of a unit interval (UI), where 1 UI represents the period of a clock signal. In the case of the TDC, 1 UI is the $1/f_{BSYNC}$ period of the controlling clock signal (see the TDC Input Clock Signal Assignment section).

The TDC postprocessor reports the phase difference as ±0.5 UI (rather than 0 UI to 1 UI). The ADF4030 stores TDC_RSLT_UI, the phase difference result as a signed 24-bit number (twos complement), in Register 0x75, Register 0x74, and Register 0x73. The least significant bit of the result (Register 0x73[0]) carries a weight of 2^{-24} UI. Therefore, the phase difference result covers a range of −0.5 UI to just below +0.5 UI with a resolution of 2^{-24} UI (or −180° to just below +180° with a resolution of 21.46 µ°).

The expression that calculates the measured time difference expressed in seconds is found via either of the following equations:

$$Time\ Difference = \frac{TDC\_RSLT\_UI}{2^{24}} \times \frac{1}{f_{BSYNC}} \quad (9)$$

If $0 \leq TDC\_RSLT\_UI \leq 2^{23} - 1$.

$$Time\ Difference = \left(\frac{TDC\_RSLT\_UI}{2^{24}} - 1\right) \times \frac{1}{f_{BSYNC}} \quad (10)$$

If $2^{23} \leq TDC\_RSLT\_UI < 2^{24}$.

The polarity of the TDC result indicates the relationship between the source and target clocks (see the TDC Input Clock Signal Assignment section). A negative result means the source clock leads the target clock, whereas a positive result means the source clock lags the target clock.

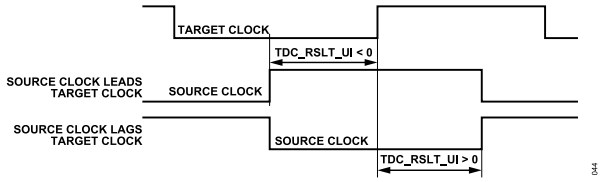

Figure 44. TDC Measurement (TDC_RSLT_UI) Sign

TDC Input Clock Signal Assignment

The purpose of the TDC is to measure the time skew between the edges of two input clock signals. To that end, the ADF4030 incorporates a multiplexer at the input to the TDC, enabling the selection from an assortment of clock signals (see Figure 19). Define one clock signal as the source clock and the other clock signal as the target clock. In this way, the polarity of a TDC measurement result (see the TDC Results section) is meaningful in terms of the relative relationship between the source and target clock signals.

Program the source clock via Bits[4:0] of Register 0x11 and the target clock via Bits[4:0] of Register 0x10. The key to the 5-bit selection code appears in Table 12. The source clock selection and target clock selection use the same code scheme.

Table 12. Selection Codes (Source and Target)

Code	Selected Clock Signal
0	RX0: Output of BSYNC0 receiver
1	RX1: Output of BSYNC1 receiver
2	RX2: Output of BSYNC2 receiver
3	RX3: Output of BSYNC3 receiver
4	RX4: Output of BSYNC4 receiver
5	RX5: Output of BSYNC5 receiver
6	RX6: Output of BSYNC6 receiver
7	RX7: Output of BSYNC7 receiver
8	RX8: Output of BSYNC8 receiver
9	RX9: Output of BSYNC9 receiver
10 to 15	Unused
16 to 25	Reserved
26	Output of REFIN receiver
27 to 31	Unused

The TDC requires the source and target clock signals to be of identical frequency. If not, the clock edges of the two signals will continuously drift away from one another over time, thereby compromising the ability of the TDC to make a time offset measurement. Excessive drift will cause the TDC to flag an error.

As presented in the TDC Core section, only the source clock can serve as the period clock. Always provide a nongapped periodic clock as the source clock. A gapped periodic clock can only be used as the target clock.

TDC Input Clock Edge Selection

The TDC can use the rising edge or the falling edge of either of the input clocks based on the state of two register bits. For the source clock signal, when Bit 7, FALL_EDGE_SRC, in Register 0x15 is 0 (default) or 1, the TDC uses the rising edge or falling edge, respectively. For the target clock signal, when Bit 6, FALL_EDGE_TGT, in Register 0x15 is 0 (default) or 1, the TDC uses the rising edge or falling edge, respectively.

TDC Status

Observe a TDC conversion in progress using Bit 4, TDC_BUSY, in Register 0x8F. It is 1 when the TDC is executing a conversion, and it is 0 when it is not. The TDC_BUSY bit is also available at the MUXOUT1 and MUXOUT2 pins. See the MUXOUT1 and MUXOUT2 section.

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If the TDC error monitor triggers an error during a TDC conversion, the error is latched into Bits[2:1], TDC_ERR, in Register 0x90.

- TDC_ERR = 00, the TDC measurement does not present any error.
- TDC_ERR = 01, at least one TDC input clock presents excessive jitter.
- TDC_ERR = 10, at least one TDC input clock is not present, is outside the allowed duty cycle range, or the frequency is much higher than 200 MHz.
- TDC_ERR = 11, excessive phase shift happened during the TDC measurement. This situation may appear when the TDC input clocks have different frequencies or when the TDC input clocks have too much jitter.

When the TDC_ERR bits become set, they remain as such until the TDC error monitor is reset using the following procedure:

- Set Bit 7, RST_TDC_ERR, in Register 0x61 to 1
- Clear the RST_TDC_ERR bit to 0

Before a TDC Measurement is started, reset the TDC error monitor.

The TDC_ERR bits can be or-ed and reflected at the MUXOUT1 and MUXOUT2 pins. See the MUXOUT1 and MUXOUT2 section. The TDC_ERR output at MUXOUT1 or MUXOUT2 pins is not latched.

MEASUREMENT TIME ESTIMATION

As described in the TDC Time Stamp Averaging section, a complete TDC time difference measurement is the result of averaging many individual TDC time difference sample measurements. Because each sample occurs at the rate of the measured clock signal, the time required for the TDC to perform a complete time offset measurement depends on the frequency (f_{BSYNC}) of the measured clock signal and the specified number (AVG) of individual time offset measurements as shown in the following equation:

$$Measurement\ Time = \frac{AVG}{f_{BSYNC}} = \frac{64 \times 2^{AVGEXP}}{f_{BSYNC}}$$

DUTY CYCLE MEASUREMENT

A duty cycle measurement implies measuring a single clock signal. Because the TDC requires two clock input signals, the same clock source as both the source clock and target clock must be assigned (see the TDC Input Clock Signal Assignment section). That is, the same 5-bit selection code is programmed into the register map for both source and target. In addition, the TDC must be set to use the rising edge of the target clock signal and the falling edge of the source clock signal.

A TDC measurement configured in this way yields a result (see the TDC Results section) that indicates the DC duty cycle as follows:

$$DC = \frac{TDC\_RSLT\_UI}{2^{24}} \times 100\ \%$$

MAXIMUM BSYNC FREQUENCY REDUCTION VS. DUTY CYCLE

When the ODIV divider in a BSYNC channel uses an odd divide value, the resulting output clock signal exhibits non-50% duty cycle (int(ODIV/2)/ODIV). The amount of duty cycle deviation from 50% depends on the divide value (smaller divide values result in larger deviation). The duty cycle of the signal can affect the ability of the TDC to perform an accurate measurement. Because of the likely possibility of a BSYNC channel generating a non-50% duty cycle clock signal, the effect on the TDC must be taken into consideration.

Notably, the maximum BSYNC frequency (f_{BSYNC}) listed in the specifications table assumes a signal with 48% to 52% duty cycle. When f_{BSYNC} is at the specified maximum (see the Specifications section) and the BSYNC signal is not 48% to 52% duty cycle, the TDC is not guaranteed to complete a measurement. As such, for BSYNC signals that do not satisfy the 48% to 52% duty cycle requirement, the maximum f_{BSYNC} specification must be degraded per Equation 11.

$$f_{BSYNC\_MAX\_ADJ} = DCF \times f_{BSYNC\_MAX} \quad (11)$$

where:

$f_{BSYNC\_MAX\_ADJ}$ is the adjusted maximum frequency based on the duty cycle.

f_{BSYNC_MAX} is the maximum BSYNC frequency (200 MHz) per the specifications table. See the Specifications section.

DCF is a duty cycle correction factor between 0 and 1.

The value of DCF, given below, relates to DC (the duty cycle of the BSYNC signal per the Duty Cycle Measurement section), where 0 < DC < 1.

- DCF = DC/0.48 when DC < 0.48
- DCF = (1 − DC)/0.48 when DC > 0.52
- DCF = 1 otherwise

A non-50% duty cycle signal can significantly reduce the specified maximum f_{BSYNC}. For example, a BSYNC signal that exhibits a duty cycle of 25% (DC = 0.25) yields a 52% reduction of the maximum specified f_{BSYNC}.

TEMPERATURE MEASUREMENT SYSTEM

The temperature measurement system contains a proportional to ambient temperature (PTAT) circuit, an ADC, and a code-to-temperature converter (CTC) (Figure 45). Ideally, the PTAT circuit generates a voltage that varies linearly with the silicon die temperature in its vicinity. The CTC output, that is the temperature measurement, is expressed in °C. There is also a temperature monitor that keeps track of the temperature change relative to a reference temperature (see the Interrupt Request (IRQ) section for details). The purpose of the temperature measurement system is to measure changes in die temperature, not the absolute junction temperature.

THEORY OF OPERATION

A temperature measurement is only possible when the ADC is configured for proper operation. First, initialize the ADF4030 (see the Device Initialization section). Then, ensure the following conditions are met:

- Bit 0, EN_ADC, in Register 0x61 is set to 1 (ADC enabled)
- Bit 4, PD_ADC, in Register 0x3C is cleared to 0 (the ADC is not explicitly powered down)
- A valid ADC clock signal (ADCCLK) is present

When the EN_ADC bit is cleared to 0, the ADC is disabled, and the PTAT circuit is powered down. When the PD_ADC bit is set to 1, that is when the ADC is powered down, the EN_ADC bit may be left equal to 1.

Bit 6, ADC_CLK_SEL, in Register 0x61 selects how the ADC clock is created. When the ADC_CLK_SEL bit is cleared to 0 (default), a clock derived from the digital core clock is used. When the ADC_CLK_SEL bit is set to 1, a clock provided at the SCLK pin is used. The frequency of the ADCCLK signal must be ≤400kHz. If the source of the ADCCLK clock is >400 kHz, divide it down using the divider K in Register 0x62. The divider value, K, must be an integer that satisfies Equation 12.

$$K \geq \frac{f_{CORECLK}}{1.6 \times 10^6} - \frac{1}{2} \quad (12)$$

where:
$f_{CORECLK}$ is the frequency of the digital core clock (see the Digital Core Clock section).
Programming Register 0x62 = K (assuming 1 ≤ K ≤ 255) ensures that f_{ADCCLK} ≤ 400kHz.
The ADC clock frequency relates to the integer K per Equation 13.

$$f_{ADCCLK} = \frac{f_{CORECLK}}{(4 \times K) + 2} \quad (13)$$

To enable the ADC clock, set Bit 1, EN_ADC_CLK, in Register 0x61 to 1. This allows the clock selected by the ADC_CLK_SEL bit to pass on to the ADC circuitry.

The ADC only performs a temperature measurement when triggered, which results from writing any 8-bit value to Register 0x72. Enable the trigger function by setting Bit 2, EN_ADC_CNV, in Register 0x61 to 1. Upon triggering, the ADC requires 17 cycles of ADCCLK to complete a temperature measurement. As such, the minimum time required for the ADC to make a temperature measurement (t_{ADC_MEAS}) is given by Equation 14.

$$t_{ADC\_MEAS} = \frac{17}{f_{ADCCLK}} \quad (14)$$

Therefore, the minimum time to perform a temperature measurement is 42.5 µs, which is obtained when f_{ADCCLK} = 400 kHz. While the ADC is performing a temperature measurement, a busy status is indicated by Bit 1, ADC_BUSY, in Register 0x8F being set to 1.

When the ADC is triggered to take a temperature measurement, the CTC stores the temperature result in the form of sign and magnitude. The 8-bit magnitude of the CTC result resides in Register 0x92 and has units of °C (that is, the measurement resolution is 1°C). For example, if Register 0x92 = 0x3C (60 decimal), the magnitude of the temperature is 60°C. The sign of the CTC result resides in Bit 0 of Register 0x93, which means the temperature is positive when the bit is 0 and is negative when the bit is 1.

Temperature results from the CTC are monitored by the temperature monitor block. The temperature monitor provides a mechanism to notify the user (via the IRQB pin) when the temperature changes by a prescribed amount (see the Interrupt Request (IRQ) section for details).

After the ADF4030 has been initialized (see the Device Initialization section), the procedure to execute a temperature measurement is as follows:

1. Write K divider value in Register 0x62
2. Initialize Bit 6, ADC_CLK_SEL, in Register 0x61 to desired value
3. Set Bit 1, EN_ADC_CLK, in Register 0x61 to 1
4. Set Bit 2, EN_ADC_CNV, in Register 0x61 to 1
5. Set Bit 0, EN_ADC, in Register 0x61 to 1 (Bit 6, Bit 2, Bit 1, and Bit 0 in Register 0x61 may be written simultaneously)
6. Clear Bit 4, PD_ADC, in Register 0x3C to 0
7. Write any 8-bit value to Register 0x72
8. Monitor Bit 1, ADC_BUSY, in Register 0x8F until it becomes 0
9. Read Bit 0 of Register 0x93 and Register 0x92 to obtain the temperature result

The recommendation is to use the core clock to clock the ADC while the ADF4030 is fully functional (ADC_CLK_SEL bit cleared to 0). If the ambient temperature measurement is desired, power down the ADF4030 circuits, with the exception of the ADC, for the die temperature to become equal to the ambient. Clock the ADC from the SCLK pin (ADC_CLK_SEL bit set to 1). Set the divider K to a value that ensures the ADCCLK clock is <400 kHz. A nonzero K divider value means more SPI SCLK cycles are required to obtain the 17 ADCCLK cycles. Read the Register 0x8F as many times is necessary to create 17 ADCCLK cycles. The additional SCLK cycles do not matter. For example, if the SCLK frequency is 75 MHz, the K divider must be at least 47, which means ADCLK ~ 395 kHz. To create 17 ADCCLK cycles, there must be 17 × (4 × 47 + 2) = 3230 SCLK cycles, so the Register 0x8F must be read 135 times or 10 SCLK cycles more than necessary (10 = 135 × 24 − 3230). The last 10 SCLK cycles do not matter.

If instead the SCLK is reduced to 800 kHz and the K divider is set to 0, the ADCCLK is 400 kHz. To create 17 ADCCLK cycles, there must be 17 × 2 = 34 SCLK cycles, meaning the Register 0x8F must be read twice, 14 SCLK cycles more than necessary (14 = 2 × 24 − 34). The last 14 SCLK cycles do not matter.

THEORY OF OPERATION

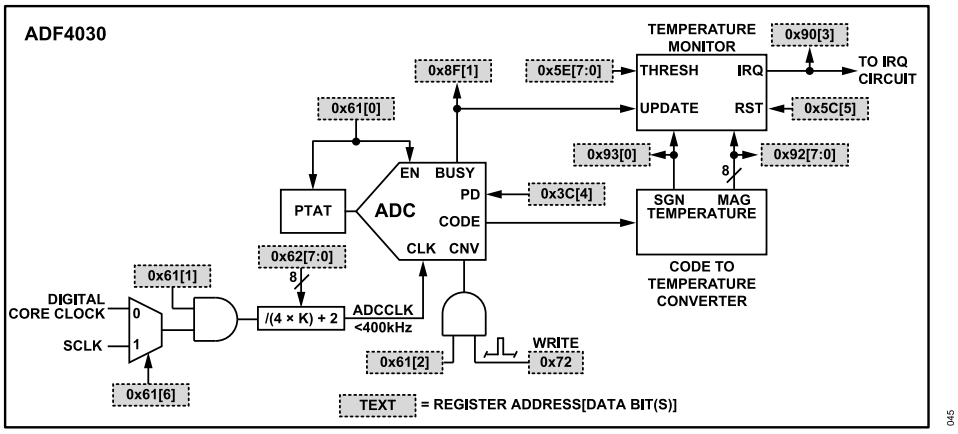

Figure 45. Temperature Measurement System Block Diagram

INTERRUPT REQUEST (IRQ)

The ADF4030 provides an interrupt request (IRQ) mechanism that culminates in a physical output signal at the IRQB pin. The IRQB pin has two user selectable output types via Bit 0, IRQB_OPEN-DRAIN, in Register 0x5C. When IRQB_OPENDRAIN bit is 0 (default), the IRQB pin behaves like a standard CMOS output (see the CMOS Output Pin Logic High Control section), but when the bit is 1, the IRQB pin becomes an open drain output. The open drain mode means that when the underlying IRQB logic level is 0, the IRQB pin is a low impedance connection to ground, but when the underlying IRQB logic level is 1, the IRQB pin is open circuit. Therefore, the open drain mode allows for multiple devices possessing an open drain IRQB pin to be connected together to form a wired-OR IRQB bus (typically requires a 1 kΩ pullup resistor on the wired-OR IRQB bus). Note the supply of the pull-up resistor is related to the CMOS_OV bit in Register 0x5C (see the CMOS Output Pin Logic High Control section). If the CMOS_OV bit is cleared to 0 and the CMOS logic outputs of the ADF4030 have a logic high level associated with 1.8 V, pull up the resistor to 1.8 V. If CMOS_OV bit is set to 1 and the ADF4030 CMOS logic outputs have a logic high level associated with 3.3 V, pull up the resistor to 3.3 V.

Normal IRQ operation allows the set up the ADF4030 to generate an interrupt (that is, force the IRQB pin to 0) based on the state of the following internal IRQ circuits:

- The PLL lock detector
- Temperature monitor
- BSYNC accumulated alignment drift monitor
- TDC error monitor
- Temporary alignment error monitor

The user chooses which combination of the IRQ circuits in the list are capable of generating an interrupt by programming their corresponding mask bit (see Figure 46) to 1. Then, the interrupt is unmasked. When a specific mask bit is 0, that specific IRQ circuit does not generate an interrupt, and the interrupt is masked. However, even though the mask bit can be 0, the associated IRQ circuit continues normal operation in the background ready to generate an interrupt if the mask bit is set to 1.

The IRQB pin responds to a logical OR (with inversion) of the individual IRQ circuits. When more than one IRQ circuit has its mask bit set to 1, assertion of the IRQB pin is ambiguous in terms of which specific IRQ circuit generated the interrupt. In this case, the appropriate status bit(s) associated with each IRQ circuit must be interrogated (per Figure 46) to determine which IRQ circuit(s) are responsible for asserting the IRQB pin.

THEORY OF OPERATION

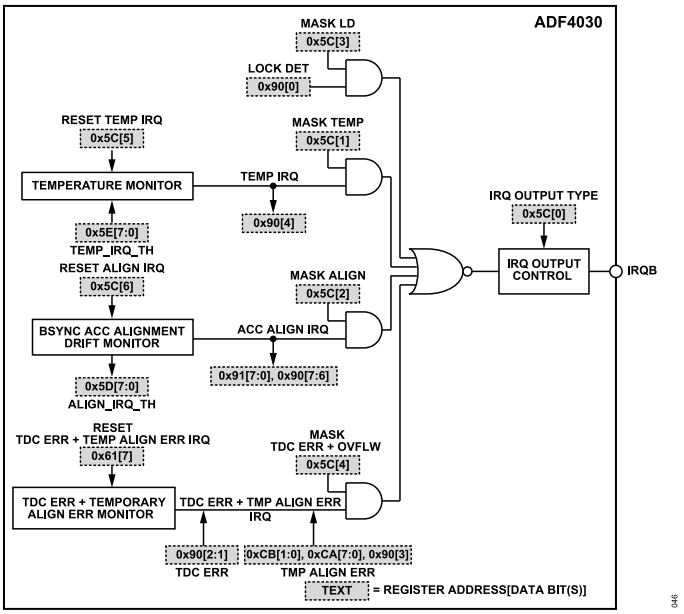

Figure 46. IRQ Block Diagram

PLL Lock Detect IRQ

The lock detect IRQ is unique in that there is no latching mechanism involved. Instead, the lock detect IRQ is a live status indicator of the PLL lock state. Assuming the PLL lock detect mask bit is 1, the IRQ pin provides an external signal that follows the state of the PLL lock detector status bit (Bit 0, PLL_LD, in Register 0x90), but with inversion. This allows for designing a system with a real-time status indicator of the state of the PLL lock detector. However, because the output of the IRQ circuits are combined through a logical OR, it is best to set the mask bits of the other IRQ circuits to 0 when the PLL lock detect mask bit is 1. Otherwise, interrupts generated by the other IRQ circuits will interfere with the real-time status indication of the PLL lock detect IRQ.

Temperature Monitor IRQ

For each temperature measurement performed by the temperature sensor (see the Temperature Measurement System section), the temperature monitor keeps track of the temperature change relative to a reference temperature. The reference temperature (T_{REF}) is the first temperature measurement that occurs after resetting the temperature IRQ via Bit 5, RST_TEMP, in Register 0x5C.

For any temperature measurement (T_n) performed after the T_{REF} measurement, the temperature monitor computes the difference temperature (T_{DIFF}) = $|T_n - T_{REF}|$. The temperature IRQ monitor compares T_{DIFF} to a user-provided threshold value (T_{THRESH}), an 8-bit unsigned number (units of °C) in Register 0x5E. The moment T_{DIFF} exceeds T_{THRESH}, the IRQ monitor generates and latches the TEMP_MON flag (Bit 4 in Register 0x90), which serves as an interrupt.

To clear a temperature IRQ, the user must toggle (write 1 then 0) Bit 5, RST_TEMP, in Register 0x5C. Note that clearing the temperature IRQ means that the next temperature measurement will establish a new T_{REF} value.

Proper operation of the temperature monitor requires the correct configuration of the temperature measurement system (see the Temperature Measurement System section).

BSYNC Accumulated Delay IRQ

Each BSYNC channel has an accumulated delay monitor. During an alignment procedure (see the BSYNC Channel Alignment section), the ADF4030 cancels, that is aligns, the delay between a target BSYNC clock and a source BSYNC clock. The monitor accumulates this delay every time an alignment is executed on a target BSYNC channel. Then, it checks this accumulated time against a threshold. When the threshold is passed, an interrupt is generated. Status bits identify the channels with accumulated delay above the threshold.

In a system, the BSYNC clocks may drift in time due to temperature or because the REFIN clock drifted. The accumulated delay monitor is a debugging tool to understand how frequently an alignment procedure must be executed in a system to maintain the desired alignment between various BSYNC channels.

Set the 8-bit unsigned ALIGN_IRQ_TH threshold in Register 0x5D. The bit weight of the ALIGN_IRQ_TH is approximately 12.5 ps, with a threshold accuracy of around ±23 ps. The recommended value is 0x10, which makes for an accumulated delay of approximately 200 ps.

THEORY OF OPERATION

Activate the monitoring by clearing Bit 6, RST_ALIGN_IRQ, in Register 0x5C to 0. After power up or reset, the recommendation is to set the RST_ALIGN_IRQ to 1, meaning the monitoring is inactive (see the Device Initialization section). If monitoring needs to be stopped, set the RST_ALIGN_IRQ bit to 1. To start a new monitoring cycle, reset the monitor by setting the RST_ALIGN_IRQ to 1 and then clearing it to 0.

Every time an alignment procedure is executed (any procedure presented in the BSYNC Channel Alignment section), the monitor accumulates the delay that the alignment procedure cancels. When the accumulated error becomes greater than the ALIGN_IRQ_TH threshold on a certain BSYNC channel, the IRQ_BSYNC[9:0] bit corresponding to that BSYNC channel becomes 1.The IRQ_BSYNC[9:2] bits are Bits[7:0] in Register 0x91, and the IRQ_BSYNC[1:0] are Bits[7:6] in Register 0x90.

Enable the interrupt by setting Bit 2, MASK_ALIGN_IRQ, in Register 0x5C to 1. Disable the interrupt by clearing the MASK_ALIGN_IRQ to 0.

TDC Error Monitor IRQ

The TDC error monitor interrupt line is shared with the ADEL overflow interrupt.

The TDC error monitor is a logical OR of Bits[2:1], TDC_ERR, in Register 0x90 (see the TDC Status section for details on these bits). A zero to one transition by the TDC error monitor latches a TDC error IRQ flag that constitutes the TDC ERR + TEMP ALIGN ERR IRQ signal in Figure 46. Activate the monitoring be clearing Bit 7, RST_TDC_ERR, in Register 0x61 to 0. After power up or reset, the recommendation is to set the RST_TDC_ERR to 1, meaning the monitoring is inactive (see the Device Initialization section). If monitoring needs to be stopped, set the RST_TDC_ERR bit to 1. To start a new monitoring cycle, reset the monitor by setting the RST_TDC_ERR to 1 and then clearing it to 0.

Enable (mask) the interrupt by setting Bit 4, MASK_TDC_ERR, in Register 0x5C to 1. Disable (unmask) the interrupt by clearing the MASK_TDC_ERR to 0. When the interrupt is triggered, check the TDC_ERR bits to understand if the interrupt has been triggered by the TDC error monitor. If the TDC_ERR bits are 00, it signifies that an interrupt was generated by the temporary alignment error interrupt.

Temporary Alignment Error IRQ

The temporary alignment error interrupt line is shared with the TDC error monitor interrupt. Enable the temporary alignment error interrupt using the same Bit 4, MASK_TDC_ERR, in Register 0x5C (see the TDC Error Monitor IRQ section).

If the ADF4030 executes one of the alignment procedures that have a closed-loop delay adjustment at the core (see the Applications Information section) and an additional alignment is required due to the temperature drift, most closed-loop delay adjustments change the ADEL_x setting only. In this case, the temperature drift may eventually exhaust the ADEL typical ~88 ps range, requiring a coarse adjustment along the ADEL_x. The adjustment may create a temporary phase offset between the BSYNC channels of up ±15 ps, and the ADF4030 signals this as a temporary alignment error.

During the single-channel alignment procedure (see the Single-Channel Alignment section), the temporary alignment error monitor flag is Bit 3, TMP_ALIGN_ERR, in Register 0x90. If a temporary alignment error happened, the TMP_ALIGN_ERR becomes 1.

During the fixed iteration alignment procedure (see the Fixed Iteration Alignment section), the TMP_ALIGN_ERR flag becoming 1 signifies that a temporary alignment error occurred during the last iteration.

During the threshold alignment procedure (see the Threshold Alignment section), the TMP_ALIGN_ERR flag becomes 1 if the alignment process reaches the maximum number of alignment cycles (ALIGN_CYCLES + 1) without the alignment becoming less than the AUTO_ALIGN_THOLD threshold.

To reset the TMP_ALIGN_ERR flag and reduce the alignment error, execute the alignment procedure again.

During the serial alignment process in which multiple BSYNC channels are aligned (see the Serial Alignment section), every BSYNC channel has an assigned temporary alignment error monitor flag within the TMP_ALIGN_ERR_CH[9:0] field. The TMP_ALIGN_ERR_CH[0] corresponds to the BSYNC0 channel, the TMP_ALIGN_ERR_CH[1] corresponds to the BSYNC1 channel, continuing to the TMP_ALIGN_ERR_CH[9] corresponding to the BSYNC9 channel. Register 0xCA bits contain the TMP_ALIGN_ERR_CH[7:0] bits, and Bits[1:0] of Register 0xCB contain the TMP_ALIGN_ERR_CH[9:8] bits. When a temporary alignment error occurs on one or multiple BSYNC channels, the Bit 3, TMP_ALIGN_ERR, in Register 0x90 is set to 1 and latches the corresponding TMP_ALIGN_ERR_CH bits to identify which channels triggered the interrupt. In such case, to resolve the temporary alignment errors, execute a single-channel alignment procedure on the channels that triggered the interrupt to clear the TMP_ALIGN_ERR and the affected TEMP_ALIGN_ERR_CH.

The temporary alignment error monitor does not work when the background serial alignment procedure is executed.

MUXOUT1 AND MUXOUT2

The MUXOUT1 and MUXOUT2 pins provide access to various signals within the ADF4030. The user selects which internal signal is to be presented at the pin via a 5-bit code. Bits[4:0], MUXCODE1, of Register 0x63, associate with the MUXOUT1 pin, and Bits[4:0], MUXCODE2, of Register 0x64 associate with the MUXOUT2 pin. Table 13 presents the available selections of MUXCODE1 and MUXCODE2 bits. When the TDC is used, do not set MUXCODE1 and MUXCODE2 bits to 28, providing the TDC input clocks at the MUXOUT pins. This setting should only be used as a debug tool to verify signals.

THEORY OF OPERATION

Table 13. MUXCODE1 and MUXCODE2 Bit Selections

MUXCODE	Selected Signal
0	High impedance.
1	Digital core clock (see Figure 23) divided by 2.
2	Period clock (see Figure 43) divided by 2.
3	State of Bit 1, ADC_BUSY, of Register 0x8F.
4	State of Bit 4, TDC_BUSY, of Register 0x8F.
5	State of Bit 3, DL_BUSY, of Register 0x8F.
6	State of Bit 0, FSM_BUSY, of Register 0x8F.
7	PLL PFD input clock from the NDIV divider divided by 2.
8	PLL PFD input clock from the RDIV divider divided by 2.
9 to 17	Reserved.
18	State of Bit 0, PLL_LD, of Register 0x90.
19	State of Bit 1, CAL_COMP, of Register 0xBA.
20	State of Bit 0, CAL_BUSY, of Register 0xBA.
21 to 22	Reserved.
23	Logical OR of the live (not latched) TDC error signals associated with Bits[2:1], TDC_ERR, of Register 0x90.
24	Logic 0.
25 to 27	Reserved.
28	TDC source clock for MUXOUT1 pin and TDC target clock for MUXOUT2 pin.
29	Logic 1.
30	General purpose output. For the MUXOUT1 pin, the state of Bit 6, GPO1, of Register 0x68. For the MUXOUT2 pin, the state of Bit 7, GPO2, of Register 0x68.
31	Unused.

PROGRAMMABLE POWER DOWN OPTIONS

To power down the entire IC, set Bit 7, PD_ALL, in Register 0x3C.

The PLL can be powered down by setting Bit 6, PD_PLL, in Register 0x3C to 1. This also powers down the ODIV output divider and the analog delay blocks on all BSYNC channels (see Figure 19 and Figure 24). When the PD_PLL bit is set to 1, the TDC can still be used to measure the phase offset between clocks received at the BSYNC channels, but the ADF4030 cannot generate any BSYNC clocks.

The TDC and the multiplexer at the input to the TDC (see TDC Input Clock Signal Assignment) can be powered down by setting Bit 5, PD_TDC, in Register 0x3C to 1.

The ADC of the temperature measurement system may be powered down by setting Bit 4, PD_ADC, in Register 0x3C to 1. If the entire temperature system needs to be powered down, in addition to setting the PD_ADC bit, clear Bit 0, EN_ADC, and Bit 1, EN_ADC_CLK, in Register 0x61 to 0. When cleared to 0, the EN_ADC bit blocks the clock inside the ADC and powers down the ADC voltage reference block. When cleared to 0, the EN_ADC_CLK bit blocks the clock inside the digital blocks of the system (see Figure 45).

The PD_TX_PATH_x bit, disables the BSYNCx transmit channel, while the PD_DRV_x bit reduces the power of the BSYNCx transmit channel without losing the alignment data in the analog delay block. When set to 1, the PD_TX_PATH_x bits power down the BSYNC transmit driver (Figure 25) and the BSYNC analog delay block (Figure 24). The PD_TX_PATH_5, 4, …, 0 are Bits[7:2] in Register 0x3B. The PD_TX_PATH_9, 8, …, 6 are Bits[3:0] in Register 0x3C. When set to 1, the PD_DRV_x bits power down the BSYNC transmit driver (Figure 25). The PD_DRV_7, 6, …, 0 are Bits[7:0] in Register 0x3A. The PD_DRV_9, PD_DRV_8 are Bits[1:0] in Register 0x3B. If the PD_TX_PATH_x bit of the BSYNCx channel is set to 1, the state of the corresponding PD_DRV_x bit is ignored. The state of the EN_DRVx bit (see the Transmit and Receive Interface section) is ignored when either the PD_TX_PATH_x bit or the PD_DRV_x bit is set to 1.

The TDC measures the phase difference between the source clock and the target clock (see TDC Core). There is no need to keep the BSYNC receivers that are not used in the TDC measurement powered. When set to 1, Bits AUTO_PD_RCV_x, allow the ADF4030 to automatically power down the unused BSYNC receivers. The AUTO_PD_RCV_0, 1, …, 9 bits are Bit 7 of Register 0x40, Register 0x42, Register 0x44, …, respectively to Register 0x52. Initialize these bits to 1 after power up. When cleared to 0, Bits AUTO_PD_RCV_x allow the corresponding BSYNC receiver to stay enabled and consuming power all the time, which is not recommended.

Table 14 restates what various power down settings presented in this section mean overall.

THEORY OF OPERATION

Table 14. ADF4030 Power Down Modes

Mode	PD_ALL	PD_PLL	PD_TX_PATH_x	PD_DRV_x	EN_DRVx	Description
0	1	-[1]	-	-	-	PD_ALL = 1, ADF4030 powered down
1	0	1	-	-	-	PLL = off, TDC may be used
2	0	0	1	-	-	PLL = on, BSYNCx transmitter = off permanently
3	0	0	0	1	-	PLL = on, BSYNCx transmitter = off temporarily
4	0	0	0	0	0	PLL = on, BSYNCx transmitter = on, but idle
5	0	0	0	0	1	PLL = on, BSYNCx transmitter = on

[1] Don't care. Value can be 0 or 1.

Table 15 clarifies what the AUTO_PD_RCV_x and AUTO_PD_COMP_x, bits mean overall.

Table 15. Power Down BSYNCx Receiver Modes

Mode	BSYNCx Selected as TDC_SOURCE or TDC_TARGET	AUTO_PD_RCV_x	Description
0	Not Selected	1	BSYNCx not selected as a TDC input, receiver powered down
1	Not Selected	0	BSYNCx not selected as a TDC input, receiver powered up (but not used)
2	Selected	-[1]	BSYNCx selected as a TDC input, receiver powered up

[1] Don't care. Value can be 0 or 1.

THEORY OF OPERATION

SPI OPERATION

SPI Pin Descriptions

The serial clock (SCLK) input pin provides the serial shift clock to the internal SPI controller. The SCLK signal synchronizes the SPI read and write operations. The rising edge of the SCLK registers write data bits, and the falling edge of SCLK registers read data bits.

The SPI port hardware configuration and data format are configured via Register 0x00. The hardware configurations are 3-wire bidirectional mode (SDO_Active = 0, default) or 4-wire unidirectional mode (SDO_Active = 1), where SDO_Active is represented by Bit 4 and Bit 3 in Register 0x00. The data formats are MSB first or LSB first (see the SPI MSB First and LSB First Formats section). The 3-wire mode uses the serial data input/output (SDIO) pin for both the instruction word and the payload (see the SPI Communication Cycle—Instruction Plus Payload section), allowing the SPI controller to accommodate read or write payloads via a single pin. The 4-wire mode uses the SDIO pin for the instruction word and for the payload during a write operation. However, for read operations the payload is set via the SDO output pin (the instruction word is still via the SDIO pin).

The chip select ($\overline{CS}$) input pin provides an active low control signal that gates the SPI communications. Forcing the $\overline{CS}$ pin low initiates a SPI communication cycle. During a SPI communication cycle, any number of payload data bytes can be transferred in a continuous stream. The register address is automatically incremented or decremented based on the address ascension setting (see the SPI Address Ascension section). The user must force the $\overline{CS}$ high following the last byte transferred in a communication cycle, thereby ending the stream of payload data. When the $\overline{CS}$ is high, SDIO and SDO enter a high impedance state.

The ADDR3, ADDR2, ADDR1, and ADDR0 pins (called ADDR pins in the following text) are inputs that accommodate a system that uses multiple ADF4030 devices sharing the same $\overline{CS}$ signal. The ADDR pins provide for a memory paging mechanism that allows up to 16 ADF4030 devices to have a dedicated page within the 15-bit memory space of the SPI controller (see the SPI Instruction Word section for details). Note the ADDR pins are floating 1.8 V or 3.3 V CMOS inputs with no internal pull-up or pull-down resistors. Therefore, the ADDR pins must be connected to GND, 1.8 V, or 3.3 V to establish the memory page associated with a specific ADF4030. For single device applications, the recommendation is to connect the ADDR pins to GND to select Page 0, which means the device occupies the first 512 address locations of the SPI controller address space.

SPI Communication Cycle—Instruction Plus Payload

The SPI protocol consists of a two-part communication cycle that starts with the falling edge of the $\overline{CS}$ signal and ends with the rising edge of the $\overline{CS}$ signal (see Figure 47). The first part of the communication cycle is an instruction word (see the SPI Instruction Word section) comprising 16 bits coinciding with the first 16 rising edges of the SCLK signal (assuming the $\overline{CS}$ signal is low). The second part is the payload (see the SPI Payload section), of which the bits relate to the SCLK pulses that follow the instruction word. The payload must consist of multiples of eight cycles of the SCLK signal.

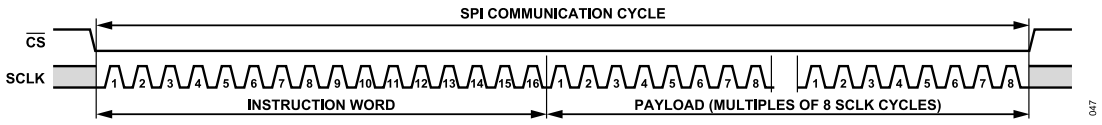

Figure 47. SPI Communication Cycle Diagram

THEORY OF OPERATION

SPI Instruction Word

The SPI instruction word constitutes the first part of a SPI communication cycle (see the SPI Communication Cycle—Instruction Plus Payload section). The 16-bit instruction word provides the internal SPI controller with information regarding the payload. The instruction word includes the R/$\overline{W}$ bit that informs the SPI controller of the direction of the payload transfer. That is, whether the SPI communication cycle constitutes a SPI read operation or a SPI write operation (see the SPI Payload section). The instruction word also indicates the 15-bit starting address associated with the first payload byte. Terminating the SPI communication cycle before completing 16 SCLK cycles causes the SPI controller to ignore the remainder of the SPI communication cycle.

The format of the instruction word appears in Figure 48. The rising edges of the SCLK signal transfer the state of the SDIO signal to the internal SPI controller. The first SCLK rising edge following the falling edge of the $\overline{CS}$ signal denotes the R/$\overline{W}$ bit. Subsequent SCLK rising edges denote the 15-bit starting address (associated with the payload that follows). The second SCLK rising edge following the falling edge of the $\overline{CS}$ signal denotes Bit 14 (A14) of the 15-bit address. Subsequent SCLK rising edges denote successive address bits in descending order.

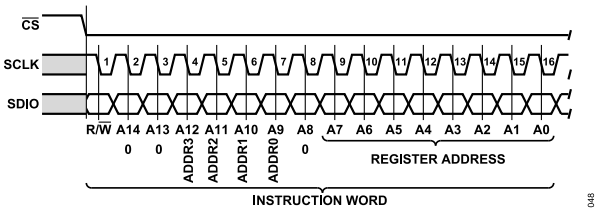

Figure 48. Instruction Word Diagram

The ordering of the 16-bit instruction word depends on whether the SPI controller is configured for MSB first mode or LSB first mode (see the SPI MSB First and LSB First Formats section). Figure 48 shows the case for MSB first mode. In LSB first mode, the ordering of the 16-bit instruction word is reversed. That is, in Figure 48, the leftmost bit becomes A0 and the rightmost bit becomes R/$\overline{W}$.

The register address range of a single ADF4030 spans 256 address locations (0x00 to 0xFF). However, the internal SPI controller allows for up to 15 bits of address range, which spans 32,768 address locations. Because the register range of a single ADF4030 only occupies 512 address locations while the SPI controller supports 32,768 address locations, a large portion of unused SPI address space exists. As such, the ADDR pins are used to establish a unique 4-bit code for a particular ADF4030 that the SPI controller interprets as an identifier for that particular ADF4030. Specifically, the ADDR3, ADDR2, ADDR1, and ADDR0 pins map one-to-one to A[12:9] of the instruction word. This means the code associated with the ADDR pins effectively assigns a page (a block of 512 address locations) to a particular ADF4030.

The following list describes certain nuances of how the SPI controller behaves with respect to the ADDR3, ADDR2, ADDR1, and ADDR0 pin codes:

- Generally, unless A[14], A[13], and A[8] are cleared to 0 and A[12:9] = ADDR3, ADDR2, ADDR1, and ADDR0 pin states, SPI write operations are ignored.
- To write Register 0x00 and Register 0x01, use the ADDR bits cleared to 0000, independent of the ADDR pin code.
- When Bit 1, EN_BRDCST, of Register 0xFF is set to 1 (see the SPI Broadcast Mode section), SPI write operations are executed regardless of the ADDR pin code.
- SPI read operations are only executed when A[14], A[13], and A[8] are cleared to 0 and A[12:9] = ADDR3, ADDR2, ADDR1, and ADDR0 pin states.

SPI Payload

The SPI payload constitutes the second part of a SPI communications cycle (see the SPI Communication Cycle—Instruction Plus Payload section). The payload constitutes data sent to or data read from the SPI registers in the ADF4030. Transfer of the payload data (to or from the ADF4030) requires an integer multiple of eight SCLK cycles, with each group of eight SCLK cycles corresponding to eight bits (1 byte) of data (see Figure 47). Terminating a SPI communication cycle during a payload transfer with anything other than an integer number of eight SCLK cycles results in the loss of the data associated with the incomplete group of eight SCLK cycles. That is, the SPI controller groups data as bytes, so any group comprising less than eight bits is ignored.

When the SPI instruction word indicates a read operation, the payload (register data) is output on the SDIO pin or the SDO pin depending on whether the ADF4030 is programmed for 3-wire or 4-wire mode, respectively (see the SPI Pin Descriptions section).

SPI MSB First and LSB First Formats

The SPI instruction word and payload can be transferred MSB first or LSB first depending on the state of Bit 6 and Bit 1, LSB_First, in Register 0x00. When LSB First = 0 (default), MSB first mode is in effect. When LSB_First = 1, LSB first mode is in effect. Immediately after programming either mode, subsequent SPI operations occur according to the programmed mode.

SPI Address Ascension

Bit 5 and Bit 2, ADDRESS_ASCENSION, in Register 0x00, constitute the ascension control bits for the internal SPI controller. When the ADDRESS_ASCENSION = 0 (default), the internal SPI controller automatically decrements the address pointer for multibyte payload transfers, starting at the address designated by the instruction word (see the SPI Instruction Word section) and steps toward Address 0x0000. Conversely, when the ADDRESS_ASCENSION = 1, the internal SPI controller automatically increments the address pointer for multibyte payload transfers, starting at the address

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designated by the instruction word, and steps toward the Address 0xFF. Reserved addresses are not skipped during multibyte payload transfers.

SPI Broadcast Mode

Bit 1, EN_BRDCST, of Register 0xFF controls the SPI broadcast mode. By default, EN_BRDCST is 0, meaning the ADF4030 is not in broadcast mode. Setting EN_BRDCST to 1 puts the ADF4030 in broadcast mode. When in broadcast mode, the SPI controller ignores the ADDR pin code (see the SPI Instruction Word section).

Therefore, programming multiple ADF4030 devices to broadcast mode allows for writing the same information to all broadcast enabled ADF4030 devices using a single SPI communication cycle (assuming the $\overline{CS}$ signal of those ADF4030 devices is low). Broadcast mode does not apply for SPI read operations.

SPI Control Diagrams

In the following figures, several SPI control diagrams are presented as examples of SPI communication between the controller and the ADF4030.

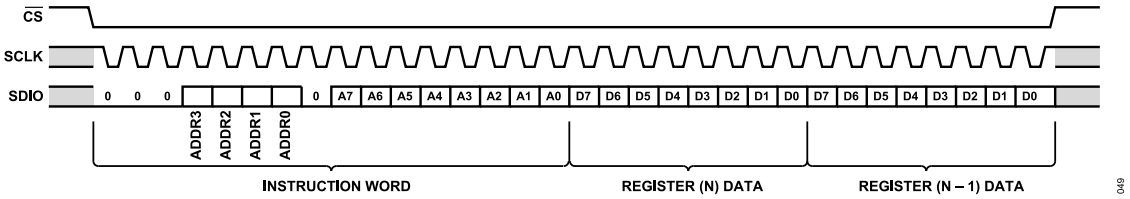

Figure 49. SPI Control Port Write—MSB First, Address Decrement, and Two Bytes of Data

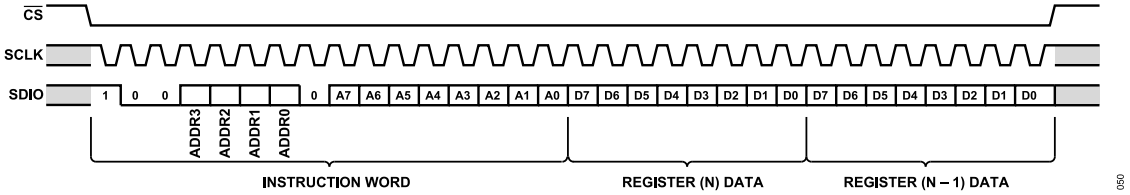

Figure 50. 3-Wire SPI Control Port Read—MSB First, Address Decrement, and Two Bytes of Data

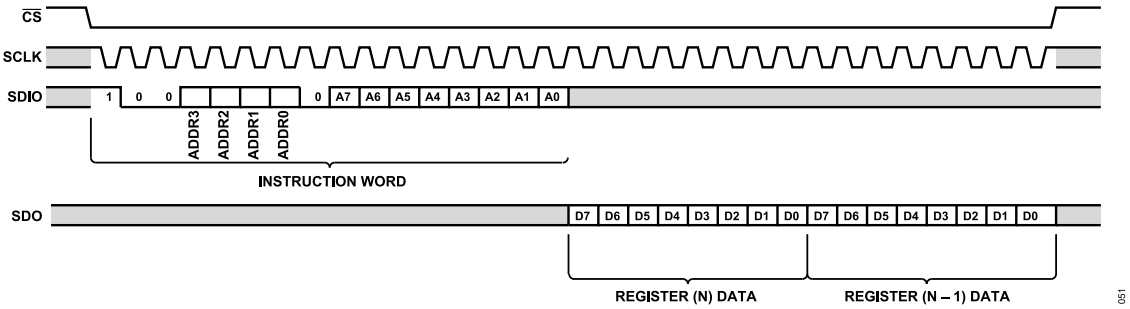

Figure 51. 4-Wire SPI Control Port Read—MSB First, Address Decrement, and Two Bytes of Data

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The ADF4030 can time align the clock edges of multiple BSYNC clocks with respect to a reference BSYNC channel clock that can be generated or received by the ADF4030. Both BSYNC clocks must have the same frequency. The desired time offset can be any number, positive or negative, within one clock period. The BSYNC clocks can be AC-coupled or DC-coupled. Although AC coupling degrades the TDC accuracy somewhat, no meaningful alignment differences have been observed relative to aligning DC-coupled clocks.

The TDC measurement does not use the PLL, but the delay adjustment and the alignment procedures require the PLL to be locked first.

TDC MEASUREMENT

To execute a TDC measurement, execute the following steps:

1. Select the source of the digital core clock (see the Digital Core Clock section). If the TDC ring oscillator is used as the source, the ADF4030 may function as a stand alone TDC.
2. Initialize Bits[3:0], AVGEXP, in Register 0x16. This procedure represents the TDC averaging number of samples. The bigger the number, the more accurate the TDC measurement. The initialization procedure (see the Device Initialization section) sets this bit to 6, which means the TDC averages 4096 measurements to produce a result.
3. Set Bit 7, MANUAL_MODE, in Register 0x11 to 1 to enable a manual TDC measurement.
4. Initialize Bits[4:0], TDC_Target, in Register 0x10 to select which BSYNC channel is the TDC target clock.
5. Initialize Bits[4:0], TDC_Source, in Register 0x11 to select which BSYNC channel is the TDC source clock.
6. Initialize Bits[7:6], FALL_EDGE_SRC and FALL_EDGE_TGT, in Register 0x15 to select the clock edge of the TDC source and target clocks used by the TDC.
7. Reset the TDC_ERR monitor bits by setting Bit 7, RST_TDC_ERR, in Register 0x61 to 1 and then clearing it to 0.
8. Set Bit 7, TDC_ARM_M, in Register 0x16 to 1 to start the TDC measurement.
9. Monitor Bit 4, TDC_BUSY, in Register 0x8F. It stays 1 while the TDC is executing the measurement and goes to 0 when the measurement ends. The state of the TDC_BUSY may also be monitored at the MUXOUT1 and MUXOUT2 pins (see the MUXOUT1 and MUXOUT2 section).The TDC_BUSY remains set to 1 for the time it takes for the BSYNC clock to generate the samples used for the TDC averaging, $(64 \times 2^{AVGEXP})/f_{BSYNC}$.
10. Check Bits[2:1], TDC_ERR, in Register 0x90 for a TDC measurement error (see the TDC Status section).
11. Check Bit 2, MATH_BUSY, in Register 0x8F. This bit becomes 1 after the TDC measurement ends (that is the TDC_BUSY clears back to 0) and the ADF4030 starts postprocessing the results. The bit becomes 0 after the ADF4030 generates the outputs.
12. Read the Bits[23:0], TDC_RSLT_UI, in Register 0x75, Register 0x74, and Register 0x73. The TDC_RSLT_UI is the phase difference between the source and target clocks at the TDC inputs.
13. Clear Bit 7, TDC_ARM_M, in Register 0x16 to 0 to end the TDC measurement.

OPEN-LOOP DELAY ADJUSTMENT

The ADF4030 open-loop delay adjustment feature changes the delay into the target BSYNC output clock. This is an open-loop adjustment because it does not involve a feedback loop. Figure 52 presents the delay adjustment process.

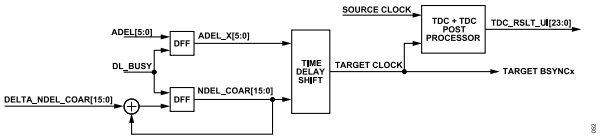

Figure 52. Open-Loop Delay Adjustment Process

The following two bit fields control the delay adjustment:

- Bits[5:0], ADEL, in Register 0x17
- Bits[15:0], DELTA_NDEL_COAR, of which Bits[15:8], DELTA_NDEL_COAR, are in Register 0x19, and the Bits[7:0], DELTA_NDEL_COAR, are in Register 0x18

The ADEL[5:0] bits are the analog adjustable delay presented in the BSYNC Channels section and adjust the delay in typically 1.4 ps steps.

The DELTA_NDEL_COAR[15:0] bits adjust the NDEL_COAR[15:0] bits, the intermediate portion of the delay control bits following this expression:

NDEL_COAR = DELTA_NDEL_COAR + existing NDEL_COAR.

The DELTA_NDEL_COAR[15:0] bits, also presented in the BSYNC Channels section, adjust the delay in steps of ~50 ps ($(1/f_{VCO})/8$, where f_{VCO} = 2.5 GHz).

Both the ADEL and DELTA_NDEL_COAR are applied to the time delay shift block through D flip-flops (DFF in Figure 52) clocked by the DL_BUSY status Bit 3 in Register 0x8F.

Therefore, the delay adjustment applied to the target BSYNC channel may be written as follows:

Delay adjustment = DELTA_NDEL_COAR /f_{VCO}/8 + (ADEL − ADEL_x) × 1.4 ps

Bit 7 and Bit 6, ONE_SHOT and CYCLES, in Register 0x34 control how the delay adjustment is applied. If ONE_SHOT = 1, the delay adjustment is applied in one single BSYNC cycle independent of cycles value. If ONE_SHOT = 0, and cycles = 0, the delay adjustment is done in steps of approximately 50 ps (1/8th of one f_{VCO}

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period). If ONE_SHOT = 0, and cycles = 1, the delay adjustment is done in steps of approximately 400 ps (one f_{VCO} period).

After the ADEL and DELTA_NDEL_COAR bits are initialized, set Bit 7, NDEL_ADJ, in Register 0x17 to 1 to start the adjustment. Monitor Bit 3, DL_BUSY, in Register 0x8F as it remains set to 1 during the delay adjustment operation and goes to 0 when the operation ends. Once the DL_BUSY bit clears to 0, clear the Bit NDEL_ADJ to 0 to end the delay adjustment.

The value of the ADEL bits on each BSYNC channel may be read back from the ADEL_x bits in Register 0x84, Register 0x85, …, Register 0x8D. Bits[2:0] of the NDEL_COAR[15:0] intermediate delay control field represent the phase output of the PLL VCO and may be read back from the DLY_TAP_STATEx bits in Register 0x95, …, Register 0x99. The NDEL_COAR[15:3] bits cannot be read back.

This adjustment procedure is an open-loop procedure. Because the bit weight of the ADEL bits is typically only known as 1.4 ps, executing a delay adjustment as presented in this section is not always reflected exactly in the obtained delay. Use the alignment procedures to align BSYNC clocks to the desired delay.

CLOSED-LOOP DELAY ADJUSTMENT

The closed-loop delay adjustment procedure is the core of the alignment procedures presented in the BSYNC Channel Alignment section. The data path starts from the TDC postprocessor output, adds the desired offset to be achieved, applies the desired delay to the time delay shift block, and has a feedback loop from the target BSYNC clock back to the TDC input (Figure 53). The advantage of the closed-loop method is that the desired skew is reflected exactly in the obtained delay between the target clock and the source clock.

The desired delays are introduced into the registers TDC_OFFSETx[15:0] and TDC_OFFSET_COM[20:0]. The TDC_OFFSETx are signed, 16-bit words. The TDC_OFFSET0 reflects the desired delay in the BSYNC0 channel, the TDC_OFFSET1 reflects the desired delay in BSYNC1 channel continuing to the TDC_OFFSET9 reflecting the desired delay in the BSYNC9. The bit weight of TDC_OFFSETx registers is equal to ~$1/f_{VCO}/2^9$ = 0.78125 ps when f_{VCO} = 2.5 GHz. This makes for a delay adjustment range of ±25.6 ns (0.78125 × 2^{15}), which signifies BSYNC clocks with frequencies down to 1/2/25.6 = 19.53125 MHz can be fully adjusted (±180°C) using the TDC_OFFSETx. Therefore, for adjustments within ±25.6 ns, the TDC_OFFSETx is all that is needed.

TDC_OFFSET_COM[20:0] is a 21-bit signed word that contains a delay that is introduced to all of the BSYNC channels. The bit weight is equal to the TDC_OFFSETx bit weight. This makes for a delay adjustment range of ±819.2 ns (0.78125 × 2^{20} when f_{VCO} = 2.5 GHz), good to phase shift the minimum BSYNC frequency of 650 kHz within ±180°C.

Figure 53 presents the process. The TDC postprocessor outputs the TDC_RSLT_UI[23:0] phase difference between the source clock and the target clock (see the TDC Results section). To bring the TDC_RSLT_UI on the same bit weight as the TDC_OFFSETx and TDC_OFFSET_COM, ~$1/f_{VCO}/2^9$, the TDC_RSLT_UI is multiplied by ODIV[11:0] × 2^9, ODIV being the divider presented in the BSYNC Channels section.

After the target clock phase is adjusted, the feedback loop brings the target clock back to the TDC. Any remaining alignment error between the source and the target clocks is then corrected by iterating the TDC measurement and the delay adjustment.

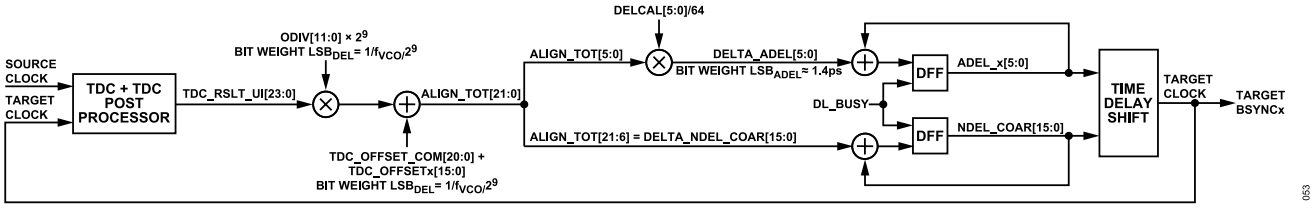

Figure 53. Closed-Loop Delay Adjustment Process

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BSYNC CHANNEL ALIGNMENT

Alignment is the recommended procedure to introduce a desired time delay between the ADF4030 BSYNC clocks. The ADF4030 can align one target BSYNC clock to a source BSYNC clock, and this procedure is called single-channel alignment. The ADF4030 can serially align multiple target BSYNC clocks to a source BSYNC clock, and this procedure is called serial alignment. Use these procedures to introduce time adjustments that compensate the propagation delays of BSYNC clocks.

The alignment procedures use the closed-loop delay adjustment data path to achieve the desired alignment.

Single-Channel Alignment

To execute a single-channel alignment, the following steps must be executed:

1. Set Bits[7:5], ALIGN_CYCLES, in Register 0x37 to 000. This setting executes one alignment cycle only.
2. Clear Bit 2, EN_SERIAL_ALIGN, in Register 0x37 to 0 to disable a serial alignment.
3. Set Bit 6, EN_ALIGN, in Register 0x11 to 1 to enable the single-channel alignment.
4. Clear Bit 7, MANUAL_MODE, in Register 0x11 to 0 to disable the manual TDC measurement.
5. Initialize Bits[3:0], AVGEXP, in Register 0x16. This procedure represents the TDC averaging number of samples. The bigger the number, the more accurate the TDC measurement. The initialization procedure (see the Device Initialization section) sets this to six, which means the TDC averages 4096 measurements to produce a result.
6. Initialize Bits[4:0], TDC_SOURCE, in Register 0x11 to select which BSYNC channel is the TDC source clock.
7. Initialize Bit 5, TDC_CLK_SEL, in Register 0x11 to select TDC source clock or the TDC target clock as the period clock.
8. Initialize Bits[7:6], FALL_EDGE_SRC and FALL_EDGE_TGT, in Register 0x15 to select the clock edge of the TDC source and target clocks used by the TDC.
9. Set the desired time delay in Bits [15:0], TDC_OFFSETx, signed register that corresponds to the target BSYNC channel. Also use Bits[20:0], TDC_OFFSET_COM, signed register if necessary (see Closed-Loop Delay Adjustment section). The bit weight of these registers is ~$1/f_{VCO}/2^9$, that is 0.78125 ps when f_{VCO} = 2.5 GHz.
10. Initialize Bits[4:0], TDC_TARGET, in Register 0x10 to select which BSYNC channel is the TDC target clock. This starts the alignment procedure.
11. Monitor Bit 0, FSM_BUSY, in Register 0x8F. The signal stays 1 while the ADF4030 executes the alignment and clears to 0 when the alignment ends.
12. Verify Bits[2:1], TDC_ERR, in Register 0x90 are 00 (see the TDC Status section). If not, repeat the procedure starting with Step 10.
13. Verify Bit 3, TMP_ALIGN_ERR, in Register 0x90 is cleared to 0 (see the Temporary Alignment Error IRQ section). If not, repeat the procedure starting with Step 10.
14. Optionally, execute a TDC measurement between the BSYNC channels object to the alignment to verify the achieved alignment error is below 1.4 ps, the bit weight of the ADEL_x bits.

If the achieved phase delay error is greater than 1.4 ps or an even better result is desired, the alignment process may be repeated. Repeat execution of the procedure starting from Step 10.

Instead of executing these last five steps again, the ADF4030 offers the following two ways of repeating the single-channel alignment: repeat the alignment process until the alignment becomes better than a threshold, which is called threshold iteration alignment, or repeat the alignment process for a fixed number of times, which is called fixed number of iterations alignment.

A gapped periodic clock can only be aligned to a nongapped periodic clock. The recommended alignment procedure follows:

- Measure the time difference between the gapped clock and the nongapped clock.
- If the time difference is ≥+350 ps, execute the single-channel alignment procedure. The resultant alignment error is within ± 5 ps at room temperature.
- If the time difference is <+350 ps, including negative values, the resultant alignment error may be bigger. In this case, generate a nongapped periodic clock first, instead of a gapped one. Align it to the nongapped periodic clock of the same frequency. Then, generate the gapped clock again. This introduces an additional approximate alignment error of ± 3 ps at room temperature.

Threshold Alignment

The threshold alignment procedure repeats the alignment until either the alignment becomes lower than a desired threshold or the alignment cycles reach the maximum number of alignment cycles stored in the ALIGN_CYCLES bit field. The following steps must be executed:

1. Set Bits[5:0], ALIGN_THOLD, in Register 0x35 to the desired alignment threshold. The adjustment weight of the LSB is equal to the LSB weight of the ADEL_x bits, that is approximately 1.4 ps. ALIGN_THOLD = 1 is the recommended alignment threshold. If the system is relatively noisy, increase the ALIGN_THOLD value only.
2. Initialize Bits[7:5], ALIGN_CYCLES, in Register 0x37 with the desired maximum number of alignment cycles to be executed minus one. The maximum allowed number of iterations is eight.
3. Initialize Bit 1, EN_CYCS_RED, in Register 0x37 to decide how many averages of the TDC time stamps are executed each iteration as follows:

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- If EN_CYCS_RED = 0, every alignment cycles uses $AVG = 64 \times 2^{AVGEXP}$ the TDC time stamps (see also TDC Time Stamp Averaging section for more details on the AVGEXP).
- If EN_CYCS_RED = 1, the first alignment cycle uses $AVG = 64 \times 2^{AVGEXP - ALIGN\_CYCLES}$ the TDC time stamps. Each successive alignment cycle uses a number of the TDC time stamps equal to the previous cycle AVG multiplied by 2.

4. Set Bit 0, EN_ITER, in Register 0x37 to enable the threshold alignment.
5. Execute the steps of the single-channel alignment procedure.

Fixed Iteration Alignment

The fixed iteration alignment procedure repeats the alignment for the number of cycles stored in the ALIGN_CYCLES bit field. The following steps must be executed:

- Initialize Bits[7:5], ALIGN_CYCLES, in Register 0x37 with the desired number of alignment cycles to be executed minus one. The maximum number of iterations is eight, which is the number of iterations recommended to use for best performance (ALIGN_CYCLES = 7). Normally, this setting gives better results than the threshold alignment procedure configured with the ALIGN_THOLD = 1.
- Initialize Bit 1, EN_CYCS_RED, in Register 0x37 to decide how many averages of the TDC time stamps are executed each iteration. See the Threshold Alignment section for more details.
- Clear Bit 0, EN_ITER, in Register 0x37 to disable the threshold iteration alignment.
- Execute the steps of the single-channel alignment procedure.

Serial Alignment

All the alignment procedures presented until now, single-channel, threshold iteration, and fixed iteration, align one single BSYNC channel to a source BSYNC clock. The ADF4030 can align several BSYNC channels serially, one after the other, in numerical order. If the TDC source channel is an incoming clock, select any BSYNC channel as the TDC source. If the TDC source channel is an outgoing clock, choose the lowest numbered BSYNC channel as the TDC source.

To execute the serial alignment procedure, the following steps must be executed:

- Identify the desired BSYNC channels to align in Bits[7:6], BSYNC_CAL_ON[1:0], in Register 0x35 and in Bits[7:0], BSYNC_CAL_ON[9:2], in Register 0x36. Each bit corresponds to one BSYNC channel. When set to 1, BSYNC_CAL_ON[0] includes the BSYNC0 channel into the serial procedure, BSYNC_CAL_ON[1] includes the BSYNC1 channel, continuing consecutively to BSYNC_CAL_ON[9] including the BSYNC9 channel.
- When the TDC source channel is an incoming clock, to reduce the power consumption during the serial alignment, set the ADF4030 to power down the drivers of all BSYNC channels that are not being used in real time. This is done by setting Bit 4, AUTO_PD_BG, in Register 0x37 to 1.
- When the TDC source is an outgoing clock, set to 1 the BSYNC_CAL_ON bit of the BSYNC channel identified as the TDC source to include the channel into the procedure. Then clear the AUTO_PD_BG bit to 0. When the AUTO_PD_BG bit is set to 1, it disables the driver of the TDC source, stopping the serial alignment process.
- Introduce the desired time delay in the TDC_OFFSETx[15:0] signed registers that correspond to all targeted BSYNC channels. Use the TDC_OFFSET_COM[20:0] signed register also, if necessary.
- Execute the steps of the threshold iteration or the fixed iteration alignment procedures. To start the alignment procedure, there is no need to identify the TDC_TARGET bits in the Register 0x10. Any writing to the Register 0x10 starts the procedure.

Background Serial Alignment

The ADF4030 can also automatically and continuously align BSYNC channels in the background until the controller stops the procedure. No SPI commands are required while the ADF4030 executes the procedure. After every passage through all BSYNC channels identified in Bits[9:0], BSYNC_CAL_ON, a temperature measurement is also executed. Then, the procedure starts another alignment cycle and continues the procedure until stopped.

If the TDC source channel is an incoming clock, select any BSYNC channel as TDC source. The background serial alignment procedure does not work when the TDC source channel is an outgoing clock.

To execute the background serial alignment, the following steps must be executed:

1. Set Bit 3, EN_BKGND_ALGN, in Register 0x37 to 1 to enable the background serial alignment procedure.
2. Initialize the temperature measurement:
   a. Write the K divider value in Register 0x62.
   b. Clear Bit 6, ADC_CLK_SEL, in Register 0x61 to 0.
   c. Set Bit 1, EN_ADC_CLK, in Register 0x61 to 1.
   d. Set Bit 2, EN_ADC_CNV, in Register 0x61 to 1.
   e. Set Bit 0, EN_ADC, in Register 0x61 to 1. Bit 6, Bit 2, Bit 1, and Bit 0 in Register 0x61 may be written simultaneously.
   f. Clear Bit 4, PD_ADC, in Register 0x3C to 0.
3. Select the BSYNC channels to align continuously in the background in Bits[9:0], BSYNC_CAL_ON, in Register 0x35 and Register 0x36 by setting the corresponding bits to 1.
4. To reduce the power consumption during the background alignment, set the ADF4030 to power down the drivers of all BSYNC

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channels that are not being used in real time. This is done by setting Bit 4, AUTO_PD_BG, in Register 0x37 to 1.

5. Execute Step 1 to Step 8 of the single channel automatic alignment procedure (see the Single-Channel Alignment section).
6. Introduce the desired time delay in the TDC_OFFSETx[15:0] signed registers that correspond to all targeted BSYNC channels. Also use the TDC_OFFSET_COM[20:0] signed register if necessary.
7. Execute a write with any value to the Register 0x10 to start the procedure. Bits[5:0], TDC_TARGET, in Register 0x10 may have any value.

The background serial alignment mode does not execute the threshold iteration or the fixed number of iterations alignment procedures. It ignores the bits that configure these modes.

To immediately stop the background serial alignment, set Bit 6, STOP_FSM, in Register 0x17 to 1. Then, clear it back to 0. To stop the background serial alignment after the ADF4030 completes the current alignment cycle, that is, after all BSYNC channels identified by the BSYNC_CAL_ON bits have been aligned, clear the EN_BKGND_ALGN bit to 0.

MEASURING ALIGNMENT RESULTS

To measure the time alignment between various BSYNC clocks, execute the following steps:

- Always use both + and − lines of the particular BSYNC channel to probe the clock.
- Use instruments that can subtract the + and − signals in real time to create a differential BSYNC clock.
- The differential BSYNC clock has jitter (see Table 1). Average several clock edges. More averaging means less jitter and better alignment measurement accuracy. Choose the particular number of averages as a function of the clock noise.
- Measure the time delay between the averaged clock edges. Typically, the BSYNC alignment errors are much lower than 1 ps.

REGISTER MAP

Table 16. ADF4030 Register Map

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	REG0000	[7:0]	SOFT_RESET	LSB_FIRST	ADDRESS_ASCENSION	SDO_ACTIVE	SDO_ACTIVE	ADDRESS_ASCENSION	LSB_FIRST	SOFT_RESET	0x00	R/W
0x01	REG0001	[7:0]	SINGLE_INSTRUCTION	REG01_RSV6	MASTER_READBACK_CONTROL	REG01_RSV4	RESERVED	REG01_RSV1	REG01_RSV0	RESERVED	0x00	R/W
0x02	REG0002	[7:0]	RESERVED				CHIP_STATUS				0x00	R
0x03	REG0003	[7:0]	RESERVED				CHIP_TYPE				0x00	R
0x04	REG0004	[7:0]	PRODUCT_ID[7:0]								0x0A	R
0x05	REG0005	[7:0]	PRODUCT_ID[15:8]								0x00	R
0x06	REG0006	[7:0]	PRODUCT_GRADE				DEVICE_REVISION				0x00	R
0x07	REG0007	[7:0]	RESERVED								0x00	R/W
0x08	REG0008	[7:0]	RESERVED								0x00	R/W
0x09	REG0009	[7:0]	RESERVED								0x00	R/W
0x0A	REG000A	[7:0]	SCRATCHPAD								0x00	R/W
0x0B	REG000B	[7:0]	SPI_REVISION								0x00	R
0x0C	REG000C	[7:0]	VENDOR_ID[7:0]								0x56	R
0x0D	REG000D	[7:0]	VENDOR_ID[15:8]								0x04	R
0x0E	REG000E	[7:0]	RESERVED								0x00	R/W
0x0F	REG000F	[7:0]	RESERVED							REG0F_RSV0	0x00	R/W
0x10	REG0010	[7:0]	RESERVED			TDC_TARGET					0x00	R/W
0x11	REG0011	[7:0]	MANUAL_MODE	EN_ALIGN	RESERVED	TDC_SOURCE					0x00	R/W
0x12	REG0012	[7:0]	EN_DRV7	EN_DRV6	EN_DRV5	EN_DRV4	EN_DRV3	EN_DRV2	EN_DRV1	EN_DRV0	0x00	R/W
0x13	REG0013	[7:0]	PRBS5	PRBS4	PRBS3	PRBS2	PRBS1	PRBS0	EN_DRV9	EN_DRV8	0x00	R/W
0x14	REG0014	[7:0]	CHAN_INV3	CHAN_INV2	CHAN_INV1	CHAN_INV0	PRBS9	PRBS8	PRBS7	PRBS6	0x00	R/W
0x15	REG0015	[7:0]	FALL_EDGE_SRC	FALL_EDGE_TGT	CHAN_INV9	CHAN_INV8	CHAN_INV7	CHAN_INV6	CHAN_INV5	CHAN_INV4	0x00	R/W
0x16	REG0016	[7:0]	TDC_ARM_M	RESERVED			AVGEXP				0x00	R/W
0x17	REG0017	[7:0]	NDEL_ADJ	STOP_FSM	ADEL						0x00	R/W
0x18	REG0018	[7:0]	DELTA_NDEL_COAR[7:0]								0x00	R/W
0x19	REG0019	[7:0]	DELTA_NDEL_COAR[15:8]								0x00	R/W
0x1A	REG001A	[7:0]	TDC_OFFSET_COM[7:0]								0x00	R/W
0x1B	REG001B	[7:0]	TDC_OFFSET_COM[15:8]								0x00	R/W
0x1C	REG001C	[7:0]	RESERVED			TDC_OFFSET_COM[20:16]					0x00	R/W
0x1D	REG001D	[7:0]	TDC_OFFSET0[7:0]								0x00	R/W
0x1E	REG001E	[7:0]	TDC_OFFSET0[15:8]								0x00	R/W
0x1F	REG001F	[7:0]	TDC_OFFSET1[7:0]								0x00	R/W
0x20	REG0020	[7:0]	TDC_OFFSET1[15:8]								0x00	R/W
0x21	REG0021	[7:0]	TDC_OFFSET2[7:0]								0x00	R/W
0x22	REG0022	[7:0]	TDC_OFFSET2[15:8]								0x00	R/W

REGISTER MAP

Table 16. ADF4030 Register Map (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x23	REG0023	[7:0]	TDC_OFFSET3[7:0]								0x00	R/W
0x24	REG0024	[7:0]	TDC_OFFSET3[15:8]								0x00	R/W
0x25	REG0025	[7:0]	TDC_OFFSET4[7:0]								0x00	R/W
0x26	REG0026	[7:0]	TDC_OFFSET4[15:8]								0x00	R/W
0x27	REG0027	[7:0]	TDC_OFFSET5[7:0]								0x00	R/W
0x28	REG0028	[7:0]	TDC_OFFSET5[15:8]								0x00	R/W
0x29	REG0029	[7:0]	TDC_OFFSET6[7:0]								0x00	R/W
0x2A	REG002A	[7:0]	TDC_OFFSET6[15:8]								0x00	R/W
0x2B	REG002B	[7:0]	TDC_OFFSET7[7:0]								0x00	R/W
0x2C	REG002C	[7:0]	TDC_OFFSET7[15:8]								0x00	R/W
0x2D	REG002D	[7:0]	TDC_OFFSET8[7:0]								0x00	R/W
0x2E	REG002E	[7:0]	TDC_OFFSET8[15:8]								0x00	R/W
0x2F	REG002F	[7:0]	TDC_OFFSET9[7:0]								0x00	R/W
0x30	REG0030	[7:0]	TDC_OFFSET9[15:8]								0x00	R/W
0x31	REG0031	[7:0]	RESERVED								0x40	R/W
0x32	REG0032	[7:0]	RESERVED								0x00	R/W
0x33	REG0033	[7:0]	RESERVED								0x00	R/W
0x34	REG0034	[7:0]	ONE_SHOT	CYCLES	DELCAL						0x3F	R/W
0x35	REG0035	[7:0]	BSYNC_CAL_ON[1:0]		ALIGN_THOLD						0x00	R/W
0x36	REG0036	[7:0]	BSYNC_CAL_ON[9:2]								0x00	R/W
0x37	REG0037	[7:0]	ALIGN_CYCLES			AU-TO_PD_BG	EN_BKGND_ALGN	EN_SERI-AL_ALIGN	EN_CYCS_RED	EN_ITER	0x02	R/W
0x38	REG0038	[7:0]	RST_BSYNC_CH[7:0]								0x00	R/W
0x39	REG0039	[7:0]	RST_SYS	MSTR_RST_BSYNC	RESERVED				RST_BSYNC_CH[9:8]		0x00	R/W
0x3A	REG003A	[7:0]	PD_DRV7	PD_DRV6	PD_DRV5	PD_DRV4	PD_DRV3	PD_DRV2	PD_DRV1	PD_DRV0	0x00	R/W
0x3B	REG003B	[7:0]	PD_TX_PATH5	PD_TX_PATH4	PD_TX_PATH3	PD_TX_PATH2	PD_TX_PATH1	PD_TX_PATH0	PD_DRV9	PD_DRV8	0x00	R/W
0x3C	REG003C	[7:0]	PD_ALL	PD_PLL	PD_TDC	PD_ADC	PD_TX_PATH9	PD_TX_PATH8	PD_TX_PATH7	PD_TX_PATH6	0x80	R/W
0x3D	REG003D	[7:0]	RESERVED								0x00	R/W
0x3E	REG003E	[7:0]	RESERVED								0x00	R/W
0x3F	REG003F	[7:0]	ODIV_SEL0	BOOST0	RCM0						0x00	R/W
0x40	REG0040	[7:0]	AU-TO_PD_RCV_0	RESERVED	FLOAT_RX0	FLOAT_TX0	LINK_RX_0	LINK_TX0	AC_COU-PLED0	RESERVED	0x00	R/W
0x41	REG0041	[7:0]	ODIV_SEL1	BOOST1	RCM1						0x00	R/W
0x42	REG0042	[7:0]	AU-TO_PD_RCV_1	RESERVED	FLOAT_RX1	FLOAT_TX1	LINK_RX_1	LINK_TX1	AC_COU-PLED1	RESERVED	0x00	R/W
0x43	REG0043	[7:0]	ODIV_SEL2	BOOST2	RCM2						0x00	R/W
0x44	REG0044	[7:0]	AU-TO_PD_RCV_2	RESERVED	FLOAT_RX2	FLOAT_TX2	LINK_RX_2	LINK_TX2	AC_COU-PLED2	RESERVED	0x00	R/W

REGISTER MAP

Table 16. ADF4030 Register Map (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x45	REG0045	[7:0]	ODIV_SEL3	BOOST3	RCM3						0x00	R/W
0x46	REG0046	[7:0]	AUTO_PD_RCV_3	RESERVED	FLOAT_RX3	FLOAT_TX3	LINK_RX_3	LINK_TX3	AC_COUPLED3	RESERVED	0x00	R/W
0x47	REG0047	[7:0]	ODIV_SEL4	BOOST4	RCM4						0x00	R/W
0x48	REG0048	[7:0]	AUTO_PD_RCV_4	RESERVED	FLOAT_RX4	FLOAT_TX4	LINK_RX_4	LINK_TX4	AC_COUPLED4	RESERVED	0x00	R/W
0x49	REG0049	[7:0]	ODIV_SEL5	BOOST5	RCM5						0x00	R/W
0x4A	REG004A	[7:0]	AUTO_PD_RCV_5	RESERVED	FLOAT_RX5	FLOAT_TX5	LINK_RX_5	LINK_TX5	AC_COUPLED5	RESERVED	0x00	R/W
0x4B	REG004B	[7:0]	ODIV_SEL6	BOOST6	RCM6						0x00	R/W
0x4C	REG004C	[7:0]	AUTO_PD_RCV_6	RESERVED	FLOAT_RX6	FLOAT_TX6	LINK_RX_6	LINK_TX6	AC_COUPLED6	RESERVED	0x00	R/W
0x4D	REG004D	[7:0]	ODIV_SEL7	BOOST7	RCM7						0x00	R/W
0x4E	REG004E	[7:0]	AUTO_PD_RCV_7	RESERVED	FLOAT_RX7	FLOAT_TX7	LINK_RX_7	LINK_TX7	AC_COUPLED7	RESERVED	0x00	R/W
0x4F	REG004F	[7:0]	ODIV_SEL8	BOOST8	RCM8						0x00	R/W
0x50	REG0050	[7:0]	AUTO_PD_RCV_8	RESERVED	FLOAT_RX8	FLOAT_TX8	LINK_RX_8	LINK_TX8	AC_COUPLED8	RESERVED	0x00	R/W
0x51	REG0051	[7:0]	ODIV_SEL9	BOOST9	RCM9						0x00	R/W
0x52	REG0052	[7:0]	AUTO_PD_RCV_9	RESERVED	FLOAT_RX9	FLOAT_TX9	LINK_RX_9	LINK_TX9	AC_COUPLED9	RESERVED	0x00	R/W
0x53	REG0053	[7:0]	ODIVA[7:0]								0x40	R/W
0x54	REG0054	[7:0]	ODIVB[3:0]				ODIVA[11:8]				0x00	R/W
0x55	REG0055	[7:0]	ODIVB[11:4]								0x00	R/W
0x56	REG0056	[7:0]	NDIV[7:0]								0x14	R/W
0x57	REG0057	[7:0]	RESERVED	CP_I	RDIV						0x01	R/W
0x58	REG0058	[7:0]	SEL_DIGCLK	EN_DIGCLK	CORE_CLK_DIV		RESERVED				0x00	R/W
0x59	REG0059	[7:0]	RST_LD	BAND_SEL_M			RESERVED				0x09	R/W
0x5A	REG005A	[7:0]	RST_PLL_CAL	PLL_CAL_EN	PLL_CAL_CNT		RESERVED				0x47	R/W
0x5B	REG005B	[7:0]	EN_LOL	EN_LDWIN	LDWIN_PW	LD_COUNT					0x00	R/W
0x5C	REG005C	[7:0]	CMOS_OV	RST_ALIGN_IRQ	RST_TEMP	MASK_TDC_ERR	MASK_LD	MASK_ALIGN_IRQ	MASK_TEMP	IRQB_OPEN DRAIN	0x00	R/W
0x5D	REG005D	[7:0]	ALIGN_IRQ_TH								0x00	R/W
0x5E	REG005E	[7:0]	TEMP_IRQ_TH								0x00	R/W
0x5F	REG005F	[7:0]	RESERVED								0x00	R/W
0x60	REG0060	[7:0]	RESERVED	ADC_C_CNV	RESERVED						0x00	R/W

REGISTER MAP

Table 16. ADF4030 Register Map (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x61	REG0061	[7:0]	RST_TDC_ERR	ADC_CLK_SEL	RESERVED			EN_ADC_CNV	EN_ADC_CLK	EN_ADC	0x00	R/W
0x62	REG0062	[7:0]	ADC_CLK_DIV								0x00	R/W
0x63	REG0063	[7:0]	RESERVED			MUXCODE1					0x00	R/W
0x64	REG0064	[7:0]	RESERVED			MUXCODE2					0x00	R/W
0x65	REG0065	[7:0]	RESERVED								0x00	R/W
0x66	REG0066	[7:0]	RESERVED								0x00	R/W
0x67	REG0067	[7:0]	RESERVED								0x00	R/W
0x68	REG0068	[7:0]	GPO2	GPO1	RESERVED						0x00	R/W
0x69	REG0069	[7:0]	RESERVED								0x00	R/W
0x6A	REG006A	[7:0]	RESERVED								0x00	R/W
0x6B	REG006B	[7:0]	RESERVED								0x00	R/W
0x6C	REG006C	[7:0]	RESERVED								0x00	R/W
0x6D	REG006D	[7:0]	RESERVED								0x00	R/W
0x6E	REG006E	[7:0]	RESERVED								0x00	R/W
0x6F	REG006F	[7:0]	RESERVED								0x00	R/W
0x70	REG0070	[7:0]	RESERVED								0x00	R
0x71	REG0071	[7:0]	RESERVED								0x00	R/W
0x72	REG0072	[7:0]	RESERVED							ADC_ST_CNV	0x00	R/W
0x73	REG0073	[7:0]	TDC_RSLT_UI[7:0]								0x00	R
0x74	REG0074	[7:0]	TDC_RSLT_UI[15:8]								0x00	R
0x75	REG0075	[7:0]	TDC_RSLT_UI[23:16]								0x00	R
0x76	REG0076	[7:0]	RESERVED								0x00	R
0x77	REG0077	[7:0]	TIMEDIFF_MEAS[7:0]								0x00	R
0x78	REG0078	[7:0]	TIMEDIFF_MEAS[15:8]								0x00	R
0x79	REG0079	[7:0]	TIMEDIFF_MEAS[23:16]								0x00	R
0x7A	REG007A	[7:0]	TIMEDIFF_MEAS[31:24]								0x00	R
0x7B	REG007B	[7:0]	RESERVED						TIMEDIFF_MEAS[33:32]		0x00	R
0x7C	REG007C	[7:0]	RESERVED								0x00	R
0x7D	REG007D	[7:0]	PERIOD_MEAS[7:0]								0x00	R
0x7E	REG007E	[7:0]	PERIOD_MEAS[15:8]								0x00	R
0x7F	REG007F	[7:0]	PERIOD_MEAS[23:16]								0x00	R
0x80	REG0080	[7:0]	PERIOD_MEAS[31:24]								0x00	R
0x81	REG0081	[7:0]	ALIGN_TOT[7:0]								0x00	R
0x82	REG0082	[7:0]	ALIGN_TOT[15:8]								0x00	R
0x83	REG0083	[7:0]	RESERVED		ALIGN_TOT[21:16]						0x00	R
0x84	REG0084	[7:0]	RESERVED		ADEL_0						0x00	R
0x85	REG0085	[7:0]	RESERVED		ADEL_1						0x00	R
0x86	REG0086	[7:0]	RESERVED		ADEL_2						0x00	R
0x87	REG0087	[7:0]	RESERVED		ADEL_3						0x00	R
0x88	REG0088	[7:0]	RESERVED		ADEL_4						0x00	R
0x89	REG0089	[7:0]	RESERVED		ADEL_5						0x00	R

REGISTER MAP

Table 16. ADF4030 Register Map (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x8A	REG008A	[7:0]	RESERVED		ADEL_6						0x00	R
0x8B	REG008B	[7:0]	RESERVED		ADEL_7						0x00	R
0x8C	REG008C	[7:0]	RESERVED		ADEL_8						0x00	R
0x8D	REG008D	[7:0]	RESERVED		ADEL_9						0x00	R
0x8E	REG008E	[7:0]	RESERVED					ALIGN_CYCLES_COUNT			0x00	R
0x8F	REG008F	[7:0]	RESERVED	REF_OK	RESERVED	TDC_BUSY	DL_BUSY	MATH_BUSY	ADC_BUSY	FSM_BUSY	0x00	R
0x90	REG0090	[7:0]	IRQ_BSYNC[1:0]		RESERVED	TEMP_MON	TMP_ALIGN_ERR	TDC_ERR		PLL_LD	0x00	R
0x91	REG0091	[7:0]	IRQ_BSYNC[9:2]								0x00	R
0x92	REG0092	[7:0]	TEMP_MEAS[7:0]								0x00	R
0x93	REG0093	[7:0]	RESERVED							TEMP_MEAS[8]	0x00	R
0x94	REG0094	[7:0]	RESERVED								0x00	R
0x95	REG0095	[7:0]	RESERVED		DLY_TAP_STATE1			DLY_TAP_STATE0			0x00	R
0x96	REG0096	[7:0]	RESERVED		DLY_TAP_STATE3			DLY_TAP_STATE2			0x00	R
0x97	REG0097	[7:0]	RESERVED		DLY_TAP_STATE5			DLY_TAP_STATE4			0x00	R
0x98	REG0098	[7:0]	RESERVED		DLY_TAP_STATE7			DLY_TAP_STATE6			0x00	R
0x99	REG0099	[7:0]	RESERVED		DLY_TAP_STATE9			DLY_TAP_STATE8			0x00	R
0x9A	REG009A	[7:0]	ACCUM_DEL_0[7:0]								0x00	R
0x9B	REG009B	[7:0]	RESERVED						ACCUM_DEL_0[9:8]		0x00	R
0x9C	REG009C	[7:0]	ACCUM_DEL_1[7:0]								0x00	R
0x9D	REG009D	[7:0]	RESERVED						ACCUM_DEL_1[9:8]		0x00	R
0x9E	REG009E	[7:0]	ACCUM_DEL_2[7:0]								0x00	R
0x9F	REG009F	[7:0]	RESERVED						ACCUM_DEL_2[9:8]		0x00	R
0xA0	REG00A0	[7:0]	ACCUM_DEL_3[7:0]								0x00	R
0xA1	REG00A1	[7:0]	RESERVED						ACCUM_DEL_3[9:8]		0x00	R
0xA2	REG00A2	[7:0]	ACCUM_DEL_4[7:0]								0x00	R
0xA3	REG00A3	[7:0]	RESERVED						ACCUM_DEL_4[9:8]		0x00	R
0xA4	REG00A4	[7:0]	ACCUM_DEL_5[7:0]								0x00	R
0xA5	REG00A5	[7:0]	RESERVED						ACCUM_DEL_5[9:8]		0x00	R
0xA6	REG00A6	[7:0]	ACCUM_DEL_6[7:0]								0x00	R
0xA7	REG00A7	[7:0]	RESERVED						ACCUM_DEL_6[9:8]		0x00	R
0xA8	REG00A8	[7:0]	ACCUM_DEL_7[7:0]								0x00	R
0xA9	REG00A9	[7:0]	RESERVED						ACCUM_DEL_7[9:8]		0x00	R
0xAA	REG00AA	[7:0]	ACCUM_DEL_8[7:0]								0x00	R
0xAB	REG00AB	[7:0]	RESERVED						ACCUM_DEL_8[9:8]		0x00	R
0xAC	REG00AC	[7:0]	ACCUM_DEL_9[7:0]								0x00	R
0xAD	REG00AD	[7:0]	RESERVED						ACCUM_DEL_9[9:8]		0x00	R
0xAE	REG00AE	[7:0]	RESERVED								0x00	R
0xAF	REG00AF	[7:0]	RESERVED								0x00	R
0xB0	REG00B0	[7:0]	RESERVED								0x00	R
0xB1	REG00B1	[7:0]	RESERVED								0x00	R
0xB2	REG00B2	[7:0]	RESERVED								0x00	R

REGISTER MAP

Table 16. ADF4030 Register Map (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0xB3	REG00B3	[7:0]	RESERVED								0x00	R
0xB4	REG00B4	[7:0]	RESERVED								0x00	R
0xB5	REG00B5	[7:0]	RESERVED								0x00	R
0xB6	REG00B6	[7:0]	RESERVED								0x00	R
0xB7	REG00B7	[7:0]	RESERVED								0x00	R
0xB8	REG00B8	[7:0]	RESERVED								0x00	R
0xB9	REG00B9	[7:0]	RESERVED								0x00	R
0xBA	REG00BA	[7:0]	RESERVED			BAND_OUT			CAL_COMP	CAL_BUSY	0x00	R
0xBB	REG00BB	[7:0]	VERSION								0x00	R
0xCA	REG00CA	[7:0]	TMP_ALIGN_ERR_CH[7:0]								0x00	R
0xCB	REG00CB	[7:0]	RESERVED						TMP_ALIGN_ERR_CH[9:8]		0x00	R
0xFF	REG00FF	[7:0]	RESERVED						EN_BRDCST	SOFTRE-SET_CHIP	0x00	R/W

REGISTER DETAILS

Address: 0x00, Reset: 0x00, Name: REG0000

Table 17. Bit Descriptions for REG0000

Bits	Bit Name	Description	Reset	Access
7	SOFT_RESET	Soft Reset. This bit must be set identical to Bit 0 (see Bit 0 for details).	0x0	R/W
6	LSB_FIRST	SPI LSB First. This bit must be set identical to Bit 1 (see Bit 1 for details).	0x0	R/W
5	ADDRESS_ASCENSION	Address Ascension. This bit must be set identical to Bit 2 (see Bit 2 for details).	0x0	R/W
4	SDO_ACTIVE	Enable SPI 4-wire mode. This bit must be set identical to Bit 3 (see Bit 3 for details).	0x0	R/W
3	SDO_ACTIVE	Enable SPI 4-wire mode. This bit selects whether the SDO pin is an active output pin (4-wire SPI mode) or tristate (3-wire SPI mode). This bit and Bit 4 of the same register must be set with the same value. 0: SDO pin tristate (SDIO pin bidirectional), 3-wire SPI mode. 1: SDO pin active output (SDIO pin input only), 4-wire SPI mode.	0x0	R/W
2	ADDRESS_ASCENSION	SPI Address Ascension. This bit controls the direction (decrement or increment) that register addressing occurs during multibyte transfers. This bit and Bit 5 of the same register must be set with the same value. 0: Decrement. 1: Increment.	0x0	R/W
1	LSB_FIRST	SPI LSB First. Bit order for the SPI port. This bit and Bit 6 of the same register must be set with the same value. 0: Most significant bit (MSB) first 1: Least significant bit (LSB) first.	0x0	R/W
0	SOFT_RESET	Soft Reset. This bit must be set to 1 together with Bit 0 of the same register to trigger a soft reset of all ADF4030 registers except for Register 0x0000. It autoclears at the next SPI SCLK clock edge. 0: Normal operation. 1: Triggers a soft reset. All ADF4030 registers, except for Register 0x0000, return to the default values.	0x0	R/W

Address: 0x01, Reset: 0x00, Name: REG0001

Table 18. Bit Descriptions for REG0001

Bits	Bit Name	Description	Reset	Access
7	SINGLE_INSTRUCTION	Single Instruction. 0: SPI streaming enabled. 1: SPI streaming disabled.	0x0	R/W
6	REG01_RSV6	Reserved.	0x0	R/W
5	MASTER_READBACK_CONTROL	Main/Subordinate Readback Control. 0: For double-buffered bit-fields readback subordinate register. 1: For double-buffered bit-fields readback main register.	0x0	R/W
4	REG01_RSV4	Reserved.	0x0	R/W
3	RESERVED	Reserved.	0x0	R
2	REG01_RSV1	Reserved.	0x0	R/W
1	REG01_RSV0	Reserved.	0x0	R/W
0	RESERVED	Reserved.	0x0	R

Address: 0x02, Reset: 0x00, Name: REG0002

Table 19. Bit Descriptions for REG0002

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	CHIP_STATUS	Not Used.	0x0	R

REGISTER DETAILS

Address: 0x03, Reset: 0x00, Name: REG0003

Table 20. Bit Descriptions for REG0003

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	CHIP_TYPE	Chip Type = 0x06.	0x0	R

Address: 0x04, Reset: 0x0A, Name: REG0004

Table 21. Bit Descriptions for REG0004

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]	This read-only 16-bit field represents the Product ID. Product_ID[7:0] bits are equal to 0x0A. Product_ID[15:8] bits are equal to 0x00.	0xA	R

Address: 0x05, Reset: 0x00, Name: REG0005

Table 22. Bit Descriptions for REG0005

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]	This read-only 16-bit field represents the Product ID. Product_ID[7:0] bits are equal to 0x0A. Product_ID[15:8] bits are equal to 0x00.	0x0	R

Address: 0x06, Reset: 0x00, Name: REG0006

Table 23. Bit Descriptions for REG0006

Bits	Bit Name	Description	Reset	Access
[7:4]	PRODUCT_GRADE	Product Grade = 0x0 (not used).	0x0	R
[3:0]	DEVICE_REVISION	Device Revision = 0x0 (not used).	0x0	R

Address: 0x07, Reset: 0x00, Name: REG0007

Table 24. Bit Descriptions for REG0007

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R

Address: 0x08, Reset: 0x00, Name: REG0008

Table 25. Bit Descriptions for REG0008

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R

Address: 0x09, Reset: 0x00, Name: REG0009

Table 26. Bit Descriptions for REG0009

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R

Address: 0x0A, Reset: 0x00, Name: REG000A

Table 27. Bit Descriptions for REG000A

Bits	Bit Name	Description	Reset	Access
[7:0]	SCRATCHPAD	SPI scratchpad.	0x0	R/W

Address: 0x0B, Reset: 0x00, Name: REG000B

Table 28. Bit Descriptions for REG000B

Bits	Bit Name	Description	Reset	Access
[7:0]	SPI_REVISION	SPI Revision = 0x01.	0x0	R

REGISTER DETAILS

Address: 0x0C, Reset: 0x56, Name: REG000C

Table 29. Bit Descriptions for REG000C

Bits	Bit Name	Description	Reset	Access
[7:0]	VENDOR_ID[7:0]	This read-only 16-bit field represents the Vendor ID. Vendor_ID[7:0] bits are equal to 0x56. Vendor_ID[15:8] bits are equal to 0x04.	0x56	R

Address: 0x0D, Reset: 0x04, Name: REG000D

Table 30. Bit Descriptions for REG000D

Bits	Bit Name	Description	Reset	Access
[7:0]	VENDOR_ID[15:8]	This read-only 16-bit field represents the Vendor ID. Vendor_ID[7:0] bits are equal to 0x56. Vendor_ID[15:8] bits are equal to 0x04.	0x4	R

Address: 0x0E, Reset: 0x00, Name: REG000E

Table 31. Bit Descriptions for REG000E

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R

Address: 0x0F, Reset: 0x00, Name: REG000F

Table 32. Bit Descriptions for REG000F

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	REG0F_RSV0	Reserved.	0x0	R/W

Address: 0x10, Reset: 0x00, Name: REG0010

Table 33. Bit Descriptions for REG0010

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R/W
[4:0]	TDC_TARGET	TDC Target Selection. This 5-bit field selects the TDC target clock. The TDC_TARGET equal to 10, 11, … , 25 and 27, 28, … , 31 are unused. Initialize these bits to 11111 after power up/reset. 00000: Source clock is RX0, the output of BSYNC0 receiver. 00001: Source clock is RX1, the output of BSYN10 receiver. 00010: Source clock is RX2, the output of BSYNC2 receiver. 00011: Source clock is RX3, the output of BSYNC3 receiver. 00100: Source clock is RX4, the output of BSYNC4 receiver. 00101: Source clock is RX5, the output of BSYNC5 receiver. 00110: Source clock is RX6, the output of BSYNC6 receiver. 00111: Source clock is RX7, the output of BSYNC7 receiver. 01000: Source clock is RX8, the output of BSYNC8 receiver. 01001: Source clock is RX9, the output of BSYNC9 receiver. 11010: Source clock is REFIN receiver output.	0x0	R/W

Address: 0x11, Reset: 0x00, Name: REG0011

Table 34. Bit Descriptions for REG0011

Bits	Bit Name	Description	Reset	Access
7	MANUAL_MODE	Set this bit to 1 to enable the BSYNC channel manual TDC measurement.	0x0	R/W
6	EN_ALIGN	This bit manages the single-channel alignment. Set this bit to 1 and clear the MANUAL_MODE bit to 0 to start the single-channel alignment. When the MANUAL_MODE bit is set to 1, the EN_ALIGN bit can have any value.	0x0	R/W
5	RESERVED	Reserved.	0x0	R/W
[4:0]	TDC_SOURCE	TDC Source Selection. This 5-bit field selects the TDC source clock. The TDC_SOURCE equal to 10, 11, … , 25 and 27, 28, … , 31 are unused. Initialize these bits to 11111 after power up/reset.	0x0	R/W

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Table 34. Bit Descriptions for REG0011 (Continued)

Bits	Bit Name	Description	Reset	Access
		00000: Source clock is RX0, the output of BSYNC0 receiver. 00001: Source clock is RX1, the output of BSYNC1 receiver. 00010: Source clock is RX2, the output of BSYNC2 receiver. 00011: Source clock is RX3, the output of BSYNC3 receiver. 00100: Source clock is RX4, the output of BSYNC4 receiver. 00101: Source clock is RX5, the output of BSYNC5 receiver. 00110: Source clock is RX6, the output of BSYNC6 receiver. 00111: Source clock is RX7, the output of BSYNC7 receiver. 01000: Source clock is RX8, the output of BSYNC8 receiver. 01001: Source clock is RX9, the output of BSYNC9 receiver. 11010: Source clock is REFIN receiver output.		

Address: 0x12, Reset: 0x00, Name: REG0012

Table 35. Bit Descriptions for REG0012

Bits	Bit Name	Description	Reset	Access
7	EN_DRV7	BSYNC 7 Transmit—Receive Control. This bit selects the BSYNC 7 channel to transmit or receive a clock signal. 0: BSYNC 7 channel receives a clock signal (default). 1: BSYNC 7 channel transmits a clock signal.	0x0	R/W
6	EN_DRV6	BSYNC 6 Transmit—Receive Control. This bit selects the BSYNC 6 channel to transmit or receive a clock signal. 0: BSYNC 6 channel receives a clock signal (default). 1: BSYNC 6 channel transmits a clock signal.	0x0	R/W
5	EN_DRV5	BSYNC 5 Transmit—Receive Control. This bit selects the BSYNC 5 channel to transmit or receive a clock signal. 0: BSYNC 5 channel receives a clock signal (default). 1: BSYNC 5 channel transmits a clock signal.	0x0	R/W
4	EN_DRV4	BSYNC 4 Transmit—Receive Control. This bit selects the BSYNC 4 channel to transmit or receive a clock signal. 0: BSYNC 4 channel receives a clock signal (default). 1: BSYNC 4 channel transmits a clock signal.	0x0	R/W
3	EN_DRV3	BSYNC 3 Transmit—Receive Control. This bit selects the BSYNC 3 channel to transmit or receive a clock signal. 0: BSYNC 3 channel receives a clock signal (default). 1: BSYNC 3 channel transmits a clock signal.	0x0	R/W
2	EN_DRV2	BSYNC 2 Transmit—Receive Control. This bit selects the BSYNC 2 channel to transmit or receive a clock signal. 0: BSYNC 2 channel receives a clock signal (default). 1: BSYNC 2 channel transmits a clock signal.	0x0	R/W
1	EN_DRV1	BSYNC 1 Transmit—Receive Control. This bit selects the BSYNC 1 channel to transmit or receive a clock signal. 0: BSYNC 1 channel receives a clock signal (default). 1: BSYNC 1 channel transmits a clock signal.	0x0	R/W
0	EN_DRV0	BSYNC 0 Transmit—Receive Control. This bit selects the BSYNC0 channel to transmit or receive a clock signal. 0: BSYNC 0 channel receives a clock signal (default). 1: BSYNC 0 channel transmits a clock signal.	0x0	R/W

Address: 0x13, Reset: 0x00, Name: REG0013

Table 36. Bit Descriptions for REG0013

Bits	Bit Name	Description	Reset	Access
7	PRBS5	BSYNC5 Gapped Periodic Clock Output Enable. This bit selects the BSYNC5 channel to output a gapped or a nongapped periodic clock signal. 0: BSYNC5 channel ODIV divider outputs a nongapped clock signal (default) 1: BSYNC5 channel ODIV divider outputs a gapped clock signal	0x0	R/W
6	PRBS4	BSYNC4 Gapped Periodic Clock Output Enable. This bit selects the BSYNC4 channel to output a gapped or a nongapped periodic clock signal.	0x0	R/W

REGISTER DETAILS

Table 36. Bit Descriptions for REG0013 (Continued)

Bits	Bit Name	Description	Reset	Access
		0: BSYNC4 channel ODIV divider outputs a nongapped clock signal (default). 1: BSYNC4 channel ODIV divider outputs a gapped clock signal.		
5	PRBS3	BSYNC3 Gapped Periodic Clock Output Enable. This bit selects the BSYNC3 channel to output a gapped or a nongapped periodic clock signal. 0: BSYNC3 channel ODIV divider outputs a nongapped clock signal (default). 1: BSYNC3 channel ODIV divider outputs a gapped clock signal.	0x0	R/W
4	PRBS2	BSYNC2 Gapped Periodic Clock Output Enable. This bit selects the BSYNC2 channel to output a gapped or a nongapped periodic clock signal. 0: BSYNC2 channel ODIV divider outputs a nongapped clock signal (default). 1: BSYNC2 channel ODIV divider outputs a gapped clock signal.	0x0	R/W
3	PRBS1	BSYNC1 Gapped Periodic Clock Output Enable. This bit selects the BSYNC1 channel to output a gapped or a nongapped periodic clock signal. 0: BSYNC1 channel ODIV divider outputs a nongapped clock signal (default). 1: BSYNC1 channel ODIV divider outputs a gapped clock signal.	0x0	R/W
2	PRBS0	BSYNC0 Gapped Periodic Clock Output Enable. This bit selects the BSYNC0 channel to output a gapped or a nongapped periodic clock signal. 0: BSYNC0 channel ODIV divider outputs a nongapped clock signal (default). 1: BSYNC0 channel ODIV divider outputs a gapped clock signal.	0x0	R/W
1	EN_DRV9	BSYNC9 Transmit—Receive Control. This bit selects the BSYNC 9 channel to transmit or receive a clock signal. 0: BSYNC 9 channel receives a clock signal (default). 1: BSYNC 9 channel transmits a clock signal.	0x0	R/W
0	EN_DRV8	BSYNC8 Transmit—Receive Control. This bit selects the BSYNC 8 channel to transmit or receive a clock signal. 0: BSYNC 8 channel receives a clock signal (default). 1: BSYNC 8 channel transmits a clock signal.	0x0	R/W

Address: 0x14, Reset: 0x00, Name: REG0014

Table 37. Bit Descriptions for REG0014

Bits	Bit Name	Description	Reset	Access
7	CHAN_INV3	BSYNC3 Output Polarity Control. This bit selects if the analog delay block inverts the BSYNC 3 channel output. 0: Analog delay block does not invert the BSYNC3 channel output (default). 1: Analog delay block inverts the BSYNC3 channel output.	0x0	R/W
6	CHAN_INV2	BSYNC2 Output Polarity Control. This bit selects if the analog delay block inverts the BSYNC 2 channel output. 0: Analog delay block does not invert the BSYNC2 channel output (default). 1: Analog delay block inverts the BSYNC2 channel output.	0x0	R/W
5	CHAN_INV1	BSYNC1 Output Polarity Control. This bit selects if the analog delay block inverts the BSYNC 1 channel output. 0: Analog delay block does not invert the BSYNC1 channel output (default). 1: Analog delay block inverts the BSYNC1 channel output.	0x0	R/W
4	CHAN_INV0	BSYNC0 Output Polarity Control. This bit selects if the analog delay block inverts the BSYNC 0 channel output. 0: Analog delay block does not invert the BSYNC0 channel output (default). 1: Analog delay block inverts the BSYNC0 channel output.	0x0	R/W
3	PRBS9	BSYNC9 Gapped Periodic Clock Output Enable. This bit selects the BSYNC9 channel to output a gapped or a nongapped periodic clock signal. 0: BSYNC9 channel ODIV divider outputs a nongapped clock signal (default). 1: BSYNC9 channel ODIV divider outputs a gapped clock signal.	0x0	R/W
2	PRBS8	BSYNC8 Gapped Periodic Clock Output Enable. This bit selects the BSYNC8 channel to output a gapped or a nongapped periodic clock signal. 0: BSYNC8 channel ODIV divider outputs a nongapped clock signal (default). 1: BSYNC8 channel ODIV divider outputs a gapped clock signal.	0x0	R/W

REGISTER DETAILS

Table 37. Bit Descriptions for REG0014 (Continued)

Bits	Bit Name	Description	Reset	Access
1	PRBS7	BSYNC7 Gapped Periodic Clock Output Enable. This bit selects the BSYNC7 channel to output a gapped or a nongapped periodic clock signal. 0: BSYNC7 channel ODIV divider outputs a nongapped clock signal (default). 1: BSYNC7 channel ODIV divider outputs a gapped clock signal.	0x0	R/W
0	PRBS6	BSYNC6 Gapped Periodic Clock Output Enable. This bit selects the BSYNC6 channel to output a gapped or a nongapped periodic clock signal. 0: BSYNC6 channel ODIV divider outputs a nongapped clock signal (default). 1: BSYNC6 channel ODIV divider outputs a gapped clock signal.	0x0	R/W

Address: 0x15, Reset: 0x00, Name: REG0015

Table 38. Bit Descriptions for REG0015

Bits	Bit Name	Description	Reset	Access
7	FALL_EDGE_SRC	Selects which source clock signal edge is used by the TDC measurements. 0: TDC uses rising edges of the source clock signal (default). 1: TDC uses falling edges of the source clock signal.	0x0	R/W
6	FALL_EDGE_TGT	Selects which target clock signal edge is used by the TDC measurements. 0: TDC uses rising edges of the target clock signal (default). 1: TDC uses falling edges of the source clock signal.	0x0	R/W
5	CHAN_INV9	BSYNC 9 Output Polarity Control. This bit selects if the analog delay block inverts the BSYNC 9 channel output. 0: Analog delay block does not invert the BSYNC9 channel output (default). 1: Analog delay block inverts the BSYNC9 channel output.	0x0	R/W
4	CHAN_INV8	BSYNC 8 Output Polarity Control. This bit selects if the analog delay block inverts the BSYNC 8 channel output. 0: Analog delay block does not invert the BSYNC8 channel output (default). 1: Analog delay block inverts BSYNC8 channel output.	0x0	R/W
3	CHAN_INV7	BSYNC 7 Output Polarity Control. This bit selects if the analog delay block inverts the BSYNC 7 channel output. 0: Analog delay block does not invert the BSYNC7 channel output (default). 1: Analog delay block inverts the BSYNC7 channel output.	0x0	R/W
2	CHAN_INV6	BSYNC 6 Output Polarity Control. This bit selects if the analog delay block inverts the BSYNC 6 channel output. 0: Analog delay block does not invert the BSYNC6 channel output (default). 1: Analog delay block inverts the BSYNC6 channel output.	0x0	R/W
1	CHAN_INV5	BSYNC 5 Output Polarity Control. This bit selects if the analog delay block inverts the BSYNC 5 channel output. 0: Analog delay block does not invert the BSYNC5 channel output (default). 1: Analog delay block inverts the BSYNC5 channel output.	0x0	R/W
0	CHAN_INV4	BSYNC 4 Output Polarity Control. This bit selects if the analog delay block inverts the BSYNC 4 channel output. 0: Analog delay block does not invert the BSYNC4 channel output (default). 1: Analog delay block inverts the BSYNC4 channel output.	0x0	R/W

Address: 0x16, Reset: 0x00, Name: REG0016

Table 39. Bit Descriptions for REG0016

Bits	Bit Name	Description	Reset	Access
7	TDC_ARM_M	This bit starts the TDC measurement in the TDC measurement procedure. 0: TDC operation is reset and stopped. Clear this bit to 0 to end the TDC measurement. 1: Start the TDC measurement.	0x0	R/W
[6:4]	RESERVED	Reserved.	0x0	R/W

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Table 39. Bit Descriptions for REG0016 (Continued)

Bits	Bit Name	Description	Reset	Access
[3:0]	AVGEXP	TDC Averaging Samples Number. This 4-bit unsigned number determines the number of TDC measurements that are averaged. The default value is 0. The expression of the number of TDC measurements is AVG = 64 × 2^{AVGEXP}. The AVGEXP values 0, 1, 2 are not supported. Initialize these bits to 0110 after power up/reset.	0x0	R/W

Address: 0x17, Reset: 0x00, Name: REG0017

Table 40. Bit Descriptions for REG0017

Bits	Bit Name	Description	Reset	Access
7	NDEL_ADJ	This bit manages when the open-loop delay adjustment starts on the target BSYNC channel. 0: Stop the open-loop delay adjustment on the target BSYNC channel. 1: Start the open-loop delay adjustment on the target BSYNC channel.	0x0	R/W
6	STOP_FSM	To immediately stop the target BSYNC channel delay adjustment, first set this bit to 1, and then clear it to 0.	0x0	R/W
[5:0]	ADEL	This unsigned 6-bit word represents the analog adjustable delay in the open-loop delay adjustment mode. The adjustment is applied to the target BSYNC identified by the TDC_TARGET bits in the Register 0x0010. The adjustment weight of the LSB is approximately 1.4 ps.	0x0	R/W

Address: 0x18, Reset: 0x00, Name: REG0018

Table 41. Bit Descriptions for REG0018

Bits	Bit Name	Description	Reset	Access
[7:0]	DELTA_NDEL_COAR[7:0]	This signed 16-bit word represents the desired variation of the coarse delay adjustment in the open-loop delay adjustment mode. The adjustment is applied to the target BSYNC identified by the TDC_TARGET bits in the Register 0x0010. The adjustment weight of the LSB is 1/8 of the VCO period.	0x0	R/W

Address: 0x19, Reset: 0x00, Name: REG0019

Table 42. Bit Descriptions for REG0019

Bits	Bit Name	Description	Reset	Access
[7:0]	DELTA_NDEL_COAR[15:8]	This signed 16-bit word represents the desired variation of the coarse delay adjustment in the open-loop delay adjustment mode. The adjustment is applied to the target BSYNC identified by the TDC_TARGET bits in the Register 0x0010. The adjustment weight of the LSB is 1/8 of the VCO period.	0x0	R/W

Address: 0x1A, Reset: 0x00, Name: REG001A

Table 43. Bit Descriptions for REG001A

Bits	Bit Name	Description	Reset	Access
[7:0]	TDC_OFFSET_COM[7:0]	Common TDC Offset. This signed 21-bit word represents the common time delay that may be introduced in all BSYNC clocks during an alignment procedure. The adjustment weight of the LSB is $1/2^9$ of the VCO period.	0x0	R/W

Address: 0x1B, Reset: 0x00, Name: REG001B

Table 44. Bit Descriptions for REG001B

Bits	Bit Name	Description	Reset	Access
[7:0]	TDC_OFFSET_COM[15:8]	Common TDC Offset. This signed 21-bit word represents the common time delay that may be introduced in all BSYNC clocks during an alignment procedure. The adjustment weight of the LSB is $1/2^9$ of the VCO period.	0x0	R/W

Address: 0x1C, Reset: 0x00, Name: REG001C

Table 45. Bit Descriptions for REG001C

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R

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Table 45. Bit Descriptions for REG001C (Continued)

Bits	Bit Name	Description	Reset	Access
[4:0]	TDC_OFFSET_COM[20:16]	Common TDC Offset. This signed 21-bit word represents the common time delay that can be introduced in all BSYNC clocks during an alignment procedure. The adjustment weight of the LSB is $1/2^9$ of the VCO period.	0x0	R/W

Address: 0x1D, Reset: 0x00, Name: REG001D

Table 46. Bit Descriptions for REG001D

Bits	Bit Name	Description	Reset	Access
[7:0]	TDC_OFFSET0[7:0]	This signed 16-bit word represents the time delay that may be introduced in the BSYNC0 clock during an alignment procedure. The adjustment weight of the LSB is $1/2^9$ of the VCO period.	0x0	R/W

Address: 0x1E, Reset: 0x00, Name: REG001E

Table 47. Bit Descriptions for REG001E

Bits	Bit Name	Description	Reset	Access
[7:0]	TDC_OFFSET0[15:8]	This signed 16-bit word represents the time delay that may be introduced in the BSYNC0 clock during an alignment procedure. The adjustment weight of the LSB is $1/2^9$ of the VCO period.	0x0	R/W

Address: 0x1F, Reset: 0x00, Name: REG001F

Table 48. Bit Descriptions for REG001F

Bits	Bit Name	Description	Reset	Access
[7:0]	TDC_OFFSET1[7:0]	This signed 16-bit word represents the time delay that may be introduced in the BSYNC1 clock during an alignment procedure. The adjustment weight of the LSB is $1/2^9$ of the VCO period.	0x0	R/W

Address: 0x20, Reset: 0x00, Name: REG0020

Table 49. Bit Descriptions for REG0020

Bits	Bit Name	Description	Reset	Access
[7:0]	TDC_OFFSET1[15:8]	This signed 16-bit word represents the time delay that may be introduced in the BSYNC1 clock during an alignment procedure. The adjustment weight of the LSB is $1/2^9$ of the VCO period.	0x0	R/W

Address: 0x21, Reset: 0x00, Name: REG0021

Table 50. Bit Descriptions for REG0021

Bits	Bit Name	Description	Reset	Access
[7:0]	TDC_OFFSET2[7:0]	This signed 16-bit word represents the time delay that may be introduced in the BSYNC2 clock during an alignment procedure. The adjustment weight of the LSB is $1/2^9$ of the VCO period.	0x0	R/W

Address: 0x22, Reset: 0x00, Name: REG0022

Table 51. Bit Descriptions for REG0022

Bits	Bit Name	Description	Reset	Access
[7:0]	TDC_OFFSET2[15:8]	This signed 16-bit word represents the time delay that may be introduced in the BSYNC2 clock during an alignment procedure. The adjustment weight of the LSB is $1/2^9$ of the VCO period.	0x0	R/W

Address: 0x23, Reset: 0x00, Name: REG0023

Table 52. Bit Descriptions for REG0023

Bits	Bit Name	Description	Reset	Access
[7:0]	TDC_OFFSET3[7:0]	This signed 16-bit word represents the time delay that may be introduced in the BSYNC3 clock during an alignment procedure. The adjustment weight of the LSB is $1/2^9$ of the VCO period.	0x0	R/W

Address: 0x24, Reset: 0x00, Name: REG0024

Table 53. Bit Descriptions for REG0024

Bits	Bit Name	Description	Reset	Access
[7:0]	TDC_OFFSET3[15:8]	This signed 16-bit word represents the time delay that may be introduced in the BSYNC3 clock during an alignment procedure. The adjustment weight of the LSB is $1/2^9$ of the VCO period.	0x0	R/W

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Address: 0x25, Reset: 0x00, Name: REG0025

Table 54. Bit Descriptions for REG0025

Bits	Bit Name	Description	Reset	Access
[7:0]	TDC_OFFSET4[7:0]	This signed 16-bit word represents the time delay that may be introduced in the BSYNC4 clock during an alignment procedure. The adjustment weight of the LSB is $1/2^9$ of the VCO period.	0x0	R/W

Address: 0x26, Reset: 0x00, Name: REG0026

Table 55. Bit Descriptions for REG0026

Bits	Bit Name	Description	Reset	Access
[7:0]	TDC_OFFSET4[15:8]	This signed 16-bit word represents the time delay that may be introduced in the BSYNC4 clock during an alignment procedure. The adjustment weight of the LSB is $1/2^9$ of the VCO period.	0x0	R/W

Address: 0x27, Reset: 0x00, Name: REG0027

Table 56. Bit Descriptions for REG0027

Bits	Bit Name	Description	Reset	Access
[7:0]	TDC_OFFSET5[7:0]	This signed 16-bit word represents the time delay that may be introduced in the BSYNC5 clock during an alignment procedure. The adjustment weight of the LSB is $1/2^9$ of the VCO period.	0x0	R/W

Address: 0x28, Reset: 0x00, Name: REG0028

Table 57. Bit Descriptions for REG0028

Bits	Bit Name	Description	Reset	Access
[7:0]	TDC_OFFSET5[15:8]	This signed 16-bit word represents the time delay that may be introduced in the BSYNC5 clock during an alignment procedure. The adjustment weight of the LSB is $1/2^9$ of the VCO period.	0x0	R/W

Address: 0x29, Reset: 0x00, Name: REG0029

Table 58. Bit Descriptions for REG0029

Bits	Bit Name	Description	Reset	Access
[7:0]	TDC_OFFSET6[7:0]	This signed 16-bit word represents the time delay that may be introduced in the BSYNC6 clock during an alignment procedure. The adjustment weight of the LSB is $1/2^9$ of the VCO period.	0x0	R/W

Address: 0x2A, Reset: 0x00, Name: REG002A

Table 59. Bit Descriptions for REG002A

Bits	Bit Name	Description	Reset	Access
[7:0]	TDC_OFFSET6[15:8]	This signed 16-bit word represents the time delay that may be introduced in the BSYNC6 clock during an alignment procedure. The adjustment weight of the LSB is $1/2^9$ of the VCO period.	0x0	R/W

Address: 0x2B, Reset: 0x00, Name: REG002B

Table 60. Bit Descriptions for REG002B

Bits	Bit Name	Description	Reset	Access
[7:0]	TDC_OFFSET7[7:0]	This signed 16-bit word represents the time delay that may be introduced in the BSYNC7 clock during an alignment procedure. The adjustment weight of the LSB is $1/2^9$ of the VCO period.	0x0	R/W

Address: 0x2C, Reset: 0x00, Name: REG002C

Table 61. Bit Descriptions for REG002C

Bits	Bit Name	Description	Reset	Access
[7:0]	TDC_OFFSET7[15:8]	This signed 16-bit word represents the time delay that may be introduced in the BSYNC7 clock during an alignment procedure. The adjustment weight of the LSB is $1/2^9$ of the VCO period.	0x0	R/W

Address: 0x2D, Reset: 0x00, Name: REG002D

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Table 62. Bit Descriptions for REG002D

Bits	Bit Name	Description	Reset	Access
[7:0]	TDC_OFFSET8[7:0]	This signed 16-bit word represents the time delay that may be introduced in the BSYNC8 clock during an alignment procedure. The adjustment weight of the LSB is $1/2^9$ of the VCO period.	0x0	R/W

Address: 0x2E, Reset: 0x00, Name: REG002E

Table 63. Bit Descriptions for REG002E

Bits	Bit Name	Description	Reset	Access
[7:0]	TDC_OFFSET8[15:8]	This signed 16-bit word represents the time delay that may be introduced in the BSYNC8 clock during an alignment procedure. The adjustment weight of the LSB is $1/2^9$ of the VCO period.	0x0	R/W

Address: 0x2F, Reset: 0x00, Name: REG002F

Table 64. Bit Descriptions for REG002F

Bits	Bit Name	Description	Reset	Access
[7:0]	TDC_OFFSET9[7:0]	This signed 16-bit word represents the time delay that may be introduced in the BSYNC9 clock during an alignment procedure. The adjustment weight of the LSB is $1/2^9$ of the VCO period.	0x0	R/W

Address: 0x30, Reset: 0x00, Name: REG0030

Table 65. Bit Descriptions for REG0030

Bits	Bit Name	Description	Reset	Access
[7:0]	TDC_OFFSET9[15:8]	This signed 16-bit word represents the time delay that may be introduced in the BSYNC9 clock during an alignment procedure. The adjustment weight of the LSB is $1/2^9$ of the VCO period.	0x0	R/W

Address: 0x31, Reset: 0x40, Name: REG0031

Table 66. Bit Descriptions for REG0031

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x40	R/W

Address: 0x32, Reset: 0x00, Name: REG0032

Table 67. Bit Descriptions for REG0032

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x33, Reset: 0x00, Name: REG0033

Table 68. Bit Descriptions for REG0033

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x34, Reset: 0x3F, Name: REG0034

Table 69. Bit Descriptions for REG0034

Bits	Bit Name	Description	Reset	Access
7	ONE_SHOT	Apply Delay Shift in One Step. 0: Delay adjustment is done function of the cycles bit value. 1: Delay adjustment is done in one single BSYNC period.	0x0	R/W
6	CYCLES	Adjustment Delay Mechanism Control. This control bit becomes functional only when ONE_SHOT bit is cleared to 0. 0: Delay adjustment is done in steps of approximately 50 ps (1/8 of the VCO period). 1: Delay adjustment is done in steps of one VCO period.	0x0	R/W
[5:0]	DELCAL	Scaling Factor for ALIGN_TOT[5:0] Field Contribution in the closed-loop delay adjustment process. Initialize these bits to 100100 after power up/reset.	0x3F	R/W

Address: 0x35, Reset: 0x00, Name: REG0035

REGISTER DETAILS

Table 70. Bit Descriptions for REG0035

Bits	Bit Name	Description	Reset	Access
[7:6]	BSYNC_CAL_ON[1:0]	This is a 10-bit field in which each bit selects the BSYNC channel on which the serial alignment procedure is executed. Bit 0 selects BSYNC0, Bit 1 selects BSYNC1, … , Bit 9 selects BSYNC9.	0x0	R/W
[5:0]	ALIGN_THOLD	This 6-bit field selects the desired threshold in the threshold alignment mode. The adjustment weight of the LSB is equal to the LSB weight of the ADEL[5:0] bits in Register 0x17. Initialize these bits to 000101 after power up/reset.	0x0	R/W

Address: 0x36, Reset: 0x00, Name: REG0036

Table 71. Bit Descriptions for REG0036

Bits	Bit Name	Description	Reset	Access
[7:0]	BSYNC_CAL_ON[9:2]	This is a 10-bit field in which each bit selects the BSYNC channel on which the serial alignment procedure is executed. Bit 0 selects BSYNC0, Bit 1 selects BSYNC1, … , Bit 9 selects BSYNC9.	0x0	R/W

Address: 0x37, Reset: 0x02, Name: REG0037

Table 72. Bit Descriptions for REG0037

Bits	Bit Name	Description	Reset	Access
[7:5]	ALIGN_CYCLES	Sets the Number of Alignment Cycles in the single-channel alignment procedures. 000: Run 1 alignment cycle. 001: Run 2 alignment cycles. 010: Run 3 alignment cycles. 011: Run 4 alignment cycles. 100: Run 5 alignment cycles. 101: Run 6 alignment cycles. 110: Run 7 alignment cycles. 111: Run 8 alignment cycles.	0x0	R/W
4	AUTO_PD_BG	This bit disables the drivers of the BSYNC clocks not being used in real time during the serial alignment and background serial alignment procedures. 0: BSYNC channels drivers remain enabled during the serial procedures. Apply this setting when the source TDC channel is an outgoing clock. 1: BSYNC channels drivers are disabled during the serial procedures if they are not being used in real time. Apply this setting when the source TDC channel is an incoming clock to reduce the power consumption during the procedures.	0x0	R/W
3	EN_BKGND_ALGN	When set to 1, this bit enables the background serial alignment procedure.	0x0	R/W
2	EN_SERIAL_ALIGN	When set to 1, this bit enables the serial alignment procedure.	0x0	R/W
1	EN_CYCS_RED	When set to 1, this bit enables the reduction of the TDC time stamps taken during the threshold and fixed iteration alignment procedures. Initialize this bit to 1 after power up/reset. 0: Every alignment cycle uses AVG = 64 × $2^{CIC\_DEC\_RATE}$ TDC time stamps. 1: The first alignment cycle uses AVG = 64 x $2^{(AVGEXP-ALIGN\_CYCLES)}$ TDC time stamps. Each successive alignment cycle uses a number of TDC time stamps equal to the previous AVG TDC time stamps multiplied by 2.	0x1	R/W
0	EN_ITER	When set to 1, this bit enables the threshold alignment procedure to run until the alignment between the BSYNC channels is lower than the threshold set in ALIGN_THOLD[5:0] bits in Register 0x35. The maximum number of iterations is determined by Bits ALIGN_CYCLES in Register 0x37.	0x0	R/W

Address: 0x38, Reset: 0x00, Name: REG0038

Table 73. Bit Descriptions for REG0038

Bits	Bit Name	Description	Reset	Access
[7:0]	RST_BSYNC_CH[7:0]	Channel Reset.	0x0	R/W

Address: 0x39, Reset: 0x00, Name: REG0039

REGISTER DETAILS

Table 74. Bit Descriptions for REG0039

Bits	Bit Name	Description	Reset	Access
7	RST_SYS	Reset Digital. Except SPI interface and Registers, digital reset to POR State.	0x0	R/W
6	MSTR_RST_BSYNC	Main Reset for BSYNC Channels.	0x0	R/W
[5:2]	RESERVED	Reserved.	0x0	R/W
[1:0]	RST_BSYNC_CH[9:8]	Channel Reset.	0x0	R/W

Address: 0x3A, Reset: 0x00, Name: REG003A

Table 75. Bit Descriptions for REG003A

Bits	Bit Name	Description	Reset	Access
7	PD_DRV7	BSYNC7 Transmit Driver Power Down. This bit powers up or down BSYNC7 transmit driver. 0: BSYNC7 transmit driver powered up. 1: BSYNC7 transmit driver powered down.	0x0	R/W
6	PD_DRV6	BSYNC6 Transmit Driver Power Down. This bit powers up or down BSYNC6 transmit driver. 0: BSYNC6 transmit driver powered up. 1: BSYNC6 transmit driver powered down.	0x0	R/W
5	PD_DRV5	BSYNC5 Transmit Driver Power Down. This bit powers up or down BSYNC5 transmit driver. 0: BSYNC5 transmit driver powered up. 1: BSYNC5 transmit driver powered down.	0x0	R/W
4	PD_DRV4	BSYNC4 Transmit Driver Power Down. This bit powers up or down BSYNC4 transmit driver. 0: BSYNC4 transmit driver powered up. 1: BSYNC4 transmit driver powered down.	0x0	R/W
3	PD_DRV3	BSYNC3 Transmit Driver Power Down. This bit powers up or down BSYNC3 transmit driver. 0: BSYNC3 transmit driver powered up. 1: BSYNC3 transmit driver powered down.	0x0	R/W
2	PD_DRV2	BSYNC2 Transmit Driver Power Down. This bit powers up or down BSYNC2 transmit driver. 0: BSYNC2 transmit driver powered up. 1: BSYNC2 transmit driver powered down.	0x0	R/W
1	PD_DRV1	BSYNC1 Transmit Driver Power Down. This bit powers up or down BSYNC1 transmit driver. 0: BSYNC1 transmit driver powered up. 1: BSYNC1 transmit driver powered down.	0x0	R/W
0	PD_DRV0	BSYNC0 Transmit Driver Power Down. This bit powers up or down BSYNC0 transmit driver. 0: BSYNC0 transmit driver powered up. 1: BSYNC0 transmit driver powered down.	0x0	R/W

Address: 0x3B, Reset: 0x00, Name: REG003B

Table 76. Bit Descriptions for REG003B

Bits	Bit Name	Description	Reset	Access
7	PD_TX_PATH5	BSYNC5 Transmit Block Power Down. This bit powers up or down BSYNC5 transmit driver and its analog delay block. Initialize this bit to 1 after power up/reset 0: BSYNC5 transmit driver and analog delay block powered up. 1: BSYNC5 transmit driver and analog delay block powered down.	0x0	R/W
6	PD_TX_PATH4	BSYNC4 Transmit Block Power Down. This bit powers up or down BSYNC4 transmit driver and its analog delay block. Initialize this bit to 1 after power up/reset 0: BSYNC4 transmit driver and analog delay block powered up. 1: BSYNC4 transmit driver and analog delay block powered down.	0x0	R/W
5	PD_TX_PATH3	BSYNC3 Transmit Block Power Down. This bit powers up or down BSYNC3 transmit driver and its analog delay block. Initialize this bit to 1 after power up/reset 0: BSYNC3 transmit driver and analog delay block powered up. 1: BSYNC3 transmit driver and analog delay block powered down.	0x0	R/W

REGISTER DETAILS

Table 76. Bit Descriptions for REG003B (Continued)

Bits	Bit Name	Description	Reset	Access
4	PD_TX_PATH2	BSYNC2 Transmit Block Power Down. This bit powers up or down BSYNC2 transmit driver and its analog delay block. Initialize this bit to 1 after power up/reset 0: BSYNC2 transmit driver and analog delay block powered up. 1: BSYNC2 transmit driver and analog delay block powered down.	0x0	R/W
3	PD_TX_PATH1	BSYNC1 Transmit Block Power Down. This bit powers up or down BSYNC1 transmit driver and its analog delay block. Initialize this bit to 1 after power up/reset 0: BSYNC1 transmit driver and analog delay block powered up. 1: BSYNC1 transmit driver and analog delay block powered down.	0x0	R/W
2	PD_TX_PATH0	BSYNC0 Transmit Block Power Down. This bit powers up or down BSYNC0 transmit driver and its analog delay block. Initialize this bit to 1 after power up/reset 0: BSYNC0 transmit driver and analog delay block powered up. 1: BSYNC0 transmit driver and analog delay block powered down.	0x0	R/W
1	PD_DRV9	BSYNC9 Transmit Driver Power Down. This bit powers up or down BSYNC9 transmit driver. 0: BSYNC9 transmit driver powered up. 1: BSYNC9 transmit driver powered down.	0x0	R/W
0	PD_DRV8	BSYN8 Transmit Driver Power Down. This bit powers up or down BSYNC8 transmit driver. 0: BSYNC8 transmit driver powered up. 1: BSYNC8 transmit driver powered down.	0x0	R/W

Address: 0x3C, Reset: 0x80, Name: REG003C

Table 77. Bit Descriptions for REG003C

Bits	Bit Name	Description	Reset	Access
7	PD_ALL	ADF4030 Power Down. This bit powers up or down the ADF4030. Initialize this bit to 1 after a power up/reset. 0: ADF4030 powered up. 1: ADF4030 powered down.	0x1	R/W
6	PD_PLL	PLL Power Down. This bit powers up or down the PLL. Initialize this bit to 1 after a power up/reset. 0: PLL powered up. 1: PLL powered down.	0x0	R/W
5	PD_TDC	TDC Power Down. This bit powers up or down the TDC and the associated multiplexer. Initialize this bit to 1 after a power up/reset. 0: TDC and multiplexer powered up. 1: TDC and multiplexer powered down.	0x0	R/W
4	PD_ADC	Temperature ADC Power Down. This bit powers up or down the ADC of the temperature measurement system. Initialize this bit to 1 after a power up/reset. 0: Temperature ADC powered up. 1: Temperature ADC powered down.	0x0	R/W
3	PD_TX_PATH9	BSYNC9 Transmit Block Power Down. This bit powers up or down BSYNC9 transmit driver and its analog delay block. Initialize this bit to 1 after a power up/reset 0: BSYNC9 transmit driver and analog delay block powered up. 1: BSYNC9 transmit driver and analog delay block powered down.	0x0	R/W
2	PD_TX_PATH8	BSYNC8 Transmit Block Power Down. This bit powers up or down BSYNC8 transmit driver and its analog delay block. Initialize this bit to 1 after a power up/reset 0: BSYNC8 transmit driver and analog delay block powered up. 1: BSYNC8 transmit driver and analog delay block powered down.	0x0	R/W
1	PD_TX_PATH7	BSYNC7 Transmit Block Power Down. This bit powers up or down BSYNC7 transmit driver and its analog delay block. Initialize this bit to 1 after a power up/reset 0: BSYNC7 transmit driver and analog delay block powered up. 1: BSYNC7 transmit driver and analog delay block powered down.	0x0	R/W
0	PD_TX_PATH6	BSYNC6 Transmit Block Power Down. This bit powers up or down BSYNC6 transmit driver and its analog delay block. Initialize this bit to 1 after a power up/reset	0x0	R/W

REGISTER DETAILS

Table 77. Bit Descriptions for REG003C (Continued)

Bits	Bit Name	Description	Reset	Access
		0: BSYNC6 transmit driver and analog delay block powered up. 1: BSYNC6 transmit driver and analog delay block powered down.		

Address: 0x3D, Reset: 0x00, Name: REG003D

Table 78. Bit Descriptions for REG003D

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED[7:0]	Reserved.	0x0	R/W

Address: 0x3E, Reset: 0x00, Name: REG003E

Table 79. Bit Descriptions for REG003E

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x3F, Reset: 0x00, Name: REG003F

Table 80. Bit Descriptions for REG003F

Bits	Bit Name	Description	Reset	Access
7	ODIV_SEL0	BSYNC0 ODIVA or ODIVB Integer Divide Ratio Select. This bit selects divide ratios for BSYNC0 channel. ODIVA (when cleared to 0 (default)) or ODIVB (when set to 1).	0x0	R/W
6	BOOST0	BSYNC 0 Driver Current Level. This bit selects the BSYNC 0 driver current level. 0: 14 mA driver current (default). 1: 20 mA driver current.	0x0	R/W
[5:0]	RCM0	BSYNC0 Driver Common Mode Resistor Value. This 6-bit field selects R_CM0, the common-mode resistor value of the BSYNC0 driver. R_CM0 = 700/(73.5 − RCM0]). V_CM0, the common-mode voltage of the BSYNC0 driver is then V_CM0 = I_DRV× (26.5 + R_CM0), where I_DRV is the BSYNC driver current level set by the BOOST0 bit. I_DRV = 20 mA when BOOST0 = 1. I_DRV = 14 mA when BOOST0 = 0.	0x0	R/W

Address: 0x40, Reset: 0x00, Name: REG0040

Table 81. Bit Descriptions for REG0040

Bits	Bit Name	Description	Reset	Access
7	AUTO_PD_RCV_0	Automatically Powers Down the BSYNC0 Receiver. This bit selects if the BSYNC0 receiver powers down or not when it is not used by the TDC. Initialize this bit to 1 after power up/reset. 0: BSYNC0 receiver stays powered up all the time. 1: BSYNC0 receiver powers down when not used in the TDC measurement.	0x0	R/W
6	RESERVED	Reserved.	0x0	R/W
5	FLOAT_RX0	Disconnect BSYNC0 Receiver 50 Ω Float Connections to Ground. This bit selects if the 50 Ω float terminations of the BSYNC0 receiver are connected to ground or not. 0: Terminations connected to ground (default). 1: Terminations not connected to ground.	0x0	R/W
4	FLOAT_TX0	Disconnect BSYNC0 Driver 50 Ω Float Connections to Ground. This bit selects if the 50 Ω float terminations of the BSYNC0 driver are connected to ground or not. 0: Terminations connected to ground (default). 1: Terminations not connected to ground.	0x0	R/W
3	LINK_RX_0	Short Together BSYNC0 Receiver 50 Ω Link Terminations. This bit selects if the 50 Ω link terminations of the BSYNC0 receiver are shorted together or not. Initialize this bit to 1 after power up/reset. 0: Terminations not shorted together (default). 1: Terminations shorted together.	0x0	R/W
2	LINK_TX0	Short Together BSYNC0 Driver 50 Ω Link Terminations. This bit selects if the 50 Ω link terminations of BSYNC0 driver are shorted together or not. 0: Terminations not shorted together (default).	0x0	R/W

REGISTER DETAILS

Table 81. Bit Descriptions for REG0040 (Continued)

Bits	Bit Name	Description	Reset	Access
		1: Terminations shorted together.		
1	AC_COUPLED0	BSYNC0 Receive AC-coupled Mode. This bit selects if the BSYNC0 receiver is set to receive AC- or DC-coupled clocks. 0: DC-coupled clocks (default). 1: AC-coupled clocks.	0x0	R/W
0	RESERVED	Reserved.	0x0	R/W

Address: 0x41, Reset: 0x00, Name: REG0041

Table 82. Bit Descriptions for REG0041

Bits	Bit Name	Description	Reset	Access
7	ODIV_SEL1	BSYNC1 ODIVA or ODIVB Integer Divide Ratio Select. This bit selects ODIVA (when cleared to 0 (default)) or ODIVB (when set to 1) divide ratios for the BSYNC1 channel.	0x0	R/W
6	BOOST1	BSYNC 1 Driver Current Level. This bit selects the BSYNC 1 driver current level. 0: 14 mA driver current (default). 1: 20 mA driver current.	0x0	R/W
[5:0]	RCM1	BSYNC1 Driver Common-Mode Resistor Value. This 6-bit field selects R_CM1, the common-mode resistor value of the BSYNC1 driver. R_CM1 = 700/(73.5 − RCM1). V_CM1, the common-mode voltage of the BSYNC1 driver, is then V_CM1 = I_DRV × (26.5 + R_CM1), where I_DRV is the BSYNC driver current level set by the BOOST1 bit. I_DRV = 20 mA when BOOST1 = 1. I_DRV = 14 mA when BOOST1 = 0.	0x0	R/W

Address: 0x42, Reset: 0x00, Name: REG0042

Table 83. Bit Descriptions for REG0042

Bits	Bit Name	Description	Reset	Access
7	AUTO_PD_RCV_1	Automatically Powers Down the BSYNC1 Receiver. This bit selects if the BSYNC1 receiver powers down or not when it is not used by the TDC. Initialize this bit to 1 after power up/reset. 0: BSYNC1 Receiver stays powered up all the time. 1: BSYNC1 Receiver powers down when not used in the TDC measurement.	0x0	R/W
6	RESERVED	Reserved.	0x0	R/W
5	FLOAT_RX1	Disconnect BSYNC1 Receiver 50 Ω Float Connections to Ground. This bit selects if the 50 Ω float terminations of the BSYNC1 receiver are connected to ground or not. 0: Terminations connected to ground (default). 1: Terminations not connected to ground.	0x0	R/W
4	FLOAT_TX1	Disconnect BSYNC1 Driver 50 Ω Float Connections to Ground. This bit selects if the 50 Ω float terminations of the BSYNC1 driver are connected to ground or not. 0: Terminations connected to ground (default). 1: Terminations not connected to ground.	0x0	R/W
3	LINK_RX_1	Short Together BSYNC1 Receiver 50 Ω LINK Terminations. This bit selects if the 50 Ω link terminations of the BSYNC1 receiver are shorted together or not. Initialize this bit to 1 after power up/reset. 0: Terminations not shorted together (default). 1: Terminations shorted together.	0x0	R/W
2	LINK_TX1	Short Together BSYNC1 Driver 50 Ω Link Terminations. This bit selects if the 50 Ω link terminations of the BSYNC1 driver are shorted together or not. 0: Terminations not shorted together (default). 1: Terminations shorted together.	0x0	R/W
1	AC_COUPLED1	BSYNC1 Receive AC-Coupled Mode. This bit selects if the BSYNC1 receiver is set to receive AC- or DC-coupled clocks. 0: DC-coupled clocks (default). 1: AC-coupled clocks.	0x0	R/W
0	RESERVED	Reserved.	0x0	R/W

REGISTER DETAILS

Address: 0x43, Reset: 0x00, Name: REG0043

Table 84. Bit Descriptions for REG0043

Bits	Bit Name	Description	Reset	Access
7	ODIV_SEL2	BSYNC2 ODIVA or ODIVB Integer Divide Ratio Select. This bit selects ODIVA (when cleared to 0 (default)) or ODIVB (when set to 1) divide ratios for BSYNC2 channel.	0x0	R/W
6	BOOST2	BSYNC 2 Driver Current Level. This bit selects the BSYNC 2 driver current level. 0: 14 mA driver current (default). 1: 20 mA driver current.	0x0	R/W
[5:0]	RCM2	BSYNC2 Driver Common-Mode Resistor Value. This 6-bit field selects R_CM2, the common-mode resistor value of the BSYNC2 driver. R_CM2 = 700/(73.5 − RCM2). V_CM2, the common-mode voltage of the BSYNC2 driver is then V_CM2 = I_DRV × (26.5 + R_CM2), where I_DRV is the BSYNC driver current level set by BOOST2 bit. I_DRV = 20 mA when BOOST2 = 1. I_DRV = 14 mA when BOOST2 = 0.	0x0	R/W

Address: 0x44, Reset: 0x00, Name: REG0044

Table 85. Bit Descriptions for REG0044

Bits	Bit Name	Description	Reset	Access
7	AUTO_PD_RCV_2	Automatically Powers Down BSYNC2 Receiver. This bit selects if the BSYNC2 receiver powers down or not when it is not used by the TDC. Initialize this bit to 1 after power up/reset. 0: BSYNC2 receiver stays powered up all the time. 1: BSYNC2 receiver powers down when not used in the TDC measurement.	0x0	R/W
6	RESERVED	Reserved.	0x0	R/W
5	FLOAT_RX2	Disconnect BSYNC2 Receiver 50 Ω Float Connections to Ground. This bit selects if the 50 Ω float terminations of the BSYNC2 receiver are connected to ground or not. 0: Terminations connected to ground (default). 1: Terminations not connected to ground.	0x0	R/W
4	FLOAT_TX2	Disconnect BSYNC2 Driver 50 Ω Float Connections to Ground. This bit selects if the 50 Ω float terminations of the BSYNC2 driver are connected to ground or not. 0: Terminations connected to ground (default). 1: Terminations not connected to ground.	0x0	R/W
3	LINK_RX_2	Short Together BSYNC2 Receiver 50 Ω Link Terminations. This bit selects if the 50 Ω link terminations of BSYNC2 receiver are shorted together or not. Initialize this bit to 1 after power up/reset. 0: Terminations not shorted together (default). 1: Terminations shorted together.	0x0	R/W
2	LINK_TX2	Short Together BSYNC2 Driver 50 Ω Link Terminations. This bit selects if the 50 Ω link terminations of BSYNC2 driver are shorted together or not. 0: Terminations not shorted together (default). 1: Terminations shorted together.	0x0	R/W
1	AC_COUPLED2	BSYNC2 Receive AC-coupled Mode. This bit selects if the BSYNC2 receiver is set to receive AC- or DC-coupled clocks. 0: DC-coupled clocks (default). 1: AC-coupled clocks.	0x0	R/W
0	RESERVED	Reserved.	0x0	R/W

Address: 0x45, Reset: 0x00, Name: REG0045

Table 86. Bit Descriptions for REG0045

Bits	Bit Name	Description	Reset	Access
7	ODIV_SEL3	BSYNC3 ODIVA or ODIVB Integer Divide Ratio Select. This bit selects ODIVA (when cleared to 0 (default)) or ODIVB (when set to 1) divide ratios for the BSYNC3 channel.	0x0	R/W
6	BOOST3	BSYNC 3 Driver Current Level. This bit selects the BSYNC 3 driver current level. 0: 14 mA driver current (default). 1: 20 mA driver current.	0x0	R/W

REGISTER DETAILS

Table 86. Bit Descriptions for REG0045 (Continued)

Bits	Bit Name	Description	Reset	Access
[5:0]	RCM3	BSYNC3 Driver Common-Mode Resistor Value. This 6-bit field selects R_CM3, the common-mode resistor value of the BSYNC3 driver. R_CM3 = 700/(73.5 − RCM3). V_CM3, the common-mode voltage of the BSYNC3 driver is then V_CM3 = I_DRV × (26.5 + R_CM3), where I_DRV is the BSYNC driver current level set by BOOST3 bit. I_DRV=20 mA when BOOST3 = 1. I_DRV = 14 mA when BOOST3 = 0.	0x0	R/W

Address: 0x46, Reset: 0x00, Name: REG0046

Table 87. Bit Descriptions for REG0046

Bits	Bit Name	Description	Reset	Access
7	AUTO_PD_RCV_3	Automatically Powers Down BSYNC3 Receiver. This bit selects if the BSYNC3 receiver powers down or not when it is not used by the TDC. Initialize this bit to 1 after power up/reset. 0: BSYNC3 receiver stays powered up all the time. 1: BSYNC3 receiver powers down when not used in the TDC measurement.	0x0	R/W
6	RESERVED	Reserved.	0x0	R/W
5	FLOAT_RX3	Disconnect BSYNC3 Receiver 50 Ω Float Connections to Ground. This bit selects if the 50 Ω float terminations of the BSYNC3 receiver are connected to ground or not. 0: Terminations connected to ground (default). 1: Terminations not connected to ground.	0x0	R/W
4	FLOAT_TX3	Disconnect BSYNC3 Driver 50 Ω FLOAT Connections to Ground. This bit selects if the 50 Ω FLOAT terminations of the BSYNC3 driver are connected to ground or not. 0: Terminations connected to ground (default). 1: Terminations not connected to ground.	0x0	R/W
3	LINK_RX_3	Short Together BSYNC3 Receiver 50 Ω Link Terminations. This bit selects if the 50 Ω link terminations of the BSYNC3 receiver are shorted together or not. Initialize this bit to 1 after power up/reset. 0: Terminations not shorted together (default). 1: Terminations shorted together.	0x0	R/W
2	LINK_TX3	Short Together BSYNC3 Driver 50 Ω Link Terminations. This bit selects if the 50 Ω link terminations of the BSYNC3 driver are shorted together or not. 0: Terminations not shorted together (default). 1: Terminations shorted together.	0x0	R/W
1	AC_COUPLED3	BSYNC3 Receive AC-coupled Mode. This bit selects if the BSYNC3 receiver is set to receive AC- or DC-coupled clocks. 0: DC-coupled clocks (default). 1: AC-coupled clocks.	0x0	R/W
0	RESERVED	Reserved.	0x0	R/W

Address: 0x47, Reset: 0x00, Name: REG0047

Table 88. Bit Descriptions for REG0047

Bits	Bit Name	Description	Reset	Access
7	ODIV_SEL4	BSYNC4 ODIVA or ODIVB Integer Divide Ratio Select. This bit selects ODIVA (when cleared to 0 (default)) or ODIVB (when set to 1) divide ratios for the BSYNC4 channel.	0x0	R/W
6	BOOST4	BSYNC 4 Driver Current Level. This bit selects the BSYNC 4 driver current level. 0: 14 mA driver current (default). 1: 20 mA driver current.	0x0	R/W
[5:0]	RCM4	BSYNC4 Driver Common-Mode Resistor Value. This 6-bit field selects R_CM4, the common-mode resistor value of the BSYNC4 driver. R_CM4 = 700/(73.5 − RCM4). V_CM4, the common-mode voltage of the BSYNC4 driver is then V_CM4 = I_DRV × (26.5 + R_CM4), where I_DRV is the BSYNC driver current level set by BOOST4 bit. I_DRV = 20 mA when BOOST4 = 1. I_DRV = 14 mA when BOOST4 = 0.	0x0	R/W

Address: 0x48, Reset: 0x00, Name: REG0048

REGISTER DETAILS

Table 89. Bit Descriptions for REG0048

Bits	Bit Name	Description	Reset	Access
7	AUTO_PD_RCV_4	Automatically Powers Down BSYNC4 Receiver. This bit selects if the BSYNC4 receiver powers down or not when it is not used by the TDC. Initialize this bit to 1 after power up/reset. 0: BSYNC4 Receiver stays powered up all the time. 1: BSYNC4 Receiver powers down when not used in the TDC measurement.	0x0	R/W
6	RESERVED	Reserved.	0x0	R/W
5	FLOAT_RX4	Disconnect BSYNC4 Receiver 50 Ω Float Connections to Ground. This bit selects if the 50 Ω float terminations of the BSYNC4 receiver are connected to ground or not. 0: Terminations connected to ground (default). 1: Terminations not connected to ground.	0x0	R/W
4	FLOAT_TX4	Disconnect BSYNC4 Driver 50 Ω Float Connections to Ground. This bit selects if the 50 Ω float terminations of the BSYNC4 driver are connected to ground or not. 0: Terminations connected to ground (default). 1: Terminations not connected to ground.	0x0	R/W
3	LINK_RX_4	Short Together BSYNC4 Receiver 50 Ω Link Terminations. This bit selects if the 50 Ω link terminations of the BSYNC4 receiver are shorted together or not. Initialize this bit to 1 after power up/reset. 0: Terminations not shorted together (default). 1: Terminations shorted together.	0x0	R/W
2	LINK_TX4	Short Together BSYNC4 Driver 50 Ω Link Terminations. This bit selects if the 50 Ω link terminations of the BSYNC4 driver are shorted together or not. 0: Terminations not shorted together (default). 1: Terminations shorted together.	0x0	R/W
1	AC_COUPLED4	BSYNC4 Receive AC-coupled Mode. This bit selects if the BSYNC4 receiver is set to receive AC- or DC-coupled clocks. 0: DC-coupled clocks (default). 1: AC-coupled clocks.	0x0	R/W
0	RESERVED	Reserved.	0x0	R/W

Address: 0x49, Reset: 0x00, Name: REG0049

Table 90. Bit Descriptions for REG0049

Bits	Bit Name	Description	Reset	Access
7	ODIV_SEL5	BSYNC5 ODIVA or ODIVB Integer Divide Ratio Select. This bit selects ODIVA (when cleared to 0 (default)) or ODIVB (when set to 1) divide ratios for the BSYNC5 channel.	0x0	R/W
6	BOOST5	BSYNC5 Driver Current Level. This bit selects the BSYNC 5 driver current level. 0: 14 mA driver current (default). 1: 20 mA driver current.	0x0	R/W
[5:0]	RCM5	BSYNC5 Driver Common-Mode Resistor Value. This 6-bit field selects R_CM5, the common-mode resistor value of the BSYNC5 driver. R_CM5 = 700/(73.5 − RCM5). V_CM5, the common-mode voltage of the BSYNC5 driver is then V_CM5 = I_DRV × (26.5 + R_CM5), where I_DRV is the BSYNC driver current level set by BOOST5 bit. I_DRV = 20 mA when BOOST5 = 1. I_DRV=14 mA when BOOST5 = 0.	0x0	R/W

Address: 0x4A, Reset: 0x00, Name: REG004A

Table 91. Bit Descriptions for REG004A

Bits	Bit Name	Description	Reset	Access
7	AUTO_PD_RCV_5	Automatically Powers Down BSYNC5 Receiver. This bit selects if the BSYNC5 receiver powers down or not when it is not used by the TDC. Initialize this bit to 1 after power up/reset. 0: BSYNC5 Receiver stays powered up all the time. 1: BSYNC5 Receiver powers down when not used in the TDC measurement.	0x0	R/W
6	RESERVED	Reserved.	0x0	R/W

REGISTER DETAILS

Table 91. Bit Descriptions for REG004A (Continued)

Bits	Bit Name	Description	Reset	Access
5	FLOAT_RX5	Disconnect BSYNC5 Receiver 50 Ω Float Connections to Ground. This bit selects if the 50 Ω FLOAT terminations of the BSYNC5 receiver are connected to ground or not. 0: Terminations connected to ground (default). 1: Terminations not connected to ground.	0x0	R/W
4	FLOAT_TX5	Disconnect BSYNC5 Driver 50 Ω Float Connections to Ground. This bit selects if the 50 Ω float terminations of the BSYNC5 driver are connected to ground or not. 0: Terminations connected to ground (default). 1: Terminations not connected to ground.	0x0	R/W
3	LINK_RX_5	Short Together BSYNC5 Receiver 50 Ω Link Terminations. This bit selects if the 50 Ω link terminations of the BSYNC5 receiver are shorted together or not. Initialize this bit to 1 after power up/reset. 0: Terminations not shorted together (default). 1: Terminations shorted together.	0x0	R/W
2	LINK_TX5	Short Together BSYNC5 Driver 50 Ω Link Terminations. This bit selects if the 50 Ω link terminations of the BSYNC5 driver are shorted together or not. 0: Terminations not shorted together (default). 1: Terminations shorted together.	0x0	R/W
1	AC_COUPLED5	BSYNC5 Receive AC-coupled Mode. This bit selects if the BSYNC5 receiver is set to receive AC- or DC-coupled clocks. 0: DC-coupled clocks (default). 1: AC-coupled clocks.	0x0	R/W
0	RESERVED	Reserved.	0x0	R/W

Address: 0x4B, Reset: 0x00, Name: REG004B

Table 92. Bit Descriptions for REG004B

Bits	Bit Name	Description	Reset	Access
7	ODIV_SEL6	BSYNC6 ODIVA or ODIVB Integer Divide Ratio Select. This bit selects ODIVA (when cleared to 0 (value)) or ODIVB (when set to 1) divide ratios for the BSYNC6 channel.	0x0	R/W
6	BOOST6	BSYNC6 Driver Current Level. This bit selects the BSYNC6 driver current level. 0: 14 mA driver current (default). 1: 20 mA driver current.	0x0	R/W
[5:0]	RCM6	BSYNC6 Driver Common-Mode Resistor Value. This 6-bit field selects R_CM6, the common-mode resistor value of the BSYNC6 driver. R_CM6 = 700/(73.5 − RCM6). V_CM6, the common-mode voltage of the BSYNC6 driver is then V_CM6 = I_DRV × (26.5 + R_CM6), where I_DRV is the BSYNC driver current level set by BOOST6 bit. I_DRV = 20 mA when BOOST6 = 1. I_DRV = 14 mA when BOOST6 = 0.	0x0	R/W

Address: 0x4C, Reset: 0x00, Name: REG004C

Table 93. Bit Descriptions for REG004C

Bits	Bit Name	Description	Reset	Access
7	AUTO_PD_RCV_6	Automatically Powers Down BSYNC6 Receiver. This bit selects if the BSYNC6 receiver powers down or not when it is not used by the TDC. Initialize this bit to 1 after power up/reset. 0: BSYNC6 Receiver stays powered up all the time. 1: BSYNC6 Receiver powers down when not used in the TDC measurement.	0x0	R/W
6	RESERVED	Reserved.	0x0	R/W
5	FLOAT_RX6	Disconnect BSYNC6 Receiver 50 Ω Float Connections to Ground. This bit selects if the 50 Ω float terminations of the BSYNC6 receiver are connected to ground or not. 0: Terminations connected to ground (default). 1: Terminations not connected to ground.	0x0	R/W
4	FLOAT_TX6	Disconnect BSYNC6 Driver 50 Ω Float Connections to Ground. This bit selects if the 50 Ω float terminations of the BSYNC6 driver are connected to ground or not.	0x0	R/W

REGISTER DETAILS

Table 93. Bit Descriptions for REG004C (Continued)

Bits	Bit Name	Description	Reset	Access
		0: Terminations connected to ground (default). 1: Terminations not connected to ground.		
3	LINK_RX_6	Short Together BSYNC6 Receiver 50 Ω Link Terminations. This bit selects if the 50 Ω LINK terminations of the BSYNC6 receiver are shorted together or not. Initialize this bit to 1 after power up/reset. 0: Terminations not shorted together (default). 1: Terminations shorted together.	0x0	R/W
2	LINK_TX6	Short Together BSYNC6 Driver 50 Ω Link Terminations. This bit selects if the 50 Ω link terminations of the BSYNC6 driver are shorted together or not. 0: Terminations not shorted together (default). 1: Terminations shorted together.	0x0	R/W
1	AC_COUPLED6	BSYNC6 Receive AC-Coupled Mode. This bit selects if the BSYNC6 receiver is set to receive AC- or DC-coupled clocks. 0: DC-coupled clocks (default). 1: AC-coupled clocks.	0x0	R/W
0	RESERVED	Reserved.	0x0	R/W

Address: 0x4D, Reset: 0x00, Name: REG004D

Table 94. Bit Descriptions for REG004D

Bits	Bit Name	Description	Reset	Access
7	ODIV_SEL7	BSYNC7 ODIVA or ODIVB Integer Divide Ratio Select. This bit selects ODIVA (when cleared to 0 (default)) or ODIVB (when set to 1) divide ratios for the BSYNC7 channel.	0x0	R/W
6	BOOST7	BSYNC 7 Driver Current Level. This bit selects the BSYNC 7 driver current level: 0: 14 mA driver current (default). 1: 20 mA driver current.	0x0	R/W
[5:0]	RCM7	BSYNC7 Driver Common-Mode Resistor Value. This 6-bit field selects R_CM7, the common-mode resistor value of the BSYNC7 driver. R_CM7 = 700/(73.5 − RCM7). V_CM7, the common-mode voltage of the BSYNC7 driver is then V_CM7 = I_DRV × (26.5 + R_CM7), where I_DRV is the BSYNC driver current level set by BOOST7 bit. I_DRV = 20 mA when BOOST7 = 1. I_DRV = 14 mA when BOOST7 = 0.	0x0	R/W

Address: 0x4E, Reset: 0x00, Name: REG004E

Table 95. Bit Descriptions for REG004E

Bits	Bit Name	Description	Reset	Access
7	AUTO_PD_RCV_7	Automatically Powers Down BSYNC7 Receiver. This bit selects if the BSYNC7 receiver powers down or not when it is not used by the TDC. Initialize this bit to 1 after power up/reset. 0: BSYNC7 Receiver stays powered up all the time. 1: BSYNC7 Receiver powers down when not used in the TDC measurement.	0x0	R/W
6	RESERVED	Reserved.	0x0	R/W
5	FLOAT_RX7	Disconnect BSYNC7 Receiver 50 Ω Float Connections to Ground. This bit selects if the 50 Ω float terminations of the BSYNC7 receiver are connected to ground or not. 0: Terminations connected to ground (default). 1: Terminations not connected to ground.	0x0	R/W
4	FLOAT_TX7	Disconnect BSYNC7 Driver 50 Ω Float Connections to Ground. This bit selects if the 50 Ω float terminations of the BSYNC7 driver are connected to ground or not. 0: Terminations connected to ground (default). 1: Terminations not connected to ground.	0x0	R/W
3	LINK_RX_7	Short Together BSYNC7 Receiver 50 Ω Link Terminations. This bit selects if the 50 Ω link terminations of the BSYNC7 receiver are shorted together or not. Initialize this bit to 1 after power up/reset. 0: Terminations not shorted together (default).	0x0	R/W

REGISTER DETAILS

Table 95. Bit Descriptions for REG004E (Continued)

Bits	Bit Name	Description	Reset	Access
		1: Terminations shorted together.		
2	LINK_TX7	Short Together BSYNC7 Driver 50 Ω Link Terminations. This bit selects if the 50 Ω link terminations of the BSYNC7 driver are shorted together or not. 0: Terminations not shorted together (default). 1: Terminations shorted together.	0x0	R/W
1	AC_COUPLED7	BSYNC7 Receive AC-coupled Mode. This bit selects if the BSYNC7 receiver is set to receive AC- or DC-coupled clocks. 0: DC-coupled clocks (default). 1: AC-coupled clocks.	0x0	R/W
0	RESERVED	Reserved.	0x0	R/W

Address: 0x4F, Reset: 0x00, Name: REG004F

Table 96. Bit Descriptions for REG004F

Bits	Bit Name	Description	Reset	Access
7	ODIV_SEL8	BSYNC8 ODIVA or ODIVB Integer Divide Ratio Select. This bit selects ODIVA (when cleared to 0(default)) or ODIVB (when set to 1) divide ratios for the BSYNC8 channel.	0x0	R/W
6	BOOST8	BSYNC 8 Driver Current Level. This bit selects the BSYNC 8 driver current level. 0: 14 mA driver current (default). 1: 20 mA driver current.	0x0	R/W
[5:0]	RCM8	BSYNC8 Driver Common Mode Resistor Value. This 6-bit field selects R_CM8, the common mode resistor value of the BSYNC8 driver. R_CM8=700/(73.5-RCM8). V_CM8, the common mode voltage of the BSYNC8 driver is then V_CM8=I_DRV x (26.5+R_CM8), where I_DRV is the BSYNC driver current level set by BOOST8 bit: I_DRV=20 mA when BOOST8=1 and I_DRV=14 mA when BOOST8=0.	0x0	R/W

Address: 0x50, Reset: 0x00, Name: REG0050

Table 97. Bit Descriptions for REG0050

Bits	Bit Name	Description	Reset	Access
7	AUTO_PD_RCV_8	Automatically Powers Down BSYNC8 Receiver. This bit selects if the BSYNC8 receiver powers down or not when it is not used by the TDC. Initialize this bit to 1 after power up/reset. 0: BSYNC8 Receiver stays powered up all the time 1: BSYNC8 Receiver powers down when not used in the TDC measurement	0x0	R/W
6	RESERVED	RESERVED	0x0	R/W
5	FLOAT_RX8	Disconnect BSYNC8 Receiver 50 Ω Float Connections to Ground. This bit selects if the 50 Ω float terminations of the BSYNC8 receiver are connected to ground or not. 0: Terminations connected to ground (default). 1: Terminations not connected to ground.	0x0	R/W
4	FLOAT_TX8	Disconnect BSYNC8 Driver 50 Ω Float Connections to Ground. This bit selects if the 50 Ω float terminations of the BSYNC8 driver are connected to ground or not. 0: Terminations connected to ground (default). 1: Terminations not connected to ground.	0x0	R/W
3	LINK_RX_8	Short Together BSYNC8 Receiver 50 Ω Link Terminations. This bit selects if the 50 Ω link terminations of the BSYNC8 receiver are shorted together or not. Initialize this bit to 1 after power up/reset. 0: Terminations not shorted together (default). 1: Terminations shorted together.	0x0	R/W
2	LINK_TX8	Short Together BSYNC8 Driver 50 Ω Link Terminations. This bit selects if the 50 Ω link terminations of the BSYNC8 driver are shorted together or not. 0: Terminations not shorted together (default). 1: Terminations shorted together.	0x0	R/W
1	AC_COUPLED8	BSYNC8 Receive AC-coupled Mode. This bit selects if the BSYNC8 receiver is set to receive AC- or DC-coupled clocks.	0x0	R/W

REGISTER DETAILS

Table 97. Bit Descriptions for REG0050 (Continued)

Bits	Bit Name	Description	Reset	Access
		0: DC-coupled clocks (default). 1: AC-coupled clocks.		
0	RESERVED	Reserved.	0x0	R/W

Address: 0x51, Reset: 0x00, Name: REG0051

Table 98. Bit Descriptions for REG0051

Bits	Bit Name	Description	Reset	Access
7	ODIV_SEL9	BSYNC9 ODIVA or ODIVB Integer Divide Ratio Select. This bit selects ODIVA (when cleared to 0, which is the default value) or ODIVB (when set to 1) divide ratios for BSYNC9 channel.	0x0	R/W
6	BOOST9	BSYNC 9 Driver Current Level. This bit selects the BSYNC 9 driver current level. 0: 14 mA driver current (default). 1: 20 mA driver current.	0x0	R/W
[5:0]	RCM9	BSYNC9 Driver Common-Mode Resistor Value. This 6-bit field selects R_CM9, the common-mode resistor value of the BSYNC9 driver. R_CM9 = 700/(73.5 − RCM9). V_CM9, the common-mode voltage of the BSYNC9 driver is then V_CM9 = I_DRV × (26.5 + R_CM9), where I_DRV is the BSYNC driver current level set by BOOST9 bit. I_DRV = 20 mA when BOOST9 = 1. I_DRV=14 mA when BOOST9 = 0.	0x0	R/W

Address: 0x52, Reset: 0x00, Name: REG0052

Table 99. Bit Descriptions for REG0052

Bits	Bit Name	Description	Reset	Access
7	AUTO_PD_RCV_9	Automatically Powers Down BSYNC9 Receiver. This bit selects if the BSYNC9 receiver powers down or not when it is not used by the TDC. Initialize this bit to 1 after power up/reset. 0: BSYNC9 Receiver stays powered up all the time. 1: BSYNC9 Receiver powers down when not used in the TDC measurement.	0x0	R/W
6	RESERVED	Reserved.	0x0	R/W
5	FLOAT_RX9	Disconnect BSYNC9 Receiver 50 Ω Float Connections to Ground. This bit selects if the 50 Ω float terminations of the BSYNC9 receiver are connected to ground or not. 0: Terminations connected to ground (default). 1: Terminations not connected to ground.	0x0	R/W
4	FLOAT_TX9	Disconnect BSYNC9 Driver 50 Ω Float Connections to Ground. This bit selects if the 50 Ω float terminations of the BSYNC9 driver are connected to ground or not. 0: Terminations connected to ground (default). 1: Terminations not connected to ground.	0x0	R/W
3	LINK_RX_9	Short Together BSYNC9 Receiver 50 Ω Link Terminations. This bit selects if the 50 Ω link terminations of the BSYNC9 receiver are shorted together or not. Initialize this bit to 1 after power up/reset. 0: Terminations not shorted together (default). 1: Terminations shorted together.	0x0	R/W
2	LINK_TX9	Short Together BSYNC9 Driver 50 Ω Link Terminations. This bit selects if the 50 Ω link terminations of the BSYNC9 driver are shorted together or not. 0: Terminations not shorted together (default). 1: Terminations shorted together.	0x0	R/W
1	AC_COUPLED9	BSYNC9 Receive AC-coupled Mode. This bit selects if the BSYNC9 receiver is set to receive AC- or DC-coupled clocks. 0: DC-coupled clocks (default). 1: AC-coupled clocks.	0x0	R/W
0	RESERVED	Reserved.	0x0	R/W

Address: 0x53, Reset: 0x40, Name: REG0053

REGISTER DETAILS

Table 100. Bit Descriptions for REG0053

Bits	Bit Name	Description	Reset	Access
[7:0]	ODIVA[7:0]	ODIVA Integer Divide Ratio. This 12-bit unsigned value represents ODIVA, the divider factor A of every BSYNC channel. Bits[11:8] are stored in Register 0x0054, while Bits[7:0] are stored in Register 0x0053. The default value is 0x040. The value of the ODIVA divide ratio is the value stored in these registers. Do not use ODIVA values lower than 10. Initialize these bits to 0000 0001 1001 after power up/reset, that is ODIVA = 25.	0x40	R/W

Address: 0x54, Reset: 0x00, Name: REG0054

Table 101. Bit Descriptions for REG0054

Bits	Bit Name	Description	Reset	Access
[7:4]	ODIVB[3:0]	ODIVB Integer Divide Ratio. This 12-bit unsigned value represents ODIVB, the divider factor B of every BSYNC channel. Bits[11:4] are stored in Register 0x0055, while Bits[3:0] are stored in Register 0x0054. The default value is 0x000. The value of the ODIVB divide ratio is the value stored in these registers. Do not use ODIVB values lower than 10. Initialize these bits to 0000 0001 1001 after power up/reset, that is ODIVB = 25.	0x0	R/W
[3:0]	ODIVA[11:8]	ODIVA Integer Divide Ratio. This 12-bit unsigned value represents ODIVA, the divider factor A of every BSYNC channel. Bits[11:8] are stored in Register 0x0054, while Bits[7:0] are stored in Register 0x0053. The default value is 0x040. The value of the ODIVA divide ratio is the value stored in these registers. Do not use ODIVA values lower than 10. Initialize these bits to 0000 0001 1001 after power up/reset, that is ODIVA = 25.	0x0	R/W

Address: 0x55, Reset: 0x00, Name: REG0055

Table 102. Bit Descriptions for REG0055

Bits	Bit Name	Description	Reset	Access
[7:0]	ODIVB[11:4]	ODIVB Integer Divide Ratio. This 12-bit unsigned value represents ODIVB, the divider factor B of every BSYNC channel. Bits[11:4] are stored in Register 0x0055, while Bits[3:0] are stored in Register 0x0054. The default value is 0x000. The value of the ODIVB divide ratio is the value stored in these registers. Do not use ODIVB values lower than 10. Initialize these bits to 0000 0001 1001 after power up/reset, that is ODIVB = 25.	0x0	R/W

Address: 0x56, Reset: 0x14, Name: REG0056

Table 103. Bit Descriptions for REG0056

Bits	Bit Name	Description	Reset	Access
[7:0]	NDIV[7:0]	PLL Feedback Divide Ratio. This 8-bit unsigned value represents the feedback divider of the PLL. The default value is 20. The value of the PLL multiplication ratio is the value stored in this register. Do not set NDIV to values lower than 8. Initialize this Register to 0x7D after power up/reset.	0x14	R/W

Address: 0x57, Reset: 0x01, Name: REG0057

Table 104. Bit Descriptions for REG0057

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R/W
[6:5]	CP_I	PLL Charge Pump Current. This 2-bit field selects the PLL charge pump. Initialize these bits to 10 after power up/reset. 00: 360 uA. 01: 450 uA. 10: 540 uA. 11: 630 uA.	0x0	R/W
[4:0]	RDIV	REF Integer Reference Divider. This 5-bit unsigned value represents the reference divider. The default value is 1. The value of the reference divider is the value stored in this register. If the reference divider is set to 0, the ADF4030 behaves as if the value was 1. Initialize these bits to 00101 after power up/reset, that is set RDIV = 5.	0x1	R/W

Address: 0x58, Reset: 0x00, Name: REG0058

Table 105. Bit Descriptions for REG0058

Bits	Bit Name	Description	Reset	Access
7	SEL_DIGCLK	Digital Core Clock Source Select. Clear this bit to 0 (default) to use the clock signal originating at the REFIN pins to create the digital core clock. If the REFIN frequency is greater than 125 MHz, program the 2-bit value	0x0	R/W

REGISTER DETAILS

Table 105. Bit Descriptions for REG0058 (Continued)

Bits	Bit Name	Description	Reset	Access
		(CORE_CLK_DIV) in Register 0x0058[5:4] to reduce the REFIN frequency as necessary. Set this bit to 1 to use the free running ring oscillator in the TDC divided by 16 (approximately 44 MHz) to create the digital core clock. 0: Digital core clock uses REFIN as frequency source 1: Digital core clock uses the free running oscillator as frequency source		
6	EN_DIGCLK	Enables the digital core clock. Initialize this bit to 1 after power up/reset.	0x0	R/W
[5:4]	CORE_CLK_DIV	Digital Core Clock Reference Divider. This 2-bit unsigned value represents the reference clock divider in the path that creates the digital core clock when Bit 7, SEL_DIGCLK, in Register 0x0058 is set to 1. The default value is 0. The digital core clock is then REFIN/$2^{CORE\_CLK\_DIV}$. Set the CORE_CLK_DIV bits to obtain a digital core clock lower than 125 MHz. Initialize these bits to 01 after power up/reset.	0x0	R/W
[3:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x59, Reset: 0x09, Name: REG0059

Table 106. Bit Descriptions for REG0059

Bits	Bit Name	Description	Reset	Access
7	RST_LD	Reset Lock Detector to the Unlocked State.	0x0	R/W
[6:4]	BAND_SEL_M	Force the Band for the PLL VCO. Initialize these bits to 100 after power up/reset.	0x0	R/W
[3:0]	RESERVED	Reserved.	0x9	R/W

Address: 0x5A, Reset: 0x47, Name: REG005A

Table 107. Bit Descriptions for REG005A

Bits	Bit Name	Description	Reset	Access
7	RST_PLL_CAL	Reset B for Calibration Circuitry.	0x0	R/W
6	PLL_CAL_EN	Enable Automatic VCO Band Calibration. Clear this bit to 0 after power up/reset.	0x1	R/W
[5:4]	PLL_CAL_CNT	Lock Timer for Band Calibration in PFD Cycles. Initialize these bits to 01 after power up/reset. 00: 511 Cycles or 25.55 µs. 01: 1023 Cycles or 51.15 µs. 10: 1535 Cycles or 76.75 µs. 11: 2047 Cycles or 102.35 µs.	0x0	R/W
[3:0]	RESERVED	Reserved.	0x7	R/W

Address: 0x5B, Reset: 0x00, Name: REG005B

Table 108. Bit Descriptions for REG005B

Bits	Bit Name	Description	Reset	Access
7	EN_LOL	Enable Loss-of-Lock Detector. Initialize this bit to 1 after power up/reset.	0x0	R/W
6	EN_LDWIN	Enable the Lock Detector Pulse Window. Initialize this bit to 1 after power up/reset.	0x0	R/W
5	LDWIN_PW	Lock Detector Pulse Window Width.	0x0	R/W
[4:0]	LD_COUNT	Number of PFD Cycles Before LD Goes High. Initialize these bits to 01001 after power up/reset.	0x0	R/W

Address: 0x5C, Reset: 0x00, Name: REG005C

Table 109. Bit Descriptions for REG005C

Bits	Bit Name	Description	Reset	Access
7	CMOS_OV	CMOS High Level Voltage Select. This bit selects the CMOS high level of the of the following pins: SDO, SDIO, IRQB, MUXOUT1, and MUXOUT2. Set the CMOS_OV bit to 1 to select a 3.3 V CMOS high level. Clear CMOS_OV bit to 0 (default) to select a 1.8 V CMOS high level. 0: 1.8 V Logic. 1: 3.3 V Logic.	0x0	R/W
6	RST_ALIGN_IRQ	Reset and/or Stop the Accumulated Delay Monitor. To reset the accumulated delay monitor and start a new monitoring cycle, set this bit to 1 and then write it again with the value cleared to 0. Initialize this bit to 1 after power up/reset.	0x0	R/W

REGISTER DETAILS

Table 109. Bit Descriptions for REG005C (Continued)

Bits	Bit Name	Description	Reset	Access
		0: Normal operation of accumulated delay monitor. 1: Stop the accumulated delay monitor.		
5	RST_TEMP	Reset and/or Stop Temperature Monitor. To reset the temperature monitor and start a new temperature monitoring cycle, set this bit to 1 and then write it again with the value cleared to 0. Initialize this bit to 1 after power up/reset. 0: Normal operation. 1: Stop the temperature monitor.	0x0	R/W
4	MASK_TDC_ERR	TDC Error and ADEL Overflow Interrupt Enable. Initialize this bit to 1 after power up/reset. 0: Disable (that is, mask) the TDC error and ADEL overflow monitors interrupt. 1: Enable (that is unmask) TDC error and ADEL overflow monitors interrupt.	0x0	R/W
3	MASK_LD	PLL Lock Detect Interrupt Enable. Initialize this bit to 1 after power up/reset. 0: Disable (mask) PLL lock detect interrupt. 1: Enable (unmask) PLL lock detect interrupt.	0x0	R/W
2	MASK_ALIGN_IRQ	BSYNC Accumulated Delay interrupt enable. Initialize this bit to 1 after power up/reset. 0: Disable (mask) BSYNC accumulated delay interrupt. 1: Enable (unmask) BSYNC accumulated delay interrupt.	0x0	R/W
1	MASK_TEMP	Temperature Monitor Interrupt Enable. Initialize this bit to 1 after power up/reset. 0: Disable (mask) temperature monitor interrupt. 1: Enable (unmask) temperature monitor interrupt.	0x0	R/W
0	IRQB_OPENDRAIN	IRQB Pin Output Type. 0: IRQB pin behaves like a standard CMOS output. 1: IRQB pin is an open drain output.	0x0	R/W

Address: 0x5D, Reset: 0x00, Name: REG005D

Table 110. Bit Descriptions for REG005D

Bits	Bit Name	Description	Reset	Access
[7:0]	ALIGN_IRQ_TH	BSYNC Accumulated Delay Threshold. This 8-bit unsigned value determines the threshold used during the BSYNC accumulated delay monitor. The bit weight is approximately 12.5 ps, with an accuracy of the threshold of around ±23 ps. Initialize this register to 0x10 after power up/reset.	0x0	R/W

Address: 0x5E, Reset: 0x00, Name: REG005E

Table 111. Bit Descriptions for REG005E

Bits	Bit Name	Description	Reset	Access
[7:0]	TEMP_IRQ_TH	Temperature Interrupt Threshold. This 8-bit unsigned value determines the temperature threshold used during the temperature monitoring. It is expressed in °C. Initialize this register to 0x32 after power up/reset.	0x0	R/W

Address: 0x5F, Reset: 0x00, Name: REG005F

Table 112. Bit Descriptions for REG005F

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x60, Reset: 0x00, Name: REG0060

Table 113. Bit Descriptions for REG0060

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R/W
6	ADC_C_CNV	ADC Continuous Conversion (Not Recommended).	0x0	R/W
[5:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x61, Reset: 0x00, Name: REG0061

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Table 114. Bit Descriptions for REG0061

Bits	Bit Name	Description	Reset	Access
7	RST_TDC_ERR	Reset and/or Stop TDC Error and ADEL Overflow Monitors. To reset the TDC error and ADEL overflow monitors and start a new TDC error and ADEL overflow monitoring cycle, write this bit with the value set to 1 and then write it again with the value cleared to 0. 0: Normal operation. 1: Stop the TDC error and ADEL overflow monitors.	0x0	R/W
6	ADC_CLK_SEL	Select ADC Clock Source. 0: The digital core clock is the ADC clock source (default). 1: A clock generated at the SCLK pin is the ADC clock source.	0x0	R/W
[5:3]	RESERVED	Reserved.	0x0	R/W
2	EN_ADC_CNV	Enable ADC Conversion. Initialize this bit to 1 after power up/reset. 0: ADC conversion is disabled (default). 1: ADC conversion is enabled.	0x0	R/W
1	EN_ADC_CLK	Enable ADC Clock Path. 0: The ADC clock path is not enabled (default). 1: The ADC clock path is enabled.	0x0	R/W
0	EN_ADC	Enable ADC. Initialize this bit to 1 after power up/reset.	0x0	R/W

Address: 0x62, Reset: 0x00, Name: REG0062

Table 115. Bit Descriptions for REG0062

Bits	Bit Name	Description	Reset	Access
[7:0]	ADC_CLK_DIV	Divider in the Digital Core Clock Path towards the ADC. This 8-bit unsigned divider K determines an ADC clock frequency $f_{ADC} = f_{CORECLOCK}/(4 \times K + 2)$. The f_{ADC} must be a maximum 400 kHz. K must also be greater or equal to $f_{CORECLOCK}/1.6E6 - 0.5$. Initialize this register to 0x4C after power up/reset.	0x0	R/W

Address: 0x63, Reset: 0x00, Name: REG0063

Table 116. Bit Descriptions for REG0063

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R/W
[4:0]	MUXCODE1	Select Signal at MUXOUT1 Pin. Initialize these bits to 11110 = 30 after power up/reset. 00000: 0 = High impedance. 00001: 1 = Digital core clock divided by 2. 00010: 2 = Period clock divided by 2. 00011: 3 = State of Bit 1, ADC_BUSY, of Register 0x8F. 00100: 4 = State of Bit 4, TDC_BUSY, of Register 0x8F. 00101: 5 = State of Bit 3, DL_BUSY, of Register 0x8F. 00110: 6 = State of Bit 0, FSM_BUSY, of Register 0x8F. 00111: 7 = PLL PFD input clock from the NDIV divider divided by 2. 01000: 8 = PLL PFD input clock from the RDIV divider divided by 2. 01001: 9 = Reserved. 01010: 10 = Reserved. 01011: 11 = Reserved. 01100: 12 = Reserved. 01101: 13 = Reserved. 01110: 14 = Reserved. 01111: 15 = Reserved. 10000: 16 = Reserved. 10001: 17 = Reserved. 10010: 18 = State if Bit 0, PLL_LD, of Register 0x90. 10011: 19 = State of Bit 1, CAL_COMP, of Register 0xBA.	0x0	R/W

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Table 116. Bit Descriptions for REG0063 (Continued)

Bits	Bit Name	Description	Reset	Access
		10100: 20 = State of Bit 0, CAL_BUSY, of Register 0xBA. 10101: 21 = Reserved. 10110: 22 = Reserved. 10111: 23 = Logical OR of the live (not latched) TDC error signals associated with Bits[2:1], TDC_ERR, of Register 0x90. 11000: 24 = Logic 0. 11001: 25 = Reserved. 11010: 26 = Reserved. 11011: 27 = Reserved. 11100: 28 = TDC Source Clock. 11101: 29 = Logic 1. 11110: 30 = The state of Bit 6, GPO1, of Register 0x68. 11111: 31 = Unused.		

Address: 0x64, Reset: 0x00, Name: REG0064

Table 117. Bit Descriptions for REG0064

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R/W
[4:0]	MUXCODE2	Select Signal at MUXOUT2 Pin. Initialize these bits to 11110 after power up/reset. 00000: 0 = High impedance. 00001: 1 = Digital core clock divided by 2. 00010: 2 = Period clock divided by 2. 00011: 3 = State of Bit 1, ADC_BUSY, of Register 0x8F. 00100: 4 = State of Bit 4, TDC_BUSY, of Register 0x8F. 00101: 5 = State of Bit 3, DL_BUSY, of Register 0x8F. 00110: 6 = State of Bit 0, FSM_BUSY, of Register 0x8F. 00111: 7 = PLL PFD input clock from the NDIV divider divided by 2. 01000: 8 = PLL PFD input clock from the RDIV divider divided by 2. 01001: 9 = Reserved. 01010: 10 = Reserved. 01011: 11 = Reserved. 01100: 12 = Reserved. 01101: 13 = Reserved. 01110: 14 = Reserved. 01111: 15 = Reserved. 10000: 16 = PLL NDIV divider output clock. 10001: 17 = PLL RDIV divider output clock. 10010: 18 = State if Bit 0, PLL_LD, of Register 0x90. 10011: 19 = State of Bit 1, CAL_COMP, of Register 0xBA. 10100: 20 = State of Bit 0, CAL_BUSY, of Register 0xBA. 10101: 21 = Reserved. 10110: 22 = Reserved. 10111: 23 = Logical OR of the live (not latched) TDC error signals associated with Bits[2:1], TDC_ERR, of Register 0x90. 11000: 24 = Logic 0. 11001: 25 = Reserved. 11010: 26 = Reserved. 11011: 27 = Reserved. 11100: 28 = TDC Target clock.	0x0	R/W

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Table 117. Bit Descriptions for REG0064 (Continued)

Bits	Bit Name	Description	Reset	Access
		11101: 29 = Logic 1. 11110: 30 = The state of Bit 7, GPO2, of Register 0x68. 11111: 31 = Unused.		

Address: 0x65, Reset: 0x00, Name: REG0065

Table 118. Bit Descriptions for REG0065

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED[7:0]	Reserved.	0x0	R/W

Address: 0x66, Reset: 0x00, Name: REG0066

Table 119. Bit Descriptions for REG0066

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x67, Reset: 0x00, Name: REG0067

Table 120. Bit Descriptions for REG0067

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x68, Reset: 0x00, Name: REG0068

Table 121. Bit Descriptions for REG0068

Bits	Bit Name	Description	Reset	Access
7	GPO2	General Purpose Output for MUXOUT2. The state of this bit is reflected at the MUXOUT2 pin when the MUXCODE2 Bits[4:0] in Register 0x0064 are set to 30.	0x0	R/W
6	GPO1	General Purpose Output for MUXOUT1. The state of this bit is reflected at the MUXOUT1 pin when the MUXCODE1 Bits[4:0] in Register 0x0063 are set to 30.	0x0	R/W
[5:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x69, Reset: 0x00, Name: REG0069

Table 122. Bit Descriptions for REG0069

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x6A, Reset: 0x00, Name: REG006A

Table 123. Bit Descriptions for REG006A

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x6B, Reset: 0x00, Name: REG006B

Table 124. Bit Descriptions for REG006B

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x6C, Reset: 0x00, Name: REG006C

Table 125. Bit Descriptions for REG006C

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x6D, Reset: 0x00, Name: REG006D

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Table 126. Bit Descriptions for REG006D

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x6E, Reset: 0x00, Name: REG006E

Table 127. Bit Descriptions for REG006E

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x6F, Reset: 0x00, Name: REG006F

Table 128. Bit Descriptions for REG006F

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x70, Reset: 0x00, Name: REG0070

Table 129. Bit Descriptions for REG0070

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R

Address: 0x71, Reset: 0x00, Name: REG0071

Table 130. Bit Descriptions for REG0071

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x72, Reset: 0x00, Name: REG0072

Table 131. Bit Descriptions for REG0072

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	ADC_ST_CNV	Write this Bit to Start an ADC Conversion. Writing any value to this bit starts an ADC conversion. The Bits[7:1] of the Register 0x0072 can also be written with any value during this write operation.	0x0	R/W

Address: 0x73, Reset: 0x00, Name: REG0073

Table 132. Bit Descriptions for REG0073

Bits	Bit Name	Description	Reset	Access
[7:0]	TDC_RSLT_UI[7:0]	Normalized Phase Offset Between the Two Input Clocks to the TDC. This phase offset is a signed 24-bit number with the less significant bit carrying a weight of $2^{(-24)}$ UI. A positive result means the source clock lags the target clock in time, and a negative result means the source clock leads the target clock in time.	0x0	R

Address: 0x74, Reset: 0x00, Name: REG0074

Table 133. Bit Descriptions for REG0074

Bits	Bit Name	Description	Reset	Access
[7:0]	TDC_RSLT_UI[15:8]	Normalized Phase Offset Between the Two Input Clocks to the TDC. This phase offset is a signed 24-bit number with the less significant bit carrying a weight of $2^{(-24)}$ UI. A positive result means the source clock lags the target clock in time, and a negative result means the source clock leads the target clock in time.	0x0	R

Address: 0x75, Reset: 0x00, Name: REG0075

Table 134. Bit Descriptions for REG0075

Bits	Bit Name	Description	Reset	Access
[7:0]	TDC_RSLT_UI[23:16]	Normalized Phase Offset Between the Two Input Clocks to the TDC. This phase offset is a signed 24-bit number with the less significant bit carrying a weight of $2^{(-24)}$ UI. A positive result means the	0x0	R

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Table 134. Bit Descriptions for REG0075 (Continued)

Bits	Bit Name	Description	Reset	Access
		source clock lags the target clock in time, and a negative result means the source clock leads the target clock in time.		

Address: 0x76, Reset: 0x00, Name: REG0076

Table 135. Bit Descriptions for REG0076

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R

Address: 0x77, Reset: 0x00, Name: REG0077

Table 136. Bit Descriptions for REG0077

Bits	Bit Name	Description	Reset	Access
[7:0]	TIMEDIFF_MEAS[7:0]	Time Difference Measurement Between Source and Target Clock Edges. This 34-bit signed word represents the average of the last four TIMEDIFF samples of the TDC post processor.	0x0	R

Address: 0x78, Reset: 0x00, Name: REG0078

Table 137. Bit Descriptions for REG0078

Bits	Bit Name	Description	Reset	Access
[7:0]	TIMEDIFF_MEAS[15:8]	This 34-bit signed word represents the average of the last four TIMEDIFF samples of the TDC post processor.	0x0	R

Address: 0x79, Reset: 0x00, Name: REG0079

Table 138. Bit Descriptions for REG0079

Bits	Bit Name	Description	Reset	Access
[7:0]	TIMEDIFF_MEAS[23:16]	This 34-bit signed word represents the average of the last four TIMEDIFF samples of the TDC post processor.	0x0	R

Address: 0x7A, Reset: 0x00, Name: REG007A

Table 139. Bit Descriptions for REG007A

Bits	Bit Name	Description	Reset	Access
[7:0]	TIMEDIFF_MEAS[31:24]	This 34-bit signed word represents the average of the last four TIMEDIFF samples of the TDC post processor.	0x0	R

Address: 0x7B, Reset: 0x00, Name: REG007B

Table 140. Bit Descriptions for REG007B

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	TIMEDIFF_MEAS[33:32]	This 34-bit signed word represents the average of the last four TIMEDIFF samples of the TDC post processor.	0x0	R

Address: 0x7C, Reset: 0x00, Name: REG007C

Table 141. Bit Descriptions for REG007C

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R

Address: 0x7D, Reset: 0x00, Name: REG007D

Table 142. Bit Descriptions for REG007D

Bits	Bit Name	Description	Reset	Access
[7:0]	PERIOD_MEAS[7:0]	This 32-bit unsigned word represents the average of the last four period samples of the TDC postprocessor.	0x0	R

Address: 0x7E, Reset: 0x00, Name: REG007E

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Table 143. Bit Descriptions for REG007E

Bits	Bit Name	Description	Reset	Access
[7:0]	PERIOD_MEAS[15:8]	This 32-bit unsigned word represents the average of the last four period samples of the TDC postprocessor.	0x0	R

Address: 0x7F, Reset: 0x00, Name: REG007F

Table 144. Bit Descriptions for REG007F

Bits	Bit Name	Description	Reset	Access
[7:0]	PERIOD_MEAS[23:16]	This 32-bit unsigned word represents the average of the last four period samples of the TDC postprocessor.	0x0	R

Address: 0x80, Reset: 0x00, Name: REG0080

Table 145. Bit Descriptions for REG0080

Bits	Bit Name	Description	Reset	Access
[7:0]	PERIOD_MEAS[31:24]	This 32-bit unsigned word represents the average of the last four period samples of the TDC postprocessor.	0x0	R

Address: 0x81, Reset: 0x00, Name: REG0081

Table 146. Bit Descriptions for REG0081

Bits	Bit Name	Description	Reset	Access
[7:0]	ALIGN_TOT[7:0]	Total Alignment Calculated During Every Alignment Cycle.	0x0	R

Address: 0x82, Reset: 0x00, Name: REG0082

Table 147. Bit Descriptions for REG0082

Bits	Bit Name	Description	Reset	Access
[7:0]	ALIGN_TOT[15:8]	Total Alignment Calculated During Every Alignment Cycle..	0x0	R

Address: 0x83, Reset: 0x00, Name: REG0083

Table 148. Bit Descriptions for REG0083

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	ALIGN_TOT[21:16]	Total Alignment Calculated During Every Alignment Cycle.	0x0	R

Address: 0x84, Reset: 0x00, Name: REG0084

Table 149. Bit Descriptions for REG0084

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	ADEL_0	This 5-bit read-only word shows the ADEL value used during a delay adjustment process on the BSYNC0 channel.	0x0	R

Address: 0x85, Reset: 0x00, Name: REG0085

Table 150. Bit Descriptions for REG0085

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	ADEL_1	This 5-bit read-only word shows the ADEL value used during a delay adjustment process on the BSYNC1 channel.	0x0	R

Address: 0x86, Reset: 0x00, Name: REG0086

Table 151. Bit Descriptions for REG0086

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	ADEL_2	This 5-bit read-only word shows the ADEL value used during a delay adjustment process on the BSYNC2 channel.	0x0	R

Address: 0x87, Reset: 0x00, Name: REG0087

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Table 152. Bit Descriptions for REG0087

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	ADEL_3	This 5-bit read-only word shows the ADEL value used during a delay adjustment process on the BSYNC3 channel.	0x0	R

Address: 0x88, Reset: 0x00, Name: REG0088

Table 153. Bit Descriptions for REG0088

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	ADEL_4	This 5-bit read-only word shows the ADEL value used during a delay adjustment process on the BSYNC4 channel.	0x0	R

Address: 0x89, Reset: 0x00, Name: REG0089

Table 154. Bit Descriptions for REG0089

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	ADEL_5	This 5-bit read-only word shows the ADEL value used during a delay adjustment process on the BSYNC5 channel.	0x0	R

Address: 0x8A, Reset: 0x00, Name: REG008A

Table 155. Bit Descriptions for REG008A

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	ADEL_6	This 5-bit read-only word shows the ADEL value used during a delay adjustment process on the BSYNC6 channel.	0x0	R

Address: 0x8B, Reset: 0x00, Name: REG008B

Table 156. Bit Descriptions for REG008B

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	ADEL_7	This 5-bit read-only word shows the ADEL value used during a delay adjustment process on the BSYNC7 channel.	0x0	R

Address: 0x8C, Reset: 0x00, Name: REG008C

Table 157. Bit Descriptions for REG008C

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	ADEL_8	This 5-bit read-only word shows the ADEL value used during a delay adjustment process on the BSYNC8 channel.	0x0	R

Address: 0x8D, Reset: 0x00, Name: REG008D

Table 158. Bit Descriptions for REG008D

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	ADEL_9	This 5-bit read-only word shows the ADEL value used during a delay adjustment process on the BSYNC9 channel.	0x0	R

Address: 0x8E, Reset: 0x00, Name: REG008E

Table 159. Bit Descriptions for REG008E

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	ALIGN_CYCLES_COUNT	Number of Alignment Cycles Performed.	0x0	R

Address: 0x8F, Reset: 0x00, Name: REG008F

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Table 160. Bit Descriptions for REG008F

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R
6	REF_OK	REFIN Receiver Peak Detector Status. Logic 1 indicates the REFIN peak detector monitor declares REF input is sufficient for normal operation. Logic 0 indicates REF input is missing or the peak level is too low for reliable operation.	0x0	R
5	RESERVED	Reserved.	0x0	R
4	TDC_BUSY	TDC Busy Signal. The TDC_BUSY bit is set to 1 when the TDC is executing a conversion and is cleared to 0 when the TDC is not executing a conversion.	0x0	R
3	DL_BUSY	Delay Line Busy.	0x0	R
2	MATH_BUSY	Math Busy.	0x0	R
1	ADC_BUSY	ADC Busy Signal. This bit is set to 1 when the ADC performs a measurement.	0x0	R
0	FSM_BUSY	Alignment Busy Signal.	0x0	R

Address: 0x90, Reset: 0x00, Name: REG0090

Table 161. Bit Descriptions for REG0090

Bits	Bit Name	Description	Reset	Access
[7:6]	IRQ_BSYNC[1:0]	BSYNC Accumulated Delay Monitor Status. This is a 10-bit field, each bit referring to one BSYNC channel. IRQ_BSYNC[0] corresponds to BSYNC0, IRQ_BSYNC[1] corresponds to BSYNC1, to continuing consecutively to IRQ_BSYNC[9] corresponding to BSYNC9. Bits[7:4] of Register 0x90 represent IRQ_BSYNC[3:0] and Bits[5:0] of Register 0x91 represent IRQ_BSYNC[9:4]. 0: BSYNC channel output clock has accumulated a delay less than or equal than the ALIGN_IRQ_TH threshold. 1: BSYNC channel output clock has accumulated a delay greater than the ALIGN_IRQ_TH threshold.	0x0	R
5	RESERVED	Reserved.	0x0	R
4	TEMP_MON	Temperature Monitor Status. 0: T_DIFF, the temperature monitor output, is less than or equal to the temperature threshold. 1: T_DIFF, the temperature monitor output, is greater than the temperature threshold.	0x0	R
3	TMP_ALIGN_ERR	Temporary Alignment Error Monitor Status. Status of temporary alignment error monitor during single-channel threshold alignment and single-channel fixed iteration alignment processes. See the Temporary Alignment Error IRQ section for details. 0: No temporary alignment error has occurred. 1: Temporary alignment error has occurred.	0x0	R
[2:1]	TDC_ERR	TDC Error Code. This 2-bit field contains an error code illustrating the TDC measurement state. 00: TDC measurement does not have any error. 01: At least one TDC input clock presents excessive jitter. 10: At least one TDC input clock is not present. 11: Excessive phase shift happened during TDC measurement.	0x0	R
0	PLL_LD	Live PLL Lock Detector Status. 0: PLL lock detector indicates the PLL is not locked. 1: PLL lock detector indicates the PLL is locked.	0x0	R

Address: 0x91, Reset: 0x00, Name: REG0091

Table 162. Bit Descriptions for REG0091

Bits	Bit Name	Description	Reset	Access
[7:0]	IRQ_BSYNC[9:2]	BSYNC Accumulated Delay Monitor Status. This is a 10-bit field, each bit referring to one BSYNC channel. IRQ_BSYNC[0] corresponds to BSYNC0, IRQ_BSYNC[1] corresponds to BSYNC1, consecutively to IRQ_BSYNC9 corresponding to BSYNC9. Bits[7:4] of Register 0x90 represent IRQ_BSYNC[3:0] and Bits[5:0] of Register 0x91 represent IRQ_BSYNC[9:4]. 0: BSYNC channel output clock has accumulated a delay lower or equal than the ALIGN_IRQ_TH threshold. 1: BSYNC channel output clock has accumulated a delay greater than the ALIGN_IRQ_TH threshold.	0x0	R

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Address: 0x92, Reset: 0x00, Name: REG0092

Table 163. Bit Descriptions for REG0092

Bits	Bit Name	Description	Reset	Access
[7:0]	TEMP_MEAS[7:0]	Temperature Measurement Result. This 9-bit field represents the temperature output value of the CTC block. It is expressed in °C. The Bits[7:0] represent the magnitude of the CTC result, and Bit 8 represents the sign of the CTC magnitude result. When Bit 8 is cleared to 0, the CTC magnitude result is positive. When Bit 8 is set to 1, the CTC magnitude result is negative.	0x0	R

Address: 0x93, Reset: 0x00, Name: REG0093

Table 164. Bit Descriptions for REG0093

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	TEMP_MEAS[8]	Temperature Measurement Result. This 9-bit field represents the temperature output value of the CTC block. It is expressed in °C. The Bits[7:0] represent the magnitude of the CTC result, and Bit 8 represents the sign of the CTC magnitude result. When Bit 8 is cleared to 0, the CTC magnitude result is positive. When Bit 8 is set to 1, the CTC magnitude result is negative.	0x0	R

Address: 0x94, Reset: 0x00, Name: REG0094

Table 165. Bit Descriptions for REG0094

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R

Address: 0x95, Reset: 0x00, Name: REG0095

Table 166. Bit Descriptions for REG0095

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:3]	DLY_TAP_STATE1	This field represents the Bits[2:0] of the NDEL_COAR[15:0] intermediate portion of the delay adjustment setting for BSYNC1. The bit weight is 1/8 of the VCO period.	0x0	R
[2:0]	DLY_TAP_STATE0	This field represents the Bits[2:0] of the NDEL_COAR[15:0] intermediate portion of the delay adjustment setting for BSYNC0. The bit weight is 1/8 of the VCO period.	0x0	R

Address: 0x96, Reset: 0x00, Name: REG0096

Table 167. Bit Descriptions for REG0096

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:3]	DLY_TAP_STATE3	This field represents the Bits[2:0] of the NDEL_COAR[15:0] intermediate portion of the delay adjustment setting for BSYNC3. The bit weight is 1/8 of the VCO period.	0x0	R
[2:0]	DLY_TAP_STATE2	This field represents the Bits[2:0] of the NDEL_COAR[15:0] intermediate portion of the delay adjustment setting for BSYNC2. The bit weight is 1/8 of the VCO period.	0x0	R

Address: 0x97, Reset: 0x00, Name: REG0097

Table 168. Bit Descriptions for REG0097

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:3]	DLY_TAP_STATE5	This field represents the Bits[2:0] of the NDEL_COAR[15:0] intermediate portion of the delay adjustment setting for BSYNC5. The bit weight is 1/8 of the VCO period.	0x0	R
[2:0]	DLY_TAP_STATE4	This field represents the Bits[2:0] of the NDEL_COAR[15:0] intermediate portion of the delay adjustment setting for BSYNC4. The bit weight is 1/8 of the VCO period.	0x0	R

Address: 0x98, Reset: 0x00, Name: REG0098

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Table 169. Bit Descriptions for REG0098

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:3]	DLY_TAP_STATE7	This field represents the Bits[2:0] of the NDEL_COAR[15:0] intermediate portion of the delay adjustment setting for BSYNC7. The bit weight is 1/8 of the VCO period.	0x0	R
[2:0]	DLY_TAP_STATE6	This field represents the Bits[2:0] of the NDEL_COAR[15:0] intermediate portion of the delay adjustment setting for BSYNC6. The bit weight is 1/8 of the VCO period.	0x0	R

Address: 0x99, Reset: 0x00, Name: REG0099

Table 170. Bit Descriptions for REG0099

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:3]	DLY_TAP_STATE9	This field represents the Bits[2:0] of the NDEL_COAR[15:0] intermediate portion of the delay adjustment setting for BSYNC9. The bit weight is 1/8 of the VCO period.	0x0	R
[2:0]	DLY_TAP_STATE8	This field represents the Bits[2:0] of the NDEL_COAR[15:0] intermediate portion of the delay adjustment setting for BSYNC8. The bit weight is 1/8 of the VCO period.	0x0	R

Address: 0x9A, Reset: 0x00, Name: REG009A

Table 171. Bit Descriptions for REG009A

Bits	Bit Name	Description	Reset	Access
[7:0]	ACCUM_DEL_0[7:0]	This is a 10-bit field representing BSYNC0 accumulated alignment delay since BSYNC alignment monitor interrupt has been activated (RST_ALIGN_IRQ bit cleared to 0).	0x0	R

Address: 0x9B, Reset: 0x00, Name: REG009B

Table 172. Bit Descriptions for REG009B

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	ACCUM_DEL_0[9:8]	This is a 10-bit field representing BSYNC0 accumulated alignment delay since BSYNC alignment monitor interrupt has been activated (RST_ALIGN_IRQ bit cleared to 0.)	0x0	R

Address: 0x9C, Reset: 0x00, Name: REG009C

Table 173. Bit Descriptions for REG009C

Bits	Bit Name	Description	Reset	Access
[7:0]	ACCUM_DEL_1[7:0]	This is a 10-bit field representing BSYNC1 accumulated alignment delay since BSYNC alignment monitor interrupt has been activated (RST_ALIGN_IRQ bit cleared to 0).	0x0	R

Address: 0x9D, Reset: 0x00, Name: REG009D

Table 174. Bit Descriptions for REG009D

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	ACCUM_DEL_1[9:8]	This is a 10-bit field representing BSYNC1 accumulated alignment delay since BSYNC alignment monitor interrupt has been activated (RST_ALIGN_IRQ bit cleared to 0).	0x0	R

Address: 0x9E, Reset: 0x00, Name: REG009E

Table 175. Bit Descriptions for REG009E

Bits	Bit Name	Description	Reset	Access
[7:0]	ACCUM_DEL_2[7:0]	This is a 10-bit field representing BSYNC2 accumulated alignment delay since BSYNC alignment monitor interrupt has been activated (RST_ALIGN_IRQ bit cleared to 0).	0x0	R

Address: 0x9F, Reset: 0x00, Name: REG009F

REGISTER DETAILS

Table 176. Bit Descriptions for REG009F

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	ACCUM_DEL_2[9:8]	This is a 10-bit field representing BSYNC2 accumulated alignment delay since BSYNC alignment monitor interrupt has been activated (RST_ALIGN_IRQ bit cleared to 0).	0x0	R

Address: 0xA0, Reset: 0x00, Name: REG00A0

Table 177. Bit Descriptions for REG00A0

Bits	Bit Name	Description	Reset	Access
[7:0]	ACCUM_DEL_3[7:0]	This is a 10-bit field representing BSYNC3 accumulated alignment delay since BSYNC alignment monitor interrupt has been activated (RST_ALIGN_IRQ bit cleared to 0).	0x0	R

Address: 0xA1, Reset: 0x00, Name: REG00A1

Table 178. Bit Descriptions for REG00A1

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	ACCUM_DEL_3[9:8]	This is a 10-bit field representing BSYNC3 accumulated alignment delay since BSYNC alignment monitor interrupt has been activated (RST_ALIGN_IRQ bit cleared to 0).	0x0	R

Address: 0xA2, Reset: 0x00, Name: REG00A2

Table 179. Bit Descriptions for REG00A2

Bits	Bit Name	Description	Reset	Access
[7:0]	ACCUM_DEL_4[7:0]	This is a 10-bit field representing BSYNC4 accumulated alignment delay since BSYNC alignment monitor interrupt has been activated (RST_ALIGN_IRQ bit cleared to 0).	0x0	R

Address: 0xA3, Reset: 0x00, Name: REG00A3

Table 180. Bit Descriptions for REG00A3

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	ACCUM_DEL_4[9:8]	This is a 10-bit field representing BSYNC4 accumulated alignment delay since BSYNC alignment monitor interrupt has been activated (RST_ALIGN_IRQ bit cleared to 0).	0x0	R

Address: 0xA4, Reset: 0x00, Name: REG00A4

Table 181. Bit Descriptions for REG00A4

Bits	Bit Name	Description	Reset	Access
[7:0]	ACCUM_DEL_5[7:0]	This is a 10-bit field representing BSYNC5 accumulated alignment delay since BSYNC alignment monitor interrupt has been activated (RST_ALIGN_IRQ bit cleared to 0).	0x0	R

Address: 0xA5, Reset: 0x00, Name: REG00A5

Table 182. Bit Descriptions for REG00A5

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	ACCUM_DEL_5[9:8]	This is a 10-bit field representing BSYNC5 accumulated alignment delay since BSYNC alignment monitor interrupt has been activated (RST_ALIGN_IRQ bit cleared to 0).	0x0	R

Address: 0xA6, Reset: 0x00, Name: REG00A6

Table 183. Bit Descriptions for REG00A6

Bits	Bit Name	Description	Reset	Access
[7:0]	ACCUM_DEL_6[7:0]	This is a 10-bit field representing BSYNC6 accumulated alignment delay since BSYNC alignment monitor interrupt has been activated (RST_ALIGN_IRQ bit cleared to 0).	0x0	R

Address: 0xA7, Reset: 0x00, Name: REG00A7

REGISTER DETAILS

Table 184. Bit Descriptions for REG00A7

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	ACCUM_DEL_6[9:8]	This is a 10-bit field representing BSYNC6 accumulated alignment delay since BSYNC alignment monitor interrupt has been activated (RST_ALIGN_IRQ bit cleared to 0).	0x0	R

Address: 0xA8, Reset: 0x00, Name: REG00A8

Table 185. Bit Descriptions for REG00A8

Bits	Bit Name	Description	Reset	Access
[7:0]	ACCUM_DEL_7[7:0]	This is a 10-bit field representing BSYNC7 accumulated alignment delay since BSYNC alignment monitor interrupt has been activated (RST_ALIGN_IRQ bit cleared to 0).	0x0	R

Address: 0xA9, Reset: 0x00, Name: REG00A9

Table 186. Bit Descriptions for REG00A9

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	ACCUM_DEL_7[9:8]	This is a 10-bit field representing BSYNC7 accumulated alignment delay since BSYNC alignment monitor interrupt has been activated (RST_ALIGN_IRQ bit cleared to 0).	0x0	R

Address: 0xAA, Reset: 0x00, Name: REG00AA

Table 187. Bit Descriptions for REG00AA

Bits	Bit Name	Description	Reset	Access
[7:0]	ACCUM_DEL_8[7:0]	This is a 10-bit field representing BSYNC8 accumulated alignment delay since BSYNC alignment monitor interrupt has been activated (RST_ALIGN_IRQ bit cleared to 0).	0x0	R

Address: 0xAB, Reset: 0x00, Name: REG00AB

Table 188. Bit Descriptions for REG00AB

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	ACCUM_DEL_8[9:8]	This is a 10-bit field representing BSYNC8 accumulated alignment delay since BSYNC alignment monitor interrupt has been activated (RST_ALIGN_IRQ bit cleared to 0).	0x0	R

Address: 0xAC, Reset: 0x00, Name: REG00AC

Table 189. Bit Descriptions for REG00AC

Bits	Bit Name	Description	Reset	Access
[7:0]	ACCUM_DEL_9[7:0]	This is a 10-bit field representing BSYNC9 accumulated alignment delay since BSYNC alignment monitor interrupt has been activated (RST_ALIGN_IRQ bit cleared to 0).	0x0	R

Address: 0xAD, Reset: 0x00, Name: REG00AD

Table 190. Bit Descriptions for REG00AD

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	ACCUM_DEL_9[9:8]	This is a 10-bit field representing BSYNC9 accumulated alignment delay since BSYNC alignment monitor interrupt has been activated (RST_ALIGN_IRQ bit cleared to 0).	0x0	R

Address: 0xAE, Reset: 0x00, Name: REG00AE

Table 191. Bit Descriptions for REG00AE

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R

Address: 0xAF, Reset: 0x00, Name: REG00AF

REGISTER DETAILS

Table 192. Bit Descriptions for REG00AF

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R

Address: 0xB0, Reset: 0x00, Name: REG00B0

Table 193. Bit Descriptions for REG00B0

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R

Address: 0xB1, Reset: 0x00, Name: REG00B1

Table 194. Bit Descriptions for REG00B1

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R

Address: 0xB2, Reset: 0x00, Name: REG00B2

Table 195. Bit Descriptions for REG00B2

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED[7:0]	Reserved.	0x0	R

Address: 0xB3, Reset: 0x00, Name: REG00B3

Table 196. Bit Descriptions for REG00B3

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED[15:8]	Reserved.	0x0	R

Address: 0xB4, Reset: 0x00, Name: REG00B4

Table 197. Bit Descriptions for REG00B4

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED[7:0]	Reserved.	0x0	R

Address: 0xB5, Reset: 0x00, Name: REG00B5

Table 198. Bit Descriptions for REG00B5

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED[15:8]	Reserved.	0x0	R

Address: 0xB6, Reset: 0x00, Name: REG00B6

Table 199. Bit Descriptions for REG00B6

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED[7:0]	Reserved.	0x0	R

Address: 0xB7, Reset: 0x00, Name: REG00B7

Table 200. Bit Descriptions for REG00B7

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R

Address: 0xB8, Reset: 0x00, Name: REG00B8

Table 201. Bit Descriptions for REG00B8

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED[7:0]	Reserved.	0x0	R

Address: 0xB9, Reset: 0x00, Name: REG00B9

REGISTER DETAILS

Table 202. Bit Descriptions for REG00B9

Bits	Bit Name	Description	Reset	Access
[7:0]	RESERVED	Reserved.	0x0	R

Address: 0xBA, Reset: 0x00, Name: REG00BA

Table 203. Bit Descriptions for REG00BA

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:2]	BAND_OUT	Band Output of Calibration Circuitry to VCO. If CAL_EN = 0, BAND_OUT = BAND_SEL.	0x0	R
1	CAL_COMP	Output the Tune Line Comparator for Test or Manual Calibration.	0x0	R
0	CAL_BUSY	PLL Calibration Busy Signal.	0x0	R

Address: 0xBB, Reset: 0x00, Name: REG00BB

Table 204. Bit Descriptions for REG00BB

Bits	Bit Name	Description	Reset	Access
[7:0]	VERSION	Chip_id. Identifies the silicon revision. Version = 0 means rev0, version = 1 = rev1, and so forth.	0x0	R

Address: 0xCA, Reset: 0x00, Name: REG00CA

Table 205. Bit Descriptions for REG00CA

Bits	Bit Name	Description	Reset	Access
[7:0]	TMP_ALIGN_ERR_CH[7:0]	Temporary Alignment Status Error Monitor. Status of the temporary alignment error monitor during a serial alignment process. This is a 10-bit field, each bit referring to one BSYNC channel. TMP_ALIGN_ERR_CH[0] corresponds to BSYNC0, TMP_ALIGN_ERR_CH[1] corresponds to BSYNC1, and so forth. Bits[7:0] of Register 0xCA represent TMP_ALIGN_ERR_CH[7:0] and Bits[1:0] of Register 0xCB represent TMP_ALIGN_ERR_CH[9:8]. See the Temporary Alignment Error IRQ IRQ section for details. 0: No temporary alignment error has occurred. 1: Temporary alignment error has occurred.	0x0	R

Address: 0xCB, Reset: 0x00, Name: REG00CB

Table 206. Bit Descriptions for REG00CB

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	TMP_ALIGN_ERR_CH[9:8]	Temporary Alignment Status Error Monitor. Status of the temporary alignment error monitor during a serial alignment process. This is a 10-bit field, each bit referring to one BSYNC channel. TMP_ALIGN_ERR_CH[0] corresponds to BSYNC0, TMP_ALIGN_ERR_CH[1] corresponds to BSYNC1, and so forth. Bits[7:0] of Register 0xCA represent TMP_ALIGN_ERR_CH[7:0] and Bits[1:0] of Register 0xCB represent TMP_ALIGN_ERR_CH[9:8]. See the Temporary Alignment Error IRQ section for details. 0: No temporary alignment error has occurred. 1: Temporary alignment error has occurred.	0x0	R

Address: 0xFF, Reset: 0x00, Name: REG00FF

Table 207. Bit Descriptions for REG00FF

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
1	EN_BRDCST	Enable SPI Broadcast Mode. 0: SPI broadcast mode is disabled. 1: SPI broadcast mode is enabled.	0x0	R/W
0	SOFTRESET_CHIP	Soft Reset of the Entire Chip. This bit resets all registers to their default values (equivalent to power cycling the device in terms of the register map). This bit clears automatically. 0: Normal operation.	0x0	R/W

REGISTER DETAILS

Table 207. Bit Descriptions for REG00FF (Continued)

Bits	Bit Name	Description	Reset	Access
		1: Triggers a soft reset of the entire chip. All ADF4030 registers return to the default values		

OUTLINE DIMENSIONS

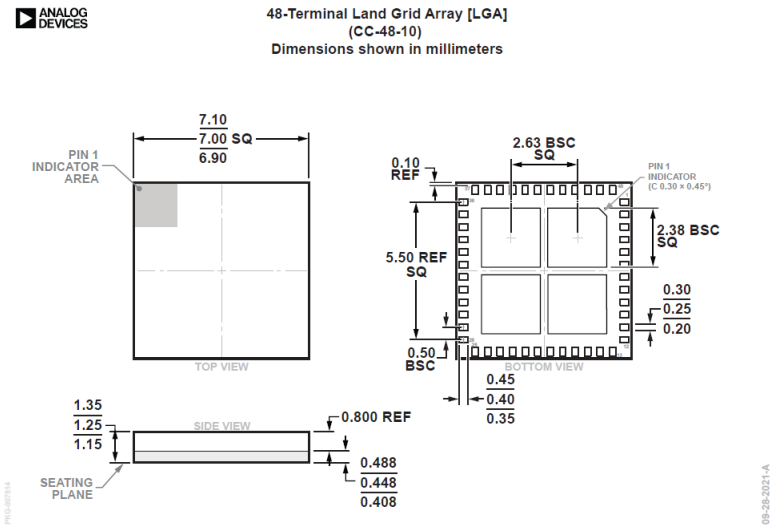

Figure 54. 48-Terminal Land Grid Array [LGA]
(CC-48-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADF4030BCCZ	−40 °C to +105 °C	48-Terminal, Land Grid Array (LGA)	Tray, 260	CC-48-10
ADF4030BCCZ-RL7	−40 °C to +105 °C	48-Terminal, Land Grid Array (LGA)	Reel, 500	CC-48-10

[1] Z=RoHS Compliant Part

EVALUATION BOARDS

Model[1]	Package Description
EV-ADF4030SD1Z	Evaluation Board
EV-ADF4030SD1Z-DUAL	Two ADF4030 Synchronization Demo
EV-ADF4030SD1Z-TRIPLE	Three ADF4030 Synchronization Demo

[1] Z=RoHS Compliant Part

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