REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outline Y. Inactivate device type -01XE. Update document paragraphs to current requirements. - ro	18-02-08	C. SAFFLE
B	Add Vendor part number AD7949SCPZ-EP-R2. Add Transportation mode and quantity column under paragraph 6.3. - ro	18-05-22	C. SAFFLE
C	Add typical limits to tested parameters in Table I. Add timing parameters with conditions of V_{DD} = 2.3 V to 4.5 V and V_{IO} = 1.8 V to V_{DD} to Table I. Update document to current requirements. - ro	24-10-13	J. ESCHMEYER

Prepared in accordance with ASME Y14.24

Vendor Item Drawing

Revision Status of Sheets

REV																						
SHEET																						
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C			
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19			

PMIC N/A

Original date of drawing
YY-MM-DD
12-11-15

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TITLE
MICROCIRCUIT, DIGITAL-LINEAR, 14 BIT, 8 CHANNEL, 250 kSPS SAR ANALOG TO DIGITAL, MONOLITHIC SILICON

SIZE	CAGE CODE
A	16236

DWG NO.
V62/12645

REV C

PAGE 1 OF 19

AMSC N/A

5962-V110-24

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 14 bit, 8 channel 250 kilo samples per second (kSPS) successive approximation register (SAR) analog to digital converter (ADC) microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12645	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type.

Device type	Generic	Circuit function
01	AD7949	14 bit, 8 channel 250 kSPS successive approximation register (SAR) analog to digital converter

1.2.2 Case outlines. The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	20	MO-220-VGGD-1	Lead frame chip scale quad package
Y	20	MO-220-WGGD-11	Lead frame chip scale quad package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Analog inputs (IN_X) and common channel inputs (COM_X)	GND – 0.3 V to V_{DD} + 0.3 V or V_{DD} ± 130 mA
Reference input/output (REF)	GND – 0.3 V to V_{DD} + 0.3 V
Internal reference output / reference buffer input (REFIN)	GND – 0.3 V to V_{DD} + 0.3 V
Supply voltages:	
Power supply (V_{DD}) and input/output interface digital power (V_{IO}) to GND	-0.3 V to +7 V
V_{IO} to V_{DD}	-0.3 V to V_{DD} + 0.3 V
Data input (DIN), convert input (CNV), serial data clock input (SCK) to GND	-0.3 V to V_{IO} + 0.3 V
Serial data output (SDO) to GND	-0.3 V to V_{IO} + 0.3 V
Junction temperature range (T_J)	150°C
Storage temperature range (T_{STG})	-65°C to +150°C
Thermal impedance, junction to case (θ_{JC})	4.4°C/W
Thermal impedance, junction to ambient (θ_{JA})	47.6°C/W

1.4 Recommended operating conditions. 2/

Operating free-air temperature range (T_A)	-55°C to +125°C

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at https://www.jedec.org.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outlines. The case outlines shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions V_{DD} = 2.3 V to 5.5 V, V_{IO} = 1.8 V to V_{DD}, V_{REF} = V_{DD}, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Resolution			-55°C to +125°C	01	14		Bits
Analog input.							
Voltage range		Unipolar mode	-55°C to +125°C	01	0	+V_{REF}	V
		Bipolar mode			-V_{REF} / 2	+V_{REF} / 2	
Absolute input voltage		Positive input, unipolar and bipolar modes	-55°C to +125°C	01	-0.1	V_{REF} + 0.1	V
		Negative or COM input, unipolar mode			-0.1	+0.1	
		Negative or COM input, bipolar mode			V_{REF} / 2 – 0.1	V_{REF} / 2 + 0.1	
					V_{REF} / 2 typical		
Analog input CMRR		f_{IN} = 250 kHz	-55°C to +125°C	01	68 typical		dB
Leakage current	I_{LK}	Acquisition phase	+25°C	01	1 typical		nA
Throughput							
Conversion rate							
Full bandwidth 2/	FBW	V_{DD} = 4.5 V to 5.5 V	-55°C to +125°C	01	0	250	kSPS
		V_{DD} = 2.3 V to 4.5 V			0	200	
1/4 bandwidth 2/		V_{DD} = 4.5 V to 5.5 V	-55°C to +125°C	01	0	62.5	kSPS
		V_{DD} = 2.3 V to 4.5 V			0	50	
Transient response		Full scale step, full bandwidth	-55°C to +125°C	01		1.8	µs
		Full scale step, 1/4 bandwidth				14.5	
Accuracy							
No missing codes	NMC		-55°C to +125°C	01	14		Bits
Integral linearity error	ILE		-55°C to +125°C	01	-1	+1	LSB 3/
					±0.5 typical		
Differential linearity error	DLE		-55°C to +125°C	01	-1	+1	LSB
					±0.25 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = 2.3 V to 5.5 V, V_{IO} = 1.8 V to V_{DD}, V_{REF} = V_{DD}, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Accuracy – continued.							
Transition noise	NT	REF = V_{DD} = 5 V	+25°C	01	0.1 typical		LSB
Gain error 4/	AE		-55°C to +125°C	01	-5	+5	LSB
					±0.5 typical		
Gain error match	AEM		-55°C to +125°C	01	-1	+1	LSB
					±0.2 typical		
Gain error temperature drift	ΔAE/ΔT		-55°C to +125°C	01	±1 typical		ppm/°C
Offset error 4/	OE		-55°C to +125°C	01	±0.5 typical		LSB
Offset error match	OEM		-55°C to +125°C	01	-1	+1	LSB
					±0.2 typical		
Offset error temperature drift	ΔOE/ΔT		-55°C to +125°C	01	±1 typical		ppm/°C
Power supply sensitivity	PSS	V_{DD} = 5 V ± 5%	-55°C to +125°C	01	±0.2 typical		LSB
AC Accuracy 5/							
Dynamic range	DR		-55°C to +125°C	01	85.6 typical		dB 6/
Signal to noise	SN	f_{IN} = 20 kHz, V_{REF} = 5 V	-55°C to +125°C	01	84.5		dB
					85.5 typical		
		f_{IN} = 20 kHz, V_{REF} = 4.096 V internal REF			85 typical		
		f_{IN} = 20 kHz, V_{REF} = 2.5 V internal REF			84 typical		
Signal to noise and distortion	SINAD	f_{IN} = 20 kHz, V_{REF} = 5 V	-55°C to +125°C	01	84		dB
					85 typical		
		f_{IN} = 20 kHz, V_{REF} = 5 V, -60 dB input			33.5 typical		
		f_{IN} = 20 kHz, V_{REF} = 4.096 V internal REF			85 typical		
		f_{IN} = 20 kHz, V_{REF} = 2.5 V internal REF			84 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = 2.3 V to 5.5 V, V_{IO} = 1.8 V to V_{DD}, V_{REF} = V_{DD}, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC Accuracy – continued. 5/							
Total harmonic distortion	THD	f_{IN} = 20 kHz	-55°C to +125°C	01	-100 typical		dB
Spurious free dynamic range	SFDR	f_{IN} = 20 kHz	-55°C to +125°C	01	108 typical		dB
Channel to channel crosstalk	CCCT	f_{IN} = 100 kHz on adjacent channel(s)	-55°C to +125°C	01	-125 typical		dB
Sampling dynamics							
-3 dB input bandwidth		Full bandwidth	-55°C to +125°C	01	1.7 typical		MHz
		1/4 bandwidth			0.425 typical		
Aperature delay		V_{DD} = 5 V	-55°C to +125°C	01	2.5 typical		ns
Internal reference							
REF output voltage		2.5 V	+25°C	01	2.490	2.510	V
					2.500 typical		
		4.096 V			4.086	4.106	
					4.096 typical		
REFIN output voltage 7/		2.5 V	+25°C	01	1.2 typical		V
		4.096 V			2.3 typical		
REF output current			-55°C to +125°C	01	±300 typical		µA
Temperature drift			-55°C to +125°C	01	±10 typical		ppm/°C
Line regulation	V_{RLINE}	V_{DD} = 5 V ± 5%	-55°C to +125°C	01	±15 typical		ppm/V
Long term drift		1000 hours	-55°C to +125°C	01	50 typical		ppm
Turn on settling time	t_{ON}	CREF = 10 µF	-55°C to +125°C	01	5 typical		ms
External reference							
Voltage reference		REF input	-55°C to +125°C	01	0.5	V_{DD} + 0.3	V
		REFIN input (buffered)			0.5	V_{DD} - 0.5	
Current drain		250 kSPS, REF = 5 V	-55°C to +125°C	01	50 typical		µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = 2.3 V to 5.5 V, V_{IO} = 1.8 V to V_{DD}, V_{REF} = V_{DD}, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Temperature sensor							
Output voltage 8/	V_{OUT}		+25°C	01	283 typical		mV
Temperature sensitivity			-55°C to +125°C	01	1 typical		mV/°C
Digital inputs							
Input low voltage	V_{IL}		-55°C to +125°C	01	-0.3	+0.3 x V_{IO}	V
Input high voltage	V_{IH}		-55°C to +125°C	01	0.7 x V_{IO}	V_{IO} + 0.3	V
Input low current	I_{IL}		-55°C to +125°C	01	-1	+1	µA
Input high current	I_{IH}		-55°C to +125°C	01	-1	+1	µA
Digital outputs							
Data format 9/							
Pipeline delay 10/							
Output low voltage	V_{OL}	I_{SINK} = +500 µA	-55°C to +125°C	01		0.4	V
Output high voltage	V_{OH}	I_{SOURCE} = -500 µA	-55°C to +125°C	01	V_{IO} - 3		V
Power supplies							
Power supply voltage	V_{DD}	Specified performance	-55°C to +125°C	01	2.3	5.5	V
Input/output interface digital power	V_{IO}	Specified performance	-55°C to +125°C	01	2.3	V_{DD} + 0.3	V
		Operating range			1.8	V_{DD} + 0.3	
Standby current 11/ 12/	I_{SB}	V_{DD} and V_{IO} = 5 V	+25°C	01	50 typical		nA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = 2.3 V to 5.5 V, V_{IO} = 1.8 V to V_{DD}, V_{REF} = V_{DD}, unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Power supplies – continued.							
Power dissipation	PD	V_{DD} = 2.5 V, 100 SPS throughput	-55°C to +125°C	01	1.5 typical		µW
		V_{DD} = 2.5 V, 100 kSPS throughput				2.0	mW
					1.45 typical		
		V_{DD} = 2.5 V, 200 kSPS throughput				4.0	
					2.9 typical		
		V_{DD} = 5 V, 250 kSPS throughput				12.5	
					10.8 typical		
		V_{DD} = 5 V, 250 kSPS throughput with internal reference				15.5	
					13.5 typical		
Energy conversion			-55°C to +125°C	01	50 typical		nJ
Temperature range specified performance				01	-55	+125	°C

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = 4.5 V to 5.5 V, V_{IO} = 1.8 V to V_{DD}, see figures 3 and 4 unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Conversion time: CNV rising edge to data available	tCONV		-55°C to +125°C	01		2.2	µs
Acquisition time	tACQ		-55°C to +125°C	01	1.8		µs
Time between conversion	tCYC		-55°C to +125°C	01	4.0		µs
Data write/read during conversion	tDATA		-55°C to +125°C	01		1.0	µs
CNV pulse width	tCNVH		-55°C to +125°C	01	10		ns
SCK period	tSCK		-55°C to +125°C	01	tDSDO + 2		ns
SCK low time	tSCKL		-55°C to +125°C	01	11		ns
SCK high time	tSCKH		-55°C to +125°C	01	11		ns
SCK falling edge to data remains valid	tHSDO		-55°C to +125°C	01	4		ns
SCK falling edge to data valid delay	tDSDO	V_{IO} above 2.7 V	-55°C to +125°C	01		18	ns
		V_{IO} above 2.3 V				23	
		V_{IO} above 1.8 V				28	
CNV low to SDO D15 MSB valid	tEN	V_{IO} above 2.7 V	-55°C to +125°C	01		18	ns
		V_{IO} above 2.3 V				22	
		V_{IO} above 1.8 V				25	
CNV high or last SCK falling edge to SDO high impedance	tDIS		-55°C to +125°C	01		32	ns
CNV low to SCK rising edge	tCLSCK		-55°C to +125°C	01	10		ns
DIN valid setup time from SCK rising edge	tSDIN		-55°C to +125°C	01	5		ns
DIN valid hold time from SCK rising edge	tHDIN		-55°C to +125°C	01	5		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions V_{DD} = 2.3 V to 4.5 V, V_{IO} = 1.8 V to V_{DD}, see figures 3 and 4 unless otherwise specified	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Conversion time: CNV rising edge to data available	tCONV		-55°C to +125°C	01		3.2	µs
Acquisition time	tACQ		-55°C to +125°C	01	1.8		µs
Time between conversion	tCYC		-55°C to +125°C	01	5.0		µs
Data write/read during conversion	tDATA		-55°C to +125°C	01		1.2	µs
CNV pulse width	tCNVH		-55°C to +125°C	01	10		ns
SCK period	tSCK		-55°C to +125°C	01	tDSDO + 2		ns
SCK low time	tSCKL		-55°C to +125°C	01	12		ns
SCK high time	tSCKH		-55°C to +125°C	01	12		ns
SCK falling edge to data remains valid	tHSDO		-55°C to +125°C	01	5		ns
SCK falling edge to data valid delay	tDSDO	V_{IO} above 3 V	-55°C to +125°C	01		24	ns
		V_{IO} above 2.7 V				30	
		V_{IO} above 2.3 V				38	
		V_{IO} above 1.8 V				48	
CNV low to SDO D15 MSB valid	tEN	V_{IO} above 3 V	-55°C to +125°C	01		21	ns
		V_{IO} above 2.7 V				27	
		V_{IO} above 2.3 V				35	
		V_{IO} above 1.8 V				45	
CNV high or last SCK falling edge to SDO high impedance	tDIS		-55°C to +125°C	01		50	ns
CNV low to SCK rising edge	tCLSCK		-55°C to +125°C	01	10		ns
DIN valid setup time from SCK rising edge	tSDIN		-55°C to +125°C	01	5		ns
DIN valid hold time from SCK rising edge	tHDIN		-55°C to +125°C	01	5		ns

See footnotes at end of table.

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ The bandwidth is set in the configuration register.

3/ LSB means least significant bit. With the 5 V input range, one LSB = 305 μV.

4/ These specifications include full temperature range variation but, not the error contribution from the external reference.

5/ Unless otherwise specified, V_{DD} = 5 V.

6/ Unless otherwise specified, all specifications expressed in decibels are referred to a full scale input FSR and tested with an input signal at 0.5 dB below full scale.

7/ This is the output from the internal band gap.

8/ The output voltage is internal and present on a dedicated multiplexer input.

9/ Unipolar mode: serial 14 bit straight binary.
Bipolar mode: serial 14 bit two's complement.

10/ Conversion results available immediately after completed conversion.

11/ With digital inputs forced to V_{IO} or GND as required.

12/ During acquisition phase.

Case X

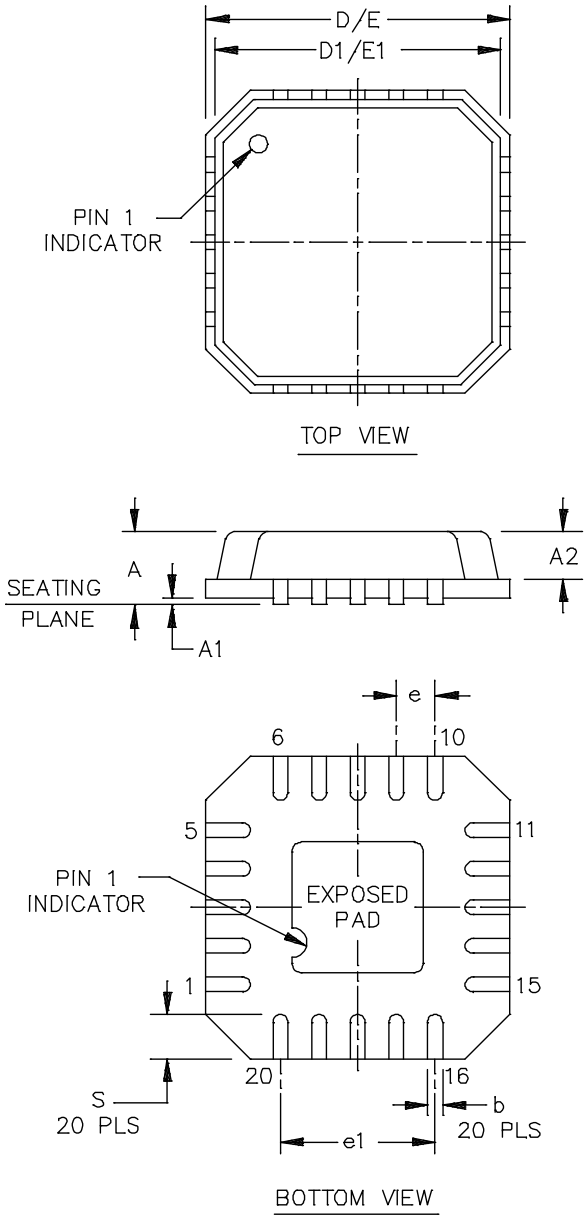


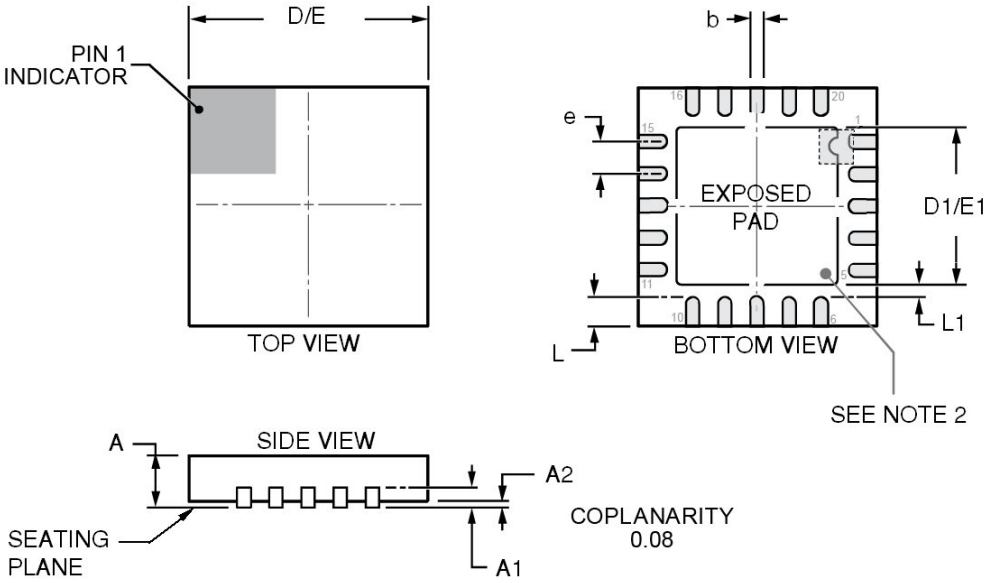
FIGURE 1. Case outlines.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.031	.039	0.80	1.00
A1	.0007	.001	0.02	0.05
A2	.025	.031	0.65	0.80
b	.007	.011	0.18	0.30
D/E	.157 BSC		4.00 BSC	
D1/E1	.147 BSC		3.75 BSC	
e	.019 BSC		0.50 BSC	
e1	.092	.104	2.35	2.65
s	.011	.019	0.30	0.50

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MO-220-VGGD-1.

FIGURE 1. Case outlines - Continued.

Case Y



Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	.0275	.0295	.0314	0.70	0.75	0.80
A1	.0078 REF			0.20 REF		
A2	---	.0007 NOM	.0019	---	0.02 NOM	0.05
b	.0078	.0098	.0118	0.20	0.25	0.30
D/E	.1535	.1574	.1614	3.90	4.00	4.10
D1/E1	.0925	.0984	.1043	2.35	2.50	2.65
e	.0196 BSC			0.50 BSC		
L	.0118	.0157	.0196	0.30	0.40	0.50
L1	.0098	---	---	0.25	---	---

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. For proper connection of the exposed pad. Refer to the pin configuration and function descriptions section of the manufacturer's datasheet.
3. Falls within reference to JEDEC MO-220-WGGD-11.

FIGURE 1. Case outlines - Continued.

Device type	01
Case outlines	X and Y
Terminal number	Terminal symbol
1	V_{DD}
2	REF
3	REFIN
4	GND
5	GND
6	IN 4
7	IN 5
8	IN 6
9	IN 7
10	COMM
11	CNV
12	DIN
13	SCK
14	SD0
15	V_{IO}
16	IN 0
17	IN 1
18	IN 2
19	IN 3
20	V_{DD}

NOTE: The exposed pad is not connected internally. For increased reliability of the solder joints, it is recommended that the pad be soldered to the system ground plane.

FIGURE 2. Terminal connections.

Terminal symbol	Type	Description
V_{DD}	Power	Power supply. Nominally 2.5 V to 5.5 V when using an external reference and decoupled with 10 μF and 100 nF capacitors. When using the internal reference for 2.5 V output, the minimum should be 3.0 V. When using the internal reference for 4.096 V output, the minimum should be 4.5 V.
REF	Analog input/ output	Reference input/output. When the internal reference is enabled, this pin produces a selectable system reference = 2.5 V or 4.096 V. When the internal reference is disabled and the buffer is enabled, REF produces a buffered version of the voltage present on the REFIN pin (4.096 V maximum), useful when using low cost, low power references. For improved drift performance, connect a precision reference to REF (0.5 V to V_{DD}). For any reference method, this pin needs decoupling with an external 10 μF capacitor connected as close to REF as possible.
REFIN	Analog input/ output	Internal reference output/ reference buffer input. When using the internal reference, the internal unbuffered reference voltage is present and needs decoupling with a 0.1 μF capacitor. When using the internal reference buffer, apply a source between 0.5 V and 4.096 V that is buffered to the REF pin as described above.
GND	Power	Power supply ground.
IN4 to IN7	Analog input	Channel 4 through channel 7 analog inputs.
COM	Analog input	Common channel input. All input channels; IN[7:0], can be referenced to a common mode point of 0 V or V_{REF} / 2 V.
CNV	Digital input	Convert input. On the rising edge, CNV initiates the conversion. During conversion, if CNV is held high, the busy indicator is enabled.
DIN	Digital input	Data input. This pin is used for writing to the 14 bits configuration register. The configuration register can be written to during and after conversion.
SCK	Digital input	Serial data clock input. This input is used to clock out the data on SDO and clock in data on DIN in an MSB first fashion.
SDO	Digital output	Serial data output. The conversion result is output on this pin, synchronized to SCK. In unipolar modes, conversion results are straight binary; in bipolar modes, conversion results are twos complement.
V_{IO}	Power	Input/output interface digital power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).
IN0 to IN3	Analog input	Channel 0 through channel 3 analog inputs.
Exposed pad	No connection	The exposed pad is not connected internally. For increased reliability of the solder joints, it is recommended that the pad be soldered to the system ground plane.

FIGURE 2. Terminal connections - continued.

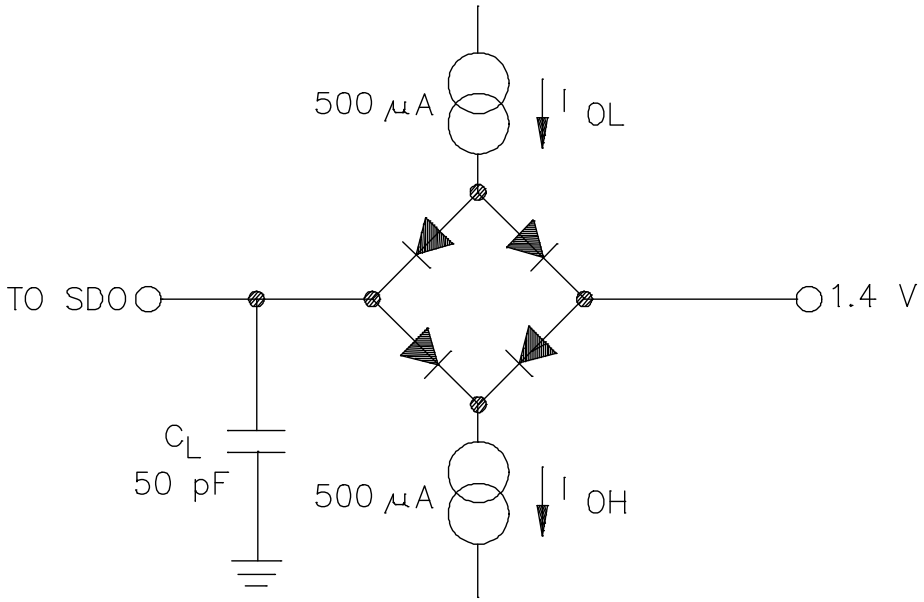
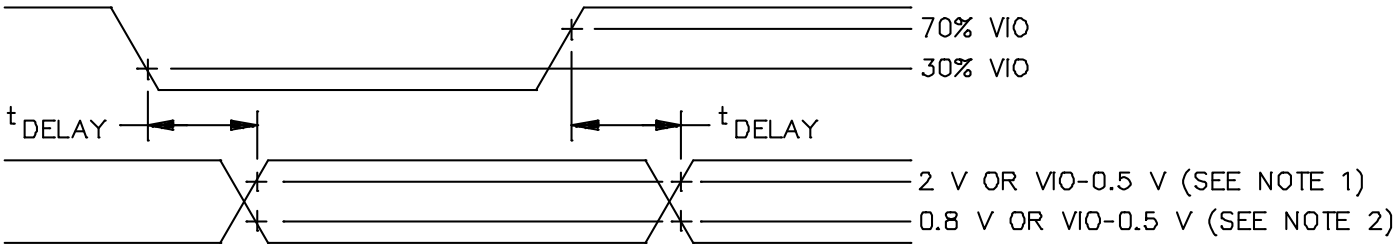


FIGURE 3. Load circuit for digital interface timing.



NOTES:

1. 2 V if V_{IO} above 2.5 V, V_{IO} – 0.5 V if V_{IO} below 2.5 V.
2. 0.8 V if V_{IO} above 2.5 V, 0.5 V if V_{IO} below 2.5 V.

FIGURE 4. Voltage levels for timing.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Transportation mode and quantity	Vendor part number
V62/12645-01XE	2/	---	AD7949SCPZ-EP-RL7
V62/12645-01YE	24355	Reel, 1500 units	AD7949SCPZ-EP-RL7
V62/12645-01YE	24355	Reel, 250 units	AD7949SCPZ-EP-R2

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ Not available from an approved source of supply.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 20 Alpha Road Chelmsford, MA 01824-4123

Mouser Electronics

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Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

AD7949SCPZ-EP-RL7 AD7949SCPZ-EP-R2