

1MHz I2C-Interfaced 8 x 7 Key-Switch Controller with GPIO Ports

General Description

The MAX7365 is an I²C-interfaced peripheral that provides microprocessors with management of up to 56 key switches.

Key codes generated for each keypress and release enable easier implementation of multiple key entries. Key inputs monitored statically, not dynamically, ensure low-EMI operation. The switches can be metallic or resistive (carbon) with up to $5k\Omega$ of resistance.

The device features autosleep and autowake to further minimize the power consumption of the device. The autosleep feature puts the device in a low-power state (1 μ A typ) after a programmable sleep timeout period. The autowake feature configures the device to return to normal operating mode from sleep upon a keypress.

The key controller debounces and maintains a FIFO of keypress and release events (including autorepeat, if enabled). An interrupt (INT) output can be configured to alert keypresses either as they occur or at the maximum rate.

Unused key switches can be used as GPI. In addition, there are five additional general-purpose input/output (GPIO) ports. GPOs can be programmed as push-pull or open-drain to high- or low-side output drivers. When programmed as open drain, an optional on-chip $100k\Omega$ pullup/pulldown resister can be enabled.

The device is available in a small (2mm x 2mm) 25-bump wafer-level package (WLP) for cell phones, pocket PCs, and other portable consumer electronic applications. The device operates over the -40° C to $+85^{\circ}$ C extended temperature range.

Applications

Netbooks Cell Phones PDAs Handheld Games Portable Consumer Electronics

Ordering Information appears at end of data sheet.

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX7365.related.

Benefits and Features

- - ♦ FIFO Queues Up to 16 Debounced Key Events
 - \diamond Hardware Interrupt at the FIFO Level or at the
 - End-of-Definable Time Period
- Increased Battery Life
 - ♦ Autosleep and Autowake Minimize Current Consumption
 - Less Than 1µA Sleep Current
- ♦ Save Board Space
 - ♦ Small (2mm x 2mm) and Low-Profile 25-Bump WLP
- Flexible Design Requirements
 - \diamond 1.62V to 3.6V Operation
 - ♦ Proprietary Ghost-Key Detection and Removal
 - Key Debounce Time User Configurable from 1ms to 31ms
 - ♦ Low-EMI Design Uses Static Matrix Monitoring
 - ♦ Five Additional GPIO Ports
 - ♦ All Key Switches Can Be Used as GPIs
 - ♦ 1Mbps, 5.5V Tolerant, Two-Wire Serial Interface
 - ♦ Selectable Two-Wire, Serial-Bus Timeout

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

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ABSOLUTE MAXIMUM RATINGS

V _{DD} to GND	0.3V to 4.0V
ROW7–ROW0, COL6–COL0,	
GPIO4–GPIO0 to GND	0.3V to (V _{DD} + 0.3V)
SDA, SCL, INT to GND	0.3V to 6V
DC Current on ROW7-ROW0, COL6-CO	OL0 to GND1mA
DC Current on GPIO4-GPIO0 to GND	12mA
GND Current	12mA

Continuous Power Dissipation ($T_A = +70^{\circ}C$) WLP (derate 19.2mW/°C above +70°C)......1536mW

Operating Temperature Range	40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	65°C to +150°C
Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

Junction-to-Ambient Thermal Resistance (θ_{JA})52°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to <u>www.maximintegrated.com/thermal-tutorial</u>.

ELECTRICAL CHARACTERISTICS

 $(V_{DD} = 1.62V \text{ to } 3.6V, T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, \text{ unless otherwise noted. Typical values are at } V_{DD} = 3.3V, T_A = +25^{\circ}\text{C.})$ (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	МАХ	UNITS	
Operating Supply Voltage	V _{DD}		1.62	3.3	3.6	V	
Operating Supply Current	1	N keys pressed; GPI static	34	+ (25 x	N)	μA	
Operating Supply Current	DD	All 56 key switches open		60	85	μA	
Sleep-Mode Supply Current	I _{SL}			0.8	5	μA	
Key-Switch Source Current	IKEY			20	36	μA	
Key-Switch Source Voltage	V _{KEY}			0.42	0.55	V	
Key-Switch Resistance	R _{KEY}	(Note 4)			5	kΩ	
Startup Time from Shutdown	^t START			2	2.4	ms	
Keyscan Frequency	fkey		51	64	82	kHz	
Maximum Allowable Load Capacitance for Keyscan Function		N keys pressed simultaneously (Note 4)			500	рF	
GPIO SPECIFICATIONS							
Input High Voltage GPIO_, ROW_, COL_, SDA, SCL	VIH		0.7 x V _{DD}			V	
Input Low Voltage GPIO_, ROW_, COL_, SDA, SCL	V _{IL}				0.3 x V _{DD}	V	
Input Leakage Current GPIO_, ROW_, COL_, SDA, SCL	I _{IN}	Input voltage = V_{DD} or V_{GND}	-2		-2	μA	
Output Logic Low Voltage INT, SDA		I _{SINK} = 6mA			0.5	V	
Output Low Voltage	M	$V_{DD} = 1.8V$ and $I_{SINK} = 5mA$		40	100		
GPIO_	VOL	V_{DD} = 1.8V and I_{SINK} = 10mA		80	200	- V	

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ELECTRICAL CHARACTERISTICS (continued)

 $(V_{DD} = 1.62V \text{ to } 3.6V, T_A = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}, \text{ unless otherwise noted. Typical values are at } V_{DD} = 3.3V, T_A = +25^{\circ}\text{C}.)$ (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	MAX	UNITS
Output High Voltage	Maria	V _{DD} = 1.8V and I _{SOURCE} = 5mA	V _{DD} - 0.1	V _{DD} - 0.05		N
GPIO_	∨ОН	$V_{DD} = 1.8V$ and $I_{SOURCE} = 10mA$	V _{DD} - 0.2	V _{DD} - 0.1		V
I ² C TIMING SPECIFICATIONS						
Input Capacitance SCL, SDA	C _{IN}	(Notes 3, 4)			10	pF
SCI Sorial Clock Fraguency	facu	Bus timeout enabled	0.05		1000	<u>к</u> Ц-7
SOE Senai-Clock Frequency	ISCL	Bus timeout disabled	0		1000	KI IZ
Bus Free Time Between a STOP and START Condition	^t BUF		0.5			μs
Hold Time (Repeated) START Condition	^t hd, sta		0.26			μs
Repeated START Condition Setup Time	^t SU, STA		0.26			μs
STOP Condition Setup Time	^t SU, STO		0.26			μs
Data Hold Time	t _{HD, DAT}	(Note 5)			0.9	μs
Data Setup Time	^t SU, DAT		50			ns
SCL Clock Low Period	tLOW		0.5			μs
SCL Clock High Period	thigh		0.26			μs
Rise Time of Both SDA and SCL Signals, Receiving	t _R	(Notes 4, 6)			120	ns
Fall Time of Both SDA and SCL Signals, Receiving	t _F	(Notes 4, 6)			120	ns
Fall Time of SDA Signal, Transmitting	^t F, TX	(Notes 4, 7)	20 + 0.1C _B		120	ns
Pulse Width of Spike Suppressed	t _{SP}	(Notes 4, 8)			50	ns
Capacitive Load for Each Bus Line	CB	(Notes 3, 4)			550	pF
Bus Timeout	^t TIMEOUT		20		40	ms

Note 2: All parameters are tested at $T_A = +25^{\circ}$ C. Specifications over temperature are guaranteed by design.

Note 3: All digital inputs at V_{DD} or V_{GND} .

Note 4: Guaranteed by design.

Note 5: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) to bridge the undefined region of SCL's falling edge.

Note 6: C_B = total capacitance of one bus line in pF. t_R and t_F measured between 0.8V and 2.1V.

Note 7: I_{SINK} = 6mA. C_B = total capacitance of one bus line in pF. t_R and t_F measured between 0.8V and 2.1V.

Note 8: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

Typical Operating Characteristics

(V_{DD} = +2.5V, T_A = +25°C, unless otherwise noted.)



SUPPLY VOLTAGE (V)



SUPPLY CURRENT vs. SUPPLY VOLTAGE



SLEEP MODE SUPPLY CURRENT vs. Supply Voltage



Pin Configuration



Pin Description

DUMD		FUNCTION
BOWP	NAME	FUNCTION
A1	ROW6	Row 6 Input from Key Matrix or General-Purpose Input
A2	ROW7	Row 7 Input from Key Matrix or General-Purpose Input
A3	COL2	Column 2 Input from Key Matrix or General-Purpose Input
A4	COL3	Column 3 Input from Key Matrix or General-Purpose Input
A5	COL4	Column 4 Input from Key Matrix or General-Purpose Input
B1	ROW4	Row 4 Input from Key Matrix or General-Purpose Input
B2	ROW5	Row 5 Input from Key Matrix or General-Purpose Input
B3	COL1	Column 1 Input from Key Matrix or General-Purpose Input
B4	COL6	Column 6 Input from Key Matrix or General-Purpose Input
B5	COL5	Column 5 Input from Key Matrix or General-Purpose Input
C1	ROW2	Row 2 Input from Key Matrix or General-Purpose Input
C2	ROW3	Row 3 Input from Key Matrix or General-Purpose Input
C3	COLO	Column 0 Input from Key Matrix or General-Purpose Input
C4	GPIO0	General-Purpose Input/Output Port 0

Pin Description (continued)

BUMP	NAME	FUNCTION
C5	GND	Ground
D1	ROW1	Row 1 Input from Key Matrix or General-Purpose Input
D2	V _{DD}	Positive Supply Voltage. Bypass to GND with a 0.1µF capacitor as close as possible to the device.
D3	SDA	I ² C-Compatible Serial-Data Input/Output
D4	GPIO4	General-Purpose Input/Output Port 4
D5	GPIO1	General-Purpose Input/Output Port 1
E1	ROW0	Row 0 Input from Key Matrix or General-Purpose Input
E2	INT	Active-Low Key-Switch Interrupt Output. INT is open drain and requires a pullup resistor.
E3	SCL	I ² C-Compatible Serial-Clock Input
E4	GPIO3	General-Purpose Input/Output Port 3
E5	GPIO2	General-Purpose Input/Output Port 2

Functional Diagram



1MHz I2C-Interfaced 8 x 7 Key-Switch Controller with GPIO Ports

Detailed Description

The MAX7365 is a microprocessor peripheral low-noise, key-switch controller that monitors up to 56 key switches with optional autorepeat. Key events are presented in a 16-byte FIFO. Key-switch functionality can be traded to provide up to 16 logic inputs. The device features an additional five GPIOs. Outputs configured as open drain feature an optional on-chip 100k Ω pullup/pulldown resistor.

The device features an automatic sleep mode and automatic wakeup that further reduce supply current consumption. The device can be configured to enter sleep mode after a programmable time following a key event. The FIFO content is maintained during sleep mode and can be read in sleep mode. When a key is held down, the device cannot enter autosleep. The autowake feature takes the device out of sleep mode following a keypress event. Autosleep and autowake can be disabled.

Interrupt requests can be configured to be issued on a programmable number of FIFO entries or can be set to a period of time to prevent overloading the microprocessor with too many interrupts. The key-switch status can be checked at any time by reading the key-switch FIFO. A 1-byte read access returns both the next key-event in the FIFO, if there is one, and the FIFO status. Interrupts are configurable per each input port with edge detection.

Register Description

On power-up, all control registers are set to power-up values (Table 1), and the device is in sleep mode.

ADDRESS CODE (hex)	READ/ WRITE	POWER-UP VALUE (hex)	REGISTER FUNCTION	DESCRIPTION
0x00	Read only	0x3F	Keys FIFO	Read FIFO keyscan data out
0x01	R/W	0x0B	Configuration	Power-down, interrupt clearing mode, key-release enable, autowake, and I ² C timeout enable
0x02	R/W	0xFF	Key-Switch Debounce	Key debounce time setting
0x03	R/W	0×00	Key-Switch Interrupt	Key-switch interrupt and INT frequency setting
0x05	R/W	0x00	Key-Switch Autorepeat	Delay and frequency for key repeat
0x06	R/W	0x07	Autosleep	Idle time to autosleep
0x30	R/W	0xF7	Key-Switch Array Size	Keyscan switch array size
0x31	R/W	0x00	GPIO Direction	Select GPIO port as input mode or output mode
0x32	R/W	0x00	GPO Output Mode	GPO open-drain/push-pull output setting for GPIO port
0x33	Read only	0×FF	GPIs LSB Value	GPI[7:0] (ROW0, COL[6:0]) port input values
0x34	Read only	0x7F	GPIs MSB Value	GPI[14:8] (ROW[7:1]) port input values
0x35	R/W	0x1F	GPIO Value	Debounced input or output values for GPIO port
0x36	R/W	0x1F	GPIs Interrupt Mask	GPIO port interrupt mask for inputs
0x37	R/W	0×FF	GPIs LSB Interrupt Mask	GPI[7:0] (ROW0, COL[6:0]) port interrupt mask for inputs
0x38	R/W	0x7F	GPIs MSB Interrupt Mask	GPI[14:8] (ROW[7:1]) port interrupt mask for inputs
0x39	R/W	0x00	GPIs Interrupt Trigger	GPIO edge-triggered interrupt setting
0x3A	R/W	0x00	GPIs LSB Interrupt Trigger Mode	GPI[7:0] (ROW0, COL[6:0]) edge-triggered interrupt setting
0x3B	R/W	0x00	GPIs MSB Interrupt Trigger Mode	GPI[14:8] (ROW[7:1]) edge-triggered interrupt setting
0x3C	R/W	0x00	GPO High-Side Open-Drain Enable	GPIO port output mode high-side open-drain setting

Table 1. Register Address Map and Power-Up Condition

Table 1. Register Address Map and Power-Up Condition (continued)

ADDRESS CODE (hex)	READ/ WRITE	POWER-UP VALUE (hex)	REGISTER FUNCTION	DESCRIPTION
0x3D	R/W	0x00	GPO Pullup/Pulldown Resistor Enable	GPIO port open-drain output mode pullup/pulldown resistor setting
0x40	R/W	0x00	GPIO Global Configuration	GPI autowake enable, I ² C timeout interrupt enable, operating mode
0x42	R/W	0x00	GPI Debounce Setting	GPIO port inputs debounce time setting
0x48	R/W	0x00	I ² C Timeout Flag	I ² C timeout since last POR

Table 2. Key-Switch Mapping

PIN	COL0	COL1	COL2	COL3	COL4	COL5	COL6
ROW0	KEY 0	KEY 8	KEY 16	KEY 24	KEY 32	KEY 40	KEY 48
ROW1	KEY 1	KEY 9	KEY 17	KEY 25	KEY 33	KEY 41	KEY 49
ROW2	KEY 2	KEY 10	KEY 18	KEY 26	KEY 34	KEY 42	KEY 50
ROW3	KEY 3	KEY 11	KEY 19	KEY 27	KEY 35	KEY 43	KEY 51
ROW4	KEY 4	KEY 12	KEY 20	KEY 28	KEY 36	KEY 44	KEY 52
ROW5	KEY 5	KEY 13	KEY 21	KEY 29	KEY 37	KEY 45	KEY 53
ROW6	KEY 6	KEY 14	KEY 22	KEY 30	KEY 38	KEY 46	KEY 54
ROW7	KEY 7	KEY 15	KEY 23	KEY 31	KEY 39	KEY 47	KEY 55

Keyscan Controller

Key inputs are scanned statically, not dynamically, to ensure low-EMI operation. Since inputs only toggle in response to switch changes, the key matrix can be routed closer to sensitive circuit nodes.

The keyscan controller debounces and maintains a FIFO buffer of keypress and release events (including autorepeated keypresses, if autorepeat is enabled). <u>Table 2</u> shows the key-switch order. The user-programmable key-switch debounce time and autosleep timer are derived from the clock, which in turn is derived from the internal oscillator. Time delay for autorepeat and key-switch interrupt is based on the key-switch debounce time. There is no limitation for the number of keys pressed simultaneously as long as no ghost keys are generated. If the application requires fewer keys to be scanned, the unused key-switch ports can be configured as GPIs.

Keys FIFO Register (0x00)

The Keys FIFO register contains the information pertaining to the status of the keys FIFO, as well as the key events that have been debounced (<u>Table 6</u>). Bits D[5:0] denote which of the 56 keys have been debounced, and the keys are numbered as shown in Table 2.

Special codes are key repeat (0x1E/0x3E), FIFO empty (0x3F), and FIFO overflow (0x7F). Bit D7 indicates if there is more data in the FIFO, except when a special key code occurs. D6 indicates if a keypress or release event has occurred.

Reading the keyscan FIFO clears the interrupt ($\overline{\text{INT}}$), depending on the setting of bit D5 in the configuration register (0x01).

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Configuration Register (0x01)

The Configuration register controls the I²C bus timeout feature, enables the key-release indicator, enables autowake, and determines how \overline{INT} is deasserted. Write to bit D7 to put the device into sleep or operating mode. Autosleep and autowake, when enabled, also change the status of D7 (<u>Table 7</u>).

Key-Switch Debounce Register (0x02)

The Key-Switch Debounce register sets the keypress and key-release time for each debounce cycle. Bits D[3:0] set the debounce time for keypresses, while bits D[7:4] set the debounce time for key releases. Both debounce times are configured in increments of 2ms starting at 1ms and ending at 31ms (Table 8).

Key-Switch Interrupt Register (0x03)

The Key-Switch Interrupt register contains information related to the settings of the interrupt request function, as well as the status of the INT output. If bits D[7:0] are set to 0x00, INT is disabled. There are two types of interrupts, the FIFO-based interrupt and the time-based interrupt. Set bits D[4:0] to assert interrupts at the end of the selected number of debounce cycles following a key event (Table 9). This number ranges from 1–31 debounce cycles. Setting bits D[7:5] sets the FIFO-based interrupt when there are 2–14 key events stored in the FIFO. Both interrupts can be configured simultaneously, and INT asserts depending on which condition is met first. INT deasserts depending on the status of bit D5 in the Configuration register.

Key-Switch Autorepeat Register (0x05)

The device's autorepeat feature notifies the host that at least one key has been pressed for a continuous period. The Autorepeat register enables or disables this feature, sets the time delay after the last key event before the key repeat code (0x7E) is entered into the FIFO, and sets the frequency at which the key-repeat code is entered into the FIFO thereafter. The autorepeat code continues to be entered in the FIFO at the frequency set by bits D[3:0] until another key event is recorded. The key being pressed is not entered again into the FIFO. Following the key-release event, if any keys are still pressed, the device restarts the autorepeat sequence. Bit D7 specifies whether the autorepeat function is enabled with 0 denoting autorepeat disabled, and 1 denoting autorepeat enabled. Bits D[3:0] specify the autorepeat delay in

terms of debounce cycles, ranging from 8–128 debounce cycles (Table 10). Bits D[6:4] specify the autorepeat rate or frequency ranging from 4–32 debounce cycles.

Autosleep Register (0x06)

Autosleep puts the device in sleep mode to draw minimal current. When enabled, the device enters sleep mode if no keys are pressed for the autoshutdown time (Table 11).

Key-Switch Array Size Register (0x30)

Bits D[7:4] set the row size of the key-switch array, and bits D[3:0] set the column size of the key-switch array (see <u>Table 12</u>). Set the bits to 0 if no key switches are used. The key-switch array should be connected beginning at ROW0 and COL0. If not used as a key-switch-matrix pin, the pin can function as a GPI port, if enabled.

Key-Switch Autosleep Mode

In sleep mode, the device draws minimal current. Switchmatrix current sources are turned off and become high. When autosleep is enabled, key-switch inactivity for a period longer than the autosleep time puts the part into sleep mode (FIFO data is maintained). Writing a 1 to D7 in the Configuration register (0x01) or a keypress can take the device out of sleep mode. Bit D7 in the Configuration register gives the sleep-mode status and can be read at any time.

To place the device in sleep mode, clear bit D7 in the Configuration register. The device is in sleep mode after power-on reset (POR). In sleep mode, the keyscan controller is disabled and the device draws minimal current. No additional supply current is drawn if no keys are pressed. All switch-matrix current sources are turned off, and the row outputs (ROW7–ROW0) are low and the column outputs (COL6–COL0) become high.

To take the device out of sleep mode and into operating mode, cause a low-to-high transition in bit D7 by setting it to a 1 in the Configuration register. The keyscan controller FIFO buffers are cleared and key monitoring starts. Note that rewriting the Configuration register bit D7 to a 1, when bit D7 is already a 1, does not clear the FIFOs. The FIFOs are only cleared when the device is changing state from shutdown to operating mode.

In sleep mode, the internal oscillator is disabled and the I²C timeout features are disabled.

Key-Switch Autowake

Keypresses initiate autowake and the device goes into operating mode. Keypresses that autowake the device are not lost. When a key is pressed while the device is in sleep mode, all analog circuitry, including switch-matrix current sources, turn on in 2ms. The initial key needs to be pressed for 2ms plus the debounce time to be stored in the FIFO. Write a 0 to bit D1 in the Configuration register (0x01) to disable autowake.

FIFO Overflow

The FIFO overflow status occurs when the FIFO is full (16 bytes) and additional events occur. If key release is disabled, then the FIFO overflow status occurs when the FIFO is full and not upon additional key events. When the FIFO is overflowed, the first byte read from the FIFO buffer is the overflow byte (0x7F). The order of the original 16 bytes of event data is preserved, but further events could be lost. When the FIFO is full, if the 18th key event is a key release, then the FIFO overflow status is removed.

The device has five GPIO ports. The ports can be used as logic inputs or logic outputs. Each GPIO port features pullup/pulldown resistors when configured as open-drain outputs. Also, the port is configurable with a high-side open-drain output.

The COLs (GPI[6:0]) and ROWs (GPI[14:7]) are also configurable as GPIs when not used for the key-switch matrix. When the device is configured with C columns and R rows for the key-switch matrix, assuming N is the larger number between R and C, then COL[6:N+1] and ROW[7:N+1] are configured as GPI ports. As an example, for a 4 x 4 matrix, COL6/COL5 and ROW7, ROW6,

Table 3. 4 x 4 Keyboard MatrixConfiguration with GPI

DOWE	COLUMNS							
ROWS	0	1	2	3	4	5	6	
0								
1	4	x 4 ke	eyboa	rd		GPI	GPI	
2		ma	ıtrix		GND		GFI	
3								
4		Gľ	١D		—	—	—	
5	GPI				—	—	—	
6	GPI			—	—	—		
7		G	PI		—	—	_	

GPIO Ports

and ROW5 are configured as GPIs, as shown in <u>Table 3</u>. Unused GPIs and pins configured neither as key-switch nor GPI should be connected to GND. <u>Table 4</u>, configured as a 3 x 4 matrix, shows ROW4 and ROW3 connected to GND, since they cannot be configured as GPI.

GPIO Direction Register (0x31)

This register configures the pins as an input or an output port. GPIO Direction register bits D[4:0] correspond with GPIO4–GPIO0 (Table 13). Set the corresponding bit to 0 to configure it as an input and 1 to configure it as an output.

When the port is initially programmed as an input, there is a delay of one debounce period prior to detecting a transition on the input port. This is to prevent a false interrupt from occurring when changing a port from an output to an input.

GPO Output Mode Register (0x32)

This register configures the pin as an open-drain or push-pull output. GPO Output Mode register bits D[4:0] correspond with GPIO4–GPIO0 (Table 14). Set the corresponding bit to 0 to configure the output mode as open drain and 1 to configure the output mode as push-pull.

GPIs LSB, MSB Port Value Registers (0x33, 0x34) (Read Only)

The GPIs LSB and MSB Port Value registers contain the debounced input data for all the GPIOs for GPI[7:0] and GPI[14:8], respectively (Table 15 and Table 16). There is one debounce period delay prior to detecting a transition on the input port. This prevents a false interrupt from occurring when changing a port from an output to an input. These registers report the state of all input ports, regardless of any interrupt mask settings.

Table 4. 3 x 4 Keyboard MatrixConfiguration with GPI

DOWE	COLUMNS							
ROWS	0	1	2	3	4	5	6	
0								
1	3	x 4 Ke ma	eyboa Itrix	rd	GND	GPI	GPI	
2		1110						
3		Gl	١D		—	—	—	
4	GND				—			
5	GPI			—	—	—		
6	GPI			_	_	_		
7		G	PI		_	_	_	

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GPIO Value Register (0x35)

The GPIO Value register consists of a read and write mode for the GPIO4–GPIO0 pins (<u>Table 17</u>). When read, this register reports the debounced input values for ports configured as a GPI. There is one debounce period delay prior to detecting a transition on the input port. This prevents a false interrupt from occurring when changing a port from an output to an input. This register reports the state of all input ports, regardless of any interrupt mask settings.

When written, this register sets the output as logic-low when written logic 0, or as logic-high when written logic 1 for ports configured as GPO.

GPIs, LSB, MSB Interrupt Mask Registers (0x36, 0x37, 0x38)

The GPIs, LSB, and MSB Interrupt Mask registers control which ports trigger an interrupt (<u>Table 18</u> for GPIO4–GPIO0, <u>Table 19</u> for GPI[7:0], and <u>Table 20</u> for GPI[14:8]). Set the bit to logic 0 to enable the interrupt. Set the bit to logic 1 to mask the interrupt.

If the port that generated the interrupt is not masked, then the interrupt causes the $\overline{\text{INT}}$ signal to assert. A read of the port value registers (0x33 to 0x35) is required to deassert the $\overline{\text{INT}}$ pin. Note that transitions that occur while $\overline{\text{INT}}$ is asserted, but before the read of the port value registers, set the appropriate bit of the port value registers only, but have no affect on the $\overline{\text{INT}}$ pin as it is already asserted.

However, transitions that occur when the I²C is active cannot be latched into the port values registers until after the read has taken place. If there are transitions that cause the \overline{INT} signal to assert during the time of an I²C read, they cause the \overline{INT} signal to reassert once the read transaction has taken place. Note that the interrupt configurations only apply when a port is configured as an input.

GPIs, LSB, MSB Interrupt Trigger Registers (0x39, 0x3A, 0x3B)

The GPIs, LSB, and MSB Interrupt Trigger registers control how an interrupt is triggered (<u>Table 21</u> for GPIO4–GPIO0, <u>Table 22</u> for GPI[7:0], and <u>Table 23</u> for GPI[14:8]). Set the bit to logic 0 for rising edge-triggered interrupts. Set the bit to logic 1 for both rising and falling edge-trigged interrupts.

GPO High-Side Open-Drain Enable Register (0x3C)

This register allows for high-side open-drain mode for GPIO4–GPIO0 (see <u>Table 24</u>). Set the bit to logic 0 for low-side open-drain mode. Set the bit to logic 1 to enable high-side open-drain mode.

GPO Pullup/Pulldown Resister Enable Register (0x3D)

This register enables the GPO $100k\Omega$ pullup resistor in low-side open-drain mode or pulldown resistor in highside open-drain mode for GPIO4–GPIO0 (Table 25). Set the bit to logic 0 to disable the internal pullup. Set the bit to logic 1 to enable the internal pullup.

GPIO Global Configuration Register (0x40)

The GPIO Global Configuration register controls the main settings for the GPIO ports (Table 26). Bit D5 enables interrupt generation for I²C timeouts. Bit D4 is the enable bit for the GPIs. Set bit D4 to logic 1 for normal GPIO operation for GPIO_, and ROW_ and COL_ configured as GPIs. GPIO_ configured as GPOs are automatically enabled.

GPI Debounce Setting Register (0x42)

The GPI Debounce Setting register sets the amount of time an input must be held in order for the device to register a logic transition (Table 27). The GPIO debounce setting is independent of the key-switch debounce setting. Bits D[4:0] set the 32 possible debounce times from 9ms up to 40ms.

I²C Timeout Flag Register (0x48) (Read Only) The I²C Timeout Flag register contains a single bit (D0) that indicates if an I²C timeout has occurred (<u>Table</u> <u>28</u>). Read this register to clear an I²C timeout-initiated interrupt.

Interrupts

Three possible sources generate $\overline{\text{INT}}$: key-switch $\overline{\text{FIFO}}$ level/debounce cycle settings, I²C timeout, and GPIOs configured as inputs (registers 0x01 or 0x40, 0x39–0x3A). Read the respective data/status registers for each type of interrupt to clear $\overline{\text{INT}}$. If multiple sources generate the interrupt, all the related status registers must be read to clear $\overline{\text{INT}}$.

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Serial Interface

The device operates as a slave that sends and receives data through an I²C-compatible two-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the device and generates the SCL clock that synchronizes the data transfer. Figure 1 shows the two-wire serial interface timing details.

The device's SDA line operates as both an input and an open-drain output. A pullup resistor, typically $4.7k\Omega$, is required on SDA. The device's SCL line operates only as an input. A pullup resistor is required on SCL if there

are multiple masters on the two-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START (S) condition (Figure 2) sent by a master, followed by the device's 7-bit slave address plus R/W bit, a register address byte, one or more data bytes, and finally, a STOP (P) condition.

START and STOP Condition

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.



Figure 1. Two-Wire Serial Interface Timing Details



Figure 2. START and STOP Conditions

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Bit Transfer

One data bit is transferred during each clock pulse (Figure 3). The data on SDA must remain stable while SCL is high.

Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 4), which the recipient uses to handshake receipt of each byte of data. Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse; therefore, the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the device, the device generates the acknowledge bit because the device is the recipient. When the device is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

Slave Addresses

The device has a 7-bit long slave address of 0x70, 0x72, 0x74, or 0x76 as determined by the suffix of the complete part number. The bit following a 7-bit slave address is the

R/W bit, which is low for a write command and high for a read command.

The device monitors the bus continuously waiting for a START condition, followed by its slave address. When the device recognizes its slave address, it acknowledges and is then ready for continued communication.

Bus Timeout

The device features a 20ms (min) bus timeout on the twowire serial interface, largely to prevent the device from holding the SDA I/O low during a read transaction should the SCL lock up for any reason before a serial transaction is completed. Bus timeout operates by causing the device to internally terminate a serial transaction (either read or write) if the time between adjacent edges on SCL exceeds 20ms. After a bus timeout, the device waits for a valid START condition before responding to a consecutive transmission. This feature can be enabled or disabled under user control by writing to the Configuration register. In sleep mode, the internal oscillator is disabled, thus the bus timeout feature is not active.



Figure 3. Bit Transfer



Figure 4. Acknowledge

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Message Format for Writing the Keyscan Controller

A write to the device comprises the transmission of the slave address with the R/W bit set to zero, followed by at least 1 byte of information. The first byte of information is the command byte. The command byte determines which register of the device is to be written by the next byte, if received. If a STOP condition is detected after the command byte is received, the device takes no further action (Figure 5) beyond storing the command byte.

Any bytes received after the command byte are data bytes. The first data byte goes into the internal register of the device selected by the command byte (Figure 6).

If multiple data bytes are transmitted before a STOP condition is detected, these bytes are generally stored insubsequent internal registers of the device because the command-byte address generally autoincrements (Table 5).

Message Format for Reading the Keyscan Controller

The device is read using the internally stored command byte as an address pointer, the same way the stored command byte is used as an address pointer for a write. The pointer generally autoincrements after each data byte is read using the same rules as for a write (Table 5). Thus, a read is initiated by first configuring the device's command byte by performing a write (Figure 5). The master can now read N consecutive bytes from the device, with the first data byte being read from the register addressed by the initialized command byte. When performing read-after-write verification, remember to reset the command byte's address because the stored command byte address is generally autoincremented after the write (Figure 7, Table 5).



Figure 5. Command Byte Received



Figure 6. Command and Single Data Byte Received



Figure 7. N Data Bytes Received

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Operation with Multiple Masters

When the device is operated on a two-wire interface with multiple masters, a master reading the device uses a repeated START between the write that sets the device's address pointer and the read(s) that takes the data from the location(s). This is because it is possible for master 2 to take over the bus after master 1 has set up the device's address pointer, but before master 1 has read the data. If master 2 subsequently resets the device's address pointer, master 1's read can be from an unexpected location.

Command Address Autoincrementing

Address autoincrementing allows the device to be configured with fewer transmissions by minimizing the number of times the command address needs to be sent. The command address stored in the device generally increments after each data byte is written or read (Table 5). Autoincrement only functions when doing a multiburst read or write.

Applications Information

Reset from I²C

After a catastrophic event such as ESD discharge or microcontroller reset, use bit D7 of the Configuration register (0x01) as a software reset for the key switches. Use bit D4 of the GPIO Global Configuration register (0x40) as a software reset for the GPIOs.

Ghost-Key Elimination

Ghost keys are a phenomenon inherent with key-switch matrices. When three switches located at the corners of a matrix rectangle are pressed simultaneously, the switch that is located at the last corner of the rectangle (the ghost key) also appears to be pressed. This occurs because the potentials at the two sides of the ghost-key switch are identical due to the other three connections—

able	5.	Autoir	ncrement	H	lules	
						_

REGISTER FUNCTION	ADDRESS CODE (hex)	AUTOINCREMENT ADDRESS (hex)	
Keys FIFO	0x00	0x00	
Autosleep	0×06	0x00	
All other key	0x01 to 0x05	Addr + 0x01	
All other GPIOs	0x30 to 0x48	Addr + 0x01	

the switch is electrically shorted by the combination of the other three switches (Figure 8). Because the key appears to be pressed electrically, it is impossible to detect which of the four keys is the ghost key.

The device employs a proprietary scheme that detects any three-key combination that generates a fourth ghost key, and does not report the third key that causes a ghost-key event. This means that although ghost keys are never reported, many combinations of three keys are effectively ignored when pressed at the same time. Applications requiring three-key combinations (such as <Ctrl><Alt>) must ensure that the three keys are not wired in positions that define the vertices of a rectangle (Figure 9). There is no limit on the number of keys that can be pressed simultaneously, as long as the keys do not generate ghost-key events and the FIFO is not full.



Figure 8. Ghost-Key Phenomenon



Figure 9. Valid Three-Key Combinations

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Low-EMI Operation

The device uses two techniques to minimize EMI radiating from the key-switch wiring. First, the voltage across the switch matrix never exceeds 0.5V if not in sleep mode, independent of supply voltage V_{DD} . This reduces the voltage swing at any node when a switch is pressed to 0.5V (max). Second, the keys are not dynamically scanned, which would cause the key-switch wiring to continuously radiate interference. Instead, the keys are monitored for current draw (only occurs when pressed), and debounce circuitry only operates when one or more keys are actually pressed.

Switch On-Resistance

The device is designed to be insensitive to resistance, either in the key switches, or the switch routing to and from the appropriate COL_ and ROW_ up to $5k\Omega$ (max). These controllers are therefore compatible with low-cost membrane and conductive carbon switches.

Hot Insertion

The \overline{INT} , SCL, and SDA remain high impedance with up to 3.6V asserted on them when the device powers down (V_{DD} = 0V). I/O ports remain high impedance with up to 4V asserted on them when not powered. The device can be used in hot-swap applications.

Power-Supply Considerations

The device operates with a 1.62V to 3.6V power-supply voltage. Bypass the power supply (V_{DD}) to GND with a 0.1µF or higher ceramic capacitor as close as possible to the device.

Register Tables

	KEYS FIFO REGISTER DATA								
SPECIAL FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0	
General bit description	FIFO not-empty flag	Key-release flag		Key number/Key event					
Key number indicated by D[5:0] is a keypress. Last data in the FIFO.	0	0	x	x	x	x	х	х	
Key number indicated by D[5:0] is a keypress. More data in the FIFO.	1	0	x	х	x	х	Х	х	
Key number indicated by D[5:0] is a key release. Last data in the FIFO.	0	1	x	x	x	х	х	х	
Key number indicated by D[5:0] is a key release. More data in the FIFO.	1	1	x	x	x	х	х	х	
FIFO is empty.	0	0	1	1	1	1	1	1	
FIFO is overflowed. Continued to read data in the FIFO.	0	1	1	1	1	1	1	1	
Key repeat. Indicates the last data in the FIFO.	0	0	1	1	1	1	1	0	
Key repeat. Indicates more data in the FIFO.	0	1	1	1	1	1	1	0	

Table 6. Keys FIFO Register (0x00)

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Table 7. Configuration Register (0x01)

REGISTER BIT	DESCRIPTION	VALUE	FUI	DEFAULT VALUE		
		X (when 0x40 D4 = 1)	Key-switch operating mode. Key switches always remain active when GPI (bit 4 of register 0x40) is high, regardles autosleep, autowake, or an I ² C write to this bit.			
D7	Sleep	0 (when 0x40 D4 = 0)	Key-switch sleep mode. The entire chip is shut down.	I ² C write, autosleep, and autowake can all change this	0	
		1 (when 0x40 D4 = 0)	Key-switch operating mode.	bit. This bit can be read back by I ² C any time for current status.		
D6	Reserved	0	—		0	
		0	INT cleared when the FIFO is	s empty.		
D5 Interrupt		1	INT cleared after host read. I FIFO until interrupt condition be lost.	0		
D4	Reserved	0	—		0	
	Key-release	0	Disable key releases.		-	
03	enable	1	Enable key releases.	Enable key releases.		
D2	Reserved	0	—		0	
D1	Autowako opablo	0	Disable keypress wakeup.		4	
		1	Enable keypress wakeup.	I		
	Timoout disable	0	I ² C timeout enabled.			
	Timeout disable	1	I ² C timeout disabled.			

X = Don't care.

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Table 8. Key-Switch Debounce Register (0x02)

	REGISTER DATA									
REGISTER DESCRIPTION	D7	D6	D5	D4	D3	D2	D1	D0		
DEBOUNCE TIME (ms)	RE	LEASE DEI	BOUNCE TI	ME	Р	RESS DEB		E		
1					0	0	0	0		
3					0	0	0	1		
5		``			0	0	1	0		
7		/	^		0	0	1	1		
9					0	1	0	0		
11					0	1	0	1		
:							:			
25					1	1	0	0		
27		```			1	1	0	1		
29		/	^		1	1	1	0		
31					1	1	1	1		
1	0	0	0	0						
3	0	0	0	1						
5	0	0	1	0		```	/			
7	0	0	1	1		1	Υ.			
9	0	1	0	0						
11	0	1	0	1						
:		-	•							
25	1	1	0	0						
27	1	1	0	1						
29	1	1	1	0		7	Λ			
31	1	1	1	1						
Power-on default (31)	1	1	1	1	1	1	1	1		

X = Don't care.

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Table 9. Key-Switch Interrupt Register (0x03)

	REGISTER DATA							
REGISTER DESCRIPTION	D7	D6	D5	D4	D3	D2	D1	D0
	FIF	O-BASE			TIM	E-BASE	D INT	
Power-up default setting All INT disabled	0	0	0	0	0	0	0	0
Time-based INT disabled				0	0	0	0	0
INT asserts every debounce cycle		Х		0	0	0	0	1
INT asserts every 2 debounce cycles				0	0	0	1	0
:						:		
INT asserts every 29 debounce cycles				1	1	1	0	1
INT asserts every 30 debounce cycles	Х			1	1	1	1	0
INT asserts every 31 debounce cycles				1	1	1	1	1
FIFO-based INT disabled	0	0	0					
INT asserts when the FIFO has 2 key events	0	0	1			Х		
INT asserts when the FIFO has 4 key events	0	1	0					
		:						
INT asserts when the FIFO has 10 key events	1	0	1					
INT asserts when the FIFO has 12 key events	1 1 0 X							
INT asserts when the FIFO has 14 key events	1	1	1					
Both time-based and FIFO-based interrupts active	1	Not all ze	ero			Not all ze	ero	

X = Don't care.

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Table 10. Key-Switch Autorepeat Register (0x05)

	REGISTER DATA							
REGISTER DESCRIPTION	D7	D6	D5	D4	D3	D2	D1	D0
	ENABLE	AUTO	DREPEAT	RATE	A	AUTOREPEAT DELAY		
Autorepeat is disabled	0	Х	Х	Х	X	Х	Х	Х
Autorepeat is enabled	1	Αι	itorepeat r	ate		Autorep	eat delay	
Autorepeat delay is 8 debounce cycles	1				0	0	0	0
Autorepeat delay is 16 debounce cycles	1		Х		0	0	0	1
Autorepeat delay is 24 debounce cycles	1				0	0	1	0
Autorepeat delay is 112 debounce cycles	1				1	1	0	1
Autorepeat delay is 120 debounce cycles	1		Х		1	1	1	0
Autorepeat delay is 128 debounce cycles	1				1	1	1	1
Autorepeat frequency is 4 debounce cycles	1	0	0	0				
Autorepeat frequency is 8 debounce cycles	1	0	0	1		2	X	
Autorepeat frequency is 12 debounce cycles	1	0	1	0				
		:	1		1			
Autorepeat frequency is 24 debounce cycles	1	1	0	1				
Autorepeat frequency is 28 debounce cycles	1	1	1	0		2	X	
Autorepeat frequency is 32 debounce cycles	1	1	1	1				
Power-on default setting	0	0	0	0	0	0	0	0

X = Don't care.

Table 11. Autosleep Register (0x06)

	REGISTER DATA							
REGISTER DESCRIPTION	RESERVED				AUTOSHUTDOWN TIME			
AUTOSLEEP (ms)	D7	D6	D5	D4	D3	D2	D1	D0
Disabled	0	0	0	0	0	0	0	0
8192	0	0	0	0	0	0	0	1
4096	0	0	0	0	0	0	1	0
2048	0	0	0	0	0	0	1	1
1024	0	0	0	0	0	1	0	0
512	0	0	0	0	0	1	0	1
256	0	0	0	0	0	1	1	0
256	0	0	0	0	0	1	1	1
Power-up default settings	0	0	0	0	0	1	1	1

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Table 12	Key-Switch	Array Size	Register (0x30)
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	REGISTER DATA								
REGISTER DESCRIPTION	D7	D6	D5	D4	D3	D2	D1	D0	
		RO	WS			COLUMNS			
No rows are key switches	0	0	0	0					
ROW0 is a key switch	0	0	0	1					
ROW0 to ROW1 are key switches	0	0	1	0]				
ROW0 to ROW2 are key switches	0	0	1	1]				
ROW0 to ROW3 are key switches	0	1	0	0)	X		
ROW0 to ROW4 are key switches	0	1	0	1					
ROW0 to ROW5 are key switches	0	1	1	0					
ROW0 to ROW6 are key switches	0	1	1	1]				
ROW0 to ROW7 are key switches	1	Х	Х	Х					
No columns are key switches					0	0	0	0	
COL0 is a key switch					0	0	0	1	
COL0 to COL1 are key switches					0	0	1	0	
COL0 to COL2 are key switches			~		0	0	1	1	
COL0 to COL3 are key switches			^		0	1	0	0	
COL0 to COL4 are key switches					0	1	0	1	
COL0 to COL5 are key switches]				0	1	1	0	
COL0 to COL6 are key switches					0	1	1	1	
Power-up default setting	1	1	1	1	0	1	1	1	

X = Don't care.

Table 13. GPIO Direction Register (0x31)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE	
D[7:5]	Reserved	000	_	000	
		0	Set as input pin		
D4	GPI04	1	Set as output pin	0	
Da		0	Set as input pin		
D3	GPI03	1	Set as output pin	0	
Do		0	Set as input pin		
D2	GPI02	1	Set as output pin	0	
		0	Set as input pin		
	GPIOT	1	Set as output pin	0	
Do	0 Set as input pin		Set as input pin		
	GPI00	1	Set as output pin	0	

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Table 14. GPO Output Mode Register (0x32)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D[7:5]	Reserved	000	—	000
		0	Port is an open-drain output	0
D4	GFI04	1	Port is a push-pull output	0
50		0	Port is an open-drain output	0
D3	GFI03	1	Port is a push-pull output	0
			Port is an open-drain output	0
D2	GPIO2	1	Port is a push-pull output	0
		0	Port is an open-drain output	0
	GFIOT	1	Port is a push-pull output	0
	0 Port is an open-drain output		Port is an open-drain output	0
DU	GFIOU	1	Port is a push-pull output	0

Table 15. GPIs LSB Value Register (0x33) (Read Only)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
	DOWO	0	Input value is low	4
	ROWU	1	Input value is high	
De		0	Input value is low	
DO	COLO	1	Input value is high	
DE		0	Input value is low	4
D5	COLS	1	Input value is high	
	COL4	0	Input value is low	-
D4		1	Input value is high	
50		0	Input value is low	4
D3	COL3	1	Input value is high	
		0	Input value is low	-
D2	COLZ	1	Input value is high	
		0	Input value is low	4
	COLI	1	Input value is high	
		0	Input value is low	1
	COLU	1	Input value is high	

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REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	Reserved		—	0
De		0	Input value is low	1
Do		1	Input value is high	
DE	DOWG	0	Input value is low	1
D5	ROVIO	1	Input value is high	
	DOWE	0	Input value is low	- 1
D4	ROVS	1	Input value is high	
	ROW4	0	Input value is low	-
D3		1	Input value is high	
		0	Input value is low	- 1
D2	nOvis	1	Input value is high	
D1	DOWO	0	Input value is low	-
	noviz	1	Input value is high	
D0		0	Input value is low	1
	KOW1	1	Input value is high	1

Table 16. GPIs MSB Value Register (0x34) (Read Only)

Table 17. GPIO Value Register (0x35)

REGISTER BIT	DESCRIPTION	R/W	VALUE	FUNCTION	DEFAULT VALUE							
D[7:5]	—	_	000	Reserved	000							
		Р	0	Input value is low	0							
D4	GPI04	н н	1	Input value is high	0							
		р	0	Input value is low	0							
03	GPIOS		1	Input value is high	0							
		р	0	Input value is low	0							
D2	GPI02		1	Input value is high	0							
		р	0	Input value is low	0							
	GPIOT	К	1	Input value is high	0							
D0		р	0	Input value is low	0							
DU	GPIOU	п	1	Input value is high	0							
		GPIO4 W	0	Set output logic-low								
D4	GFI04		1	Set output logic-high								
50									10/	0	Set output logic-low	
D3	GFIUS	vv	1	Set output logic-high								
		14/	0	Set output logic-low								
D2	GFIOZ	vv	1	Set output logic-high								
D1 GPI		۱۸/	0	Set output logic-low								
	GFIOT	v v	1	Set output logic-high								
	CRIOO	\\/	0	Set output logic-low								
Do	GPIO0	VV	1	Set output logic-high	1 —							

Table 18. GPIs Interrupt Mask Register (0x36)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D[7:5]	Reserved	000	—	000
		0	Interrupt is unmasked	-1
D4	GPI04	1	Interrupt is masked	
50		0	Interrupt is unmasked	-1
D3	GPI03	1	Interrupt is masked	
50	GPIO2	0	Interrupt is unmasked	- 1
D2		1	Interrupt is masked	
		0	Interrupt is unmasked	
DI	GPIOT	1	Interrupt is masked	
	GRIOO	0	Interrupt is unmasked	1
Do	GPIOU	1	Interrupt is masked	

Table 19. GPIs LSB Interrupt Mask Register (0x37)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
	DOM/0	0	Interrupt is unmasked	-
	ROVVO	1	Interrupt is masked	
De		0	Interrupt is unmasked	4
Do	COL6	1	Interrupt is masked	
Dr		0	Interrupt is unmasked	-
D5	COLS	1	Interrupt is masked	
	COL4	0	Interrupt is unmasked	- 1
D4		1	Interrupt is masked	
D2	COL3	0	Interrupt is unmasked	- 1
D3		1	Interrupt is masked	
		0	Interrupt is unmasked	4
D2	COLZ	1	Interrupt is masked	
		0	Interrupt is unmasked	- 1
D1	COLI	1	Interrupt is masked	
DO		0	Interrupt is unmasked	4
	COLU	1	Interrupt is masked	

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REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	Reversed		—	0
DC		0	Interrupt is unmasked	4
Do	ROW7	1	Interrupt is masked	
DE	DOWC	0	Interrupt is unmasked	4
Do	ROW6	1	Interrupt is masked	
	DOWE	0	Interrupt is unmasked	-
D4	ROWS	1	Interrupt is masked	
	ROW4	0	Interrupt is unmasked	4
D3		1	Interrupt is masked	
50	DOW2	0	Interrupt is unmasked	1
D2	ROW3	1	Interrupt is masked	
	DOWO	0	Interrupt is unmasked	4
DI	ROW2	1	Interrupt is masked	
DO	DOW/1	0	Interrupt is unmasked	
DO	ROWI	1	Interrupt is masked	

Table 20. GPIs MSB Interrupt Mask Register (0x38)

Table 21.	GPIs	Interrupt	Trigger	Mode	Register	(0x39))
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REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D[7:5]	Reserved	000	—	000
		0	Rising edge-triggered interrupts	0
D4	GF104	1	Rising and falling edge-triggered interrupts	0
202		0	Rising edge-triggered interrupts	- 0
D3	GPI03	1	Rising and falling edge-triggered interrupts	
50	GPIO2	0	Rising edge-triggered interrupts	0
D2		1	Rising and falling edge-triggered interrupts	
		0	Rising edge-triggered interrupts	0
	GPIOT	1	Rising and falling edge-triggered interrupts	
	CRIOO	0	Rising edge-triggered interrupts	
	GPIOU	1	Rising and falling edge-triggered interrupts	0

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REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
	ROWO	0	Rising edge-triggered interrupts	0
	ROVU	1	Rising and falling edge-triggered interrupts	
De	0016	0	Rising edge-triggered interrupts	0
DO	COLO	1	Rising and falling edge-triggered interrupts	
DE		0	Rising edge-triggered interrupts	0
D5	COLS	1	Rising and falling edge-triggered interrupts	0
	0014	0	Rising edge-triggered interrupts	- 0
D4	COL4	1	Rising and falling edge-triggered interrupts	
D2	COL3	0	Rising edge-triggered interrupts	- 0
03		1	Rising and falling edge-triggered interrupts	
	001.0	0	Rising edge-triggered interrupts	0
D2	COLZ	1	Rising and falling edge-triggered interrupts] 0
		0	Rising edge-triggered interrupts	0
	COLI	1	Rising and falling edge-triggered interrupts	
D0	001.0	0	Rising edge-triggered interrupts	0
DO	COLO	1	Rising and falling edge-triggered interrupts	

Table 22. GPIs LSB Interrupt Trigger Mode Register (0x3A)

Table 23. GPIs MSB Input Interrupt Trigger Mode Register (0x3B)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	—	Х	Don't care	0
De	DOW/7	0	Rising edge-triggered interrupts	0
Do		1	Rising and falling edge-triggered interrupts	
DE	DOWC	0	Rising edge-triggered interrupts	0
D5	ROVVO	1	Rising and falling edge-triggered interrupts	
	DOWE	0	Rising edge-triggered interrupts	0
D4	ROW5	1	Rising and falling edge-triggered interrupts	
	ROW4	0	Rising edge-triggered interrupts	0
D3		1	Rising and falling edge-triggered interrupts	1 0
Da	DOWO	0	Rising edge-triggered interrupts	0
D2	ROW3	1	Rising and falling edge-triggered interrupts	
	DOWA	0	Rising edge-triggered interrupts	0
D1	ROW2	1	Rising and falling edge-triggered interrupts	1 0
DO	DOW/1	0	Rising edge-triggered interrupts	0
	ROW1	1	Rising and falling edge-triggered interrupts	

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REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D[7:5]	Reserved	000	—	000
		0	Set low-side open-drain mode	0
D4	GFI04	1	Set high-side open-drain mode	0
		0	Set low-side open-drain mode	0
D3	GPIOS	1	Set high-side open-drain mode	
	GPIO2	0	Set low-side open-drain mode	- 0
D2		1	Set high-side open-drain mode	
		0	Set low-side open-drain mode	0
	GPIOT	1	Set high-side open-drain mode	
D0	CRIOO	0	Set low-side open-drain mode	0
	DU	GPIOU	1	Set high-side open-drain mode

Table 24. GPO High-Side Open-Drain Enable Register (0x3C)

Table 25. GPO Pullup/Pulldown Resistor Enable Register (0x3D)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D[7:5]	Reserved	000	—	000
		0	Disable internal pullup/pulldown	
D4	GPIO4	1	Enable internal pullup/pulldown for open- drain output	0
		0	Disable internal pullup/pulldown	
D3	GPIO3	1	Enable internal pullup/pulldown for open- drain output	0
	GPIO2	0	Disable internal pullup/pulldown	
D2		D2 GPIO2	1	Enable internal pullup/pulldown for open- drain output
		0	Disable internal pullup/pulldown	
D1	GPIO1	1	Enable internal pullup/pulldown for open- drain output	0
D0		0	Disable internal pullup/pulldown	
	GPIO0	1	Enable internal pullup/pulldown for open- drain output	0

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Table 26. GPIO Global Configuration Register (0x40)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE	
D[7:6]	Reserved	00	—	00	
D5		0	Disable I ² C timeout interrupt		
	I ² C Interrupt Timeout Enable	1	Enable I ² C timeout interrupt. INT is deas- serted when a read is performed on the I ² C timeout flag register (0x48)	0	
	Operating Mode		0	Standby mode	0
D4		1	Normal mode		
D[3:0]	Reserved		—	0000	

Table 27. GPI Debounce Setting Register (0x42)

	REGISTER DATA							
REGISTER DESCRIPTION	D7	D6	D5	D4	D3	D2	D1	D0
	RESERVED				DEBOUNCE TIME			
Power-up default setting Debounce time is 9ms	0	0	0	0	0	0	0	0
Debounce time is 10ms	0	0	0	0	0	0	0	1
Debounce time is 11ms	0	0	0	0	0	0	1	0
Debounce time is 12ms	0	0	0	0	0	0	1	1
Debounce time is 37ms	0	0	0	1	1	1	0	0
Debounce time is 38ms	0	0	0	1	1	1	0	1
Debounce time is 39ms	0	0	0	1	1	1	1	0
Debounce time is 40ms	0	0	0	1	1	1	1	1

Table 28. I²C Timeout Flag Register (0x48) (Read Only)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D[7:1]	Reserved	0000000	—	0000000
D0	I ² C Timeout Flag	0	No I ² C timeout has occurred since last read or POR.	
		1	I ² C timeout has occurred since last read or POR. This bit is reset to zero when a read is performed on this register. I ² C timeouts must be enabled for this function to work (Table 26).	0

Wafer-Level Packaging (WLP) Applications Information

For the latest application details on WLP construction, dimensions, tape-carrier information, PCB techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to Application Note 1891: *Wafer-Level Packaging (WLP) and Its Applications*, available at <u>www.maximintegrated.com/</u> an1891.



Typical Application Circuit

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Ordering Information

Chip Information

PART	TEMP RANGE	PIN- PACKAGE	l ² C ADDRESS (hex)
MAX7365EWA70+	-40°C to +85°C	25 WLP	70
MAX7365EWA72+	-40°C to +85°C	25 WLP	72
MAX7365EWA74+	-40°C to +85°C	25 WLP	74
MAX7365EWA76+	-40°C to +85°C	25 WLP	76

+Denotes a lead(Pb)-free/RoHS-compliant package.

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to <u>www.maximintegrated.com/packages</u>. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE	PACKAGE	OUTLINE	LAND PATTERN NO.	
TYPE	CODE	NO.		
25 WLP	W252B2+1	<u>21-0180</u>	Refer to Application Note 1891	

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Revision History

REVISION	REVISION	DESCRIPTION	PAGES
NUMBER	DATE		CHANGED
0	9/11	Initial release	—



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