LTC6433-15 Low Frequency to 1.4GHz 50Ω Gain Block IF Amplifier

DESCRIPTION

Demonstration circuit 2168A features the LTC®6433-15 50Ω gain block amplifier. The LTC6433-15 has a power gain of 15.9dB and it is part of the LTC6431-YY amplifier series.

The DC2168A demo board is optimized for a frequency range from 100kHz to 1000MHz. It is a single application circuit on a demo board that covers 13 octaves of frequency range. The application circuit features a wideband output network with flat frequency response. The amplifier exhibits excellent NF at low frequencies to 100kHz compared to other GaAs FET type amplifiers. The LTC6433-15 provides 50Ω single-ended input and output impedances. SMA connections facilitate direct connections to most commercially available RF test equipment.

Design files for this circuit board are available at http://www.linear.com/demo/DC2168A

BLOCK DIAGRAM

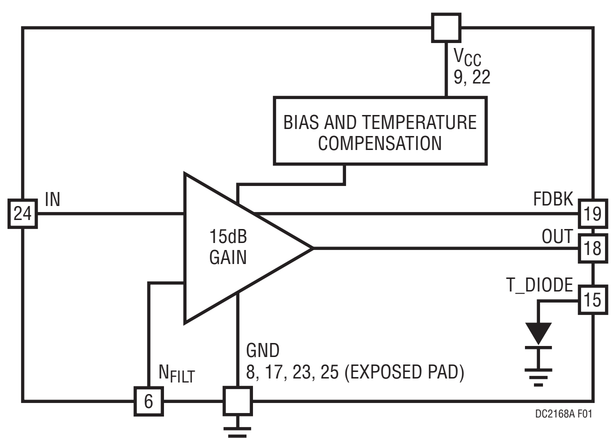

Figure 1. LTC6433-15 Device Block Diagram

PERFORMANCE SUMMARY Specifications are at T_A = 25°C

Table 1. Typical Demo Board Performance Summary

SYMBOL	PARAMETER	CONDITIONS	VALUE / UNIT
Power Supply			
V_{CC}	Operating Supply Range	All V_{CC} Pins Plus OUT	4.75V to 5.25V
I_{CC}	Current Consumption	Total Current	95mA

FREQUENCY (MHz)	POWER GAIN |S21|	OUTPUT THIRD-ORDER INTERCEPT POINT[1] OIP3	OUTPUT THIRD-ORDER INTERMODULATION[1] OIM3	SECOND HARMONIC DISTORTION[2] HD2	THIRD HARMONIC DISTORTION[2] HD3	OUTPUT 1dB COMPRESSION POINT P1dB	NOISE FIGURE[3] NF
0.1	15.2	47.8	–91.6	–65.0	–70.0	19.2	6.7
1	15.2	52.0	–100.0	–73.0	–81.0	19.1	3.9
10	15.1	47.6	–91.2	–54.0	–77.0	19.3	3.7
50	15.0	48.0	–92.0	–56.0	–84.0	19.3	2.9
100	14.8	47.5	–91.0	–55.0	–80.0	19.2	3.1
150	14.9	47.2	–90.4	–54.0	–78.0	19.2	3.2
200	15.0	44.2	–84.4	–53.4	–76.3	19.1	3.3
240	15.0	43.1	–82.2	–53.0	–73.0	19.1	3.4
300	14.9	41.5	–79.0	–51.9	–72.0	19.0	3.6
400	14.6	39.7	–75.4	–51.6	–69.0	19.0	3.7
500	14.5	38.4	–72.8	–51.0	–70.0	18.9	3.9
600	14.3	37.1	–70.2	–50.9	–65.2	18.7	4.1
700	14.1	35.7	–67.4	–50.4	–64.4	18.4	4.2
800	13.8	34.9	–65.9	–47.0	–59.5	18.0	4.3
900	13.6	34.1	–64.2	–46.1	–58.3	17.6	4.5
1000	13.3	33.3	–62.6	–45.0	–57.0	17.3	4.8
Units	dB	dBm	dBc	dBc	dBc	dBm	dB

Notes: All figures are referenced to J1 (Input Port) and J2 (Output Port).

1 Two-tone test conditions: Output power level = +2dBm/tone, tone spacing = 1MHz.
2 Single-tone test conditions: Output power level = +6dBm.
3 Small-signal noise figure.

OPERATION

The DC2168A is a high linearity, fixed gain amplifier. It is designed for ease of use. Both the input and output are internally matched to 50Ω single-ended impedance. Figure 2 shows the DC2168A's S-parameters.

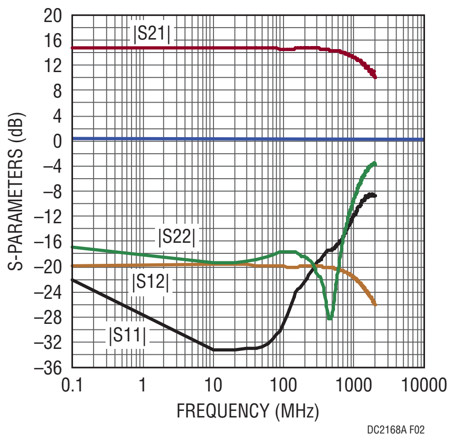

Figure 2. Demo Board S-Parameters

Figure 4 shows the demo circuit's schematic. The input and output DC blocking capacitors (C1 and C17) are required because this device is internally DC biased for optimal operation. The V_{CC} pull-up network (L1, L2, R5 and R6) and the decoupling capacitors (C3, C4, C16 and C19) provide the proper DC bias to the RF output node. Only a single 5V supply is necessary for the V_{CC} pins on the device.

A parallel 1µF (C2) and 348Ω (R1) input network has been added to ensure low frequency stability. Note that the input stability network does degrade the input return loss at low frequencies. Performance can be improved by increasing the value of capacitor C2.

The T_DIODE Pin (Turret E1) can be forward biased to ground with 1mA of current. The measured voltage will be an indicator of the chip junction temperature (TJ).

Please note that a number of DNC pins are connected on the demo board. These connections are not necessary for normal operation and should be deleted from the PCB. Table 2 shows the function of each input and output on the board.

Table 2. DC2168A Board I/O Descriptions

CONNECTOR	FUNCTION
J1 (IN)	Single-ended input. Impedance matched to 50Ω. Drive from a 50Ω network analyzer or signal source.
J2 (OUT)	Single-ended output. Impedance matched to 50Ω. Drives a 50Ω network analyzer or spectrum analyzer.
E1 (T_DIODE)	When forward biased, the measured voltage will be an indicator of the chip junction temperature.
E2 (VCC)	Positive supply voltage source.
E3 (GND)	Supply ground.

OPERATION

Additional Information

As with any RF device, minimizing ground inductance is critical. Care should be taken during the board layout when using these exposed pad packages. The maximum number of small-diameter vias should be placed underneath the exposed pad. This will ensure a good RF ground and low thermal impedance. Maximizing the copper ground plane will also improve heat spreading and lower the inductance to ground.

The DC2168A is a wideband demo board, but it is not intended for operation down to DC.

Table 3 shows the LTC643X-YY amplifier series and the associated demo boards. Each demo board lists the typical working frequency range and the input and output impedance of the amplifiers.

Table 3. The LTC643X-YY Amplifier Family and Corresponding Application Demo Boards

DEMO BOARD NUMBER	FREQUENCY RANGE (MHz)	NOTES/APPLICATIONS	BOARD'S IN/OUT IMPEDANCE	AMPLIFIER	AMPLIFIER'S IMPEDANCE
DC1774A-A	50 to 350	Low Frequency	50Ω	LTC6430-15	Differential 100Ω
DC1774A-B	400 to 1000	Mid Frequency	50Ω	LTC6430-15	Differential 100Ω
DC1774A-C	100 to 1200	Wide Frequency	50Ω	LTC6431-15	Single-Ended 50Ω
DC2032A	50 to 1000	Cable Infrastructure	75Ω	LTC6430-15	Differential 100Ω
DC2077A	100 to 1200	Wide Frequency	50Ω	LTC6431-20	Single-Ended 50Ω
DC2153A	700 to 1700	High Frequency	50Ω	LTC6430-15	Differential 100Ω
DC2090A	50 to 1200	Power Doubler	50Ω	Dual LTC6430-15	Differential 50Ω
DC2076A-A	50 to 350	Low Frequency	50Ω	LTC6430-20	Differential 100Ω
DC2076A-B	350 to 1000	Mid Frequency	50Ω	LTC6430-20	Differential 100Ω
DC2078A	50 to 1000	Cable Infrastructure	75Ω	LTC6430-20	Differential 100Ω
DC2168A	0.1 to 1000	Very Low Frequency	50Ω	LTC6433-15	Single-Ended 50Ω

OPERATION

Setup Signal Sources and Spectrum Analyzer

The LTC6433-15 is an amplifier with high linearity performance. Therefore, the output intermodulation products are very low. Even using high dynamic range test equipment, third-order intercept (IP3) measurements can drive test setups to their limits. Consequently, accurate measurement of IP3 for a low distortion IC such as the LTC6433-15 requires certain precautions to be observed in the test setup as well as the testing procedure.

Setup Signal Sources

Figure 3 shows a proposed IP3 test setup. This setup has low phase noise, good reverse isolation, high dynamic range, sufficient harmonic filtering and wideband impedance matching. The setup is outlined below:

a. High performance signal generators 1 and 2 (HP8644A) are used. These suggested generators have low harmonic distortion and very low phase noise.

b. High linearity amplifiers are used to improve the reverse isolation. This prevents crosstalk between the two signal generators and provides higher output power.

c. A lowpass filter is used to suppress the harmonic content from interfering with the test signal. Note that second order inputs can "mix" with the fundamental frequency to form intermodulation (IM) products of their own. We suggest filtering the harmonics to –50dBc or better.

d. The signal combiner from Mini-Circuits (ADP-2-9) combines the two isolated input signals. This combiner has a typical isolation of 27dB. For improved VSWR and isolation, the H-9 signal combiner from MA/COM is an alternative which features >40dB isolation and a wider frequency range. Passive devices (e.g. combiners) with magnetic elements can contribute nonlinearity to the signal chain and should be used cautiously.

e. The attenuator pads on all three ports of the signal combiner will further support isolation of the two input signal sources. They also reduce reflections and promote maximum power transfer with wideband impedance matching.

Setup the Spectrum Analyzer

a. Adjust the spectrum analyzer for maximum possible resolution of the intermodulation products' amplitude in dBc. A narrower resolution bandwidth will take a longer time to sweep.

b. Optimize the dynamic range of the spectrum analyzer by adjusting the input attenuation. First increase the spectrum analyzer's input attenuation (normally in steps of 5dB or 10dB). If the IM product levels decrease when the input attenuation is increased, then the input power level is too high for the spectrum analyzer to make a valid measurement. Most likely, the spectrum analyzer's 1st mixer was overloaded and producing its own IM products. If the IM reading holds constant with increased input attenuation, then a sufficient amount of attenuation was present. Adding too much attenuation will bury the intended IM signal in the noise floor. Therefore, select just enough attenuation to achieve a stable and valid measurement.

c. In order to achieve this valid measurement result, the test system must have lower total distortion than the DUT's intermodulation. For example, to measure a 47dBm OIP3, the measured intermodulation products will be –90dBc below the –14dBm per tone input level and the test system must have intermodulation products approximately –96dBc or better. For best results, the IM products and noise floor should measure at least –100dBc before connecting the DUT.

QUICK START PROCEDURE

DC2168A can be set up to evaluate the performance of the LTC6433-15. Refer to Figure 3 for proper equipment connections and follow the procedure below:

Two-Tone Measurement

Connect all test equipment as suggested in Figure 3.

1. The power labels of V_{CC} 4.75V–5.25V and GND directly correspond to the power supply. Typical current consumption of the LTC6433-15 is about 95mA.
2. Apply two independent signals f1 and f2 from signal generator 1 and signal generator 2 at 150MHz and 151MHz, while setting the amplitude to –14dBm/tone at the demo board input (J1).
3. Monitor the output tone level on the spectrum analyzer. Adjust the signal generator levels such that the output power measures +2dBm/tone at the amplifier output J2, after correcting for external cable losses and attenuations.
4. Change the spectrum analyzer's center frequency and observe the two IM3 tones at 1MHz below and above the input frequencies. The frequencies of IM3_LOW and IM3_HIGH are 149MHz and 152MHz, respectively. The measurement levels should be approximately –90.4dBc; +47.2dBm is typical OIP3 performance for the LTC6433-15 at 150MHz.

The OIP3 calculation is:

$$OIP3 = POUT + \Delta IMD3/2$$

where:

POUT is the lower output signal power of the fundamental products.

$\Delta IMD3 = POUT – PIM3$;

PIM3 is the higher third-order intermodulation product.

Single-Tone Measurement

5. Continue with Step 4 above, turn off one signal source to measure gain and harmonic distortions.

QUICK START PROCEDURE

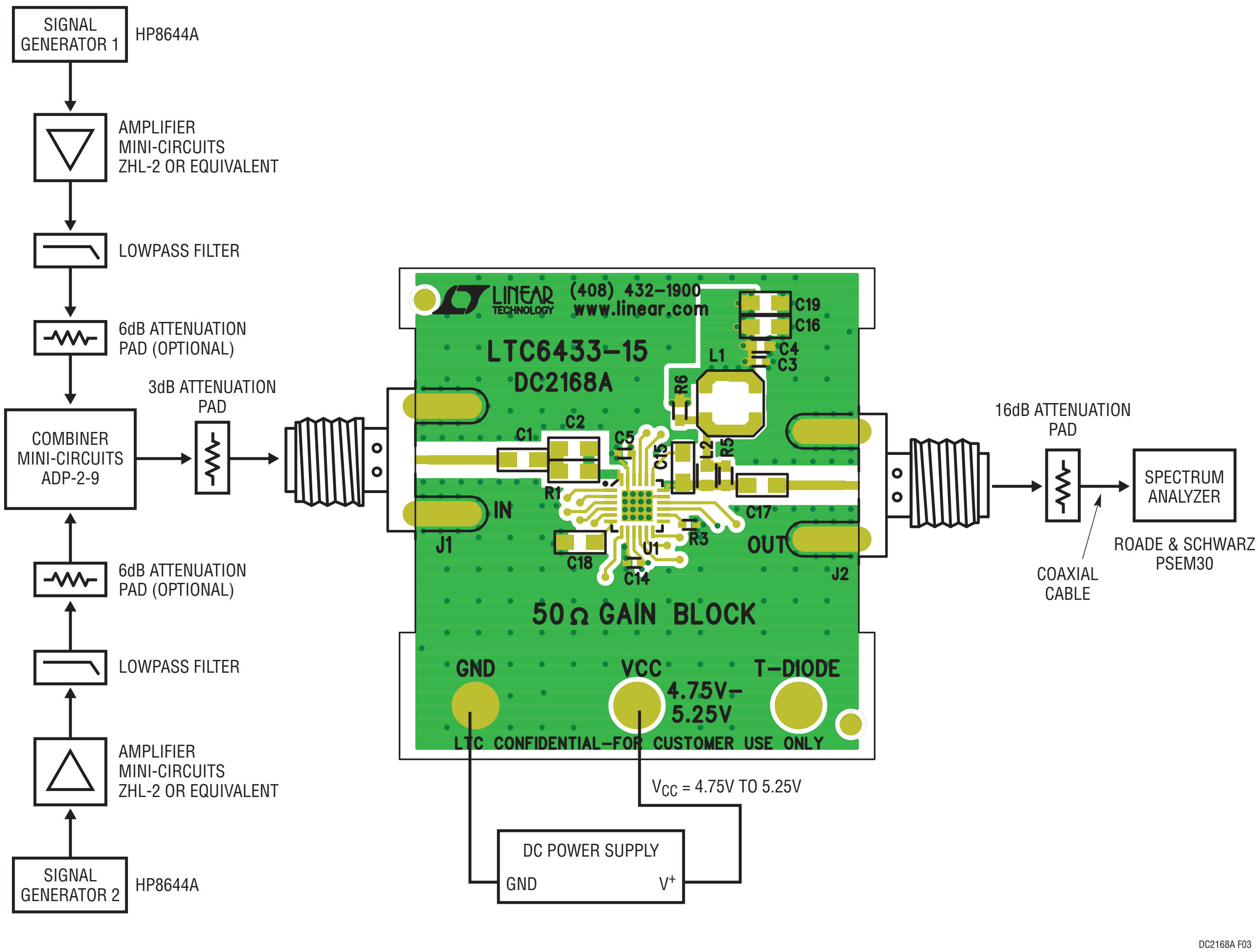

Figure 3. Proper Equipment Setup for IP3 Measurement

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	5	C1, C2, C15, C16, C17, C18	CAP., X8R, 1µF, 16V, 10%, 0805	TDK, C2012X8R1C105K125AB
2	3	C3, C5, C14	CAP., X7R, 1000pF, 50V 10%, 0402	MURATA, GRM155R71H102KA01D
3	1	C4	CAP., X7R, 0.1µF, 25V, 10%, 0603	MURATA, GRM188R71E104KA01D
4	1	C19	CAP., X7S, 10µF, 25V,10%, 0805	MURATA, GRM21BC71E106KE11L
5	3	E1-E3	TESTPOINT, TURRET, .093"	MILL-MAX, 2501-2-00-80-00-00-07-0
6	2	J1, J2	CONN., SMA 50Ω EDGE-LAUNCH	CINCH CONNECTIVITY SOLUTIONS JOHNSON, 142-0701-851
7	1	L1	IND., POWER, 470µH, 20%, LPS5030	COILCRAFT, LPS5030-474MRB
8	1	L2	IND., 0603, 240nH	COILCRAFT, 0603LS-241XJLB
9	1	R1	RES., CHIP, 348 , 1%, 0805	VISHAY, CRCW0805348RFKEA
10	0	R3	RES., 0402, OPT	
11	1	R5	RES., CHIP, 280 , 1%, 0603	VISHAY, CRCW0603280RFKEA
12	1	R6	RES., CHIP, 249 , 1%, 0603	VISHAY, CRCW0603249RFKEA
13	1	U1	BALANCED AMPLIFIER QFN24UF-4X4	LINEAR TECH., LTC6433AIUF-15#PBF
14	1	Z1	DIODE, ZENER, 6.2V 1.5W 5%, SMA CASE	CENTRAL SEMI., CMZ5920B TR13
15	1		PCB, PRINTED CIRCUIT BOARD	DEMO BOARD 2168A - A2

SCHEMATIC DIAGRAM

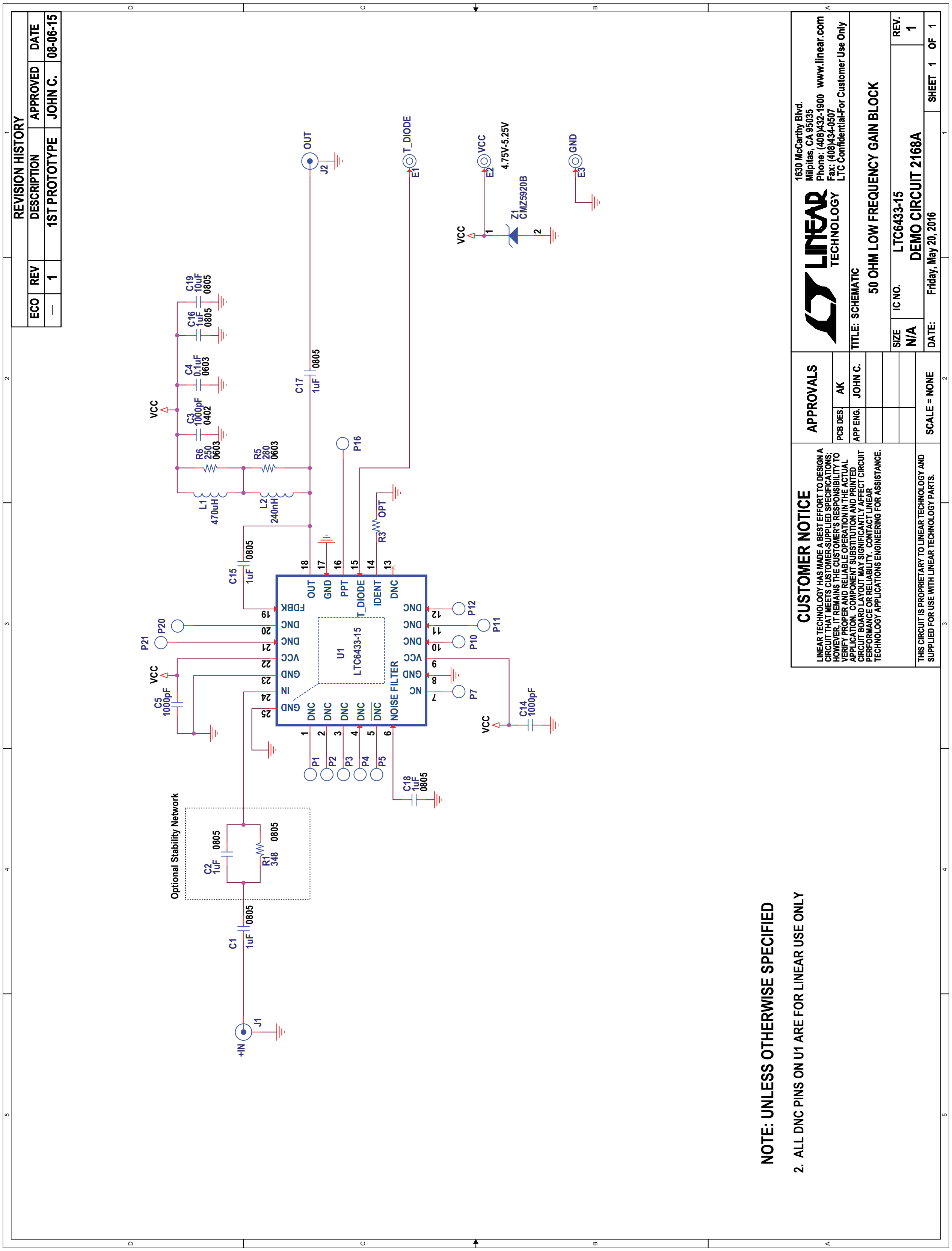

Figure 4. DC2168A Demo Circuit Schematic

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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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