Product Document

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TCS3707

ALS/Color Sensor with Flicker Detection

General Description

The TCS3707 features ambient light and color (RGB) sensing, proximity and flicker detection. The device comes in a low-profile and small footprint, L2.5mm x W2.0mm x H0.5mm package.

The Ambient Light and Color Sensing function provides five concurrent ambient light sensing channels: Red, Green, Blue, Clear, and Wideband. The RGB and Clear channels have a UV/IR blocking filter. This architecture accurately measures ambient light and enables the calculation of illuminance, chromaticity, and color temperature to manage display appearance.

The device integrates direct detection of 50Hz or 60Hz ambient light flicker. Flicker detection is executed in parallel with ambient light and color sensing and has independent gain configuration. The flicker detection engine can also buffer data for calculating other flicker frequencies externally.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TCS3707 are listed below:

Figure 1:
Added Value of Using TCS3707

Benefits	Features

• Invisible ALS and color sensing under any glass type	• Configurable, high sensitivity
	  • Programmable gain and integration time
	  • 1024x dynamic range by gain adjustment only
	  • 1mlux minimum detectable illuminance (100ms)
	• Tailored ALS and color response
	  • UV/IR blocking filter for RGBC channels
	  • Wideband reference channel without filters
	• ALS/color interrupt with thresholds

• Unique fast ALS integration mode	• Flicker-immune ALS sensing within 10ms
• Integrated ambient light flicker detection on chip	• Independently configurable timing and gain • Automatic gain adjustment • 50Hz and 60Hz flicker detection flags • Flicker detected interrupt
• Low power consumption and minimum I^2C traffic	• $1.8V_{DD}$ operation • Configurable sleep mode • Interrupt-driven device • On-chip self-calibration of ALS and proximity functions
• Integrated status checking for all functions	• Digital and analog ALS saturation flags • Proximity saturation flag

Applications

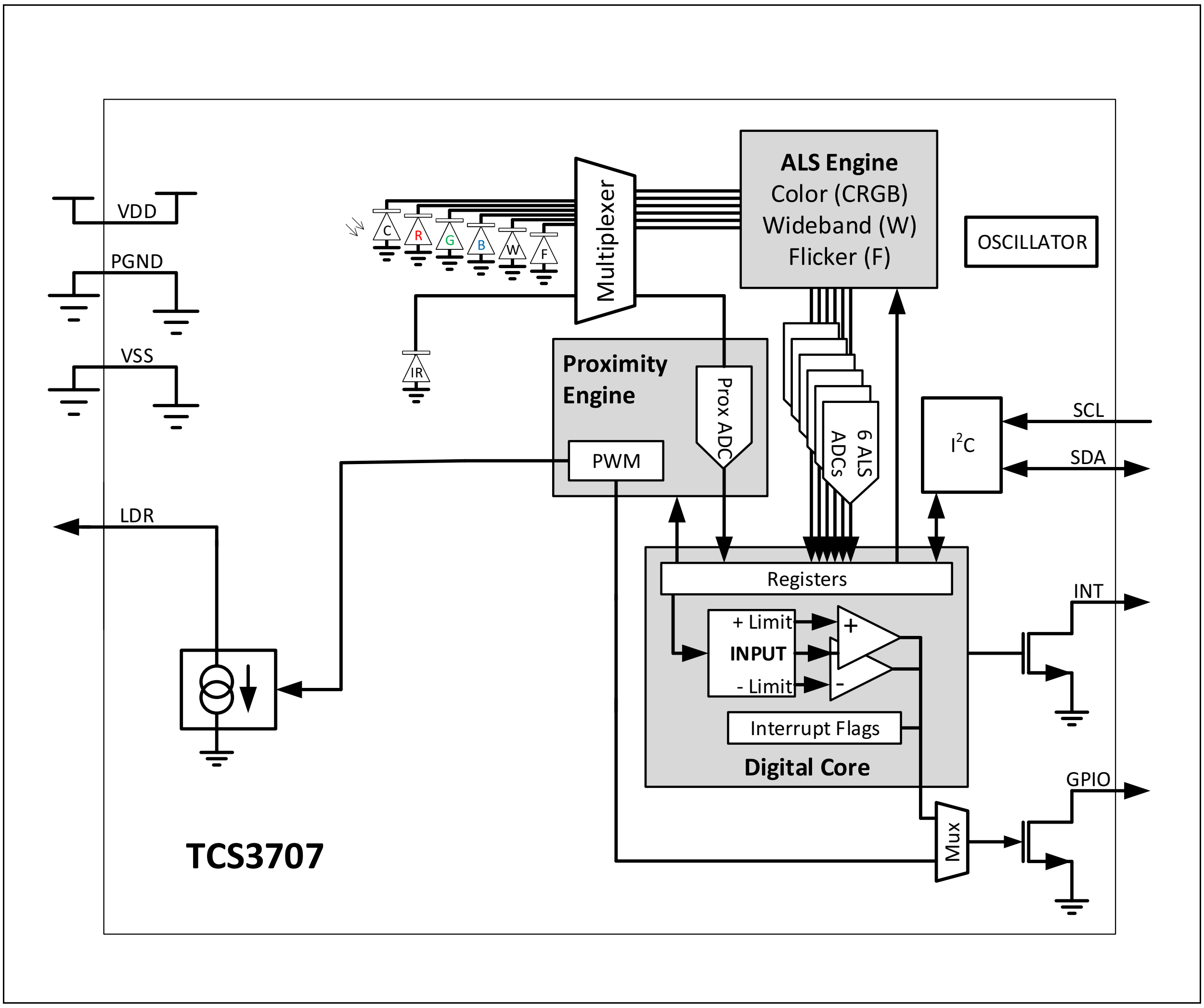
TCS3707 integrates multiple applications within one device. The applications for TCS3707 include:

- Brightness management for displays
- Color management for displays
- Camera image processing
- Flicker-immune camera operation
- Touch screen disable

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of TCS3707



Pin Assignments

Device pinout is described below.

Figure 3:
Pin Diagram of TCS3707

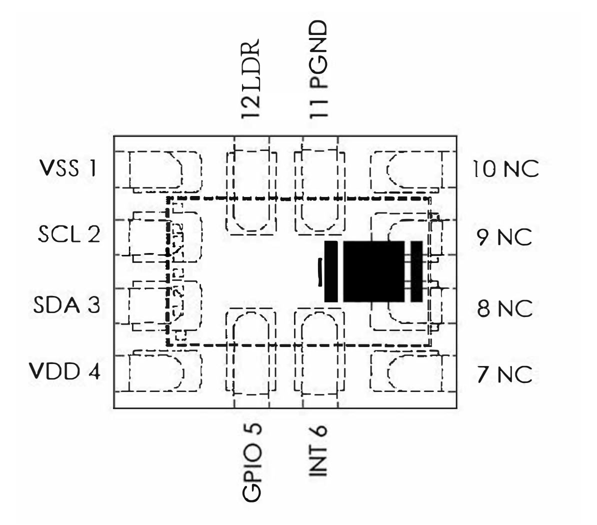


Figure 4:
Pin Description of TCS3707

Pin Number	Pin Name	Description
1	VSS	Ground. All voltages are referenced to VSS/PGND, and both ground pins must be connected to ground.
2	SCL	I²C serial clock terminal
3	SDA	I²C serial data I/O terminal
4	VDD	Supply voltage (1.8V)
5	GPIO	Open-drain general purpose input/output
6	INT	Interrupt. Open-drain output plus supports additional output options.
7	NC	No connect
8	NC	No connect
9	NC	No connect
10	NC	No connect
11	PGND	Ground. All voltages are referenced to VSS/PGND, and both ground pins must be connected to ground.
12	LDR	Connection to internal LED driver. Capable to drive external IR emitter LED or VCSEL. Connect to ground or leave floating if not used.

Note(s):

1. NC pins do not have an internal electrical connection. For device. ESD protection, it is recommended to connect it to ground.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

All voltages with respect to VSS/PGND. Device parameters are guaranteed at V_{DD} = 1.8 V and T_A = 25°C unless otherwise noted.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
V_{DD}	Supply voltage	-0.3	2.2	V	
V_{LDR}	External LED anode supply	-0.3	3.6		
V_{IO}	Digital I/O terminal voltage	-0.3	3.6		
I_{IO}	Output terminal current	-1	20	mA	
Electrostatic Discharge					
ESD_{HBM}	Electrostatic discharge HBM	±2000		V	JEDEC/ESDA JS-001-2014
Temperature Ranges and Storage Conditions					
T_{STRG}	Storage temperature range	-40	85	°C	
T_A	Operating temperature range	-30	85		

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Comments
Electrical Parameters						
V_{DD}	Supply voltage	1.7	1.8	2.0	V	
V_{LDR}	External LED anode supply		3.3		V	
Temperature Ranges and Storage Conditions						
T_A	Operating free-air temperature (1)	-30	25	70	°C	

Note(s):

1. While the device is operational across the temperature range, functionality will vary with temperature.

Optical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. Device parameters are guaranteed with V_{DD} = 1.8 V and T_A = 25°C unless otherwise noted.

Figure 7:
ALS/Color Characteristics of TCS3707, ALS Gain = 128x, Integration Time = 11ms (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Unit
Dark ADC count value (1)	$E_e = 0\mu W/cm^2$ ALS gain: 512x Integration time: 98ms	0	0	3	counts
ALS gain ratios (2)	0.5x		1/256		
	1x		1/128		
	2x		1/64		
	4x		1/32		
	8x		1/16		
	16x		1/8		
	32x		1/4		
	64x		1/2		
	256x		2.05		
	512x		4.29		
	1024x		8.26		
Clear channel irradiance responsivity	White LED, 2700K (3)	53.9	63.4	72.9	counts/ ($\mu W/cm^2$)
Wideband channel irradiance responsivity			23.6		
Lux accuracy (4)	White LED, 2700K (3)	90	100	110	%
ADC noise (5)	White LED, 2700K (3) Integration time: 100ms		0.05		
Red/Clear channel ratios	White LED, 2700K	52		72	%
	Blue LED, λ_D = 465nm(6)	0		20	
	Red LED, λ_D = 615nm(7)	81		111	
Green/Clear channel ratios	White LED, 2700K	21		42	
	Green LED, λ_D = 525nm(8)	63		86	
	Red LED, λ_D = 615nm	0		20	

Parameter	Conditions	Min	Typ	Max	Unit
Blue/Clear channel ratios	White LED, 2700K	1		30	%
	Blue LED, λ_D = 465nm	73		100	
	Red LED, λ_D = 615nm	0		20	
Wideband/Clear channel ratio	White LED, 2700K	33		50	
Wideband/IR channel ratio	IR LED = 940nm (9)	12		22	

Note(s):

1. The typical 3-sigma distribution shows less than 1 count for an ATIME setting of less than 98ms.
2. The ALS gain ratios are calculated relative to ALS gain = 128x and measured with an integration time of 11ms.
3. The White LED is an InGaN light-emitting diode with integrated phosphor and the following characteristic: correlated color temperature = 2700K.
4. Lux accuracy is an illuminance estimated using the red, green, blue, and clear channels and is not 100% production tested.
5. ADC noise is calculated as the standard deviation relative to full scale.
6. The Blue LED is an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 465nm, spectral halfwidth Δλ½ = 22nm.
7. The Red LED is an AlInGaP light-emitting diode with the following characteristics: dominant wavelength λ_D = 615nm, spectral halfwidth Δλ½ = 15nm.
8. The Green LED is an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 525nm, spectral halfwidth Δλ½ = 35nm.
9. The IR Emitter shall be an AlGaAs light-emitting diode with a peak wavelength of λ_P = 940nm.

Figure 8:
Proximity Characteristics of TCS3707

Parameter	Conditions	Min	Typ	Max	Unit
Response, relative variation (1)	PGAIN = 4x PLDRIVE0 = 4mA PPULSE_LEN = 8µs PPULSE = 8 pulse	75	100	125	%

Note(s):

1. Production tested result is the average of 4 readings expressed relative to a calibrated response. Proximity sensor field is directly illuminated with an external IR-emitter LED with a peak wavelength of λ_P = 940nm.

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 9:
Electrical Characteristics of TCS3707, V_{DD} = 1.8 V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD;ALS}$	ALS supply current (1)	Active ALS state (2) (PON=AEN=1, PEN=0)		196	280	µA
$I_{DD;PROX}$	Proximity supply current (1)	Active proximity state (PON=PEN=1, AEN=0)		190	250	
$I_{DD;IDLE}$	Idle current (1)	Idle state (3) (PON=1, AEN=PEN=0)		40	60	
$I_{DD;SLEEP}$	Sleep current (1)	Sleep state (4)		0.7	5	
I_{LEAK}	Leakage current	Measured on SDA, SCL, INT, GPIO	-5		5	
V_{OL}	INT, SDA, GPIO output low voltage	6mA sink current			0.4	V
V_{IH}	SCL, SDA input high voltage		1.26			
V_{IL}	SCL, SDA input low voltage				0.54	
C_I	Input pin capacitance			10		pF

Note(s):

1. Values are shown at the VDD pin and do not include current through the IR LED.
2. This parameter indicates the supply current during periods of ALS integration. The ALS gain setting will have an effect on the active supply current. The ALS gain setting used for this parameter is 128x.
3. Idle state occurs when PON=1 and all functions are disabled. This parameter is measured with LOWPOWER_IDLE=1.
4. Sleep state occurs when PON = 0 and I²C bus is idle. If Sleep state has been entered as the result of operational flow, SAI = 1, PON will remain high.

Timing Characteristics

The timing parameters are specified by design and characterization and are not production tested unless otherwise noted. All parameters are measured with V_{DD} = 1.8 V and T_A = 25°C unless otherwise noted.

Figure 10:
I^2C Timing Characteristics of TCS3707

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	I^2C clock frequency	0		400	kHz
t_{BUF}	Bus free time between start and stop condition	1.3			µs
$t_{HS;STA}$	Hold time after (repeated) start condition. After this period, the first clock is generated	0.6			
$t_{SU;STA}$	Repeated start condition setup time	0.6			
$t_{SU;STO}$	Stop condition setup time	0.6			
t_{LOW}	SCL clock low period	1.3			
t_{HIGH}	SCL clock high period	0.6			
$t_{HD;DAT}$	Data hold time	0			ns
$t_{SU;DAT}$	Data setup time	100			
t_F	Clock/data fall time			300	
t_R	Clock/data rise time			300	

Figure 11:
Timing Diagram for TCS3707

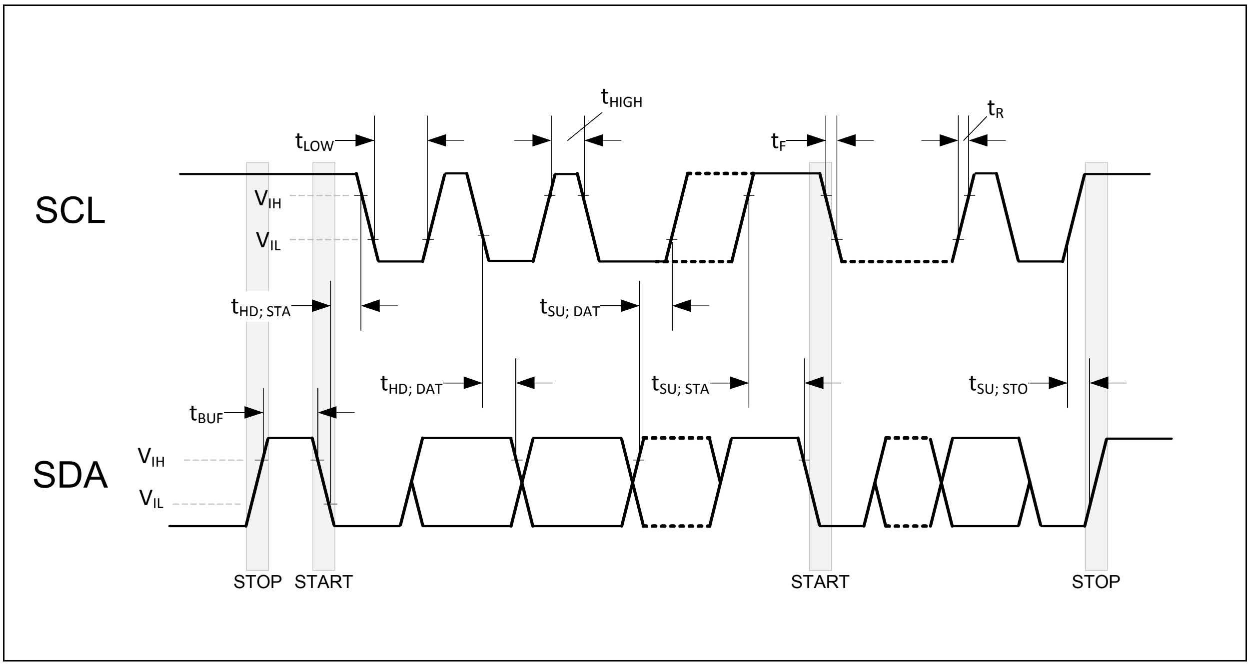


Figure 12:
Functional Timing Characteristics of TCS3707

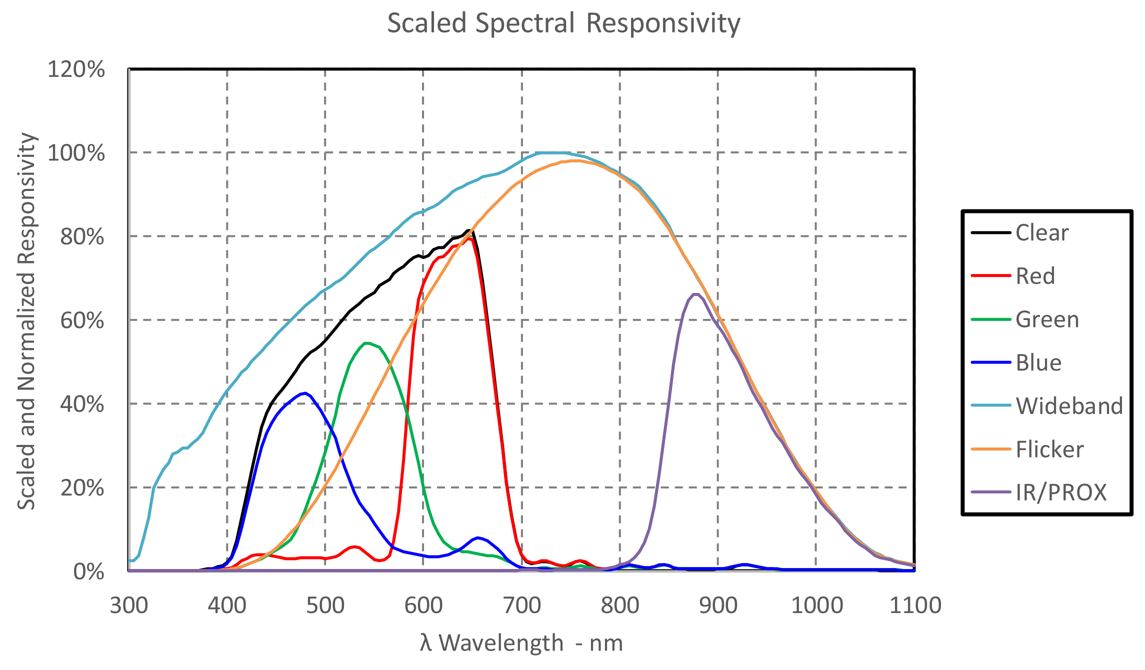
Symbol	Parameter	Min	Typ	Max	Unit
f_{OSC}	Oscillator clock frequency (1)	700	720	740	kHz
t_{OSL}	Oscillator clock cycle (1)	1.35	1.39	1.43	µs
$t_{(PROX\ ADC)}$	Proximity ADC conversion time		20		

Note(s):

1. 100% production tested.

Typical Operating Characteristics

Figure 13:
Spectral Responsivity



Note(s):

1. The spectral responsivities shown in the figure are scaled based on the photodiode area of each channel. The scaling factors used to generate this figure are (relative to CLEAR): 1.7 for WIDEBAND, and 0.28 for FLICKER and IR. Once scaled, the responsivities are normalized.

Figure 14:
Normalized Angular Response

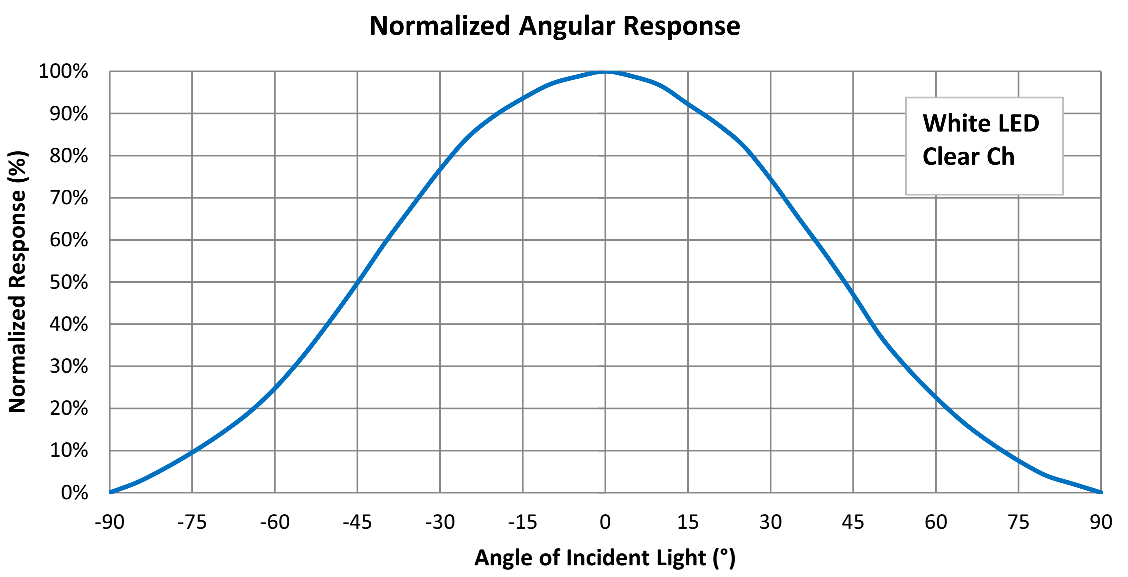


Figure 15:
Responsivity Temperature Coefficient

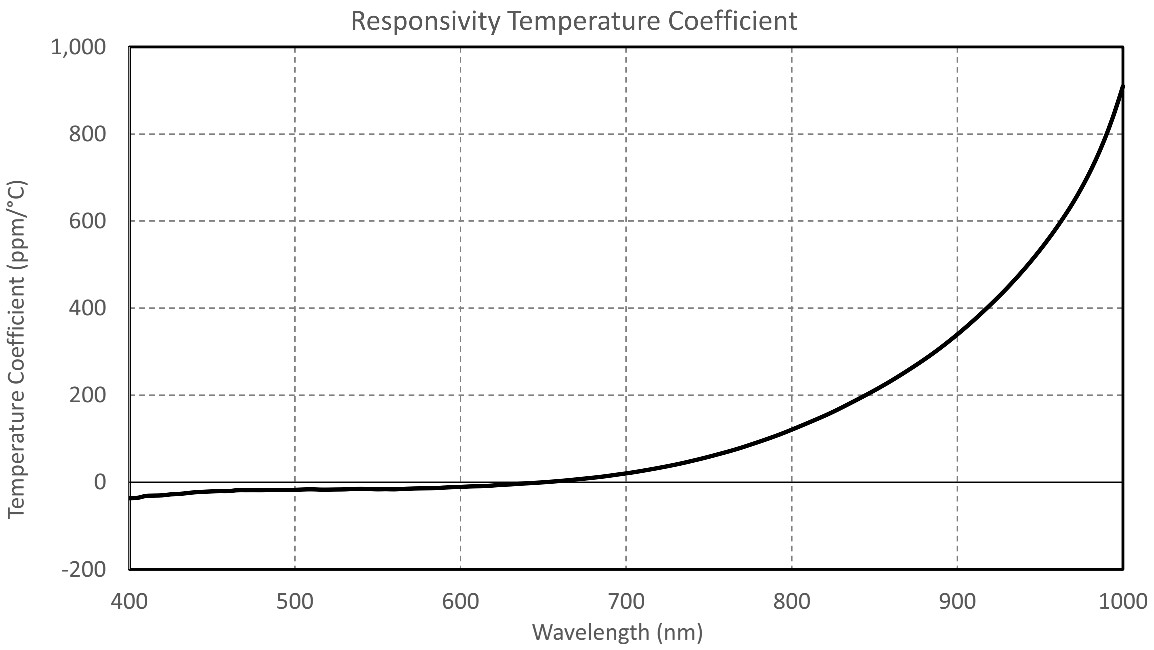


Figure 16:
Illuminance (Lux) vs. Counts (Clear Channel)

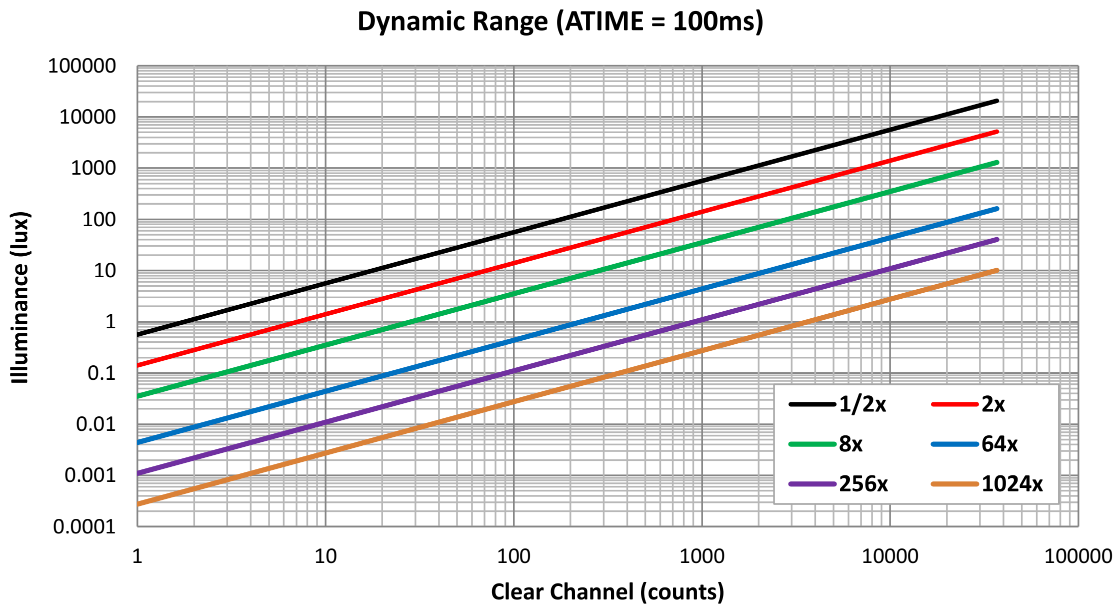
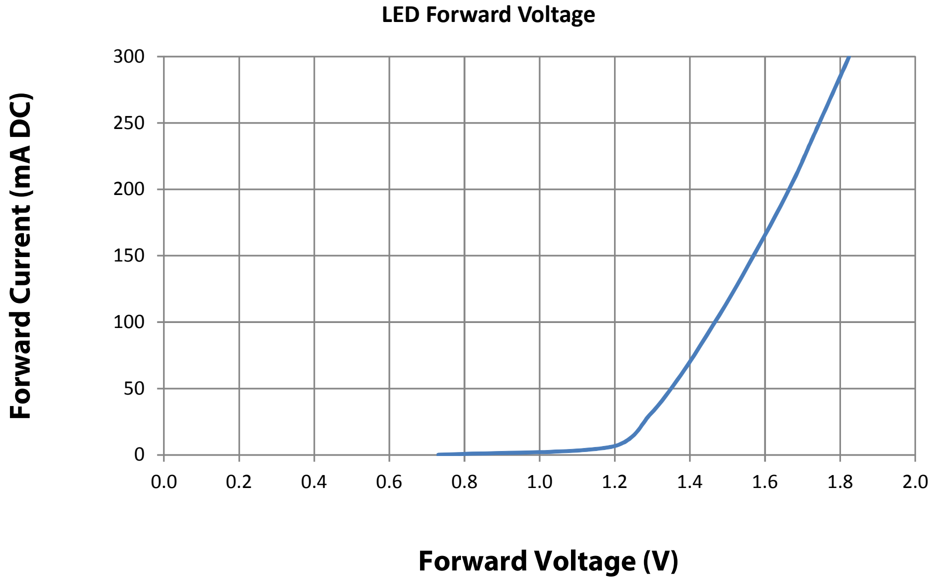


Figure 17:
Recommended 950nm LED Forward Voltage vs. Current



Note(s):

1. The LED supply voltage (V_{LEDA}) must be sufficiently large to guarantee proper operation of the regulated current sink.

Detailed Description

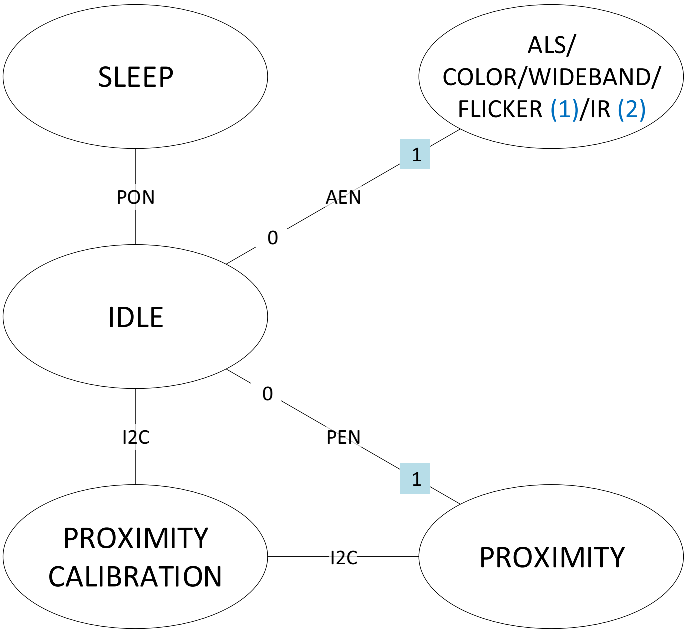
Upon power-up, POR, the device initializes. During initialization (typically 200µs), the device will deterministically send NAK on I^2C and cannot accept I^2C transactions. All communication with the device must be delayed, and all outputs from the device must be ignored including interrupts. After initialization, the device enters the SLEEP state. In this operational state the internal oscillator and other circuitry are not active, resulting in ultra-low power consumption. If an I^2C transaction occurs during this state, the I^2C core wakes up temporarily to service the communication. Once the Power ON bit, PON, is enabled, the device enters the IDLE state in which the internal oscillator and attendant circuitry are active, but power consumption remains low. Whenever a function is enabled (PEN | AEN = 1)the device exits the IDLE state. If all functions are disabled (PEN = 0 & AEN = 0), the device returns to the IDLE state.

As depicted in Figure 18 and Figure 19, the proximity and CRGBW color sensing functions operate in parallel when enabled (CONCURRENT_PROX_AND_ALS = 1). In addition, when proximity calibration is requested, it will temporarily disable the proximity function. Each function is individually configured (e.g. gain, ADC integration time, wait time, persistence, thresholds, etc.).

If Sleep after Interrupt is enabled (SAI = 1 in register 0xAC), the state machine will enter SLEEP when an interrupt occurs. Entering SLEEP does not automatically change any of the register settings (e.g. PON bit is still high, but the normal operational state is over-ridden by SLEEP state). SLEEP state is terminated when the SAI_ACTIVE bit is cleared (the status bit is in register 0xA7 and the clear status bit is in register 0xFA).

State Machine Diagrams

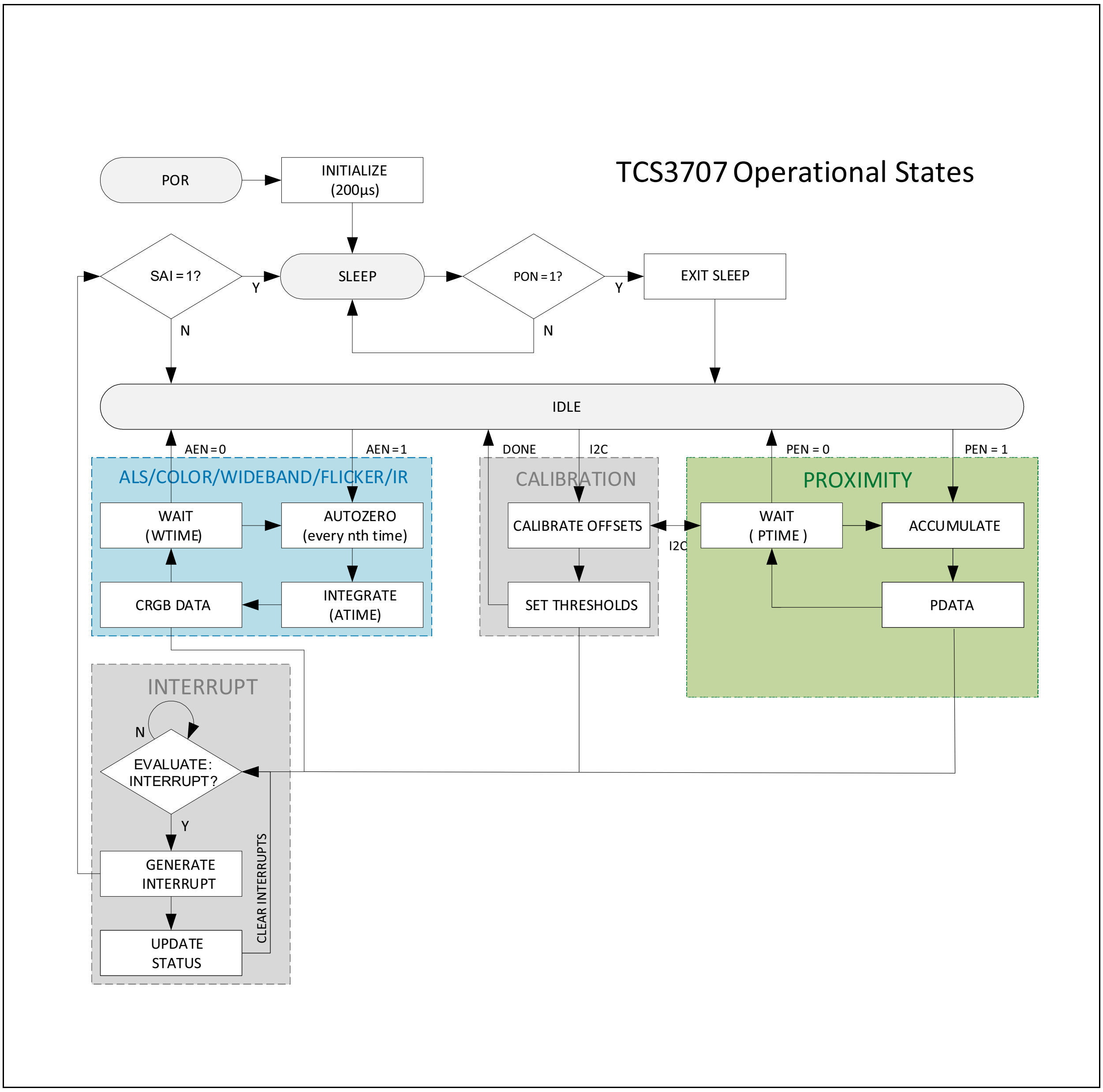
Figure 18:
Simplified State Diagram



Note(s):

1. For flicker detection to work correctly, proximity must be disabled (PEN = 0) during flicker detection data collection or PROX_BEFORE_EACH_ALS must be set to 1.
2. To access the IR channel, proximity must be disabled (PEN = 0), flicker detection must be disabled (FDEN = 0), and SWAP_PROX_ALS5 must be set to 1.

Figure 19:
Detailed State Diagram



I²C Protocol

The device uses I²C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and full-speed clock frequency modes. Read and Write transactions comply with the standard set by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification.

Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (I.e. valid even after the master issues a STOP command and the I²C bus is released). During consecutive Read transactions, the future/repeated I²C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address +1.

All 16-bit fields have a latching scheme for reading and writing. In general it is recommended to use I²C bursts whenever possible, especially in this case when accessing two bytes of one logical entity. When reading these fields, the low byte must be read first, and it triggers a 16-bit latch that stores the 16-bit field. The high byte must be read immediately afterwards. When writing to these fields, the low byte must be written first, immediately followed by the high byte. Reading or writing to these registers without following these requirements will cause errors.

A Write transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS WRITE, DATA BYTE(S), and STOP. Following each byte (9TH clock pulse) the slave places an ACKNOWLEDGE/NOT- ACKNOWLEDGE (ACK/NACK) on the bus. If NACK is transmitted by the slave, the master may issue a STOP.

A Read transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS, RESTART, CHIP-ADDRESSREAD, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9TH clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

Register Overview

The device is controlled and monitored by registers accessed through the I^2C serial interface. These registers provide device control functions and are read to determine device status and acquire device data.

Register Map

The register set is summarized in Figure 20. The values of all registers and fields that are listed as reserved or are not listed must not be changed at any time. The power-on reset values of each bit are indicated in these columns. Two-byte fields are always latched with the low byte followed by the high byte.

Figure 20:
Register Map

Addr	Name	Type	Description	Reset
0x80	ENABLE	R/W	Enable device states	0x00
0x81	ATIME	R/W	ALS integration time	0x00
0x82	PTIME	R/W	Proximity time	0x00
0x83	WTIME	R/W	Wait time	0x00
0x84	AILT	R/W	ALS interrupt low threshold	0x00
0x85				0x00
0x86	AIHT	R/W	ALS interrupt high threshold	0x00
0x87				0x00
0x88	PILT0	R/W	Proximity interrupt low threshold zero	0x00
0x89				0x00
0x8A	PILT1	R/W	Proximity interrupt low threshold one	0x00
0x8B				0x00
0x8C	PIHT0	R/W	Proximity high threshold zero	0x00
0x8D				0x00
0x8E	PIHT1	R/W	Proximity high threshold one	0x00
0x8F				0x00
0x90	AUXID	R	Auxiliary identification	0x02
0x91	REVID	R	Revision identification	0x11
0x92	ID	R	Device identification	0x18
0x93	STATUS	R/W	Device status one	0x00
0x94	ASTATUS	R	ALS status	0x00

Addr	Name	Type	Description	Reset
0x95	ADATA0	R	ALS channel zero data	0x00
0x96				0x00
0x97	ADATA1	R	ALS channel one data	0x00
0x98				0x00
0x99	ADATA2	R	ALS channel two data	0x00
0x9A				0x00
0x9B	ADATA3	R	ALS channel three data	0x00
0x9C				0x00
0x9D	ADATA4	R	ALS channel four data	0x00
0x9E				0x00
0x9F	ADATA5	R	ALS channel five data	0x00
0xA0				0x00
0xA1	PDATA	R	Proximity data	0x00
0xA2				0x00
0xA3	STATUS2	R/W	Device status two	0x00
0xA4	STATUS3	R/W	Device status three	0x08
0xA5	STATUS4	R/W	Device status four	0x00
0xA6	STATUS5	R/W	Device status five	0x00
0xA7	STATUS6	R/W	Device status six	0x00
0xA9	CFG0	R/W	Configuration zero	0x00
0xAA	CFG1	R/W	Configuration one	0x09
0xAC	CFG3	R/W	Configuration three	0x0C
0xAD	CFG4	R/W	Configuration four	0x00
0xAF	CFG6	R/W	Configuration six	0x00
0xB1	CFG8	R/W	Configuration eight	0x80
0xB2	CFG9	R/W	Configuration nine	0x00
0xB3	CFG10	R/W	Configuration ten	0xF2
0xB4	CFG11	R/W	Configuration eleven	0x40
0xB5	CFG12	R/W	Configuration twelve	0x00
0xB7	CFG14	R/W	Configuration fourteen	0x00

Addr	Name	Type	Description	Reset
0xB8	PCFG1	R/W	Proximity configuration one	0x00
0xB9	PCFG2	R/W	Proximity configuration two	0x00
0xBB	PCFG4	R/W	Proximity configuration four	0x02
0xBC	PCFG5	R/W	Proximity configuration five	0x4F
0xBD	PERS	R/W	Persistence configuration	0x00
0xBE	GPIO	R/W	GPIO configuration	0x02
0xC7	POFFSET	R/W	Proximity offset	0x00
0xC8				0x00
0xCA	ASTEP	R/W	ALS integration step size	0xE7
0xCB				0x03
0xCF	AGC_GAIN_MAX	R/W	Maximum AGC gains	0x99
0xD0	PXAVG	R/W	Proximity average	0x00
0xD1				0x00
0xD2	PBSLN	R/W	Proximity baseline	0x00
0xD3				0x00
0xD6	AZ_CONFIG	R/W	Autozero configuration	0xFF
0xDB	FD_STATUS	R	Flicker detection configuration zero	0x00
0xEA	CALIB	R/W	Calibration start	0x00
0xEB	CALIBCFG0	R/W	Calibration configuration zero	0x00
0xEC	CALIBCFG1	R/W	Calibration configuration one	0x0C
0xED	CALIBCFG2	R/W	Calibration configuration two	0x00
0xEE	CALIBSTAT	R/W	Calibration status	0x00
0xF9	INTENAB	R/W	Enable interrupts	0x00
0xFA	CONTROL	R/W	Control	0x00

Register Descriptions

Power, Enable, and Operation

The enable register has fields that power on the device and enable the functions. To operate the device, first set all configuration fields for all functions, then set PON = 1, and finally enable functions. Changing configuration register values while functions are operating may result in invalid results. PEN, and AEN require PON to be asserted for each respective function to operate correctly. When PEN, or AEN are asserted, the visible bit is only updated when the state machine has completed the process of enabling the associated function.

Figure 21:
ENABLE

Addr: 0x80		ENABLE		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	Reserved	0		
6	FDEN	0	R/W	**Flicker Detection Enable.** Writing a 1 activates flicker detection. Writing a 0 disables flicker detection.
5:4	Reserved	0		
3	WEN	0	R/W	**Wait Enable.** Writing a 1 activates the wait timer. Writing a 0 disables the wait timer.
2	PEN	0	R/W	**Proximity Enable.** Writing a 1 enables proximity. Writing a 0 disables proximity.
1	AEN	0	R/W	**ALS Enable.** Writing a 1 enables ALS/Color. Writing a 0 disables ALS/Color.
0	PON	0	R/W	**Power ON.** When asserted, the internal oscillator is activated, allowing timers and ADC channels to operate. Writing a 0 disables the oscillator and clears PEN, and AEN. Only set this bit after all other registers have been initialized by the host.

Note(s):

1. Return to the Register Map (0x80).

Figure 22:
CALIB

Addr: 0xEA		CALIB		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:1	Reserved	0		
0	START_OFFSET_CALIB	0	PUSH	**Start Offset Calibration.** Starts the proximity offset register calibration routine. Results are stored in the Proximity Offset Registers (0xC7 – 0xC8). The CALIB_FINISHED flag is asserted when calibration is complete and an interrupt (CINT) is asserted if CIEN is set. Calibration can be stopped immediately by writing a 0 to this field.

Note(s):

1. Return to the Register Map (0xEA).

Figure 23:
INTENAB

Addr: 0xF9		INTENAB		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	ASIEN	0	R/W	**ALS and Flicker Detect Saturation Interrupt Enable.** When asserted permits ALS saturation interrupts to be generated.
6	PSIEN	0	R/W	**Proximity Saturation Interrupt Enable.** When asserted permits proximity saturation interrupts to be generated.
5	PIEN1	0	R/W	**Proximity Interrupt One Enable.** When asserted permits proximity one interrupts to be generated, subject to the proximity thresholds and persistence filter.
4	PIEN0	0	R/W	**Proximity Interrupt Zero Enable.** When asserted permits proximity zero interrupts to be generated, subject to the proximity thresholds and persistence filter.
3	AIEN	0	R/W	**ALS Interrupt Enable.** When asserted permits ALS interrupts to be generated, subject to the ALS thresholds and persistence filter.
2	Reserved	0		
1	CIEN	0	R/W	**Calibration Interrupt Enable.** When asserted permits calibration interrupts to be generated.
0	SIEN	0	R/W	**System Interrupt Enable.** When asserted permits system interrupts to be generated. Indicates that flicker detection status has changed.

Note(s):

1. Return to the Register Map (0xF9).

Figure 24:
CONTROL

Addr: 0xFA		CONTROL		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:3	Reserved	0		
2	ALS_MANUAL_AZ	0	R/W	**ALS Manual Autozero.** Starts a manual autozero of the ALS engines. Set AEN = 0 before starting a manual autozero for it to work.
1	Reserved	0		
0	CLEAR_SAI_ACTIVE	0	R/W	**Clear Sleep-After-Interrupt Active.** Clears SAI_ACTIVE, ends sleep, and restarts device operation.

Note(s):

1. Return to the Register Map (0xFA).

Identification

The identification registers provide auxiliary identification for special cases, wafer revision data, and device identification. All identification registers are read only.

Figure 25:
Identification Registers

Bits	Addr	Field	Description
7:0	0x90	AUXID	Auxiliary Identification (0x02)
7:0	0x91	REVID	Revision Identification (0x11)
7:0	0x92	ID	Device Identification (0x18)

Note(s):

1. Return to the Register Map (0x90, 0x91, 0x92).

ALS Configuration

The ALS/color integration time is set using the ATIME field and ASTEP field (ASTEP register). The ALS integration time, in milliseconds, is equal to (ATIME + 1) × (ASTEP + 1) / 360. The reset value for ASTEP is 999 (2.78ms), and the recommended configuration for these two fields is ASTEP = 599 and ATIME = 29, which results in an integration time of 50ms. The ALS integration time also establishes the full scale ADC range, which is equal to (ATIME + 1) × (ASTEP + 1).

If wait is enabled (WEN = 1), each new ALS sample is started based on WTIME. It is necessary for WTIME to be sufficiently large for ALS integration and any other functions to be completed within the time frame. The device will warn the user if the timing is configured incorrectly. If WTIME is too short, then ALS_TRIGGER_ERROR will be 1.

Figure 26:
ATIME

<table>
<tr><th colspan="2">Addr: 0x81</th><th colspan="4">ATIME</th></tr>
<tr><th>Bit</th><th>Field</th><th>Reset</th><th>Type</th><th colspan="2">Description</th></tr>
<tr><td rowspan="5">7:0</td><td rowspan="5">ATIME</td><td rowspan="5">0x00</td><td rowspan="5">R/W</td><td colspan="2">ALS Integration Time. Sets the number of ALS/color integration steps from 1 to 256.</td></tr>
<tr><td>VALUE</td><td>INTEGRATION TIME</td></tr>
<tr><td>0</td><td>ASTEP</td></tr>
<tr><td>n</td><td>ASTEP × (<i>n</i>+1)</td></tr>
<tr><td>255</td><td>256 × ASTEP</td></tr>
</table>

Note(s):

1. Return to the Register Map (0x81).

Figure 27:
ASTEP

Addr: 0x82		ASTEP		
Bits	**Field**	**Reset**	**Description**	
7:0	ASTEP	0xE7	**ALS Integration Time Step Size.** Sets the integration time per step in increments of 2.78µs. The default value is 999. Type is read/write.	
15:8		0x03	**VALUE**	**STEP SIZE**
			0	2.78µs
			n	2.78µs × (n+1)
			599	1.67ms
			999	2.78ms
			17999	50ms
			65535	182ms

Note(s):

1. Return to the Register Map (0xCA, 0xCB).

Figure 28:
WTIME

Addr: 0x83		WTIME			
Bit	**Field**	**Reset**	**Type**	**Description**	
7:0	WTIME	0x00	R/W	**Wait Time.** Sets the sample rate of the ALS/color function.	
				VALUE	**TIME**
				0	2.78ms
				n	2.78ms × (n+1)
				255	711ms

Note(s):

1. Return to the Register Map (0x83).

ALS level detection uses data generated by the ADC Channel X. The channel can be selected via ALS_TH_CHANNEL (see CFG12).The ALS Interrupt Threshold registers provide 16-bit values to be used as the high and low thresholds for comparison to the 16-bit ADATAX values. If AIEN is enabled and ADATAX is not between AILT and AIHT for the number of consecutive samples specified in APERS an interrupt is asserted on the interrupt pin. These registers are read/write.

Figure 29:
ALS Interrupt Thresholds

Bits	Addr	Field	Description
7:0	0x84	AILT	ALS Interrupt Low Threshold
15:8	0x85		
7:0	0x86	AIHT	ALS Interrupt High Threshold
15:8	0x87		

Note(s):

1. Return to the Register Map (0x84, 0x85, 0x86, 0x87).

Figure 30:
CFG1

<table>
<tr><th colspan="2">Addr: 0xAA</th><th colspan="4">CFG1</th></tr>
<tr><th>Bit</th><th>Field</th><th>Reset</th><th>Type</th><th colspan="2">Bit Description</th></tr>
<tr><td>7:5</td><td>Reserved</td><td>0</td><td></td><td colspan="2"></td></tr>
<tr><td rowspan="14">4:0</td><td rowspan="14">AGAIN</td><td rowspan="14">9</td><td rowspan="14">R/W</td><td colspan="2">ALS Gain. Sets the ALS sensitivity.</td></tr>
<tr><td>VALUE</td><td>GAIN</td></tr>
<tr><td>0</td><td>0.5x</td></tr>
<tr><td>1</td><td>1x</td></tr>
<tr><td>2</td><td>2x</td></tr>
<tr><td>3</td><td>4x</td></tr>
<tr><td>4</td><td>8x</td></tr>
<tr><td>5</td><td>16x</td></tr>
<tr><td>6</td><td>32x</td></tr>
<tr><td>7</td><td>64x</td></tr>
<tr><td>8</td><td>128x</td></tr>
<tr><td>9</td><td>256x</td></tr>
<tr><td>10</td><td>512x</td></tr>
<tr><td>11</td><td>1024x</td></tr>
</table>

Note(s):

1. Return to the Register Map (0xAA).

Figure 31:
CFG10

<table>
<tr><th colspan="2">Addr: 0xB3</th><th colspan="4">CFG10</th></tr>
<tr><th>Bit</th><th>Field</th><th>Reset</th><th>Type</th><th colspan="2">Bit Description</th></tr>
<tr><td rowspan="6">7:6</td><td rowspan="6">ALS_AGC_HIGH_HYST</td><td rowspan="6">3</td><td rowspan="6">R/W</td><td colspan="2">ALS AGC High Hysteresis. Sets the ALS data threshold at which AGAIN is reduced when ALS AGC mode is enabled. The threshold is automatically calculated internally as a percentage of full-scale. Note that full-scale is equal to (ATIME + 1) × (ASTEP + 1).</td></tr>
<tr><td>VALUE</td><td>SIGNAL</td></tr>
<tr><td>0</td><td>50%</td></tr>
<tr><td>1</td><td>62.5%</td></tr>
<tr><td>2</td><td>75%</td></tr>
<tr><td>3</td><td>87.5%</td></tr>
<tr><td rowspan="6">5:4</td><td rowspan="6">ALS_AGC_LOW_HYST</td><td rowspan="6">3</td><td rowspan="6">R/W</td><td colspan="2">ALS AGC Low Hysteresis. Sets the ALS data threshold at which AGAIN is increased when ALS AGC mode is enabled. The threshold is automatically calculated internally as a percentage of full-scale. Note that full-scale is equal to (ATIME + 1) × (ASTEP + 1).</td></tr>
<tr><td>VALUE</td><td>SIGNAL</td></tr>
<tr><td>0</td><td>12.5%</td></tr>
<tr><td>1</td><td>25%</td></tr>
<tr><td>2</td><td>37.5%</td></tr>
<tr><td>3</td><td>50%</td></tr>
<tr><td>3</td><td>Reserved</td><td>0</td><td></td><td colspan="2"></td></tr>
<tr><td>2:0</td><td>FD_PERS</td><td>2</td><td>R/W</td><td colspan="2">Flicker Detect Persistence. Sets the number of consecutive flicker detect results that must be different before the flicker detect status will be changed. Flicker detection interrupts on SINT are affected by this setting. Flicker detect persistence is equal to $2^{(FD\_PERS - 1)}$.</td></tr>
</table>

Note(s):

1. Return to the Register Map (0xB3).

Figure 32:
CFG12

<table>
<tr><th colspan="2">Addr: 0xB5</th><th colspan="5">CFG12</th></tr>
<tr><th>Bit</th><th>Field</th><th>Reset</th><th>Type</th><th colspan="3">Bit Description</th></tr>
<tr><td>7:3</td><td>Reserved</td><td>0</td><td></td><td colspan="3"></td></tr>
<tr><td rowspan="7">2:0</td><td rowspan="7">ALS_TH_CHANNEL</td><td rowspan="7">0</td><td rowspan="7">R/W</td><td colspan="3">ALS Thresholds Channel. Sets the channel used by interrupts, persistence, and the ALS AGC, if enabled, to determine device status and ALS gain settings.</td></tr>
<tr><td>VALUE</td><td>CHANNEL</td><td>DEFAULT</td></tr>
<tr><td>0</td><td>0</td><td>CLEAR</td></tr>
<tr><td>1</td><td>1</td><td>RED</td></tr>
<tr><td>2</td><td>2</td><td>GREEN</td></tr>
<tr><td>3</td><td>3</td><td>BLUE</td></tr>
<tr><td>4</td><td>4</td><td>WIDEBAND</td></tr>
</table>

Note(s):

1. Return to the Register Map (0xB5).

ALS autozero configuration is used to set how often the ALS engine offsets are reset to compensate for changes in device temperature.

Figure 33:
AZ_CONFIG

<table>
<tr><th colspan="2">Addr: 0xD6</th><th colspan="4">AZ_CONFIG</th></tr>
<tr><th>Bit</th><th>Field</th><th>Reset</th><th>Type</th><th colspan="2">Bit Description</th></tr>
<tr><td rowspan="9">7:0</td><td rowspan="9">AZ_NTH_ITERATION</td><td rowspan="9">255</td><td rowspan="9">R/W</td><td colspan="2">ALS Autozero Frequency. Sets the frequency at which the device performs autozero of the ALS pulse counter.</td></tr>
<tr><td>VALUE</td><td>AUTOZERO FREQUENCY</td></tr>
<tr><td>0</td><td>Never</td></tr>
<tr><td>1</td><td>Every cycle</td></tr>
<tr><td>2</td><td>Every 2 cycles</td></tr>
<tr><td>…</td><td>Every <i>(AZ_NTH_ITERATION)</i> cycles</td></tr>
<tr><td>253</td><td>Every 253 cycles</td></tr>
<tr><td>254</td><td>Every 254 cycles</td></tr>
<tr><td>255</td><td>Only once (before 1st cycle)</td></tr>
</table>

Note(s):

1. Return to the Register Map (0xD6).

Figure 34:
AGC_GAIN_MAX

Addr: 0xCF		AGC_GAIN_MAX		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	AGC_FD_GAIN_MAX	9	R/W	**Flicker Detection AGC Gain Max.** Sets the maximum gain for flicker detection to $2^{(AGC\_FD\_GAIN\_MAX - 1)}$. Reset value is 9 (256x). This field has a range from 0 (0.5x) to 11 (1024x).
3:0	AGC_AGAIN_MAX	9	R/W	**ALS AGC Gain Max.** Sets the maximum gain for the ALS AGC engine to $2^{(AGC\_AGAIN\_MAX - 1)}$. Reset value is 9 (256x). This field has a range from 0 (0.5x) to 11 (1024x).

Note(s):

1. Return to the Register Map (0xCF).

Proximity Configuration

Proximity can be executed with its own sample rate independent of and parallel to ALS/color integration. However, ambient flicker detection will not be valid if proximity occurs during flicker data collection. If ambient flicker detection is enabled, it is recommended to assert the PROX_BEFORE_EACH_ALS field. In this case, PTIME is ignored and the proximity state is executed before each ALS/color cycle. If PTIME is too short for the number of pulses and pulse length configured for proximity, PROX_TRIGGER_ERROR will be 1.

Figure 35:
PTIME

<table>
<tr><th colspan="2">Addr: 0x82</th><th colspan="4">PTIME</th></tr>
<tr><th>Bit</th><th>Field</th><th>Reset</th><th>Type</th><th colspan="2">Description</th></tr>
<tr><td rowspan="5">7:0</td><td rowspan="5">PTIME</td><td rowspan="5">0x00</td><td rowspan="5">R/W</td><td colspan="2">Proximity Sample Time. Sets the sample rate of proximity.</td></tr>
<tr><td>VALUE</td><td>TIME</td></tr>
<tr><td>0</td><td>2.78ms</td></tr>
<tr><td>n</td><td>2.78ms × (<i>n</i>+1)</td></tr>
<tr><td>255</td><td>711ms</td></tr>
</table>

Note(s):

1. Return to the Register Map (0x82).

The Proximity Interrupt Threshold Registers set the high and low trigger points for the comparison function which generates an interrupt. Interrupt generation is subject to the value set in persistence filter (PPERS). These registers are read/write.

Figure 36:
Proximity Interrupt Thresholds

Bits	Addr	Field	Description
7:0	0x88	PILT0	Proximity Interrupt Low Threshold Zero
15:8	0x89		
7:0	0x8A	PILT1	Proximity Interrupt Low Threshold One
15:8	0x8B		
7:0	0x8C	PIHT0	Proximity Interrupt High Threshold Zero
15:8	0x8D		
7:0	0x8E	PIHT1	Proximity Interrupt High Threshold One
15:8	0x8F		

Note(s):

1. Return to the Register Map (0x88, 0x89, 0x8A, 0x8B, 0x8C, 0x8D, 0x8E, 0x8F).

The proximity configuration registers include fields used to control proximity operation.

Figure 37:
CFG14

Addr: 0xB7		CFG14		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	Reserved	0		
6	AUTO_CO_CAL_EN	0	R/W	**Automatic Coarse Calibration Enable.** If asserted, the coarse offset range is calibrated automatically.
5	EN_PRX_OFFSET_RANGE	0	R/W	**Coarse Offset Range Enable.** If asserted, the coarse offset range is enabled.
4:0	PRX_OFFSET_COARSE	0	R/W	**Proximity Offset Range.** If AUTO_CO_CAL_EN and EN_PRX_OFFSET_RANGE are enabled, the offset range is set automatically and can be read here. If they are not enabled, the user programs the offset range here.

Note(s):

1. Using features described in CFG14 may lead to malfunction if not properly applied. Please contact **ams** application support for help.
2. Return to the Register Map (0xB7).

Figure 38:
PCFG1

<table>
<tr><th colspan="2">Addr: 0xB8</th><th colspan="4">PCFG1</th></tr>
<tr><th>Bit</th><th>Field</th><th>Reset</th><th>Type</th><th colspan="2">Bit Description</th></tr>
<tr><td>7</td><td>HXTALK_MODE2</td><td>0</td><td>R/W</td><td colspan="2">High Crosstalk Mode. If asserted, the proximity engine uses a 10-bit output mode intended for extremely high optical crosstalk systems. HXTALK_MODE1 and HXTALK_MODE2 must both be asserted for this function to work.</td></tr>
<tr><td>6:3</td><td>Reserved</td><td>0</td><td></td><td colspan="2"></td></tr>
<tr><td>2</td><td>PROX_FILTER_DOWNSAMPLE</td><td>0</td><td>R/W</td><td colspan="2">Proximity Filter Downsample. Sets how often proximity results are checked for interrupts and persistence when PROX_FILTER is enabled.</td></tr>
<tr><td rowspan="6">1:0</td><td rowspan="6">PROX_FILTER</td><td rowspan="6">0</td><td rowspan="6">R/W</td><td colspan="2">Proximity Filter. Selects the filter size for proximity, <i>n</i>. The average is a moving window of length <i>n</i>, and the result is updated and used either every cycle (PROX_FILTER_DOWNSAMPLE = 0) or every <i>n</i> cycles (PROX_FILTER_DOWNSAMPLE = 1).</td></tr>
<tr><td>VALUE</td><td>FILTER LENGTH</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>1</td><td>2</td></tr>
<tr><td>2</td><td>4</td></tr>
<tr><td>3</td><td>8</td></tr>
</table>

Note(s):

1. Return to the Register Map (0xB8).

Figure 39:
PCFG2

<table>
<tr><th colspan="2">Addr: 0xB9</th><th colspan="4">PCFG2</th></tr>
<tr><th>Bit</th><th>Field</th><th>Reset</th><th>Type</th><th colspan="2">Bit Description</th></tr>
<tr><td>7</td><td>Reserved</td><td>0</td><td></td><td colspan="2"></td></tr>
<tr><td rowspan="7">6:0</td><td rowspan="7">PLDRIVE0</td><td rowspan="7">0</td><td rowspan="7">R/W</td><td colspan="2">Proximity LED Drive Strength Zero. Configures nominal LED current used for an internal proximity measurement linearly in steps of 2mA (actual current depends on factory-configuration of LED drive strength). The LED drive strength is equal to 2 × PLDRIVE0 + 4.</td></tr>
<tr><td>VALUE</td><td>LED STRENGTH</td></tr>
<tr><td>0</td><td>4mA</td></tr>
<tr><td>1</td><td>6mA</td></tr>
<tr><td>…</td><td>2mA × PLDRIVE0 + 4mA</td></tr>
<tr><td>126</td><td>256mA</td></tr>
<tr><td>127</td><td>258mA</td></tr>
</table>

Note(s):

1. If PLDRIVE0_HALF bit is asserted, the LED drive current is divided by 2.
2. Return to the Register Map (0xB9).

Figure 40:
PCFG4

Addr: 0xBB		PCFG4		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	Reserved	0		
3	PLDRIVE0_HALF	0	R/W	If asserted the LED drive current set by PLDRIVE0 is divided by 2.
2	Reserved	0		

Addr: 0xBB		PCFG4			
Bit	**Field**	**Reset**	**Type**	**Bit Description**	
1:0	PGAIN	2	R/W	**Proximity Gain Control.** Sets the proximity sensitivity gain.	
				VALUE	**PROXIMITY GAIN**
				0	1x
				1	2x
				2	4x
				3	8x

Note(s):

1. Return to the Register Map (0xBB).

Figure 41:
PCFG5

Addr: 0xBC		PCFG5			
Bit	**Field**	**Reset**	**Type**	**Bit Description**	
7:6	PPULSE_LEN	1	R/W	**Proximity Pulse Length.** Sets the proximity pulse length.	
				VALUE	**PULSE LENGTH**
				0	4µs
				1	8µs
				2	16µs
				3	32µs
5:0	PPULSE	15	R/W	**Proximity Pulse Count.** Specifies the maximum number of proximity pulses per sample. The pulse count can be set between 1 and 64 pulses. The number of pulses is equal to PPULSE + 1.	

Note(s):

1. Return to the Register Map (0xBC).

Proximity offset values have a range of ±255 and are expressed as 9-bit two's-complement values. Only the lower 9 bits are significant, but the high byte must only be programmed with values of 0x00 (indicates that the low byte has a positive value) or 0xFF (indicates that the low byte has a negative value). These registers are read/write.

Figure 42:
Proximity Offset

Bits	Addr	Field	Description
7:0	0xC7	POFFSET	Proximity Offset
15:8	0xC8		

Note(s):

1. Return to the Register Map (0xC7, 0xC8).

Figure 43:
CALIBCFG0

<table>
<tr><th colspan="2">Addr: 0xEB</th><th colspan="4">CALIBCFG0</th></tr>
<tr><th>Bit</th><th>Field</th><th>Reset</th><th>Type</th><th colspan="2">Bit Description</th></tr>
<tr><td>7</td><td>DCAVG_AUTO_BSLN</td><td>0</td><td>R/W</td><td colspan="2">DC Averaging Automatic Baseline. Load the DC average calculated during offset calibration into the PBSLN registers at the end of calibration. Note that if the offset is adjusted (by zero detection) during the DC averaging, the average may be incorrect.</td></tr>
<tr><td>6</td><td>DCAVG_AUTO_OFFSET_ ADJUST</td><td>0</td><td>R/W</td><td colspan="2">DC Averaging Auto Offset Adjust. If set, then during DC averaging, whenever an ADC measurement is zero, the appropriate offset register will be decreased and the OFFSET_ADJUSTED flag is set. Note also that DC averaging is not automatically restarted when this happens, so the calculated baseline might be wrong. Software could restart averaging in this case.</td></tr>
<tr><td>5:4</td><td>Reserved</td><td>0</td><td></td><td colspan="2"></td></tr>
<tr><td>3</td><td>BINSRCH_SKIP</td><td>0</td><td>R/W</td><td colspan="2">Binary Search Skip. When asserted the calibration routine will skip the binary search step. It is useful if zeroes are detected during the DC averaging process to manually reset the baseline and reduce the likelihood of zero counts.</td></tr>
<tr><td rowspan="8">2:0</td><td rowspan="8">DCAVG_ITERATIONS</td><td rowspan="8">0</td><td rowspan="8">R/W</td><td colspan="2">DC Averaging Iterations. Sets the number of proximity results during calibration that are averaged after the binary search is complete. During this period, whenever a result is zero, the appropriate offset register is automatically decremented.</td></tr>
<tr><td>VALUE</td><td>ITERATIONS</td></tr>
<tr><td>0</td><td>Skip</td></tr>
<tr><td>1</td><td>2</td></tr>
<tr><td>2</td><td>4</td></tr>
<tr><td>…</td><td>$2^{DCAVG\_ITERATIONS}$</td></tr>
<tr><td>6</td><td>64</td></tr>
<tr><td>7</td><td>128</td></tr>
</table>

Note(s):

1. Return to the Register Map (0xEB).

Figure 44:
CALIBCFG1

<table>
<tr><th colspan="2">Addr: 0xEC</th><th colspan="4">CALIBCFG1</th></tr>
<tr><th>Bit</th><th>Field</th><th>Reset</th><th>Type</th><th colspan="2">Bit Description</th></tr>
<tr><td>7</td><td>Reserved</td><td>0</td><td></td><td colspan="2"></td></tr>
<tr><td>6</td><td>PROX_AUTO_OFFSET_ ADJUST</td><td>0</td><td>R/W</td><td colspan="2">Proximity Auto Offset Adjust. During proximity mode, if set, whenever an ADC measurement is zero, the appropriate offset register will be decreased. If this happens, OFFSET_ADJUSTED will be set to 1 and CINT will occur if enabled.</td></tr>
<tr><td>5:4</td><td>Reserved</td><td>0</td><td></td><td colspan="2"></td></tr>
<tr><td>3</td><td>PXAVG_AUTO_BSLN</td><td>1</td><td>R/W</td><td colspan="2">Proximity Average Auto Baseline Adjust. If asserted, PBSLN is automatically updated with the value of PXAVG whenever PXAVG is less than previous PBSLN. If this happens, BASELINE_ ADJUSTED will be set to 1 and CINT will occur if enabled.</td></tr>
<tr><td rowspan="8">2:0</td><td rowspan="8">PXAVG_ITERATIONS</td><td rowspan="8">4</td><td rowspan="8">R/W</td><td colspan="2">Proximity Average Iterations. Sets the number of proximity results that are averaged during normal proximity operation. The resulting proximity average is stored as a 14-bit value in the PXAVG registers after each set of iterations is complete.</td></tr>
<tr><td>VALUE</td><td>ITERATIONS</td></tr>
<tr><td>0</td><td>Skip</td></tr>
<tr><td>1</td><td>2</td></tr>
<tr><td>2</td><td>4</td></tr>
<tr><td>…</td><td>$2^{PXAVG\_ITERATIONS}$</td></tr>
<tr><td>6</td><td>64</td></tr>
<tr><td>7</td><td>128</td></tr>
</table>

Note(s):

1. Return to the Register Map (0xEC).

Figure 45:
CALIBCFG2

Addr: 0xED		CALIBCFG2			
Bit	Field	Reset	Type	Bit Description	
7:5	BINSRCH_TARGET	0	R/W	**Binary Search Target.** Sets the target value for proximity used during calibration. The target value is $2^{(\mathrm{BINSRCH\_TARGET} + 2)} - 1$ counts.	
				VALUE	**COUNTS**
				0	3
				1	7
				2	15
				…	$2^{(\mathrm{BINSRCH\_TARGET} + 2)} - 1$
				6	255
				7	511
4:0	Reserved	0			

Note(s):

1. Return to the Register Map (0xED).

General Configuration

The configuration registers include fields used to control device operation for all functions.

Figure 46:
CFG0

<table>
<tr><th colspan="2">Addr: 0xA9</th><th colspan="4">CFG0</th></tr>
<tr><th>Bit</th><th>Field</th><th>Reset</th><th>Type</th><th colspan="2">Bit Description</th></tr>
<tr><td>7:6</td><td>Reserved</td><td>0</td><td></td><td colspan="2"></td></tr>
<tr><td>5</td><td>LOWPOWER_IDLE</td><td>0</td><td>R/W</td><td colspan="2">Low Power Idle. When asserted, the device will automatically run in a low power mode whenever all functions are in wait states or disabled.</td></tr>
<tr><td>4</td><td>Reserved</td><td>0</td><td></td><td colspan="2"></td></tr>
<tr><td>3</td><td>PROX_TRIGGER_LONG</td><td>0</td><td>R/W</td><td colspan="2">Proximity Trigger Long. Increases the PTIME setting by a factor of 16.</td></tr>
<tr><td>2</td><td>ALS_TRIGGER_LONG</td><td>0</td><td>R/W</td><td colspan="2">ALS Trigger Long. Increases the WTIME setting by a factor of 16.</td></tr>
<tr><td rowspan="5">1:0</td><td rowspan="5">RAM_BANK</td><td rowspan="5">0</td><td rowspan="5">R/W</td><td colspan="2">RAM Bank Selection. Specifies the RAM bank to access in registers 0x00 to 0x7F.</td></tr>
<tr><td>VALUE</td><td>BANK</td></tr>
<tr><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td></tr>
<tr><td>2 or 3</td><td>Other (1)</td></tr>
</table>

Note(s):

1. Set RAM_BANK = 2 or 3 to access the 16 words at 0xB0 … 0xBF. These words are the time table for remote control and are mirrored over the entire 0x00 to 0x7F range.
2. Return to the Register Map (0xA9).

Figure 47:
CFG3

Addr: 0xAC		CFG3		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:6	Reserved	0		
5	HXTALK_MODE1	0	R/W	**High Crosstalk Mode.** If asserted, the proximity engine uses a 10-bit output mode intended for extremely high optical crosstalk systems. HXTALK_MODE1 and HXTALK_MODE2 must both be asserted for this function to work.
4	SAI	0	R/W	**Sleep After Interrupt.** If asserted, the oscillator is turned off whenever interrupt is active (low). SAI_ACTIVE is set in this event. To activate the oscillator again, service and clear all interrupts plus clear the SAI_ACTIVE bit.
3:0	Reserved	12		

Note(s):

1. Return to the Register Map (0xAC).

Figure 48:
CFG4

Addr: 0xAD		CFG4			
Bit	**Field**	**Reset**	**Type**	**Bit Description**	
7	Reserved	0			
6:4	INT_PINMAP	0	R/W	**Interrupt Pin Map.** Selects the signal to output on the INT pin.	
				VALUE	**SIGNAL**
				0	Normal interrupts
				1	RESERVED
				2	AINT
				3	PINT0
				4	PINT1
3	INT_INVERT	0	R/W	**Interrupt Invert.** If asserted, the interrupt signal is inverted (active = high).	

Addr: 0xAD		CFG4			
Bit	**Field**	**Reset**	**Type**	**Bit Description**	
2:0	GPIO_PINMAP	0	R/W	**GPIO Pin Map.** Selects the signal to output on the GPIO pin.	
				VALUE	**SIGNAL**
				0	Default
				1	RESERVED
				2	AINT
				3	PINT0
				4	PINT1

Note(s):

1. Return to the Register Map (0xAD).

Figure 49:
CFG6

Addr: 0xAF		CFG6		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	Reserved	0		
6	ALS_AGC_MAX_GAIN_START	0	R/W	Enables the same AGC behavior for ALS as used during flicker detection for finding the highest reasonable again setting. The AGC will start with agc_again_max as the again value. The again setting is reduced to the next lower setting until the output does not result in asat_analog or until again=0 (0.5x) is reached.
5:0	Reserved	000000		

Note(s):

1. Return to the Register Map (0xAF).

Figure 50:
CFG8

Addr: 0xB1		CFG8		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:6	Reserved	2		
5	Reserved	0		
4	CONCURRENT_PROX_AND_ALS	0	R/W	**Concurrent Proximity and ALS.** If asserted, device uses PTIME and executes proximity and ALS in parallel.
3	Reserved	0		
2	ALS_AGC_ENABLE	0	R/W	**ALS AGC Enable.** If asserted, device uses automatic gain control for the ALS engines to maximize ALS signal while avoiding saturation.
1	SWAP_PROX_ALS5	0	R/W	**Swap Proximity Diode into ALS Engine Five.** This bit will not function unless PROX_BEFORE_EACH_ALS = 0 is true. If asserted, the proximity diode is used as normal for proximity detection and then is connected to the ALS engine five to produce an IR-sensitive ALS channel. This feature is only possible if proximity and ALS operate serially.
0	Reserved	0		

Note(s):

1. Return to the Register Map (0xB1).

Figure 51:
CFG9

Addr: 0xB2		CFG9		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	Reserved	0		
6	SIEN_FD	0	R/W	**System Interrupt Flicker Detection.** Enables system interrupt when flicker detection status change has occurred.
5:0	Reserved	000000		

Note(s):

1. Return to the Register Map (0xB2).

Figure 52:
CFG11

Addr: 0xB4		CFG11		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	AINT_DIRECT	0	R/W	**ALS Interrupt Direct.** Enables the direct mode of ALS interrupt. Interrupts (aint) are only generated when adataX (selected by als_th_channel) moves over the hysteresis edges (aint_ailt and aint_aiht). If "0", interrupts are always generated if adataX is above aiht or below ailt. The status of the ALS interrupt is directly output on the INT or GPIO pin if this mode is enabled and either of those pins are configured to do so according to the INT_PINMAP and GPIO_PINMAP settings.
6	PINT_DIRECT	1	R/W	**Proximity Interrupt Direct.** If asserted, the proximity interrupt has a hysteresis loop built into the interrupt. After setting PEN = 1, the device interrupts once PDATA is below PILT or above PIHT. After this initial interrupt, the device will then interrupt based on the direction that the PDATA changes relative to each threshold. An interrupt is generated when PDATA increases from below to above PIHT to indicate a Detect condition, and an interrupt is generated when PDATA decreases from above to below PILT to indicate a Release condition. With built-in hysteresis, it is no longer necessary to change the thresholds between Detect or Release interrupts. This bit applies to PINT0 and PINT1 by using PDATA0 and PDATA1 respectively, as well as the respective thresholds.
5:0	Reserved	0		

Note(s):

1. Return to the Register Map (0xB4).

Persistence filters limit the rate of interrupts generated for proximity and ALS/color data.

Figure 53:
PERS

<table>
<tr><th colspan="2">Addr: 0xBD</th><th colspan="4">PERS</th></tr>
<tr><th>Bit</th><th>Field</th><th>Reset</th><th>Type</th><th colspan="2">Bit Description</th></tr>
<tr><td rowspan="7">7:4</td><td rowspan="7">PPERS</td><td rowspan="7">0</td><td rowspan="7">R/W</td><td colspan="2">Proximity Interrupt Persistence. Defines a filter for the number of consecutive occurrences that PDATA must remain outside the threshold range between PILT and PIHT before an interrupt is generated. Any sample that is inside the threshold range resets the counter to 0.</td></tr>
<tr><td>VALUE</td><td>CONSECUTIVE PDATA OUT OF RANGE TO INTERRUPT</td></tr>
<tr><td>0</td><td>Every proximity cycle generates an interrupt.</td></tr>
<tr><td>1</td><td>1</td></tr>
<tr><td>2</td><td>2</td></tr>
<tr><td>…</td><td>PPERS</td></tr>
<tr><td>15</td><td>15</td></tr>
<tr><td rowspan="11">3:0</td><td rowspan="11">APERS</td><td rowspan="11">0</td><td rowspan="11">R/W</td><td colspan="2">ALS Interrupt Persistence. Defines a filter for the number of consecutive occurrences that ALS/color data must remain outside the threshold range between AILT and AIHT before an interrupt is generated. The ALS data channel used for the persistence filter is set by ALS_TH_CHANNEL. Any sample that is inside the threshold range resets the counter to 0.</td></tr>
<tr><td>VALUE</td><td>CONSECUTIVE ADATA OUT OF RANGE TO INTERRUPT</td></tr>
<tr><td>0</td><td>Every ALS cycle generates an interrupt.</td></tr>
<tr><td>1</td><td>1</td></tr>
<tr><td>2</td><td>2</td></tr>
<tr><td>3</td><td>3</td></tr>
<tr><td>4</td><td>5</td></tr>
<tr><td>5</td><td>10</td></tr>
<tr><td>…</td><td>5 × (APERS – 3)</td></tr>
<tr><td>14</td><td>55</td></tr>
<tr><td>15</td><td>60</td></tr>
</table>

Note(s):

1. Return to the Register Map (0xBD).

The GPIO is configured to take inputs or outputs used for interrupts, external proximity synchronization.

Figure 54:
GPIO

Addr: 0xBE		GPIO		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	Reserved	0		
3	GPIO_INVERT	0	R/W	**GPIO Invert.** If asserted, the output on GPIO is inverted. This is useful for direct interrupt output if active = high.
2	GPIO_IN_EN	0	R/W	**GPIO Input Enable.** If asserted, the GPIO pin accepts a non-floating input.
1	GPIO_OUT	1	R/W	**GPIO Output.** If asserted, the output state of the GPIO is active directly.
0	GPIO_IN	0	R/W	**GPIO Input.** Indicates the status of the GPIO input if GPIO_IN_EN is asserted.

Note(s):

1. Return to the Register Map (0xBE).

Status Registers

The primary status register for TCS3707 indicates if there are saturation or interrupt events that need to be handled by the user. This register is self-clearing, meaning that writing a 1 to any bit in the register clears that status bit. In this way, the user should read the STATUS register, handle all indicated event(s), then write the register value back to STATUS to clear the handled events. Writing 0 to these bits will not clear those bits if they have a value of 1, which means that new events that occurred since the last read of the STATUS register will not be accidentally cleared.

Figure 55:
STATUS

Addr: 0x93		STATUS		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	ASAT	0	R	**ALS and Flicker Detect Saturation.** If ASIEN is set, indicates ALS saturation. Check the STATUS2 register to differentiate between analog or digital saturation.
6	PSAT	0	R	**Proximity Saturation.** If PSIEN is set, indicates analog saturation during a previous proximity cycle. Check the STATUS3 register to differentiate between ambient or reflected light saturation.
5	PINT1	0	R	**Proximity Interrupt One.** If PIEN1 is set, indicates that a proximity detect or release event that met the programmed proximity thresholds (PILT1 or PIHT1) and persistence (PPERS) occurred.
4	PINT0	0	R	**Proximity Interrupt Zero.** If PIEN0 is set, indicates that a proximity detect or release event that met the programmed proximity thresholds (PILT0 or PIHT0) and persistence (PPERS) occurred.
3	AINT	0	R	**ALS Interrupt.** If AIEN is set, indicates that an ALS event that met the programmed ALS thresholds (AILT or AIHT) and persistence (APERS) occurred.
2	Reserved	0		
1	CINT	0	R	**Calibration Interrupt.** If CIEN is set, indicates that either calibration is finished or that one of certain events have occurred during normal operation. If each function is enabled, CINT will be asserted if too many zeroes occur too often in a period of samples, if the proximity baseline has decreased, or if at least one offset register has been adjusted. Check the CALIBSTAT register to identify the triggering event(s).

Addr: 0x93		STATUS		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
0	SINT	0	R	**System Interrupt.** If SIEN is set, indicates that one or more of several events has occurred or is complete. The events related to this interrupt are indicated in the STATUS5 register (0xA6): flicker detection register status has changed.

Note(s):

1. Return to the Register Map (0x93).

Additional status registers indicate details about saturation, interrupts, and device execution.

Figure 56:
STATUS2

Addr: 0xA3		STATUS2		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	Reserved	0		
6	AVALID	0	R	**ALS Valid.** Indicates that the ALS state has completed a cycle since either an assertion of AEN or the last readout of the ASTATUS register.
5	PVALID	0	R	**Proximity Valid.** Indicates that the proximity state has completed a cycle since either an assertion of PEN or the last readout of PDATA.
4	ASAT_DIGITAL	0	R	**ALS Digital Saturation.** Indicates that the maximum counter value has been reached. Maximum counter value depends on integration time set in the ATIME register.
3	ASAT_ANALOG	0	R	**ALS Analog Saturation.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS analog circuit.
2	Reserved	0		
1	FDSAT_ANALOG	0	R	**Flicker Detect Analog Saturation.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS analog circuit for flicker detection.
0	FDSAT_DIGITAL	0	R	**Flicker Detect Digital Saturation.** Indicates that the maximum counter value has been reached during flicker detection.

Note(s):

1. Return to the Register Map (0xA3).

Figure 57:
STATUS3

Addr: 0xA4		STATUS3		
Bit	Field	Reset	Type	Bit Description
7:6	Reserved	0		
5	AINT_AIHT	0	R	**ALS Interrupt High.** Indicates that an ALS interrupt occurred because the ALS data exceeded the high threshold.
4	AINT_AILT	0	R	**ALS Interrupt Low.** Indicates that an ALS interrupt occurred because the ALS data is below the low threshold.
3	Reserved	1		
2	PSAT_ADC	0	R	**Proximity ADC Saturation.** Indicates that the maximum proximity ADC value has occurred.
1	PSAT_REFLECTIVE	0	R	**Proximity Reflective Saturation.** Indicates that the intensity of reflected light has exceeded the maximum integration level for the proximity analog circuit.
0	PSAT_AMBIENT	0	R	**Proximity Ambient Saturation.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the proximity analog circuit.

Note(s):

1. Return to the Register Map (0xA4).

Figure 58:
STATUS5

Addr: 0xA6		STATUS5		
Bit	Field	Reset	Type	Bit Description
7:4	Reserved	0		
3	SINT_FD	0	R	**Flicker Detect Interrupt.** If SIEN_FD is set, indicates that the FD_STATUS register status has changed.
2	Reserved	0		
1	Reserved	0		
0	Reserved	0		

Note(s):

1. Return to the Register Map (0xA6).

Figure 59:
STATUS6

Addr: 0xA7		STATUS6		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	Reserved	0		
6	Reserved	0		
5	OVTEMP_DETECTED	0	R	**Over Temperature Detected.** Indicates the device temperature is too high. Write 1 to clear this bit.
4	FD_TRIGGER_ERROR	0	R	**Flicker Detect Trigger Error.** Indicates that there is a timing error that prevents flicker detect from functioning correctly.
3	PROX_TRIGGER_ERROR	0	R	**Proximity Trigger Error.** Indicates that there is a timing error that prevents proximity from functioning correctly. The number of pulses and/or pulse length are too long for the PTIME configured for the device.
2	ALS_TRIGGER_ERROR	0	R	**ALS Trigger Error.** Indicates that there is a timing error that prevents ALS from functioning correctly. The WTIME is too short for the ATIME configured for the device.
1	SAI_ACTIVE	0	R	**Sleep After Interrupt Active.** Indicates that the device is in SLEEP due to an interrupt. To exit SLEEP mode, clear this bit.
0	INIT_BUSY	0	R	**Initialization Busy.** Indicates that the device is initializing. This bit will remain 1 for about 300µs after power on. Do not interact with the device until initialization is complete.

Note(s):

1. Return to the Register Map (0xA7).

ALS Data and Status

The ASTATUS register is required for automatic gain control (AGC). It provides an ALS saturation and ALS gain status associated to each set of ALS data. Reading the ASTATUS register (0x94) latches all 12 ALS data bytes to that status read. Reading these 13 bytes consecutively (0x94 - 0xA0) ensures that the data is concurrent. All ALS data are stored as 16-bit values. If flicker detection is enabled, ALS channel five is used for the flicker detection function and ADATA5 will read 0. The ASTATUS and ALS data registers are read only.

Figure 60:
ASTATUS

Addr: 0x94		ASTATUS		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	ASAT_STATUS	0	R	**ALS Saturation Status.** Indicates if the latched data is affected by analog or digital saturation.
6:4	Reserved	0		
3:0	AGAIN_STATUS	0	R	**ALS Gain Status.** Indicates the ALS gain applied for the ALS data latched to this ASTATUS read. The ALS gain from this status read is required to calculate ALS results if AGC is enabled.

Note(s):

1. Return to the Register Map (0x94).

Figure 61:
ALS Data Registers

Bits	Addr	Field	Description
7:0	0x95	ADATA0	**ALS Channel Zero Data:** CLEAR data
15:8	0x96		
7:0	0x97	ADATA1	**ALS Channel One Data.** RED data
15:8	0x98		
7:0	0x99	ADATA2	**ALS Channel Two Data.** GREEN data
15:8	0x9A		
7:0	0x9B	ADATA3	**ALS Channel Three Data.** BLUE data
15:8	0x9C		

Bits	Addr	Field	Description
7:0	0x9D	ADATA4	**ALS Channel Four Data.** WIDEBAND data
15:8	0x9E		
7:0	0x9F	ADATA5	**ALS Channel Five Data.** FLICKER data
15:8	0xA0		

Note(s):

1. Return to the Register Map (0x95, 0x96, 0x97, 0x98, 0x99, 0x9A, 0x9B, 0x9C, 0x9D, 0x9E, 0x9F, 0xA0).

The flicker detection status register indicates if flicker detection data is valid and whether 100Hz or 120Hz ambient light flicker frequencies are present.

Figure 62:
FD_STATUS

Addr: 0xDB		FD_STATUS		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:6	Reserved	0		
5	FD_MEASUREMENT_VALID	0	R	**Flicker Detection Measurement Valid.** Indicates that flicker detection measurement is complete. Write 1 to this bit to clear this field.
4	FD_SATURATION_DETECTED	0	R	**Flicker Saturation Detected.** Indicates that saturation occurred during the last flicker detection measurement, and the result may not be valid. Write 1 to this bit to clear this field.
3	FD_120HZ_FLICKER_VALID	0	R	**Flicker Detection 120Hz Flicker Valid.** Indicates that the 120Hz flicker detection calculation is valid. Write 1 to this bit to clear this field.
2	FD_100HZ_FLICKER_VALID	0	R	**Flicker Detection 100Hz Flicker Valid.** Indicates that the 100Hz flicker detection calculation is valid. Write 1 to this bit to clear this field.
1	FD_120HZ_FLICKER	0	R	**Flicker Detected at 120Hz.** Indicates if an ambient light source is flickering at 120Hz.
0	FD_100HZ_FLICKER	0	R	**Flicker Detected at 100Hz.** Indicates if an ambient light source is flickering at 100Hz.

Note(s):

1. Return to the Register Map (0xDB).

Proximity Data and Status

Proximity data is stored as a 14-bit value (two bytes). Reading the low byte first latches the high byte.

Proximity detection uses an Automatic Pulse Control (APC) mechanism that adjusts the number of pulses per measurement based on the magnitude of the reflected IR signal. As the magnitude of the signal increases, the number of pulses decreases. Proximity detection uses a 10-bit ADC that is extended to a 14-bit dynamic range for PDATA using the following formula:

$$\text{PDATA} = \text{ADC}_{\text{value}} \times (16 / \text{actual pulses})$$

PDATA is therefore proportional to the reflected energy per pulse, independent of the number of pulses used.

PXAVG and PBSLN provide the most recent average PDATA and a proximity baseline—the minimum average PDATA since the last calibration. Execute calibration to initialize the proximity baseline, and then the baseline can automatically provide the lowest average PDATA measured if this feature is enabled.

Figure 63:
Proximity Data

Bits	Addr	Field	Description
7:0	0xA1	PDATA	Proximity Data
15:8	0xA2		

Note(s):

1. If HXTALK_MODE is asserted, PDATA is 10-bit.
2. Return to the Register Map (0xA1, 0xA2).

Figure 64:
STATUS4

Addr: 0xA5		STATUS4		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	Reserved	0		
3	PINT1_PIHT	0	R	**Proximity Interrupt One High.** Indicates that proximity interrupt one occurred because the proximity data exceeded the high threshold. Write 1 to this bit to clear it.
2	PINT1_PILT	0	R	**Proximity Interrupt One Low.** Indicates that proximity interrupt one occurred because the proximity data is below the low threshold. Write 1 to this bit to clear it.
1	PINT0_PIHT	0	R	**Proximity Interrupt Zero High.** Indicates that proximity interrupt zero occurred because the proximity data exceeded the high threshold. Write 1 to this bit to clear it.
0	PINT0_PILT	0	R	**Proximity Interrupt Zero Low.** Indicates that proximity interrupt zero occurred because the proximity data is below the low threshold. Write 1 to this bit to clear it.

Note(s):

1. Return to the Register Map (0xA5).

Figure 65:
Proximity Average

Bits	Addr	Field	Description
7:0	0xD0	PXAVG	**Proximity Average.** Indicates the average of a configurable number of PDATA. To configure the data window, set PXAVG ITERATIONS.
15:8	0xD1		

Note(s):

1. Return to the Register Map (0xD0, 0xD1).

Figure 66:
Proximity Baseline

Bits	Addr	Field	Description
7:0	0xD2	PBSLN	**Proximity Baseline.** Indicates the minimum proximity average since the last proximity calibration. If PROX_AUTO_BASELINE is set, PBSLN will update whenever PXAVG is less than PBSLN.
15:8	0xD3		

Note(s):

1. Return to the Register Map (0xD2, 0xD3).

Figure 67:
CALIBSTAT

Addr: 0xEE		CALIBSTAT		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:3	Reserved	0		
2	BASELINE_ADJUSTED	0	R	**Baseline Adjusted Automatically.** Indicates that PBSLN was reduced because PXAVG was smaller than PBSLN. Only occurs if PXAVG_AUTO_BSLN is set. Clear bit by writing 1 to it.
1	OFFSET_ADJUSTED	0	R	**Offset Adjusted Automatically.** Indicates that proximity offset has been adjusted automatically. Only occurs if PROX_AUTO_OFFSET_ADJUST is set. Clear bit by writing 1 to it.
0	CALIB_FINISHED	0	R	**Calibration Finished.** Indicates that calibration is complete. Clear bit by writing 1 to it.

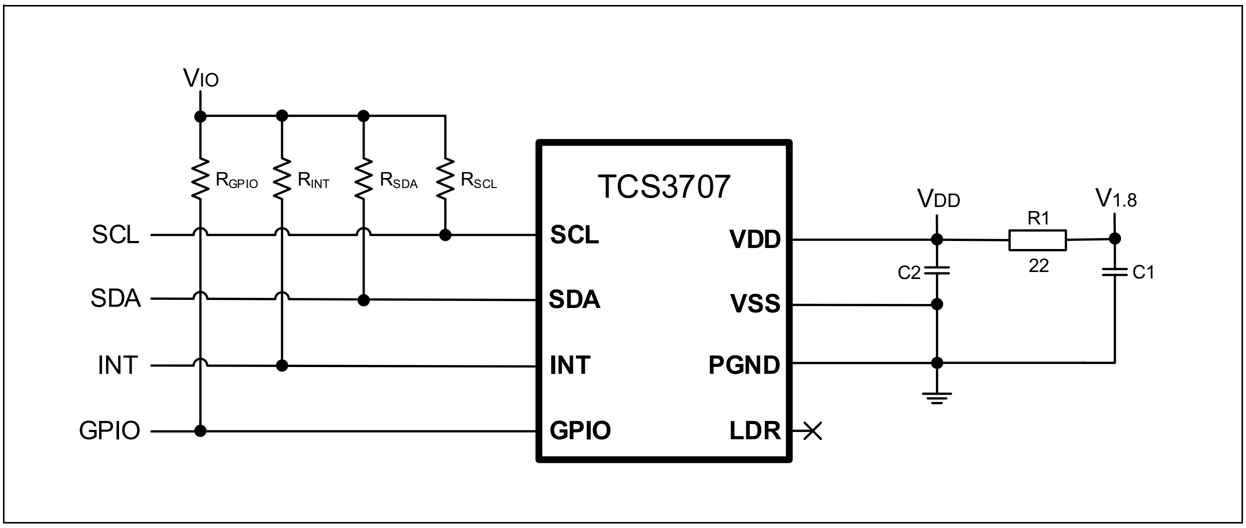
Note(s):

1. Return to the Register Map (0xEE).

Application Information

It is highly recommended to consult the **ams** application team for circuit diagram and layout review at design-in.

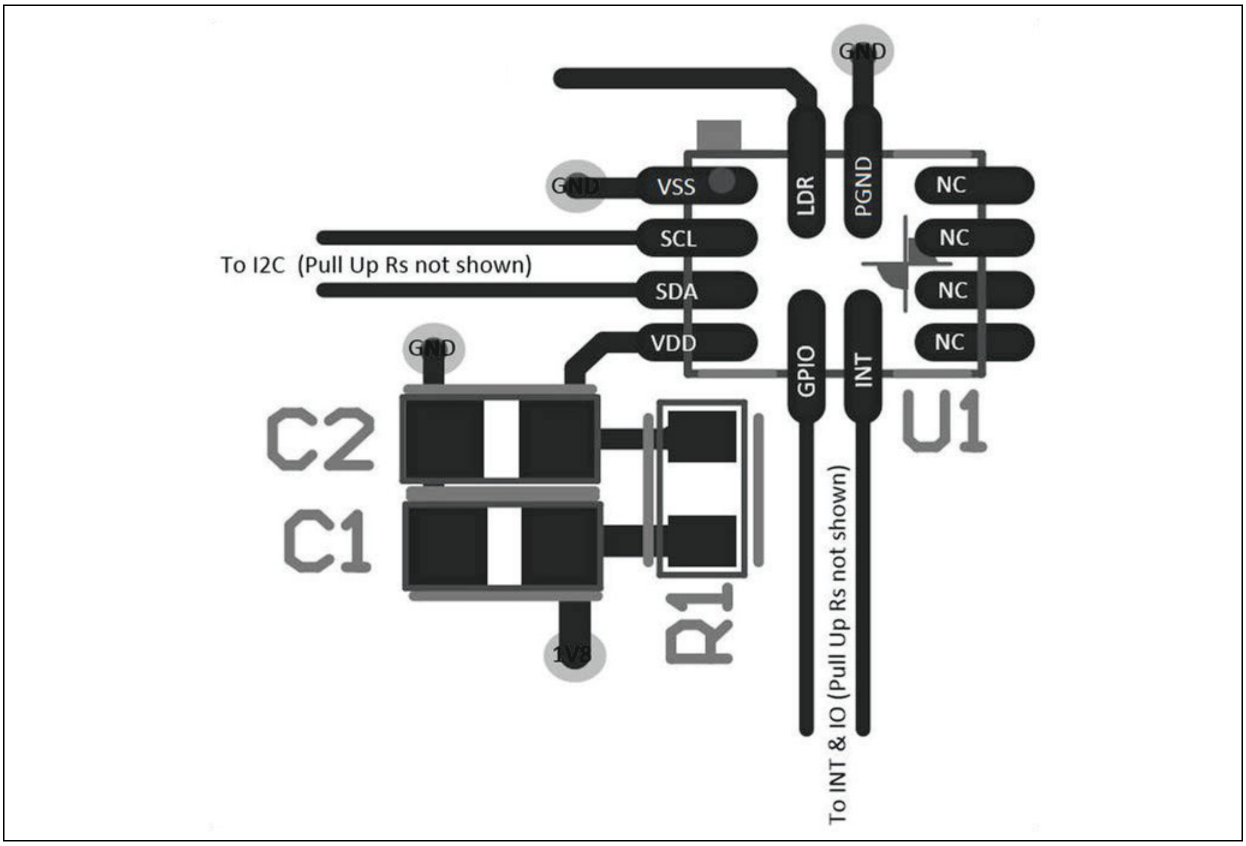
Figure 68:
TCS3707 Typical Application Circuit



Note(s):

1. C1 in the graphic above shall be 4.7µF, 6.3V, 10% and C2 in the graphic above shall be 1µF, 6.3V, 20%. All ground vias shall connected to a solid ground plane.

Figure 69:
TCS3707 Recommended Part Placement

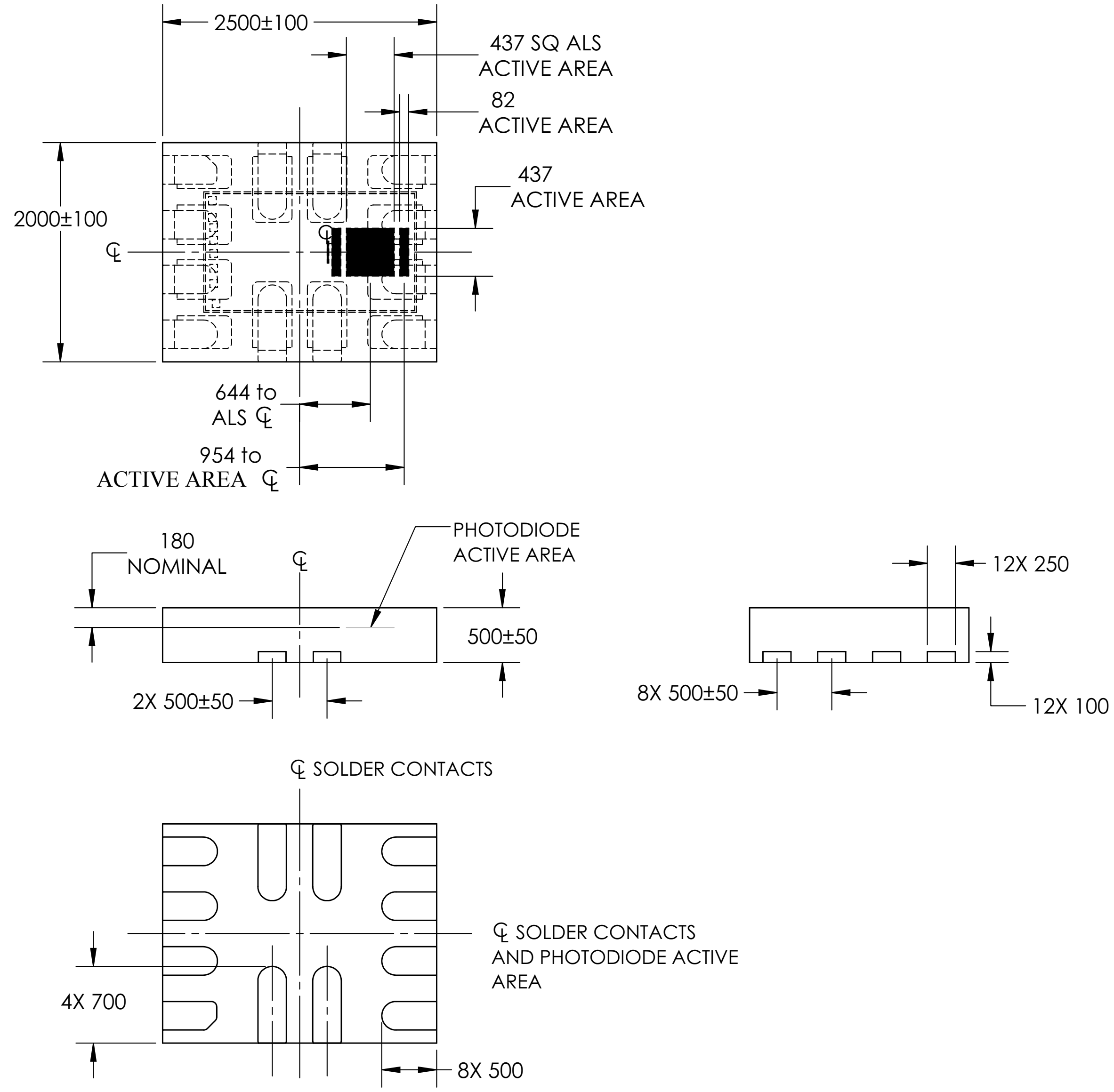


Note(s):

1. NC pins do not have an internal electrical connection. For device ESD protection, it is recommended to connect it to ground.

Package Drawings & Markings

Figure 70:
TCS3707 Module Dimensions



RoHS

Green

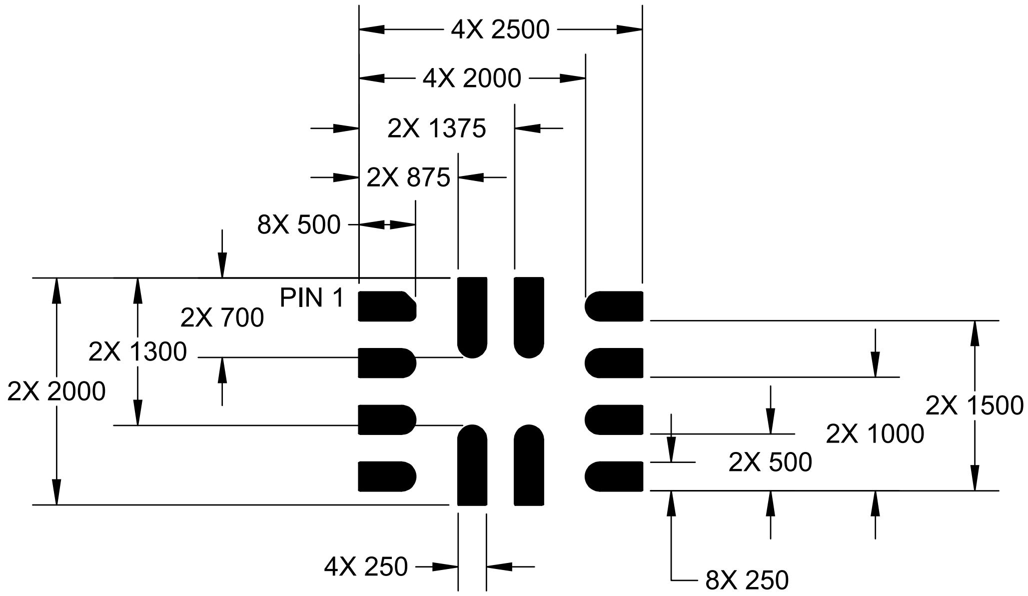
Note(s):

1. All linear dimensions are in micrometers.
2. The die is centered within the package within a tolerance of ±75 micrometers.
3. Package top surface is molded with an electrically nonconductive clear plastic compound having an index of refraction of 1.55.
4. Contact finish is copper alloy A194 with pre-plated NiPdAu lead finish.
5. This package contains no lead (Pb).
6. This drawing is subject to change without notice.

PCB Pad Layout

Suggested PCB pad layout guidelines for the surface mount module are shown. Flash Gold is recommended as a surface finish for the landing pads.

Figure 71:
Recommended PCB Pad Layout

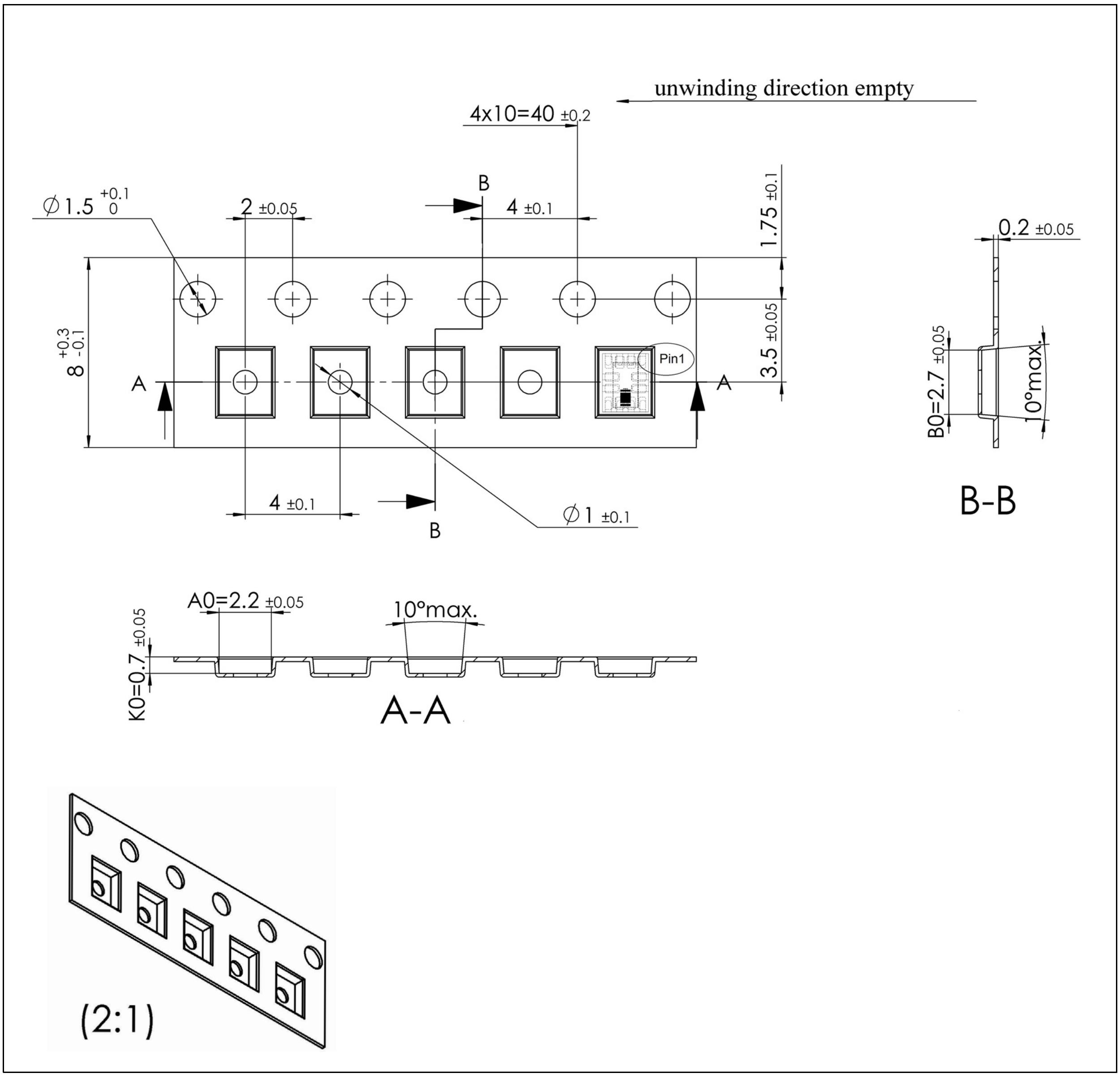


Note(s):

1. All linear dimensions are in micrometers.
2. Dimension tolerances are ±0.05mm unless otherwise noted.
3. This drawing is subject to change without notice.

Tape & Reel Information

Figure 72:
Tape and Reel Mechanical Drawing



Note(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ± 0.10 mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing Ao, Bo, and Ko are defined in ANSI EIA Standard 481−B 2001.
4. Each reel is generally 330 millimeters in diameter and contains 10000 parts. Please reconfirm for actual orders.
5. **ams** packaging tape and reel conform to the requirements of EIA Standard 481−B.
6. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.

Soldering & Storage Information

Soldering Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

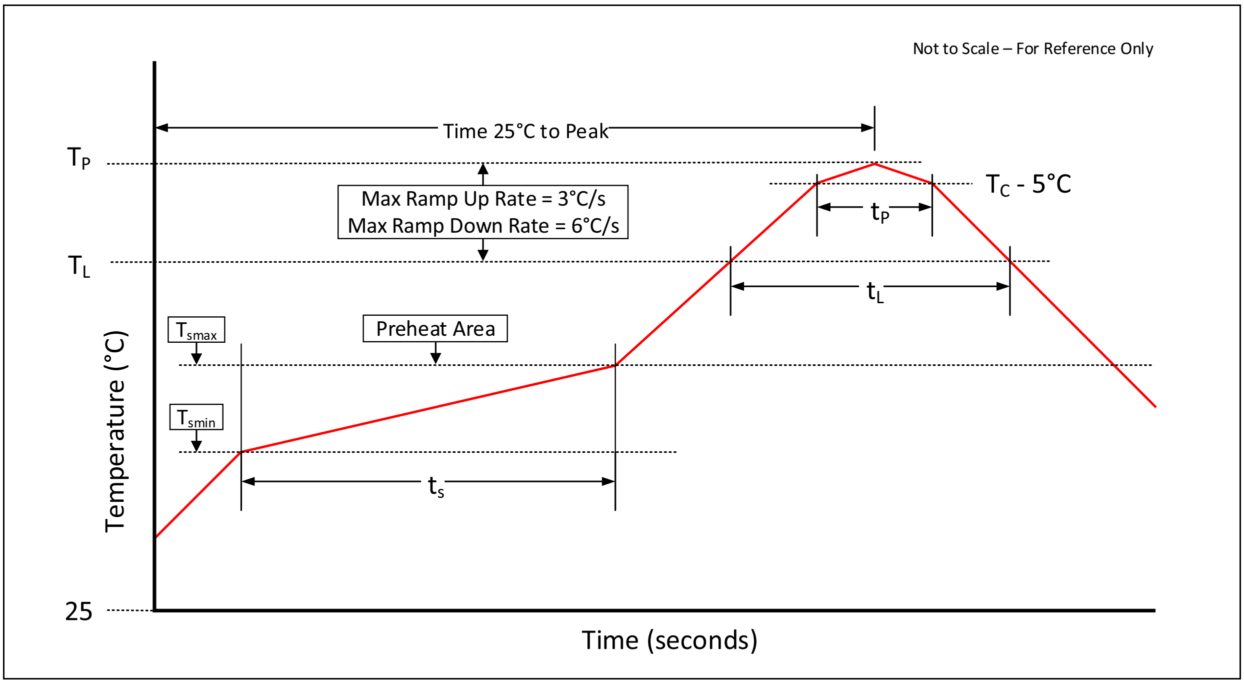
Figure 73:
Solder Reflow Profile

Profile Feature Preheat/Soak	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Temperature Min (T_{smin})	100°C	150°C
Temperature Max (T_{smax})	150°C	200°C
Time (t_s) from (T_{smin} to T_{smax})	60-120 seconds	60-120 seconds
Ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183°C 60-150 seconds	217°C 60-150 seconds
Peak package body temperature (T_P)	For users T_P must not exceed the Classification temp of 235°C For suppliers T_P must equal or exceed the Classification temp of 235°C	For users T_P must not exceed the Classification temp of 260°C For suppliers T_P must equal or exceed the Classification temp of 260°C
Time (t_P)(1) within 5°C of the specified classification temperature (T_c)	20(1)seconds	30(1)seconds
Ramp-down rate (T_P to T_L)	6°C/second max.	6°C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.

Note(s):

1. Tolerance for peak profile temperature (TP) is defined as a supplier minimum and a user maximum.

Figure 74:
Solder Reflow Profile Graph



Storage Information

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: <40°C
- Relative Humidity: <90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: <30°C
- Relative Humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

Ordering & Contact Information

Figure 75:
Ordering Information

Ordering Code	Address	Interface	Delivery Form	Delivery Quantity
TCS37073	0x39	1.8V I^2C	Tape & Reel	10000 pcs/reel

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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
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Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Revision Information

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Added notes under figure 4	4
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Updated figure 69	55
Updated figure 70	56
1-04 (2019-Feb-11) to 1-05 (2019-May-13)	
Updated figure 7 title to "ALS/Color Characteristics of TCS3707, ALS Gain = 128x, Integration Time = 11ms (unless otherwise noted)"	6
Updated "Detailed Description"	14
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Updated figure 72	59
Updated figure 75	63

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide