Product Document

Datasheet

DS000628

AS6204

Digital Temperature Sensor

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Content Guide

1 General Description

The AS6204 IC is a high accuracy temperature sensor system that communicates via a 2 wire digital bus with other devices. It consists of a Si bandgap temperature sensor, an ADC and a digital signal processor.

It has a very high temperature accuracy (±0.2 °C between -10 °C to 20 °C) and an ultra-low power consumption (low operation and quiescent current) which makes it ideally suited for mobile/battery powered applications.

The AS6204 is an easy to integrate and use solution, featuring a factory calibrated sensor, integrated linearization and the possibility to use 2 different I²C addresses, enabling to use two AS6204 devices on one bus.

Additionally the AS6204 temperature sensor system also features an alert functionality, which triggers e.g. an interrupt to protect devices from excessive temperatures.

1.1 Key Benefits & Features

The benefits and features of AS6204 are listed below:

Figure 1:
Added Value of Using AS6204

| Benefits	Features
High Measurement Accuracy	± 0.4 °C (20 - 65 °C) ± 1 °C remaining operating temperature span
Low Power Consumption	6 µA @Operation (typical, @ 4 Hz) 0.1 µA @Standby (typical)
Supply Voltage Range	1.8 – 3.6 V
Small PCB Footprint	1.5 mm x 1 mm (WLCSP)

1.2 Applications

- Electronic Equipment
- Tablets
- Convertibles
- Laptop
- Personal Computers

1.3   Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of AS6204
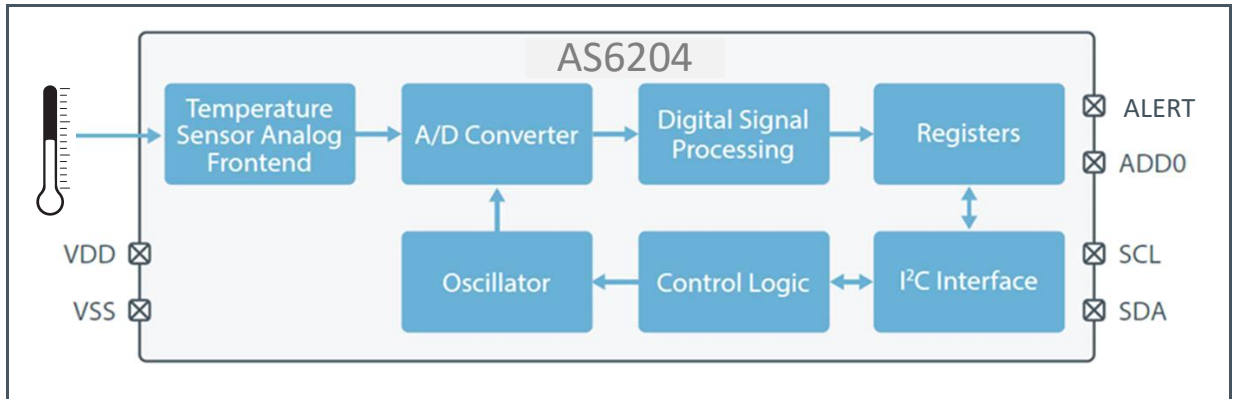
In Figure 2 the functional blocks are depicted. The sensing element for sensing the temperature is a Si bipolar transistor. The analog signal of the sensing element is converted into a digital signal by the A/D converter and the signal is further processed by a digital signal processor and written into the registers. The registers can be accessed via the serial bus interface (I²C bus).

2   Ordering Information

Ordering Code	Package	Marking	Delivery Form	Delivery Quantity
AS6204-AWLM-S	WLCSP	AS6204	Tape & Reel	500 pcs/reel
AS6204-AWLT-L	WLCSP	AS6204	Tape & Reel	5000 pcs/reel

3 Pin Assignment

3.1 Pin Diagram

Figure 3:
Pin Assignment WLCSP
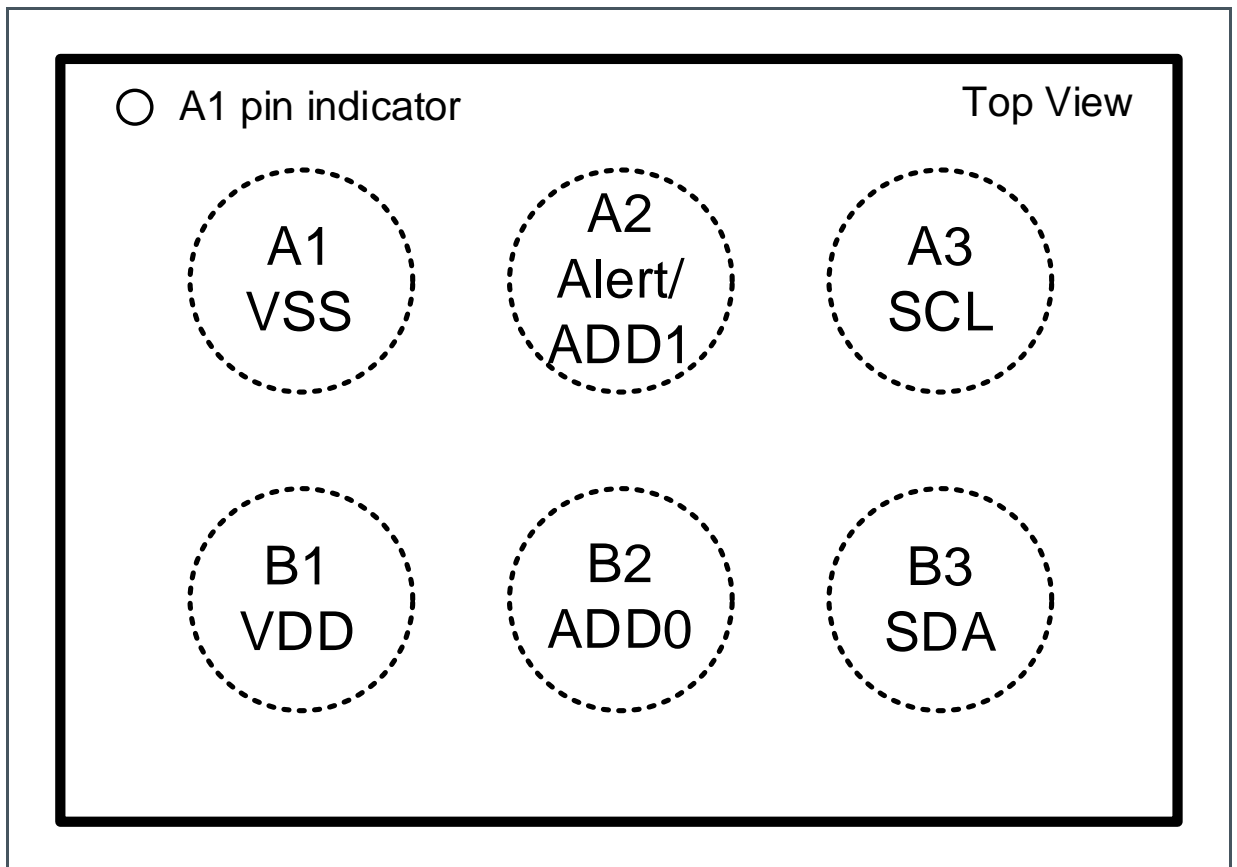
In Figure 3 the pin assignment of the WLCSP package is shown. The viewing side is from the top. The A1 pin is also marked with a point on the top side.

3.2 Pin Description

Figure 4:
Pin Description of AS6204 (WLCSP)

Pin Number	Pin Name	Pin Type[1]	Description
A1	VSS	S	Ground Pin
A2	ALERT	DO_OD	Alert output (interrupt), external pull up resistors recommended
A3	SCL	DI_S	Serial Interface Clock, external pull up resistors recommended
B1	VDD	S	Positive Supply Voltage
B2	ADD0	DI_S	Address Select Pin, must not be left unconnected (refer to the bus address section for further details).
B3	SDA	DIO_SOD	Serial Interface Data, external pull up resistors recommended

[1]   Explanation of abbreviations:
   S   Supply
   DO_OD   Digital output - open drain
   DI_S   Digital Schmitt trigger input
   DIO_SOD   Digital Schmitt trigger input/output- open drain

4 Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Operating Conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings of AS6204

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
V_{SUP} / V_{GND}	Supply Voltage to Ground	-0.3	4	V	
V_{IN}	Input Pin Voltage to Ground	-100	100	V	
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM		±2000	V	
Temperature Ranges and Storage Conditions					
T_A	Operating Ambient Temperature	-40	125	°C	
T_J	Operating Junction Temperature		125	°C	
T_{STRG}	Storage Temperature Range	-55	125	°C	
T_{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020[1]
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level		1		Represents unlimited floor life time

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices."

5 Typical Operating Characteristics

The AS6204 is a complete sensor system that has an integrated sensing element, the analog frontend, the A/D converter and the digital signal processing part.

The digital signal processing part consists of the signal processor, the registers and the serial bus interface.

5.1 Analog System Parameters

In Figure 6 an overview of the analog system parameters is given.

The current consumption for less than 4 conversions per second is lower than the values given in Figure 6

Figure 6:
Analog System Parameters of AS6204

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD	1.8 2.0	3.0 3.0	3.6 3.6	V	T= 0 °C to125 °C T=-40 °C to 125 °C
Temperature range	T	-40		125	°C	
Standby current consumption	IDD		0.1 0.3	0.4 0.9	µA	T=-40 °C to 65 °C T=65 °C to 125 °C
Current consumption (4 conversion /s)	IDD		6	7 16	µA	T=-40 – 65 °C Serial bus inactive T=65 °C to 125 °C Serial bus inactive
Accuracy[1]	T_ERR	-1.0 -0.4 -1.0		+1.0 +0.4 +1.0	°C	T=-40 °C to 0 °C T=-0 °C to 65 °C T=65 °C to 125 °C
Resolution	N		12		Bits	
Conversion time	t_S	24	34	46	ms	
Conversion rate	NS		0.25 1 4 8	0.35 1.35 5.5 10.7	Conv/s	CR[1:0]=00 CR[1:0]=01 CR[1:0]=10 CR[1:0]=11
Supply voltage rise time	t_{Rise_VDD}			20	ms	0.1 V to 1.6 V
Supply voltage slew rate	SR_VDD	50			mV/ms	0.1 V to 1.6 V

(1)   The accuracy is based on measurements and reflects 4.5 σ statistics.

5.2 Digital System Parameters
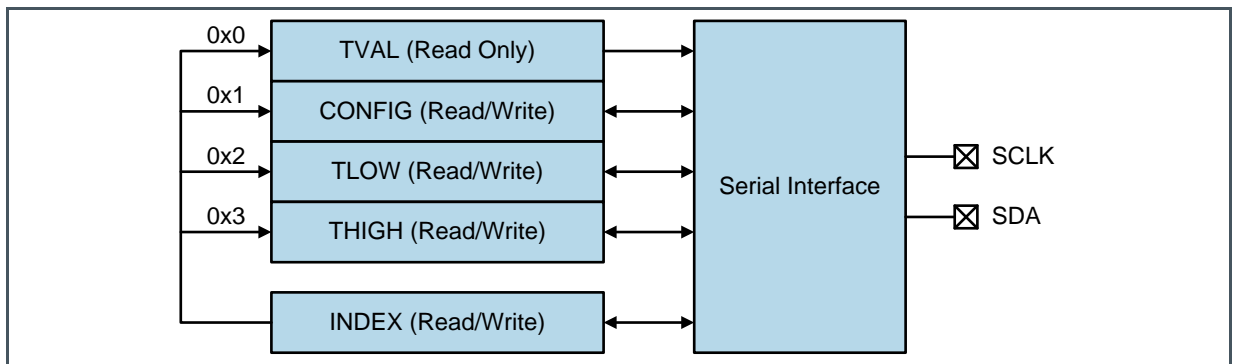
Figure 7:

Digital System Parameters of AS6204

Parameter	Symbol	Pins	Min	Max	Unit	Note
High level input voltage	V_IH	SCL, ADD0, SDA	0.7 * VDD		V	
Low level input voltage	V_IL	SCL,ADD0, SDA		0.3 * VDD	V	
Low level output voltage	V_OL	Alert, SDA		VSS+0.4	V	Alert pin: I_OL=3 mA[1]
Tristate leakage current	I_OZ	SDA	-10	10	µA	To VSS

(1)   This value describes the minimum current sank of Alert pin at maximum V_OL (Low level output voltage).

6 Register Description

6.1 Register Overview

Figure 8:
Register Map with Serial Interface

In Figure 8 the registers that the device contains are shown.

With the use of the index register, it is possible to address the specific register. The index register is an 8-bit register, where only bits 0 and 1 are used as shown in Figure 9 and all other bits are set to 0 and read only.

6.1.1 Index Register

Figure 9:
Index Register

Bit	Bit Name	Default	Access
0	Address Bit	0	RW
1	Address Bit	0	RW
2	Reserved	0	RO
3	Reserved	0	RO
4	Reserved	0	RO
5	Reserved	0	RO
6	Reserved	0	RO
7	Reserved	0	RO

Address	Symbol	Register	Description
0x0	TVAL	Temperature Register	Contains the temperature value
0x1	CONFIG	Configuration Register	Configuration settings of the temperature sensor
0x2	TLOW	T$_{LOW}$ Register	Low temperature threshold value
0x3	THIGH	T$_{HIGH}$ Register	High temperature threshold value

The 2-bit addresses in the index register define the access to the registers shown in Figure 10. This means that in order to access the different registers, the index register must be set accordingly. With the exception of the TVAL register (which contains the temperature value data), all registers are read/write accessible.

6.2 Detailed Register Description

6.2.1 Configuration Register (Address 0x1)

Figure 11:
CONFIGURATION Register

Address 0x1				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
0	Reserved	0	RO	Reserved
1	Reserved	0	RO	Reserved
2	Reserved	0	RO	Reserved
3	Reserved	0	RO	Reserved
4	Reserved	0	RO	Reserved, do not change
5	AL	1	RO	ALERT Bit (AL)
6	CR	0	RW	Conversion RATE (CR)
7	CR	1	RW	Conversion RATE (CR)
8	SM	0	RW	Sleep Mode (SM)
9	IM	0	RW	Interrupt Mode (IM)
10	POL	0	RW	Polarity (POL)
11	CF	0	RW	Consecutive Faults (CF)
12	CF	0	RW	Consecutive Faults (CF)
13	Reserved	0	RO	Reserved
14	Reserved	1	RO	Reserved
15	SS	0	RW	Single Shot

The configuration register is a 16-bit register, which defines the operation modes of the device. Any read/write operations processes the MSB byte first.

In Figure 11 the configuration register is shown. The bits 0-4 and 13-14 are not to be used and are set to read only (RO). The bit 4 is reserved (RW) and must not be changed from the default value. The explanation of the other bits are described in detail in the following sections.

6.2.2   Alert Bit

The alert bit can be used to easily compare the current temperature reading to the thresholds that can be set in the TLOW and THIGH registers.

If the polarity bit is set to 0, the AL bit is read as 1 until the converted temperature value exceeds the defined value in the high temperature threshold register THIGH for the number of defined consecutive faults (bits CF). Such an event causes the AL bit to toggle to 0 and the value is kept until the converted temperature value falls below the defined value in the low temperature threshold register TLOW for the number of defined consecutive faults. If this condition is met, the AL bit is reset to 1.

The polarity bit (POL) defines the active state of the alert bit as depicted in the following figure.

The alert bit has the same setting as the alert output as long as the device is configured for the comparator mode.

Figure 12:
State Diagram of the Alert Bit
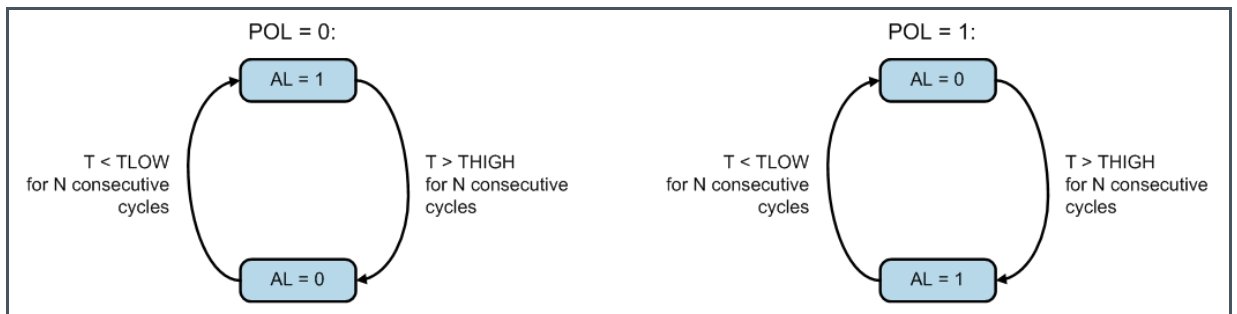
6.2.3   Conversion Rate Bits

The conversion rate bits define the number of executed temperature conversions per time unit. Additional readouts of the temperature register between conversions is possible but not recommended because the value is changed only after a conversion is finished.

Values of 125 ms, 250 ms, 1 s and 4 s per conversion can be configured while the default rate is set to 250 ms. This corresponds to a value of four conversions per second. The following table summarizes the different configuration settings:

Figure 13:
Conversion Rate Configuration

Conversion Rate Bits		Conversion Rate	Conversion Frequency
Bit 7	Bit 6		
0	0	4 s	0.25 Hz
0	1	1 s	1 Hz
1	0	250 ms	4 Hz (default)
1	1	125 ms	8 Hz

The device immediately starts a conversion after a power-on sequence and provides the first result after conversion time TS. A higher power consumption occurs during the actual conversion while the device stays in the standby mode after a finished conversion until the next conversion is activated as shown in the following figure.

Figure 14:
Conversion Sequence
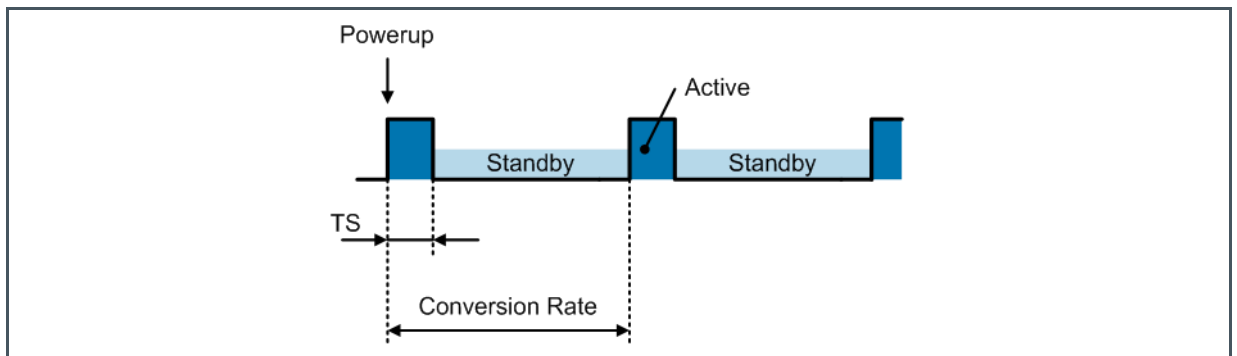
6.2.4 Sleep Mode

The sleep mode is activated by setting the bit SM in the configuration register to 1. This shuts the device down immediately and reduces the power consumption to a minimum value.

Entering the sleep mode will take some time (120 ms maximum) and the first conversion after the sleep mode takes longer than the values specified in Figure 6. Therefore, it is recommended to trigger a single shot conversion at the same time while entering sleep mode. After 150ms, the device enters the sleep mode and subsequent conversion times are as specified in Figure 6.

The serial interface is the only active circuitry in the sleep mode in order to provide access to the digital registers.

After resetting the SM bit to 0, the device enters the continuous conversion mode.

Figure 15:
Sleep Mode Configuration

Sleep Mode Bit	Operation Mode
0	Continuous Conversion Mode
1	Sleep Mode

6.2.5 Interrupt Mode

The interrupt mode bit defines whether the device operates in the temperature comparator mode or the interrupt mode. This defines the operation of the ALERT output as described in the polarity section bit.
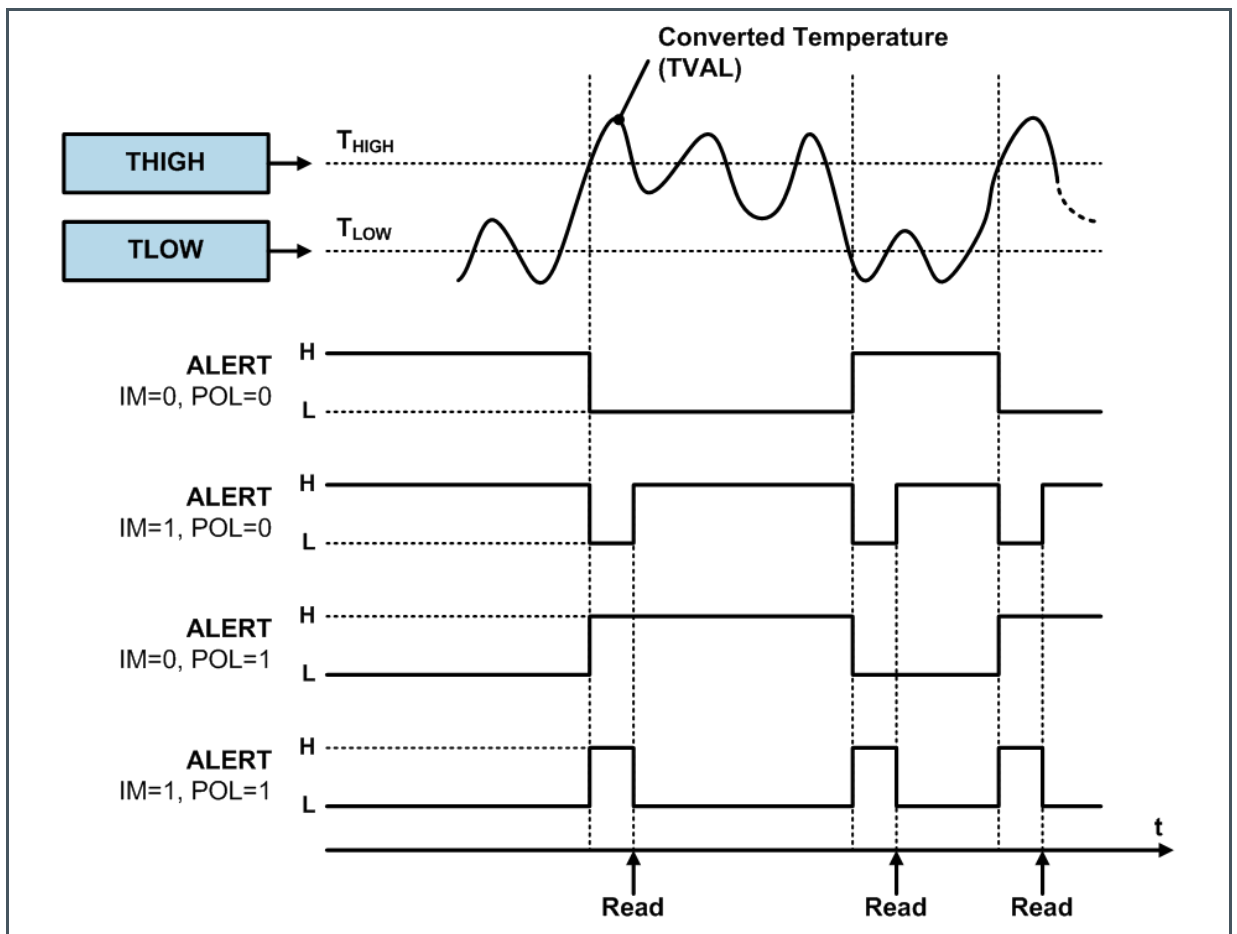
Figure 16:
Interrupt Mode Configuration

Interrupt Mode Bit	Operation Mode
0	Comparator Mode
1	Interrupt Mode

The comparator mode: If the temperature value exceeds the THIGH value, the alert output is changed (e.g. from high to low if the polarity bit is set to 0 and vice versa). The alert output stays in that condition until the measured temperature drops below the defined TLOW value.

The interrupt mode: The alert output changes as soon as the measured temperature crosses the THIGH or TLOW value threshold.

The alert bit has the same setting as the alert output if the device is set to comparator mode.

Figure 17:
Alert Output Functionality

6.2.6   Polarity Bit

The polarity bit configures the polarity of the ALERT output. If the polarity bit is cleared, the ALERT output is low active while it becomes high active if the polarity bit is set to '1'.

Figure 18:
Polarity Bit Configuration

Polarity Bit	ALERT Output
0	Active low
1	Active high

6.2.7　Consecutive Faults

A fault condition persists if the measured temperature either exceeds the configured value in register THIGH or falls below the defined value in register TLOW. As a result, the ALERT pin indicates the fault condition if a defined number of consecutive temperature readings meets this fault condition. The number of consecutive faults are defined with two bits (12 and 11) and prevent a false alert if environmental temperature noise is present. The register configuration is shown in the following table.

Figure 19:
Consecutive Faults Bit Settings

Consecutive Fault Bits		Consecutive Faults (N)
Bit 12	**Bit 13**	
0	0	1
0	1	2
1	0	3
1	1	4

6.2.8　Single Shot Conversion

The device features a single shot measurement mode if the device is in sleep mode (SM=1). By setting the "Single Shot-bit" to 1, a single temperature conversion is started and the SS-bit can be read as 1 during the active conversion operation. Once the conversion is completed, the device enters the sleep mode again and the SS-bit is set to 0. The single shot conversion allows very low power consumption since a temperature conversion is executed on demand only. This allows a user defined timing of the temperature conversions to be executed and is used if the consecutive operation mode is not required.

The recommendation to trigger the first conversion simultaneously with entering the sleep mode is described in detail in section: Sleep Mode

As the device exhibits a very short conversion time, the effective conversion rate can be increased by setting the single shot bit repetitively after a conversion has finished. However, it has to be ensured that the additional power is limited; otherwise, self-heating effects have to be considered.

Figure 20:
Single Shot Conversion Bit Settings

Single Shot Bit	Conversion
0	No conversion ongoing/ conversion finished
1	Start single shot conversion / conversion ongoing

6.2.9 High and Low Limit Registers

If the comparator mode is configured (IM=0), the ALERT output becomes active if the temperature equals or exceeds the defined value in register THIGH for the configured number of consecutive faults (N). This configuration is defined by the field CF in the configuration register. The ALERT output remains assigned until the converted temperature value equals or falls below the defined value in register TLOW for the same number of consecutive fault cycles.

If the interrupt mode is configured (IM=1), the ALERT output becomes active if the temperature equals or exceeds the defined value in register THIGH for the configured number of consecutive fault cycles. It remains active until a read operation is executed on any register. The ALERT output is also cleared if the device is set into sleep mode by setting bit SM in the configuration register.

Once the ALERT output is cleared, it is activated again only if the temperature value falls below the configured value in register TLOW. It remains active unless a read operation has taken place.

This sequence is repeated unless the device is set into the comparator mode or reset by the General Call Reset command. This reset command clears the interrupt mode bit and consequently puts the device into the comparator mode.

The sequential behavior is summarized in the following Figure 21.

Figure 21:
Alert Operation Modes
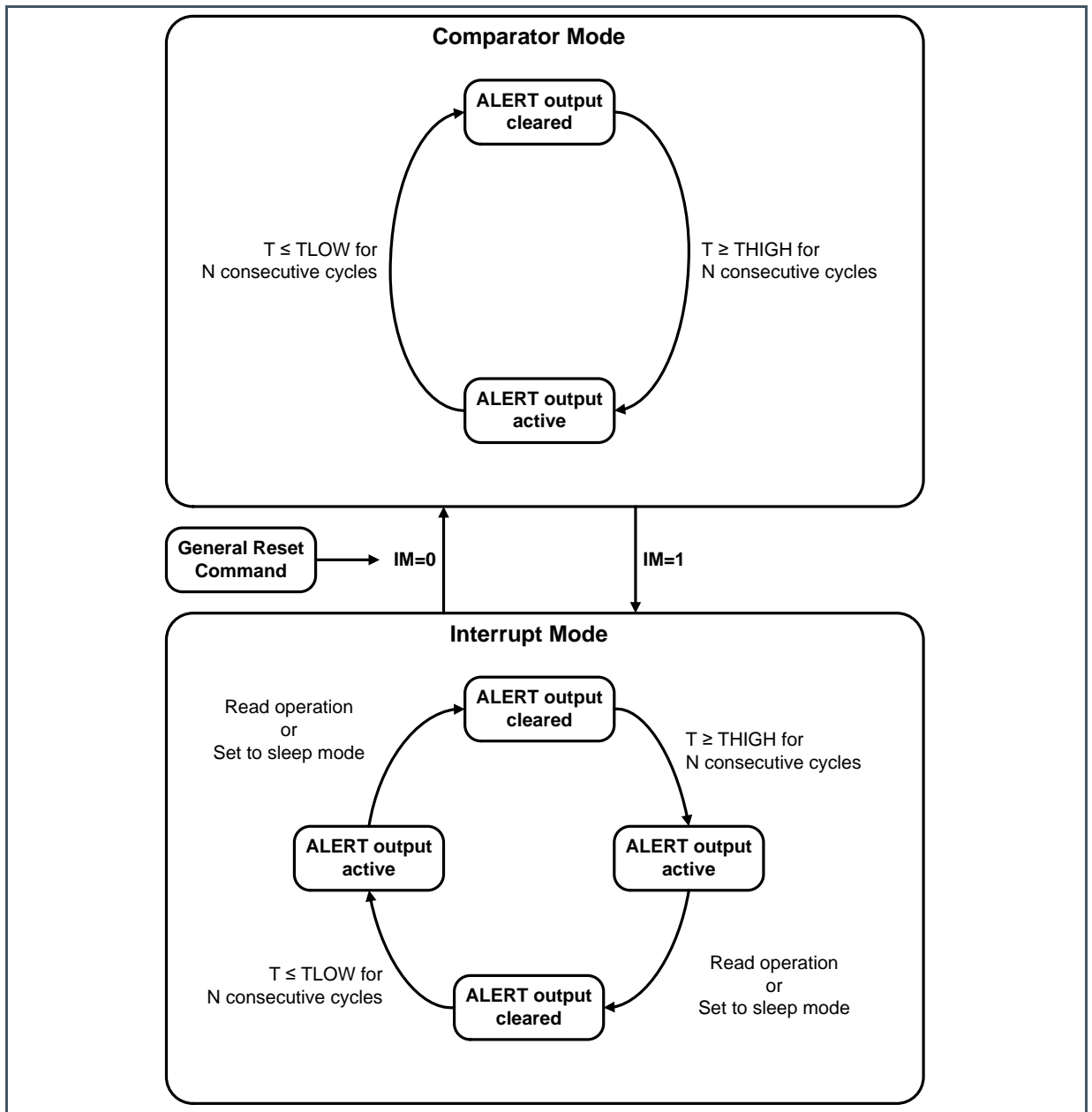
The following table defines the content of the registers TLOW and THIGH. For data transmission, the MSB byte is transmitted first, followed by the LSB byte. The data format for representing the threshold temperatures is equal to the temperature register (TVAL). After a power up, the registers are initialized with the following default values:

Figure 22:
Default Values for THIGH and TLOW

Register	Temperature	Binary Value
TLOW	75 °C	L11..L0 = 0100 1011 0000
THIGH	80 °C	H11.H0 = 0101 0000 0000

The following table defines the register bits of the THIGH and TLOW register.

Figure 23:
Register Bit Settings for THIGH/TLOW

Address 0x2 / 0x3			
Bit	Bit Name for TLOW	Bit Name for THIGH	Access
0	0	0	RW
1	0	0	RW
2	0	0	RW
3	0	0	RW
4	L1	H1	RW
5	L2	H2	RW
6	L3	H3	RW
7	L4	H4	RW
8	L5	H5	RW
9	L6	H6	RW
10	L7	H7	RW
11	L8	H8	RW
12	L9	H9	RW
13	L10	H10	RW
14	L11	H11	RW
15	L12	H12	RW

6.2.10 Temperature Register (Address 0x0)

Figure 24:
Temperature Value Register

Address 0x0	
Bit	**Bit Name**
0	0
1	0
2	0
3	0
4	T1
5	T2
6	T3
7	T4
8	T5
9	T6
10	T7
11	T8
12	T9
13	T10
14	T11
15	T12

The temperature register contains the digitally converted temperature value and can be read by setting the index pointer to the TVAL register (0x0).

Two consecutive bytes must be read to obtain the complete temperature value. The MSB byte (Bits D15…D8) is transmitted upon the first read access and the LSB byte (Bits D7…D0) is transmitted after the second read access. The least significant bits D3…D0 are set to 0.

A temperature value is represented as a two complement value in order to cover also negative values. After power up, the temperature value is read as 0°C until the first conversion has been completed. One LSB corresponds to 0.0625°C.

The binary values can be calculated according to the following formulas:

Positive values: |Value| / LSB

Negative values: Complement (|Value| / LSB) + 1

Equation 1: Example 75 °C

$$\frac{75°C}{0.0625°C} = 1200 = Binary\ 0100\ 1011\ 0000 = Hex\ 4B0$$

Equation 2: Example -40°C

$$\frac{|-40°C|}{0.0625°C} + 1 = \overline{640} + 1 = Binary\ \overline{0010\ 1000\ 0000} + 1 = 1101\ 0111\ 1111 + 1 = 1101\ 10000\ 0000$$
$$= Hex\ D80$$

Figure 25:
Temperature Conversion Examples

Temperature (°C)	Digital Output (Binary)	Digital Output (Hex)
100.0	0110 0100 0000	640
75.0	0100 1011 0000	4B0
50.0	0011 0010 0000	320
25.0	0001 1001 0000	190
0.125	0000 0000 0010	002
0.0625	0000 0000 0001	001
0.0	0000 0000 0000	000
-0.0625	1111 1111 1111	FFF
-0.125	1111 1111 1110	FFE
-25.0	1110 0111 0000	E70
-40 .0	1101 1000 0000	D80

6.3 Serial Interface

The device employs a standard I²C-serial bus.

6.3.1 Bus Description

A data transfer must be invoked by a master device (e.g. microcontroller), which defines the access to the slave device. The master device defines and generates the serial clock (SCL) and the start/stop conditions.

In order to address a specific device, the master device must generate a START condition by pulling the data line (SDA) from a logic high level to a logic low lev-el while the serial clock signal (SCL) is kept at high level.

After the start condition, the slave address byte is transmitted which is completed with a ninth bit which indicates a read (bit='1') or a write operation (bit='0') respectively. All slaves read the data on the rising edge of the clock. An acknowledge signal is generated by the addressed slave during the ninth clock pulse. This acknowledge signal is produced by pulling the pin SDA to a low level by the selected slave.

Subsequently, the byte data transfer is started and finished by an acknowledge bit. A change in the data signal (SDA) while the clock signal (SCL) is high causes a START or STOP condition. Hence, it must be ensured such a condition is prevented during a data transfer phase.

After completing the data transfer, the master generates a STOP condition by pulling the data line (SDA) from low level to high level while the clock signal (SCL) is kept at high level.

6.3.2 Data Interface

A bus connection is created by connecting the open drain input/output lines SDA and SCL to the two-wire bus. The inputs of SDA and SCL feature Schmitt-trigger inputs as well as low pass filters in order to suppress noise on the bus line. This improves the robustness against spikes on the two-wire interface.

Both fast transmission mode (1 kHz to 400 kHz) and high-speed transmission mode (1 kHz to 3.4 MHz) are employed to cover different bus speed settings.

Any data transfer transmits the MSB first and the LSB as last bit.

6.3.3 Bus Address

A slave address consists of seven bits, followed by a data direction bit (read/write operation). The slave address can be selected from a pool of two different address settings by connecting the input pin ADD0 to an appropriate signal as summarized in the following table.

The ADD0 must be left open.

Figure 26:
I²C Address Select Configuration

ADD0 Connection	Device Address (bin)	Device Address (hex)
VSS	0100 1000	0x48
VDD	0100 1001	0x49
SDA	0100 1010	0x4A
SCL	0100 1011	0x4B

6.3.4 Read/Write Operation

In order to access an internal data register, the index register must be written in advance. This register contains the actual register address and selects the appropriate register for an access. A typical transfer consists of the transmission of the slave address with a write operation indication, followed by the transmission of the register address and is finalized with the actual register content data transfer. This implies that every write operation to the temperature sensor device requires a value for the index register prior to the transmission of the actual register data.

The index register defines the register address for both the write and read operation. Consequently, if a read operation is executed, the register address is taken from the index register, which was defined from the last write operation.

If a different register needs to be read, the index register has to be written in advance to define the new register address. This is accomplished by transmitting the slave address with a low R/W bit, followed by the new content of the index register. Subsequently, the master provokes a START condition on the bus and transmits the slave address with a high R/W bit in order to initiate a read operation.

Since the index register always keeps its last value, reads can be executed repetitively on the same register.

Similarly, to the byte transfer where the MSB is transmitted first, a two-byte transfer executes the transfer of a 16-bit word whereas the MSB byte is always transmitted first.

6.3.5 Slave Operation

The device employs a slave functionality only (slave transmitter and slave receiver) and cannot operate as a bus master. Consequently, the device never actively drives the SCL line.

6.3.6 Slave Receiver Mode

The master device invokes any transmission by transmitting the slave address with a low R/W bit. Subsequently, the slave device acknowledges the reception of the valid address by pulling the ninth bit to a low level. Following to acknowledge, the master transmits the content of the index register. The slave device again acknowledges this transfer. The next data byte(s) are written to the actual data register, which is selected by the index register while each transfer is acknowledged upon a completed transfer by the slave device. A data transfer can be finished if the master transmits a START or a STOP condition on the bus.

6.3.7 Slave Transmitter

The master transmits the slave address with a high R/W bit. In turn, the slave acknowledges a valid slave address. Subsequently, the slave transmits the MSB byte of the actual selected data register by the index register. After the MSB byte transmission, acknowledge is sent by the master. Afterwards, the LSB byte is transmitted by the slave which is also acknowledged by the master after the

completed transmission. The master can terminate the data transfer by transmitting a Not-Acknowledge after the transmitted slave data or by invoking a START or a STOP condition on the bus.

6.3.8 Alert Function

If the device is configured for an interrupt mode operation (IM=1), the ALERT output can be used as an alert signal.

If the polarity bit is set to '0' (POL='0'), the alert condition bit is set to '0' in case the temperature has exceeded the configured value in register THIGH. Accordingly, the alert condition bit is set to '1' if the temperature has fallen below the configured value in register TLOW.

If the polarity bit is set to '1' (POL='1'), the alert condition bit is inverted. The following table summarizes the status of the alert condition bit with different alert conditions and polarity configurations.

Figure 27:
Alert Condition Bit

Polarity Bit	Alert Condition	Alert Condition Bit (AC-Bit)
0	T ≥ THIGH	0
0	T ≤ TLOW	1
1	T ≥ THIGH	1
1	T ≤ TLOW	0

6.3.9 High Speed Mode

The bus operation is limited to 400 kHz unless the master device issues a high-speed command as the first byte after a START condition. This switches the bus to a high-speed operation, which allows data transfer frequencies up to 3.4 MHz. The slave does not acknowledge such a command but the input-filter time constants on the serial interface (SDA and SCL) are adapted to allow the higher transfer rate.

The slave does not acknowledge such a command but the input-filter time constants on the serial interface (SDA and SCL) are adapted to allow the higher transfer rate.

After a high-speed command, the master transmits the slave address in order to invoke a data transfer. The bus keeps operating at the higher operating frequency until the master issues a STOP condition on the serial bus. Upon the reception of the STOP condition by the slave, the input filters are switched to their initial time constants, which allow lower transfer rates only.

Figure 28:
Summary of Bus Commands

Command	Address	Data Value
High Speed Command		0000 1xxx

6.3.10   General Call

A general call is issued by the master by transmitting the general call address (000 0000) with a low R/W bit. When this command is issued on the bus, the device acknowledges this command. The device also acknowledges the second byte but ignores the data. Subsequent bytes sent by the master during the general call are not acknowledged.

6.3.11   Start Byte

When the master transmits address 000 0000 and a high R/W bit ("START byte") the device acknowledges the address. The device then sends the MSB data byte and LSB data byte, where the data corresponds to the content of the register whose address has been last written to. After reset, this corresponds to the temperature register.

6.3.12   Timeout Function

The serial interface of the slave device is reset if the clock signal SCL is kept low for typ. 30 ms. Such a condition results in a release of the data line by the slave in case it has been pulled to low level. The slave remains inactive after a timeout and waits for a new START command invoked by the bus master. In order to prevent a timeout, the bus transfer rate must be higher than 1 kHz.

6.3.13   Bus Conditions

The following conditions occur on the serial bus, which is compatible to the I²C-Bus.

Bus Idle

The signals SDA and SCL are not actively driven and pulled to a high level by an external pull-up resistor.

Start Data Transfer

A transition of the SDA input from high to low level while the SCL signal is kept at high-level results in a START condition. Such a START condition must precede any data transfer.

Stop Data Transfer

A transition of the SDA input from low to high level while the SCL signal is kept at high-level results in a STOP condition. Any data transfer is finished by generating a STOP or START condition.

Data Transfer

The master device defines the number of data bytes between a START and STOP condition and there is no limitation of transmitted data.

If it is desired to read only a single MSB byte without the LSB byte, a termination of the data transfer can be provoked by issuing a START or STOP condition on the bus.

Acknowledge

It is mandatory for each slave device to respond with acknowledge if the device is addressed by the master. Acknowledge is indicated by pulling down the data line (SDA) while the clock signal (SCL) is high in the acknowledge clock phase. In order to avoid an unwanted START or STOP condition on the bus, setup and hold times must be met.

The master can signal an end of data transmission by transmitting a Not-Acknowledge on the last transmitted data byte by keeping the acknowledge bit at high level.

6.3.14   Timing Characteristics
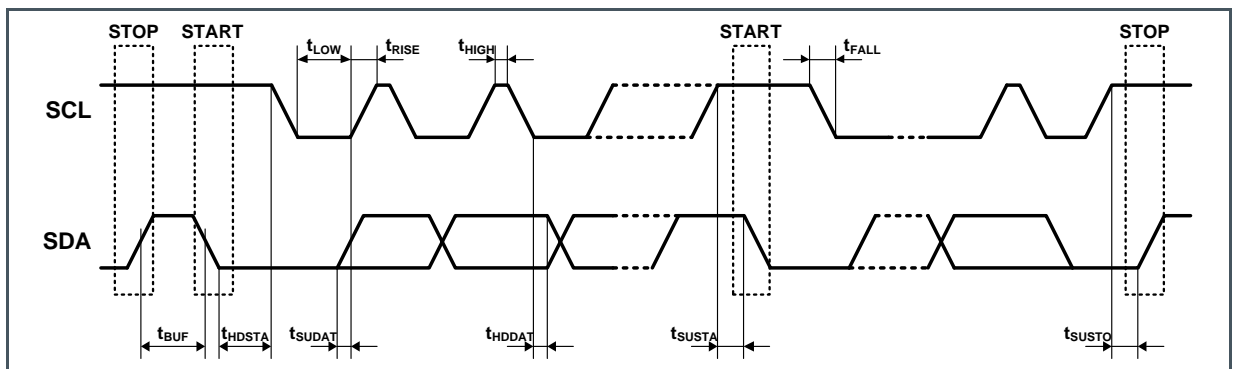
Figure 29:
Serial Interface Timing Diagram

Figure 30:
Bus Timing Specifications

Parameter	Symbol	Fast Mode		High Speed Mode		Unit
		Min	Max	Min	Max	
SCL Clock Frequency	f_{SCL}	0.001	0.4	0.001	3.4	MHz
Bus free time between STOP and START condition	t_{BUF}	600		160		ns
Hold time after repeated START condition	t_{HDSTA}	100		100		ns
Repeated START condition setup time	t_{SUSTA}	100		100		ns
Data in hold time	t_{HDDAT}	10		10		ns
Data out hold time[1]	t_{DH}	100		100		ns
Data setup time	t_{SUDAT}	100		10		ns
SCL clock low period	t_{LOW}	1300		160		ns
SCL clock high period	t_{HIGH}	600		60		ns
Clock/Data fall time	t_F		300		160	ns
Clock/Data rise time	t_R		300		160	ns
Clock/Data rise time for SCL≤100 kHz	t_R		1000			ns

[1]   The device will hold the SDA line high for 100 ns during the falling edge of the SCL.

6.3.15   Timing Diagrams

The following timing diagrams depict the different bus operation modes and data transmission:
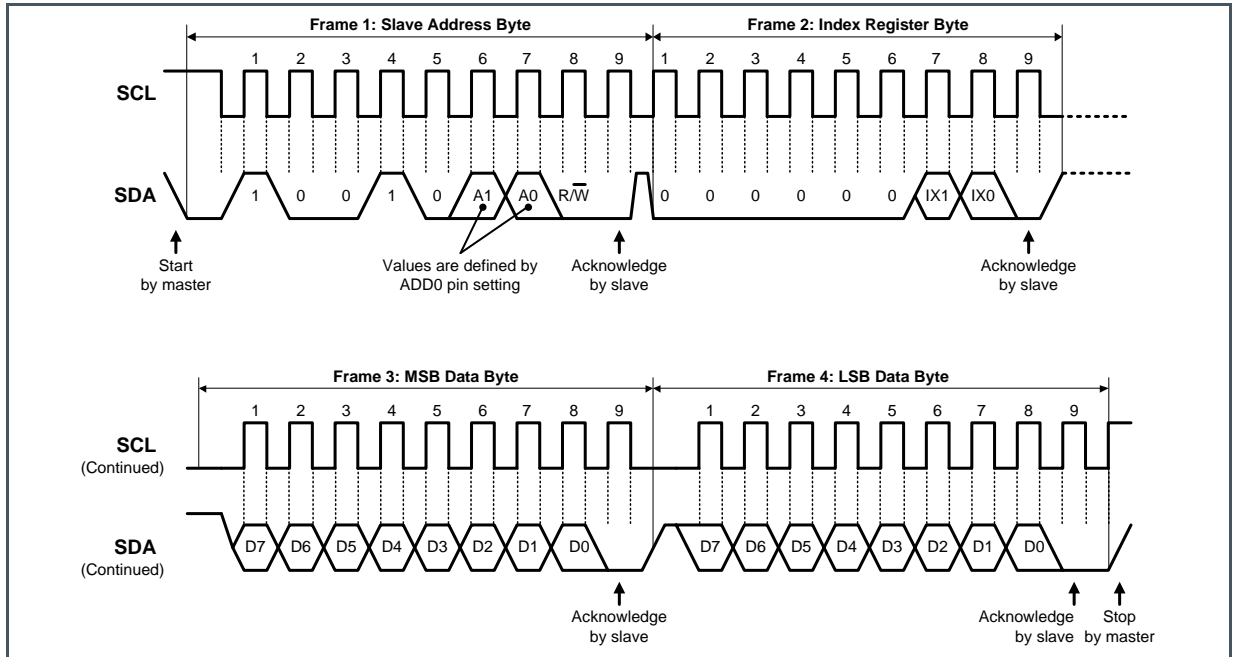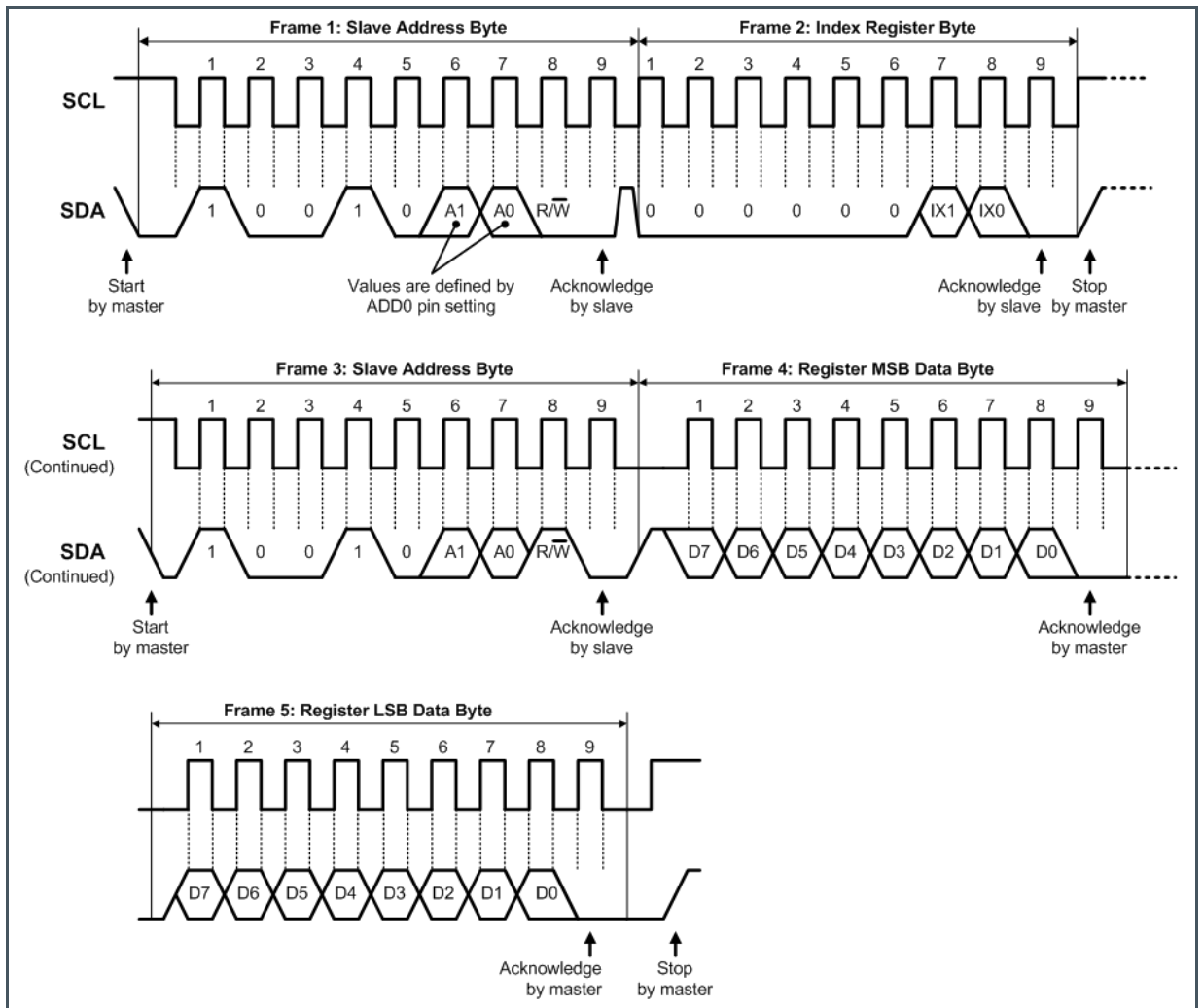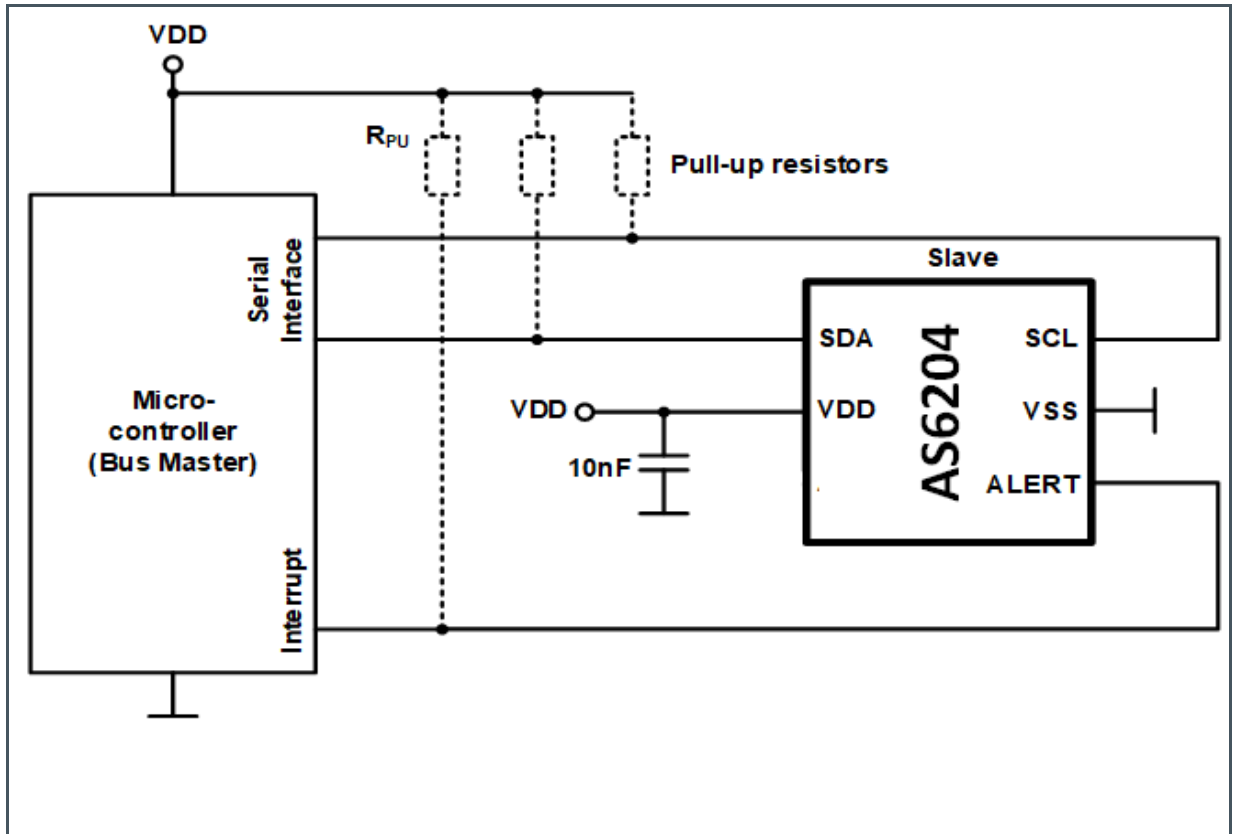
Figure 31:
Timing Diagram for Word Write

Figure 32:
Timing Diagram for Word Read

7 Application Information

Figure 33:
Typical Application for the AS6204 Temperature Sensor

In Figure 33 the connections of the AS6204 temperature sensors to a microcontroller and the supply voltage are shown.

The AS6204 is connected to a microcontroller via an I²C bus (SDA and SCL only). Additionally the Alert output can also be used for temperature monitoring (e.g. using the interrupt mode, refer to IM bit settings), an example is given in Figure 33 where the Alert output is connected to microcontroller.

The I²C of the AS6204 address of the can be selected by connecting the ADD0 pin to VDD or VSS (refer to Figure 26). This pin must not be left unconnected.

7.1 External Components
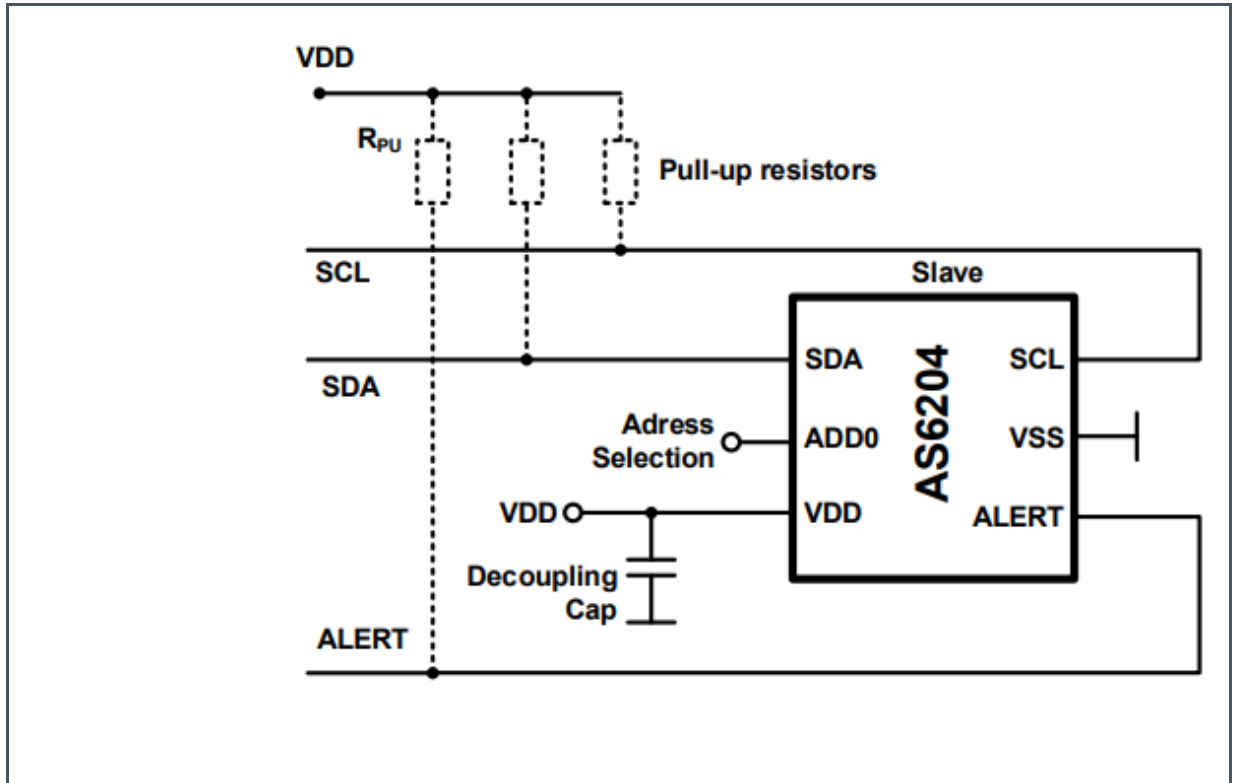
Figure 34:
Schematic with External Components

Figure 35:
Values for External Components

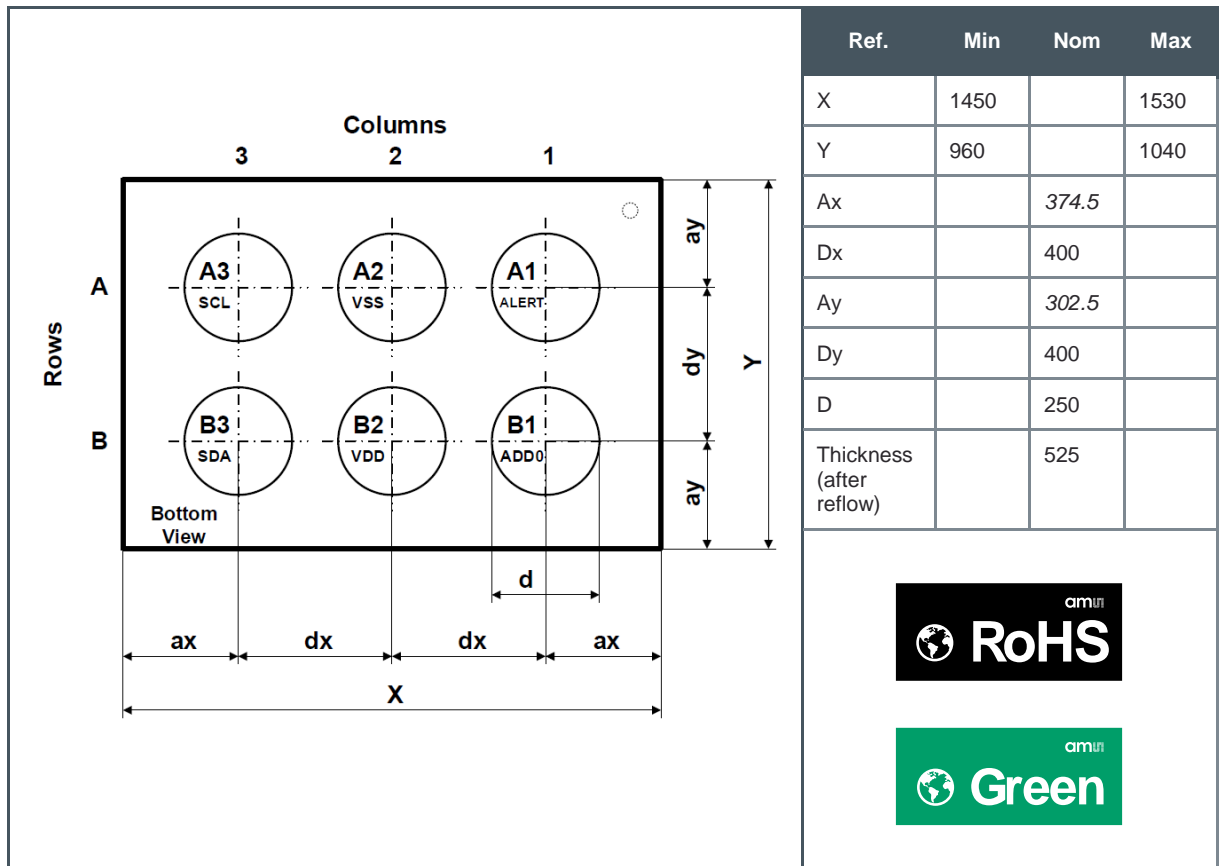| Parameter	Min	Max	Unit
Decoupling capacitor	10		nF
Pull up resistors	10	15	kΩ

In Figure 34 and Figure 35 the schematics and the recommended values for external components are shown.

The decoupling capacitor for the supply should have a value of at least 10 nF.

The pull up resistors on the serial interface and the interrupt also depend on the bus capacitance and on the clock speed.

8 Package Drawings & Markings

Figure 36:
WLCSP Package Outline Drawing

Ref.	Min	Nom	Max
X	1450		1530
Y	960		1040
Ax		*374.5*	
Dx		400	
Ay		*302.5*	
Dy		400	
D		250	
Thickness (after reflow)		525	

(1)   All dimensions are in micrometers. Angles in degrees.
(2)   Dimensioning and tolerance conform to ASME Y14.5M-1994.
(3)   This package contains no lead (Pb).
(4)   This drawing is subject to change without notice.

Figure 37:
WLCSP Package Marking/Code

XXXX   Trace code
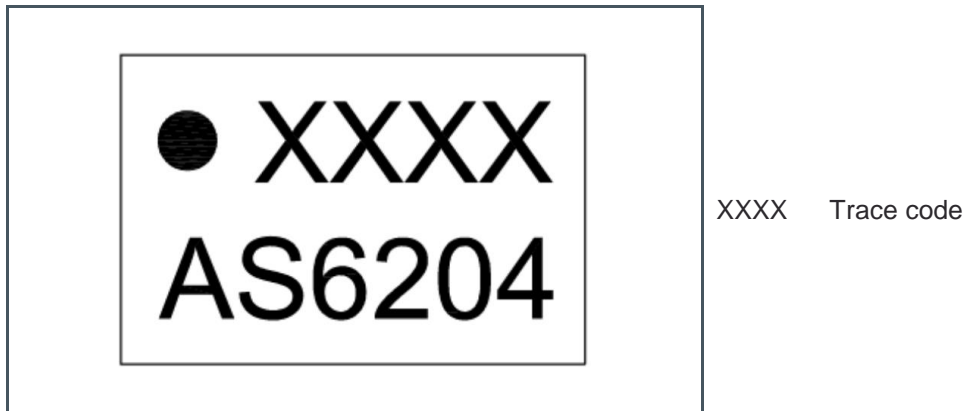
The actual date code is transformed in accordance to ASSY-346 to the four letter converted assembly code XXXX. Please refer to ASSY-346 for further information.

9 Revision Information

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
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Changes from previous version to current revision v4-00	Page
Updated Figure 5	8

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

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