Brief Description

The ZSPM9060 is IDT's next-generation, fully optimized, ultra-compact, integrated MOSFET plus driver power stage solution for high-current, high-frequency, synchronous buck DC-DC applications. The ZSPM9060 integrates a driver IC, two power MOSFETs, and a bootstrap Schottky diode into a thermally enhanced, ultra-compact 6x6mm package.

With an integrated approach, the complete switching power stage is optimized with regard to driver and MOSFET dynamic performance, system inductance, and power MOSFET $R_{DS(ON)}$. The ZSPM9060 uses innovative high-performance MOSFET technology, which dramatically reduces switch ringing, eliminating the need for a snubber circuit in most buck converter applications.

A driver IC with reduced dead times and propagation delays further enhances the performance. A thermal warning function warns of a potential over-temperature situation. The ZSPM9060 also provides a Skip Mode (SMOD#) for improved light-load efficiency. It also provides a tri-state 3.3V PWM input for compatibility with a wide range of PWM controllers.

The ZSPM9060 DrMOS is compatible with IDT's ZSPM1000, a leading-edge configurable digital power-management system controller for non-isolated point-of-load (POL) supplies.

Features

- Based on the Intel® 4.0 DrMOS standard
- High-current handling: up to 60A
- High-performance PQFN copper-clip package
- Tri-state 3.3V PWM input driver
- Skip Mode (low-side gate turn-off) input (SMOD#)
- Warning flag for over-temperature conditions
- Driver output disable function (DISB# pin)
- Internal pull-up and pull-down for SMOD# and DISB# inputs, respectively
- Integrated Schottky diode technology in the low-side MOSFET
- Integrated bootstrap Schottky diode
- Adaptive gate drive timing for shoot-through protection
- Under-voltage lockout (UVLO)
- Optimized for switching frequencies ≤ 1MHz

Benefits

- Fully optimized system efficiency: >93% peak
- Clean switching waveforms with minimal ringing
- 72% space-saving compared to conventional discrete solutions
- High current handling
- Optimized for use with IDT's ZSPM1000 true digital PWM controller

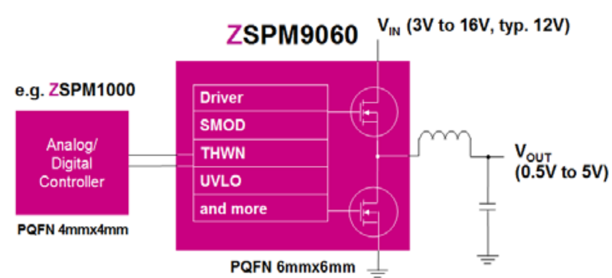
Available Support

- ZSPM8060-KIT: Open-Loop Evaluation Board for ZSPM9060

Physical Characteristics

- Operation temperature: -40°C to +125°C
- V_{IN}: 3V to 16V (typical 12V)
- I_{OUT}: up to 60A
- Low-profile SMD package: 6mmx6mm PQFN40
- IDT green packaging and RoHS compliant

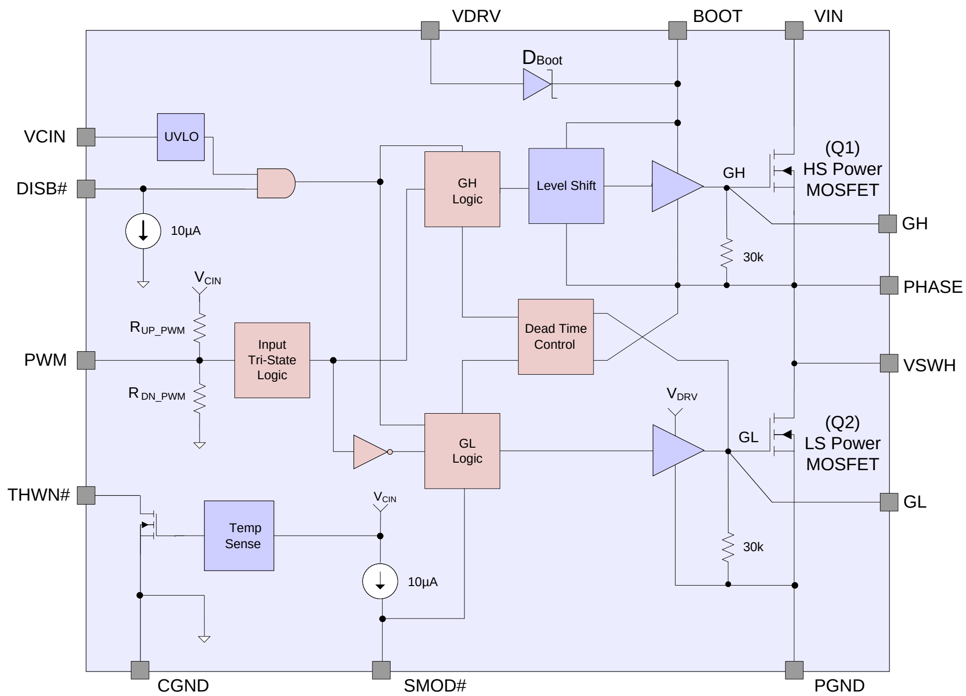
Typical Application



ZSPM9060 Block Diagram

Typical Applications

- High-performance gaming motherboards
- Compact blade servers, Vcore and non-Vcore DC-DC converters
- Desktop computers, Vcore and Non-Vcore DC-DC converters
- Workstations
- High-current DC-DC point-of-load converters
- Networking and telecom microprocessor voltage regulators
- Small form-factor voltage regulator modules



Ordering Information

Sales Code	Description	Package
ZSPM9060ZA1R	ZSPM9060 RoHS-Compliant Clip-Bond PQFN40 - Temperature range: -40 to +125 °C	Reel
ZSPM8060-KIT	Open-Loop Evaluation Board for ZSPM9060	Circuit Board

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1 IC Characteristics

1.1. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. The device might not function or be operable above the recommended operating conditions. Stresses exceeding the absolute maximum ratings might also damage the device. In addition, extended exposure to stresses above the recommended operating conditions might affect device reliability. IDT does not recommend designing to the "Absolute Maximum Ratings."

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Maximum Voltage to CGND – VCIN, VDRV, DISB#, PWM, SMOD#, GL, THWN# pins			-0.3	6.0	V
Maximum Voltage to PGND or CGND – VIN pin			-0.3	25.0	V
Maximum Voltage to VSWH or PHASE – BOOT, GH pins			-0.3	6.0	V
Maximum Voltage to CGND – BOOT, PHASE, GH pins			-0.3	25.0	V
Maximum Voltage to CGND or PGND – VSWH pin		DC only	-0.3	25.0	V
Maximum Voltage to PGND – VSWH pin		< 20ns	-8.0	28.0	V
Maximum Voltage to VDRV – BOOT pin				22.0	V
Maximum Voltage to VDRV – BOOT pin		< 20ns		25.0	V
Maximum Sink Current – THWN# pin	$I_{THWN\#}$		-0.1	7.0	mA
Maximum Average Output Current [1)]	$I_{OUT(AV)}$	f_{SW}=300kHz, V_{IN}=12V, V_{OUT}=1.0V		60	A
		f_{SW}=1MHz, V_{IN}=12V, V_{OUT}=1.0V		55	A
Junction-to-PCB Thermal Resistance	θ_{JPCB}			2.7	°C/W
Ambient Temperature Range	T_{AMB}		-40	+125	°C
Maximum Junction Temperature	T_{jMAX}			+150	°C
Storage Temperature Range	T_{STOR}		-55	+150	°C
Electrostatic Discharge Protection	ESD	Human Body Model, JESD22-A114	2000		V
		Charged Device Model, JESD22-C101	2500		V

1) $I_{OUT(AV)}$ is rated using a DrMOS Evaluation Board, T_A = 25°C, natural convection cooling. This rating is limited by the peak DrMOS temperature, T_{jMAX} = 150°C, and varies depending on operating conditions, PCB layout, and PCB board to ambient thermal resistance. This rating can be changed with different application settings.

1.2. Recommended Operating Conditions

The "Recommended Operating Conditions" table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. IDT does not recommend exceeding them or designing to the "Absolute Maximum Ratings."

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Control Circuit Supply Voltage	V_{CIN}		4.5	5.0	5.5	V
Gate Drive Circuit Supply Voltage	V_{DRV}		4.5	5.0	5.5	V
Output Stage Supply Voltage	V_{IN}		3.0	12.0	16.0 [1)]	V

1) Operating at high V_{IN} can create excessive AC overshoots on the VSWH-to-GND and BOOT-to-GND nodes during MOSFET switching transients. For reliable DrMOS operation, VSWH-to-GND and BOOT-to-GND must remain at or below the "Absolute Maximum Ratings" shown in the table above. Refer to sections 3 and 5 of this datasheet for additional information.

1.3. Electrical Parameters

Typical values are V_{IN} = 12V, V_{CIN} = 5V, V_{DRV} = 5V, and T_{AMB} = +25°C unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Basic Operation						
Quiescent Current	I_Q	I_Q=I_{VCIN}+I_{VDRV}, PWM=LOW or HIGH or float			2	mA
Under-Voltage Lock-Out						
UVLO Threshold	UVLO	V_{CIN} rising	2.9	3.1	3.3	V
UVLO Hysteresis	$UVLO_{\_Hyst}$			0.4		V
PWM Input						
Pull-Up Impedance	R_{UP_PWM}	V_{PWM}=5V VCIN = VDRV = 5V ±10%		26		kΩ
Pull-Down Impedance	R_{DN_PWM}	V_{PWM}=0V VCIN = VDRV = 5V ±10%		12		kΩ
PWM High-Level Voltage	V_{IH_PWM}	VCIN = VDRV = 5V ±10%	1.88	2.25	2.61	V
		VCIN = VDRV = 5V ±5%	2.00	2.25	2.50	V
Tri-state Upper Threshold	V_{TRI_HI}	VCIN = VDRV = 5V ±10%	1.84	2.20	2.56	V
		VCIN = VDRV = 5V ±5%	1.94	2.20	2.46	V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Tri-state Lower Threshold	V_{TRI_LO}	VCIN = VDRV = 5V ±10%	0.70	0.95	1.19	V
		VCIN = VDRV = 5V ±5%	0.75	0.95	1.15	V
PWM Low-Level Voltage	V_{IL_PWM}	VCIN = VDRV = 5V ±10%	0.62	0.85	1.13	V
		VCIN = VDRV = 5V ±5%	0.66	0.85	1.09	V
Tri-state Shutoff Time	$t_{D\_HOLD-OFF}$			160	200	ns
Tri-state Open Voltage	V_{HiZ_PWM}	VCIN = VDRV = 5V ±10%	1.40	1.60	1.90	V
		VCIN = VDRV = 5V ±5%	1.45	1.60	1.80	V
PWM Minimum Off Time	$t_{PWM-OFF\_MIN}$		120			ns
DISB# Input						
High-Level Input Voltage	$V_{IH\_DISB\#}$		2			V
Low-Level Input Voltage	$V_{IL\_DISB\#}$				0.8	V
Pull-Down Current	I_{PLD}			10		µA
Propagation Delay DISB#, GL Transition from HIGH to LOW	t_{PD_DISBL}	PWM=GND		25		ns
Propagation Delay DISB#, GL Transition from LOW to HIGH	t_{PD_DISBH}	PWM=GND		25		ns
SMOD# Input						
High-Level Input Voltage	$V_{IH\_SMOD\#}$		2			V
Low-Level Input Voltage	$V_{IL\_SMOD\#}$				0.8	V
Pull-Up Current	I_{PLU}			10		µA
Propagation Delay SMOD#, GL Transition from HIGH to LOW	t_{PD_SLGLL}	PWM=GND		10		ns
Propagation Delay SMOD#, GL Transition from LOW to HIGH	t_{PD_SHGLH}	PWM=GND		10		ns
Thermal Warning Flag						
Activation Temperature	T_{ACT}			150		°C
Reset Temperature	T_{RST}			135		°C
Pull-Down Resistance	R_{THWN}	I_{PLD}=5mA		30		Ω
250ns Timeout Circuit						
Timeout Delay Between GH Transition from HIGH to LOW and GL Transition from LOW to HIGH	$t_{D\_TIMEOUT}$	SW=0V		250		ns

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High-Side Driver (f_{SW} = 1000kHz, I_{OUT} = 30A, T_{AMB} = +25°C)						
Output Impedance, Sourcing	R_{SOURCE_GH}	Source Current=100mA		1		Ω
Output Impedance, Sinking	R_{SINK_GH}	Sink Current=100mA		0.8		Ω
Rise Time for GH=10% to 90%	t_{R_GH}			10		ns
Fall Time for GH=90% to 10%	t_{F_GH}			10		ns
LS to HS Deadband Time: GL going LOW to GH going HIGH, 1.0V GL to 10% GH	t_{D_DEADON}			15		ns
PWM LOW Propagation Delay: PWM going LOW to GH going LOW, V_{IL_PWM} to 90% GH	t_{PD_PLGHL}			20	30	ns
PWM HIGH Propagation Delay with SMOD# Held LOW: PWM going HIGH to GH going HIGH, V_{IH_PWM} to 10% GH	t_{PD_PHGHH}	SMOD# = LOW I_{D_LS}>0		30		ns
Propagation Delay Exiting Tri-state: PWM (from Tri-state) going HIGH to GH going HIGH, V_{IH_PWM} to 10% GH	t_{PD_TSGHH}			30		ns
Low-Side Driver (f_{SW} = 1000kHz, I_{OUT} = 30A, T_{AMB} = +25°C)						
Output Impedance, Sourcing	R_{SOURCE_GL}	Source Current=100mA		1		Ω
Output Impedance, Sinking	R_{SINK_GL}	Sink Current=100mA		0.5		Ω
Rise Time for GL = 10% to 90%	t_{R_GL}			30		ns
Fall Time for GL = 90% to 10%	t_{F_GL}			15		ns
HS to LS Deadband Time: SW going LOW to GL going HIGH, 2.2V SW to 10% GL	$t_{D\_DEADOFF}$			15		ns
PWM-HIGH Propagation Delay: PWM going HIGH to GL going LOW, V_{IH_PWM} to 90% GL	t_{PD_PHGLL}			10	25	ns
Propagation Delay Exiting Tri-state: PWM (from Tri-state) going LOW to GL going HIGH, V_{IL_PWM} to 10% GL	t_{PD_TSGLH}			20		ns
Boot Diode						
Forward-Voltage Drop	V_F	I_F=20mA		0.3		V
Breakdown Voltage	V_R	I_R=1mA	22			V

1.4. Typical Performance Characteristics

Test conditions: V_{IN}=12V, V_{OUT}=1.0V, V_{CIN}=5V, V_{DRV}=5V, L_{OUT}=250nH, T_{AMB}=25°C, and natural convection cooling, unless otherwise specified.

Figure 1.1 Safe Operating Area

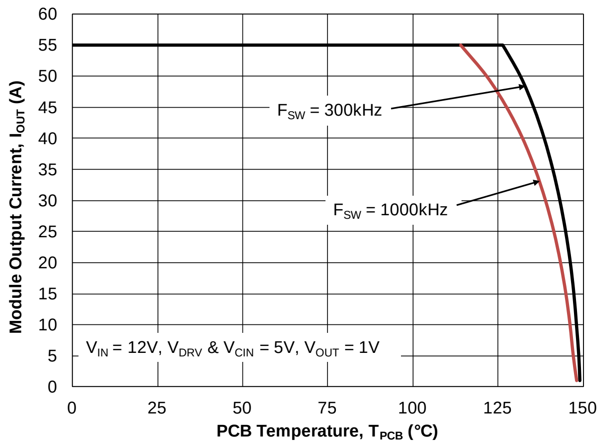


Figure 1.2 Module Power Loss vs. Output Current

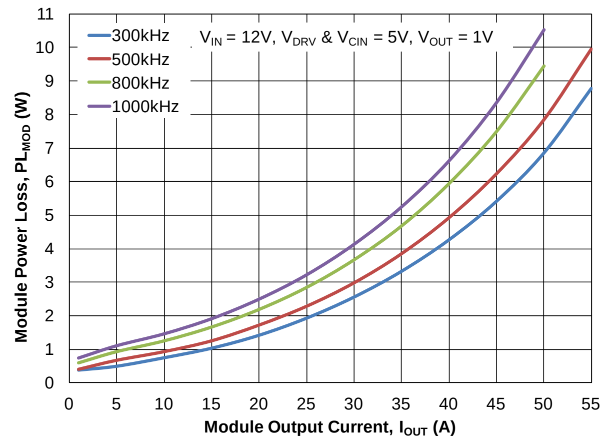


Figure 1.3 Power Loss vs. Switching Frequency

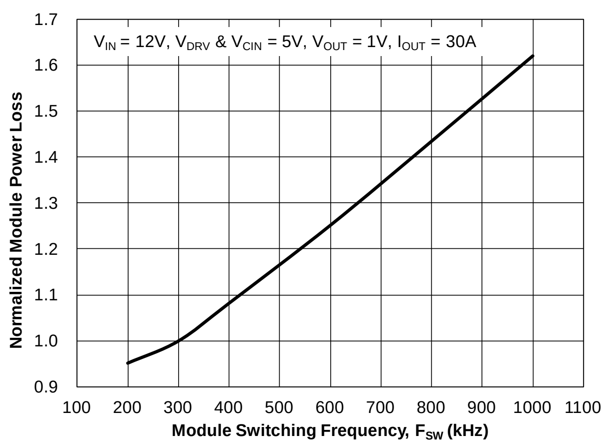


Figure 1.4 Power Loss vs. Input Voltage

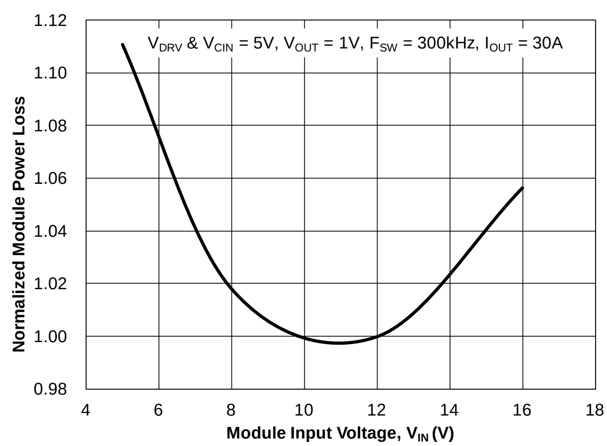


Figure 1.5 Power Loss vs. Driver Supply Voltage

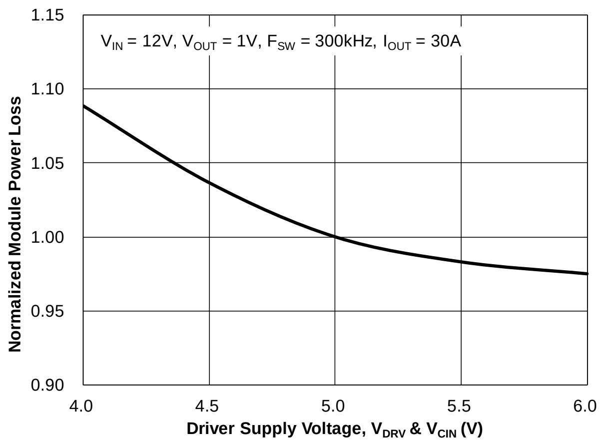


Figure 1.6 Power Loss vs. Output Voltage

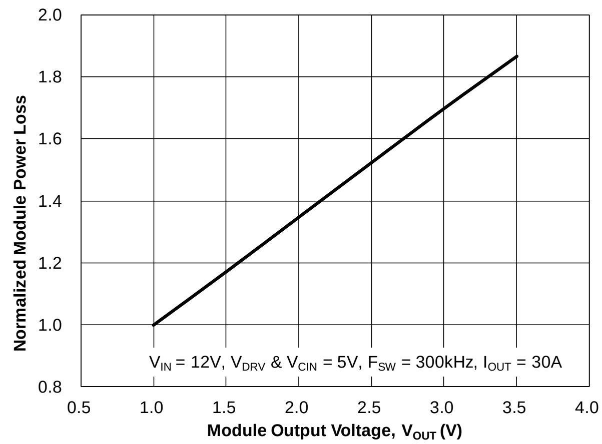


Figure 1.7 Power Loss vs. Output Inductance

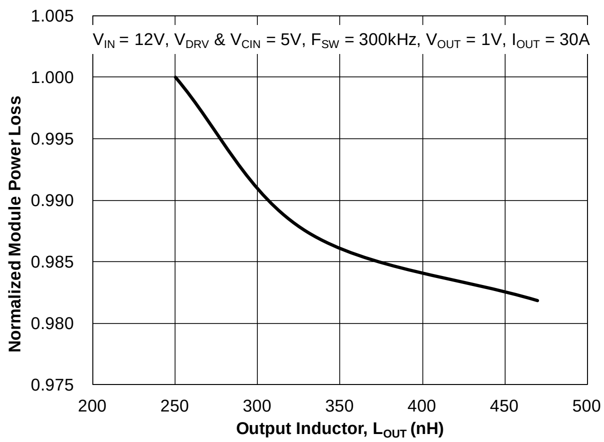


Figure 1.8 Driver Supply Current vs. Switch Frequency

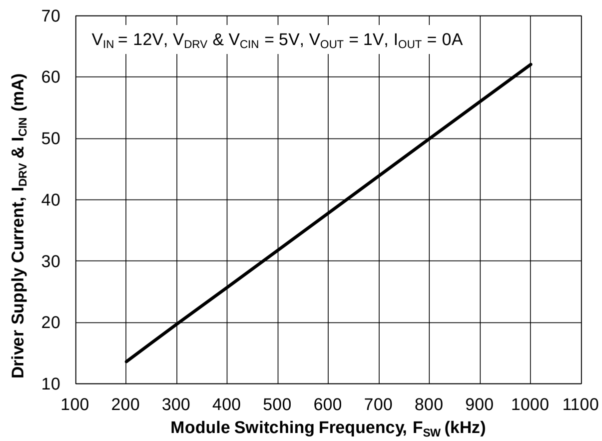


Figure 1.9 Driver Supply Current vs. Driver Supply Voltage

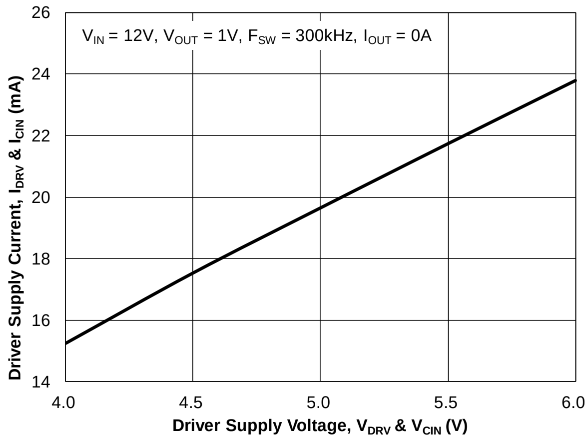


Figure 1.10 Driver Supply Current vs. Output Current

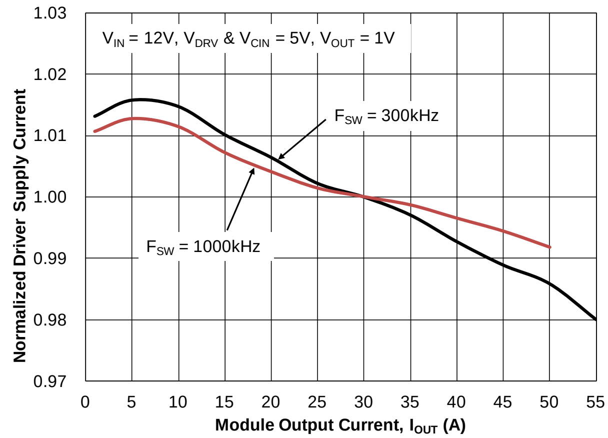


Figure 1.11 UVLO Threshold vs. Temperature

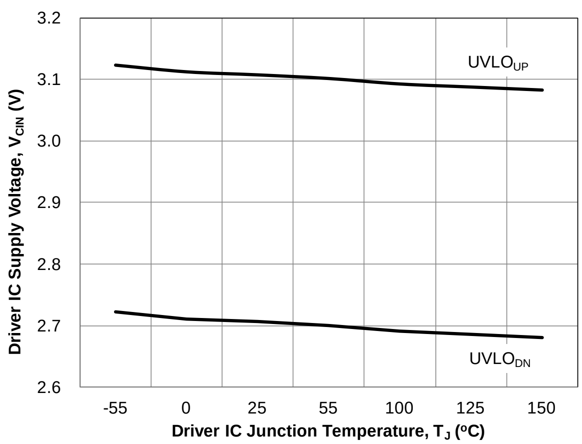


Figure 1.12 PWM Thresholds vs. Driver Supply Voltage

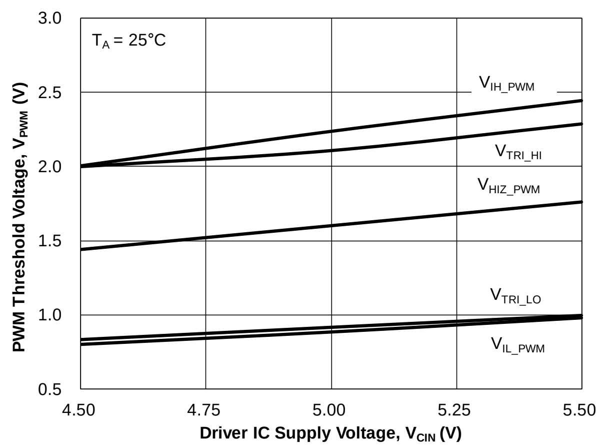


Figure 1.13 PWM Threshold vs. Temperature

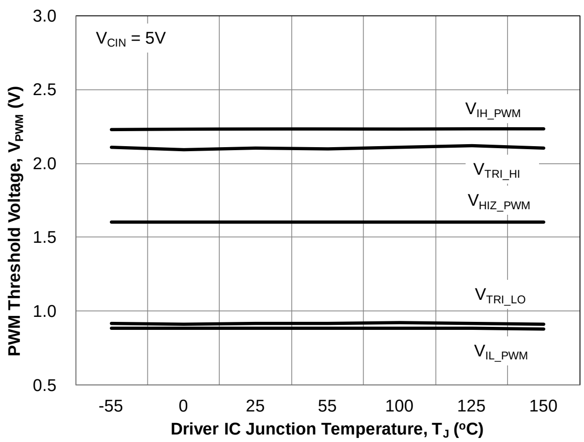


Figure 1.14 SMOD# Threshold vs. Driver Supply Voltage

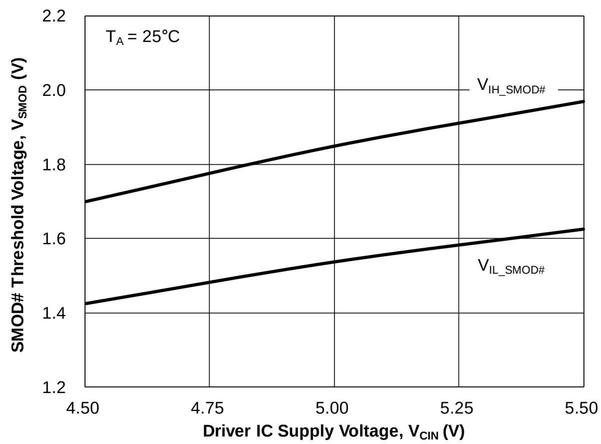


Figure 1.15 SMOD# Thresholds vs. Temperature

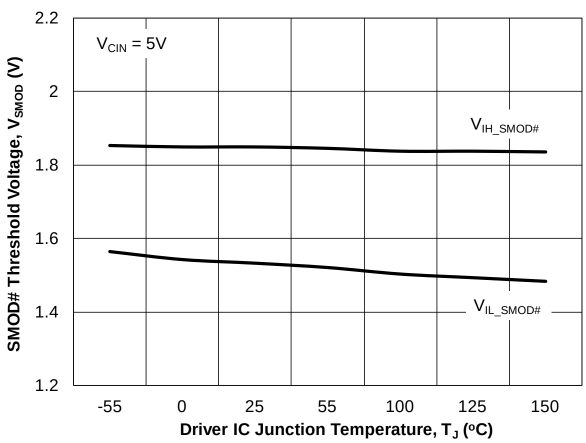


Figure 1.16 SMOD# Pull-Up Current vs. Temperature

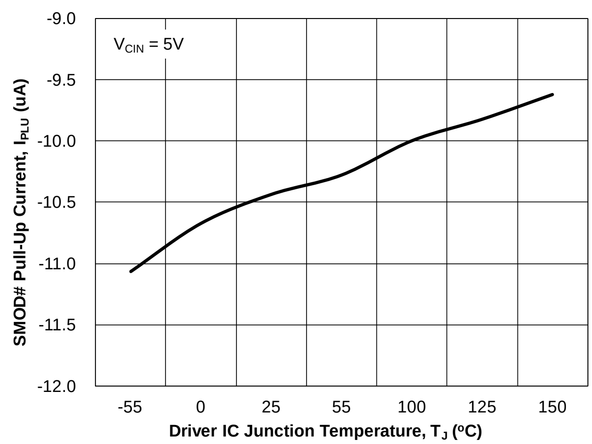


Figure 1.17 Disable (DISB#) Thresholds vs. Driver Supply Voltage

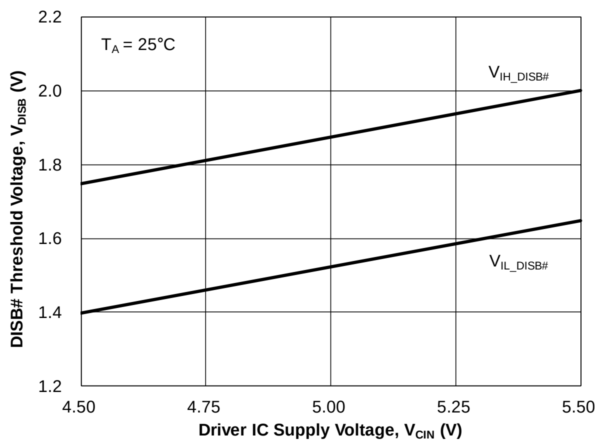


Figure 1.18 Disable (DISB#) Thresholds vs. Temperature

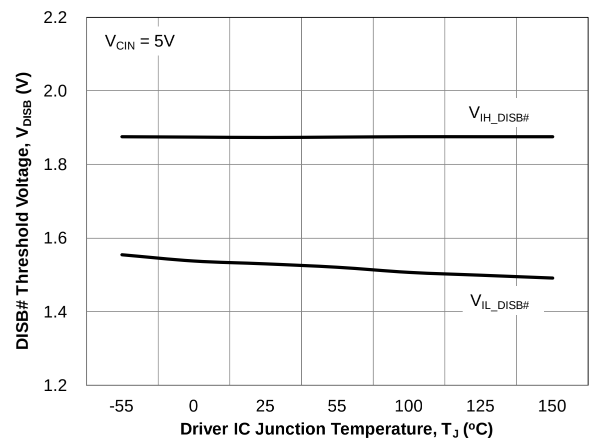


Figure 1.19 Disable Pull-Down Current vs. Temperature

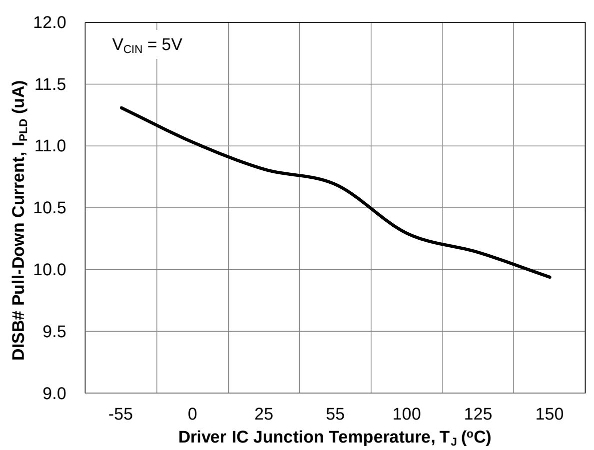
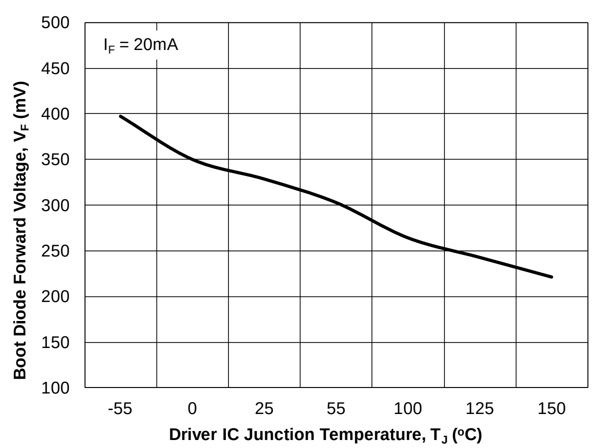


Figure 1.20 Boot Diode Forward Voltage vs. Temperature



2 Functional Description

The ZSPM9060 is a driver-plus-FET module optimized for the synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and the low-side MOSFETs. It is capable of driving speeds up to 1MHz.

Figure 2.1 Typical Application Circuit with PWM Control

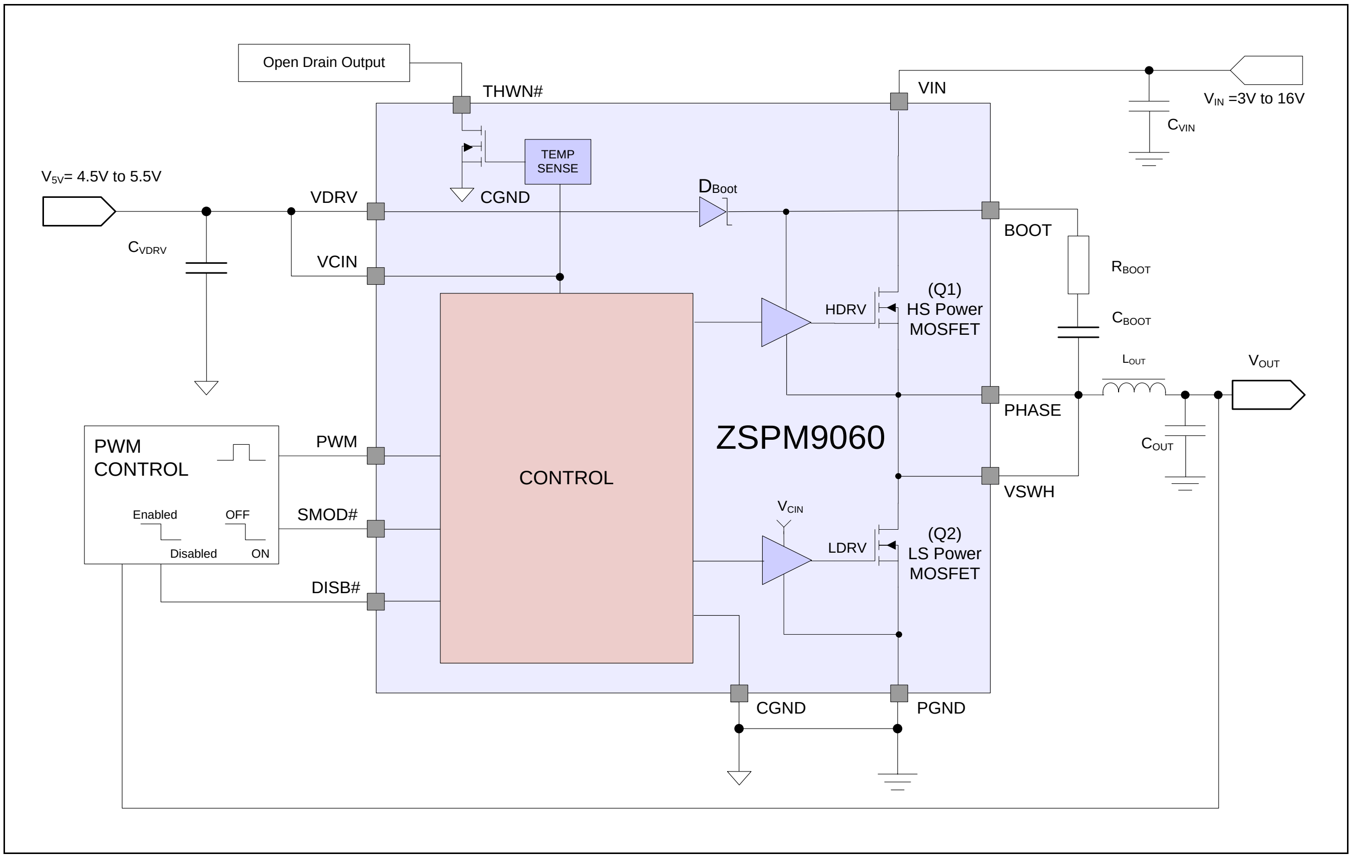
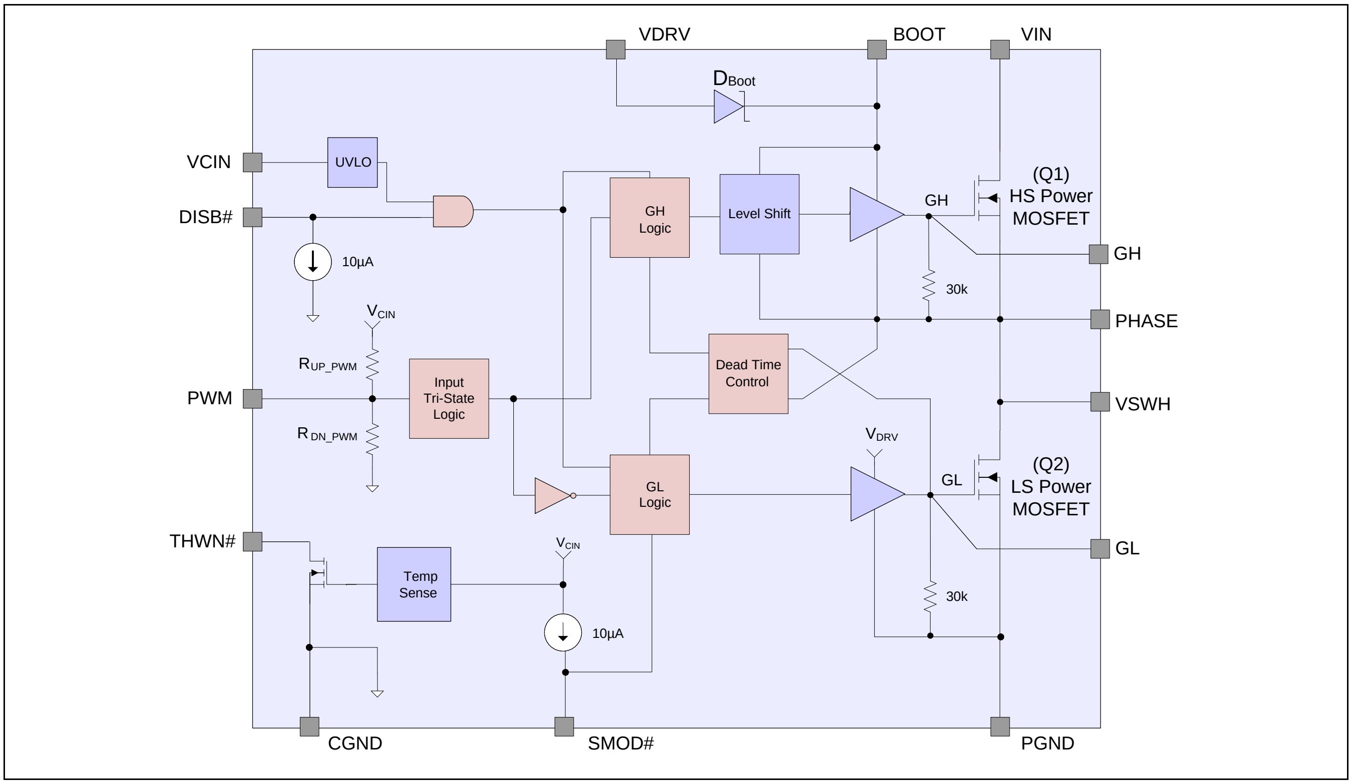


Figure 2.2 ZSPM9060 Block Diagram



2.1. VDRV and Disable (DISB#)

The VCIN pin is monitored by an under-voltage lockout (UVLO) circuit. When V_{CIN} rises above ~3.1V, the driver is enabled. When V_{CIN} falls below ~2.7V, the driver is disabled (GH, GL= 0; see Figure 2.2 and section 4.2). The driver can also be disabled by pulling the DISB# pin LOW (DISB# < V_{IL_DISB}), which holds both GL and GH LOW regardless of the PWM input state. The driver can be enabled by raising the DISB# pin voltage HIGH (DISB# > V_{IH_DISB}).

Table 2.1 UVLO and Disable Logic

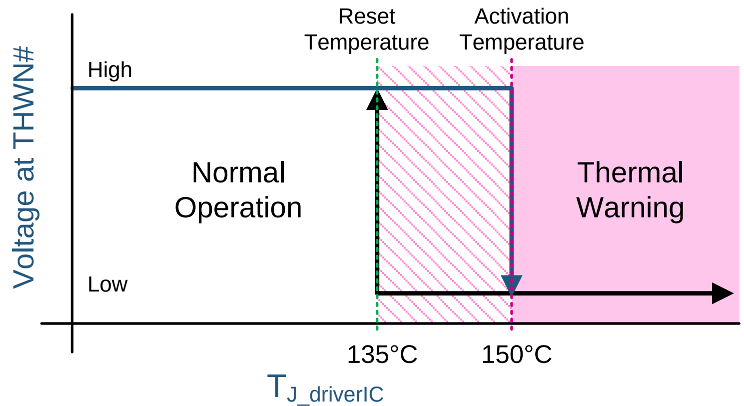
Note: DISB# internal pull-down current source is 10µA (typical).

UVLO	DISB#	Driver State
0	X	Disabled (GH=0, GL=0)
1	0	Disabled (GH=0, GL=0)
1	1	Enabled (see Table 2.2)
1	Open	Disabled (GH=0, GL=0)

2.2. Thermal Warning Flag (THWN#)

The ZSPM9060 provides a thermal warning flag (THWN#) to indicate over-temperature conditions. The thermal warning flag uses an open-drain output that pulls to CGND when the activation temperature (150°C) is reached. The THWN# output returns to the high-impedance state once the temperature falls to the reset temperature (135°C). For use, the THWN# output requires a pull-up resistor, which can be connected to VCIN. Note that THWN# does NOT disable the DrMOS module.

Figure 2.3 Thermal Warning Flag (THWN) Operation

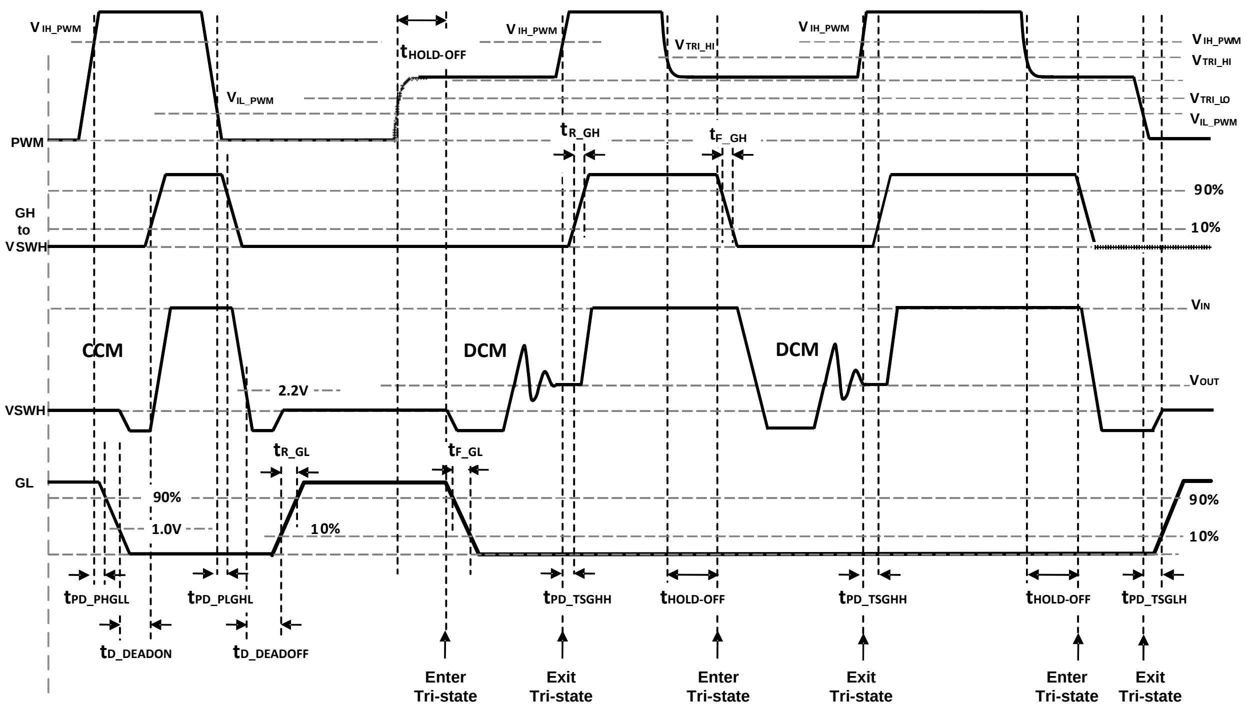


2.3. Tri-state PWM Input

The ZSPM9060 incorporates a tri-state 3.3V PWM input gate drive design. The tri-state gate drive has both logic HIGH and LOW levels, with a tri-state shutdown voltage window. When the PWM input signal enters and remains within the tri-state voltage window for a defined hold-off time ($t_{D\_HOLD-OFF}$), both GL and GH are pulled LOW. This feature enables the gate drive to shut down both high and low side MOSFETs using only one control signal. For example, this can be used for phase shedding in multi-phase voltage regulators.

When exiting a valid tri-state condition, the ZSPM9060 follows the PWM input command. If the PWM input goes from tri-state to LOW, the low-side MOSFET is turned on. If the PWM input goes from tri-state to HIGH, the high-side MOSFET is turned on, as illustrated in Figure 2.4. The ZSPM9060's design allows for short propagation delays when exiting the tri-state window (see section 1.3).

Figure 2.4 PWM and Tri-State Timing Diagram



Notes:

t_{PD_xxx} = Propagation delay from external signal (PWM, SMOD#, etc.) to IC generated signal; example: t_{PD_PHGLL} = PWM going HIGH to LS V_{GS} (GL) going LOW
t_{D_xxx} = Delay from IC generated signal to IC generated signal; example: t_{D_DEADON} = LS V_{GS} LOW to HS V_{GS} HIGH

PWM
t_{PD_PHGLL} = PWM rise to LS V_{GS} fall, V_{IH_PWM} to 90% LS V_{GS}
t_{PD_PLGHL} = PWM fall to HS V_{GS} fall, V_{IL_PWM} to 90% HS V_{GS}
t_{PD_PHGHH} = PWM rise to HS V_{GS} rise, V_{IH_PWM} to 10% HS V_{GS} (assumes SMOD# held Low)

Exiting Tri-state
t_{PD_TSGHH} = PWM tri-state to HIGH to HS V_{GS} rise, V_{IH_PWM} to 10% HS V_{GS}
t_{PD_TSGLH} = PWM tri-state to LOW to LS V_{GS} rise, V_{IL_PWM} to 10% LS V_{GS}

SMOD# (See Figure 2.5)
t_{PD_SLGLL} = SMOD# fall to LS V_{GS} fall, V_{IL_SMOD} to 90% LS V_{GS}
t_{PD_SHGLH} = SMOD# rise to LS V_{GS} rise, V_{IH_SMOD} to 10% LS V_{GS}

Dead Times
t_{D_DEADON} = LS V_{GS} fall to HS V_{GS} rise, LS-comp trip value (~1.0V GL) to 10% HS V_{GS}
$t_{D\_DEADOFF}$ = VSWH fall to LS V_{GS} rise, SW-comp trip value (~2.2V GL) to 10% LS V_{GS}

CCM = Continuous Conduction Mode
DCM = Discontinuous Conduction Mode

2.4. Adaptive Gate Drive Circuit

The low-side driver (GL) is designed to drive a ground-referenced low $R_{DS(ON)}$ N-channel MOSFET. The bias for GL is internally connected between VDRV and CGND. When the driver is enabled, the driver's output is 180° out of phase with the PWM input. When the driver is disabled (DISB#=0V), GL is held LOW.

The high-side driver (GH) is designed to drive a floating N-channel MOSFET. The bias voltage for the high-side driver is developed by a bootstrap supply circuit consisting of the internal Schottky diode and external bootstrap capacitor (C_{BOOT}). During startup, the VSWH pin is held at PGND, allowing C_{BOOT} (see section 3.2) to charge to V_{DRV} through the internal diode. When the PWM input goes HIGH, GH begins to charge the gate of Q1, the high-side MOSFET. During this transition, the charge is removed from C_{BOOT} and delivered to the gate of Q1. As Q1 turns on, V_{SWH} rises to V_{IN}, forcing the BOOT pin to V_{IN} + V_{BOOT}, which provides sufficient V_{GS} enhancement for Q1.

To complete the switching cycle, Q1 is turned off by pulling GH to V_{SWH}. C_{BOOT} is then recharged to V_{DRV} when V_{SWH} falls to PGND. The GH output is in-phase with the PWM input. The high-side gate is held LOW when the driver is disabled or the PWM signal is held within the tri-state window for longer than the tri-state hold-off time, $t_{D\_HOLD\text{-}OFF}$.

The driver IC design ensures minimum MOSFET dead time while eliminating potential shoot-through (cross-conduction) currents. It senses the state of the MOSFETs and adjusts the gate drive adaptively to prevent simultaneous conduction. Figure 2.4 provides the relevant timing waveforms. To prevent overlap during the LOW-to-HIGH switching transition (Q2 off to Q1 on), the adaptive circuitry monitors the voltage at the GL pin. When the PWM signal goes HIGH, Q2 begins to turn off after a propagation delay (t_{PD_PHGLL}). Once the GL pin is discharged below ~1V, Q1 begins to turn on after adaptive delay t_{D_DEADON}.

To prevent overlap during the HIGH-to-LOW transition (Q1 off to Q2 on), the adaptive circuitry monitors the voltage at the GH-to-PHASE pin pair. When the PWM signal goes LOW, Q1 begins to turn off after a propagation delay (t_{PD_PLGHL}). Once the voltage across GH-to-PHASE falls below approximately 2.2V, Q2 begins to turn on after adaptive delay $t_{D\_DEADOFF}$.

2.5. Skip Mode (SMOD#)

The Skip Mode function allows higher converter efficiency under light-load conditions. When SMOD# is pulled LOW, the low-side MOSFET gate signal is disabled (held LOW), preventing discharging of the output capacitors as the filter inductor current attempts reverse current flow – also known as Diode Emulation Mode.

When the SMOD# pin is pulled HIGH, the synchronous buck converter works in Synchronous Mode. This mode allows gating on the low-side MOSFET. When the SMOD# pin is pulled LOW, the low-side FET is gated off. See the timing diagram in Figure 2.5 for further details. If the SMOD# pin is connected to the PWM controller, the controller can actively enable or disable SMOD# when the controller detects light-load operation via output current sensing. Normally the SMOD# pin is active LOW.

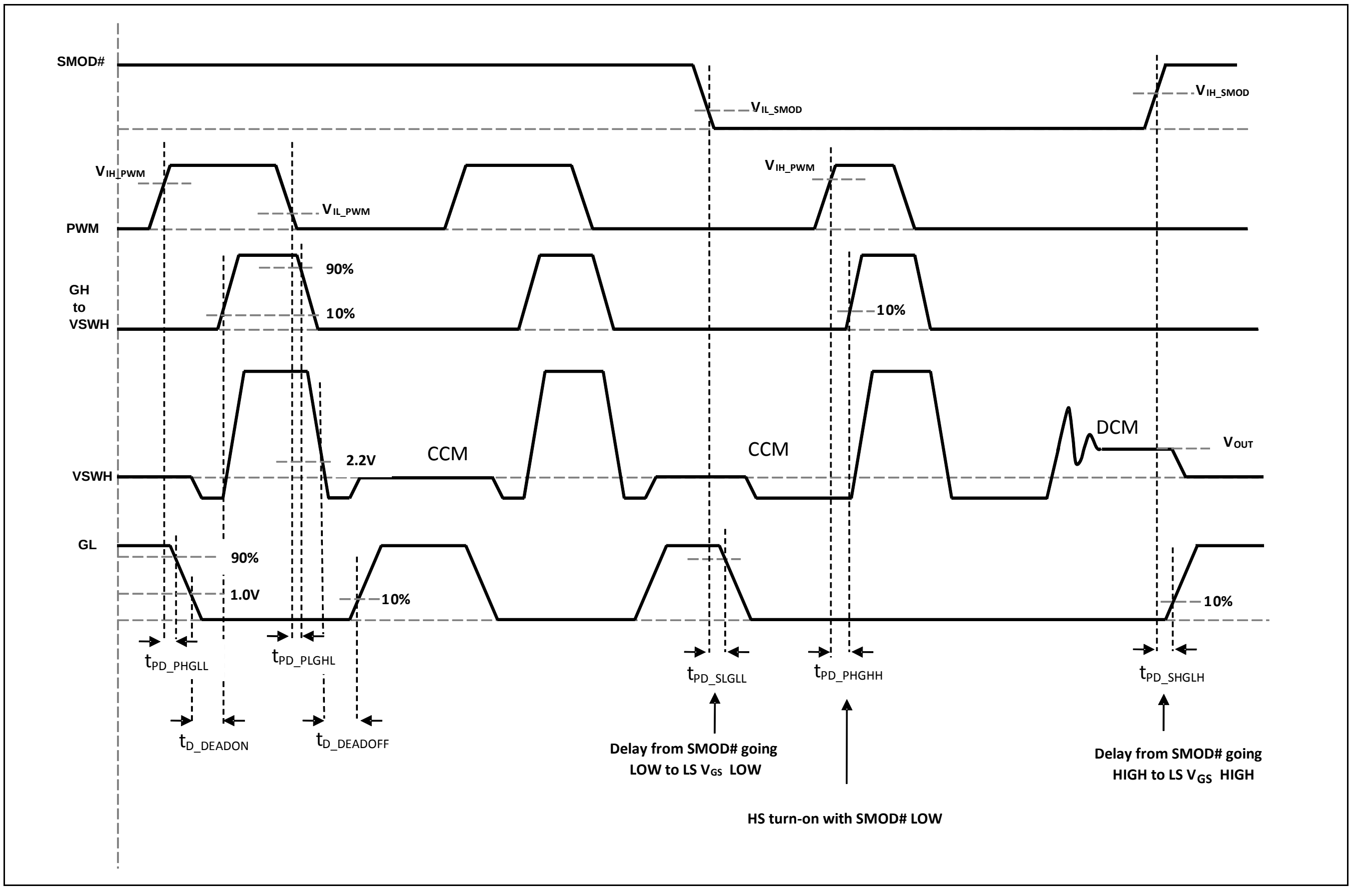
Table 2.2 SMOD# Logic

Note: The SMOD feature is intended to have a short propagation delay between the SMOD# signal and the low-side MOSFET V_{GS} response time to control diode emulation on a cycle-by-cycle basis.

DISB#	PWM	SMOD#	GH	GL
0	X	X	0	0
1	Tri-State	X	0	0
1	0	0	0	0
1	1	0	1	0
1	0	1	0	1
1	1	1	1	0

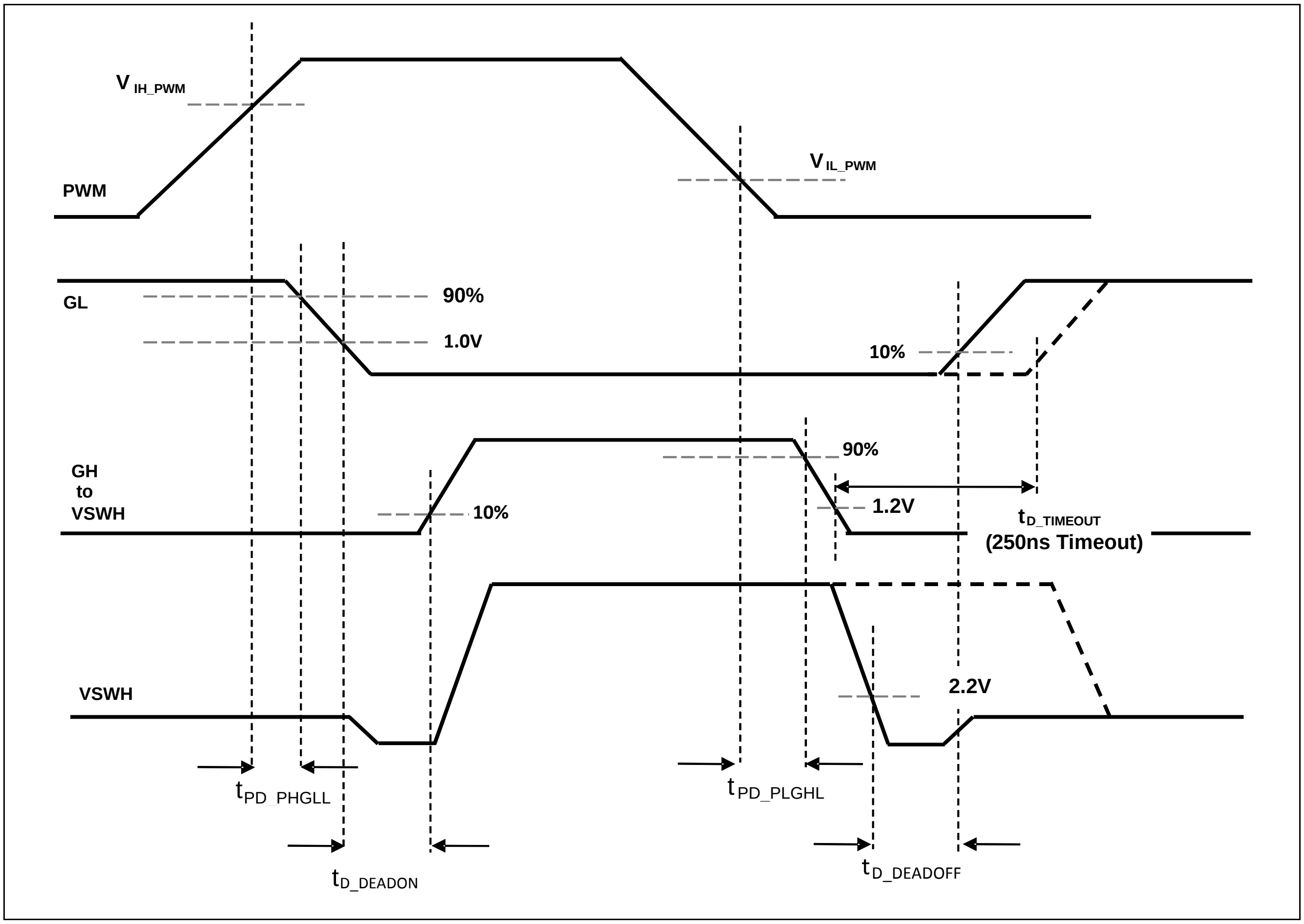
Figure 2.5 SMOD# Timing Diagram

See Figure 2.4 for the definitions of the timing parameters.



2.6. PWM

Figure 2.6 PWM Timing



3 Application Design

3.1. Supply Capacitor Selection

For the supply inputs (VCIN and VDRV), a local ceramic bypass capacitor is required to reduce noise and is used to supply the peak transient currents during gate drive switching action. Recommendation: use at least a 1µF capacitor with an X7R or X5R dielectric. Keep this capacitor close to the VCIN and VDRV pins, and connect it to the CGND ground plane with vias.

3.2. Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BOOT}), as shown in Figure 3.1. A bootstrap capacitance of 100nF using a X7R or X5R capacitor is typically adequate. A series bootstrap resistor might be needed for specific applications to improve switching noise immunity. The boot resistor might be required when operating with V_{IN} above 15V, and it is effective at controlling the high-side MOSFET turn-on slew rate and V_{SWH} overshoot. Typically, R_{BOOT} values from 0.5Ω to 3.0Ω are effective in reducing V_{SWH} overshoot.

3.3. VCIN Filter

The VDRV pin provides power to the gate drive of the high-side and low-side power MOSFETs. In most cases, VDRV can be connected directly to VCIN, which supplies power to the logic circuitry of the gate driver. For additional noise immunity, an RC filter can be inserted between VDRV and VCIN. Recommendation: use a 10Ω resistor (R_{VCIN}) between VDRV and VCIN and a 1µF capacitor (C_{VCIN}) from VCIN to CGND (see Figure 3.1).

Figure 3.1 ***V_{CIN} Filter Block Diagram***

Note: Blue lines indicate the optional recommended filter.

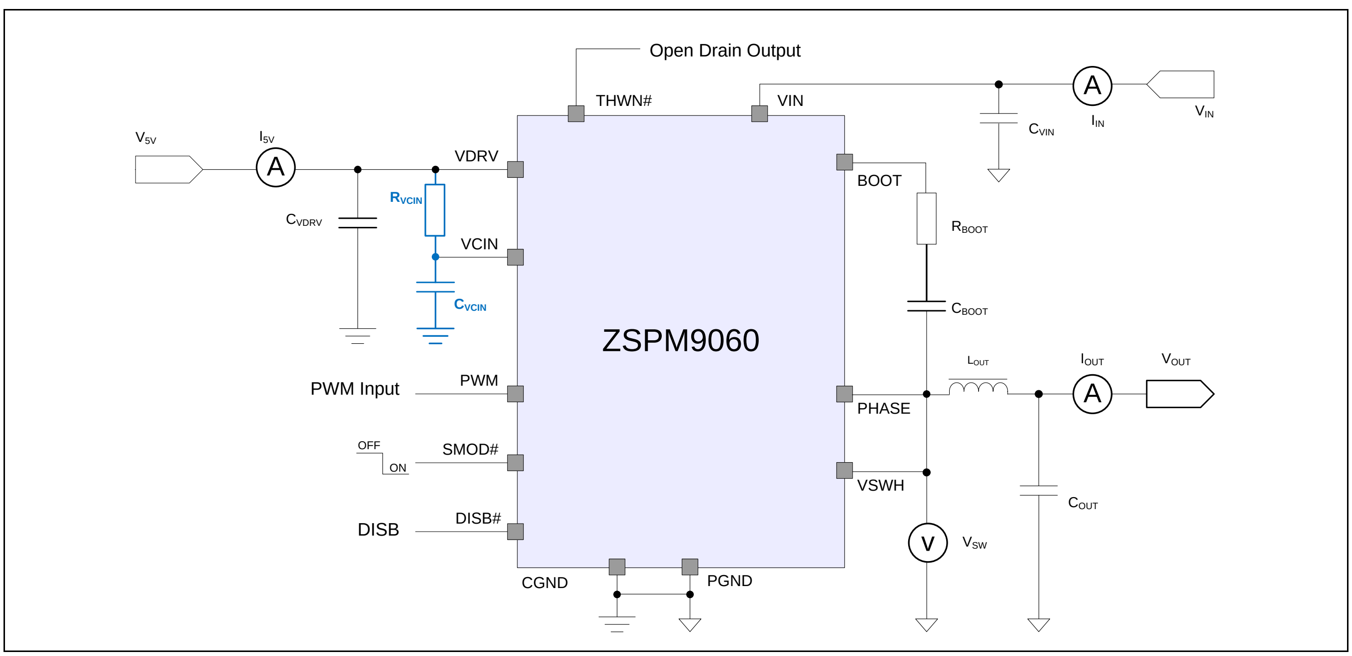
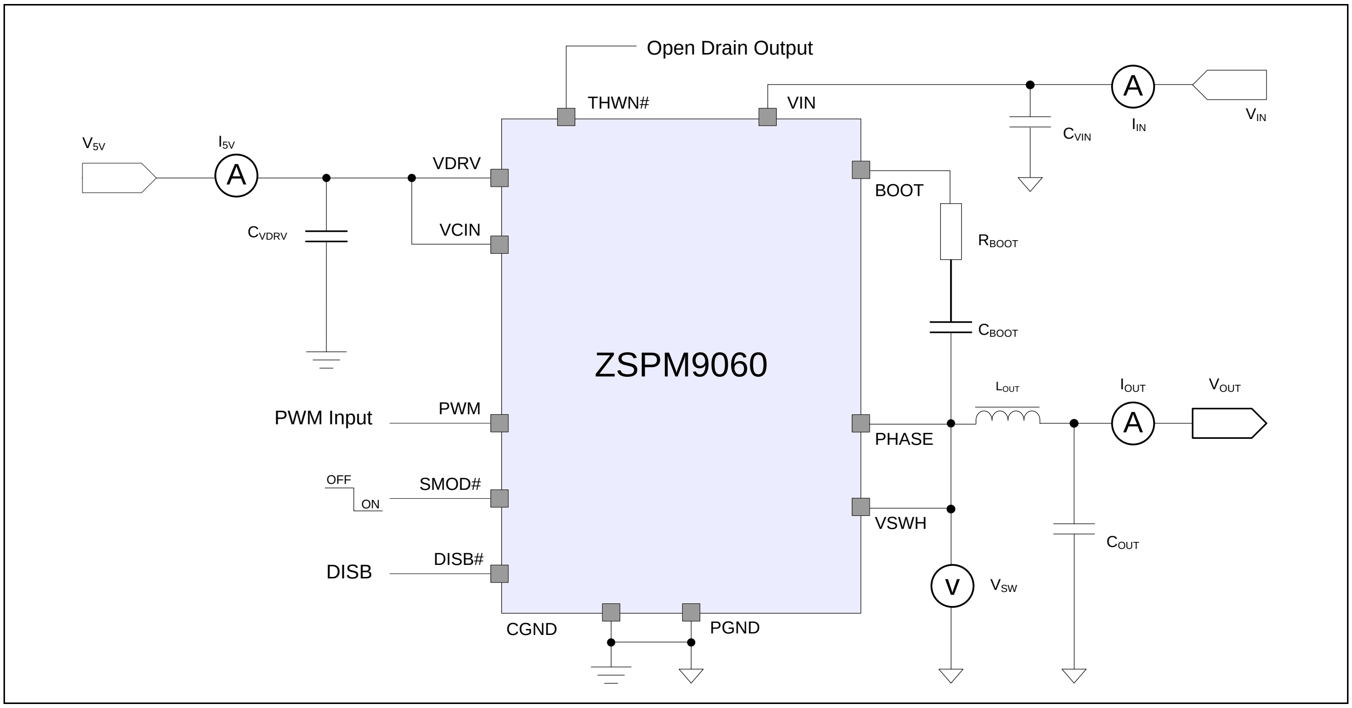


Figure 3.2 Power Loss Measurement Block Diagram



3.4. Power Loss and Efficiency Testing Procedures

The circuit in Figure 3.2 has been used to measure power losses in the following example. The efficiency has been calculated based on equations (1) to (7).

Power loss calculations in Watts:

$$P_{IN} = (V_{IN} * I_{IN}) + (V_{5V} * I_{5V}) \quad (1)$$

$$P_{SW} = (V_{SW} * I_{OUT}) \quad (2)$$

$$P_{OUT} = (V_{OUT} * I_{OUT}) \quad (3)$$

$$P_{LOSS\_MODULE} = (P_{IN} - P_{SW}) \quad (4)$$

$$P_{LOSS\_BOARD} = (P_{IN} - P_{OUT}) \quad (5)$$

Efficiency calculations:

$$EFF_{MODULE} = \left(100 * \frac{P_{SW}}{P_{IN}}\right)\% \qquad \textbf{(6)}$$

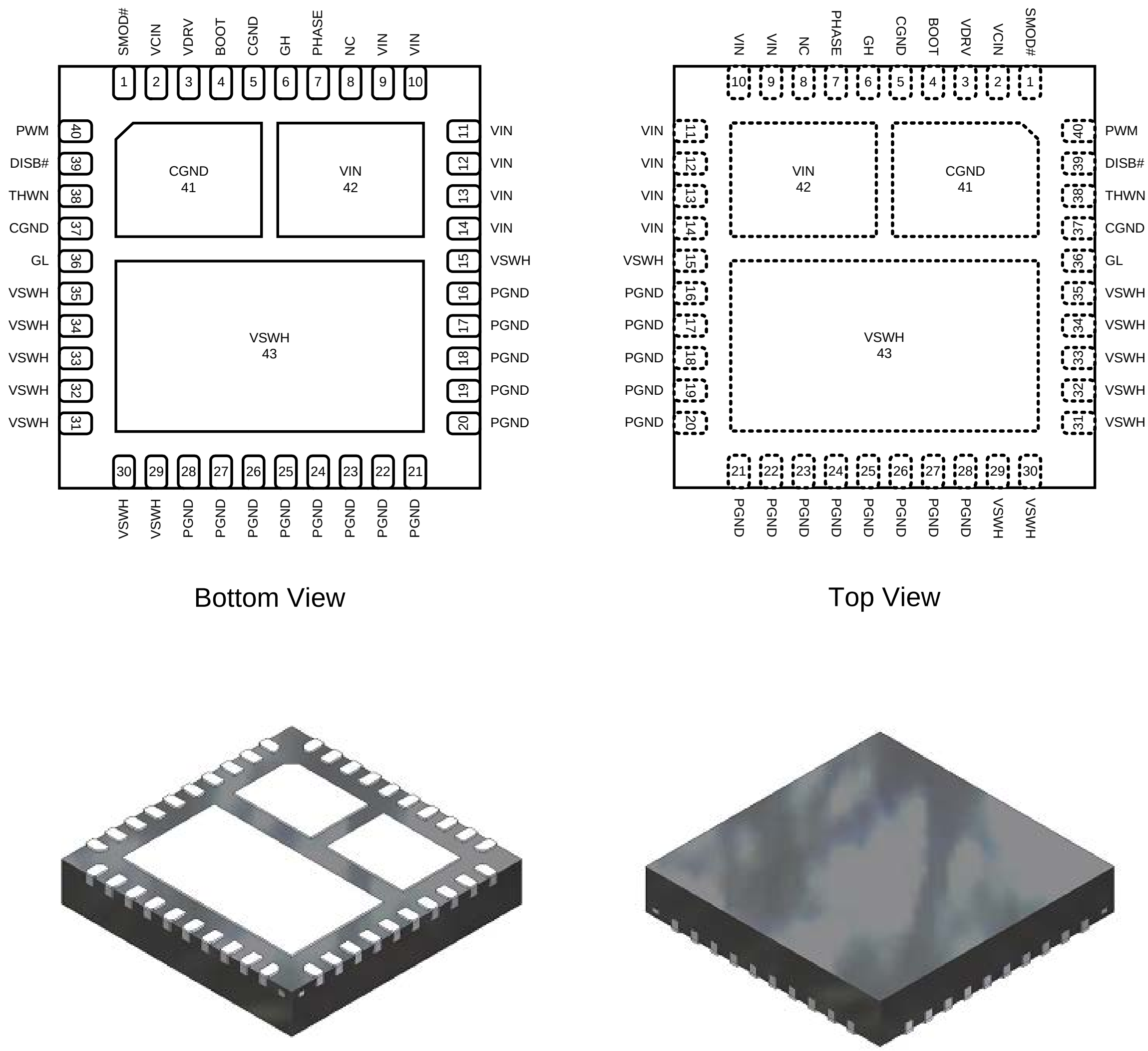
$$EFF_{BOARD} = \left(100 * \frac{P_{OUT}}{P_{IN}}\right)\% \qquad \textbf{(7)}$$

4 Pin Configuration and Package

4.1. Available Packages

The ZSPM9060 is available in a 40-lead clip-bond PQFN package. The pin-out is shown in Figure 4.1. See Figure 4.2 for the mechanical drawing of the package.

Figure 4.1 Pin-out PQFN40 Package

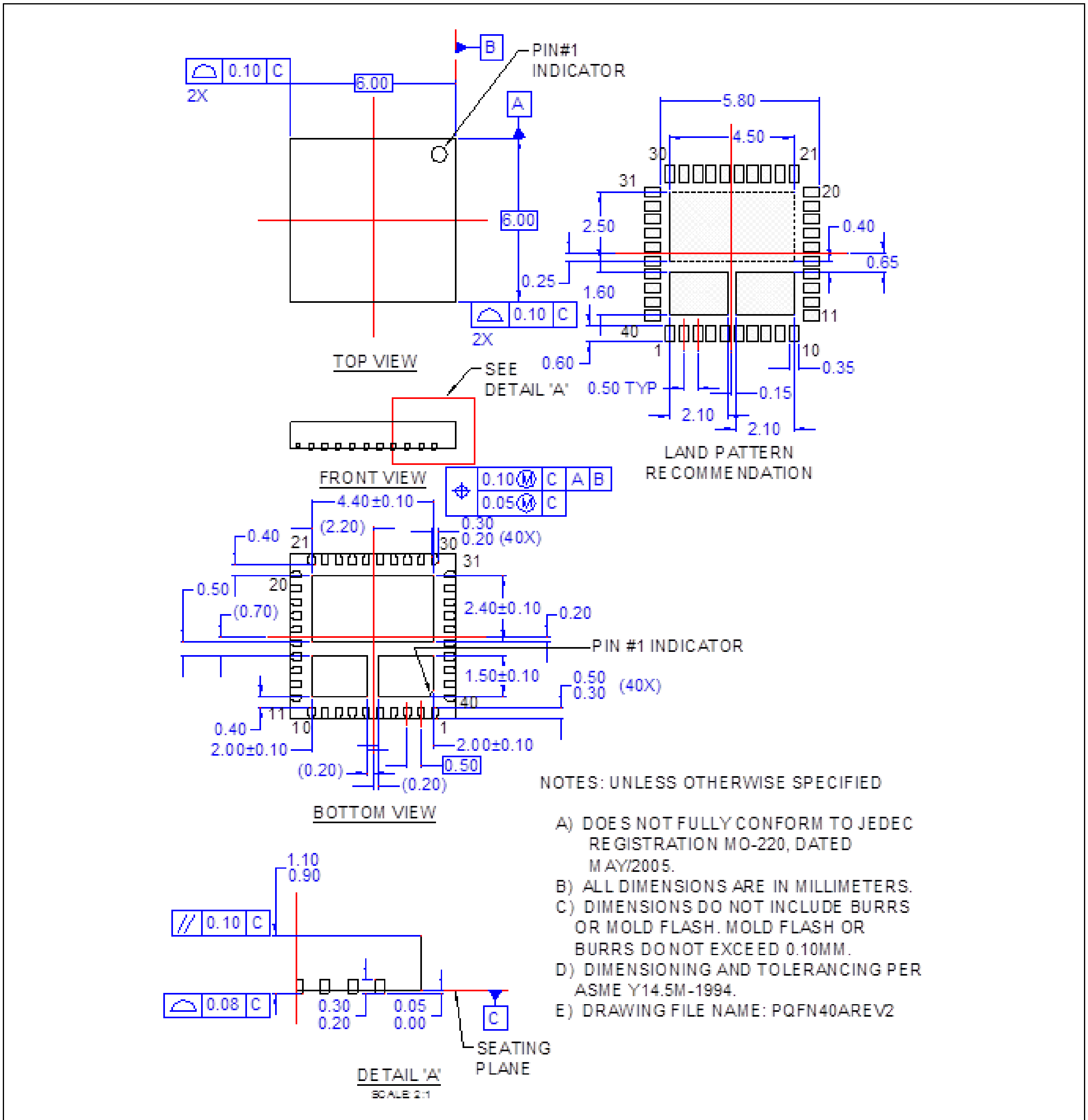


4.2. Pin Description

Pin	Name	Description
1	SMOD#	When SMOD#=HIGH, the low-side driver is the inverse of PWM input. When SMOD#=LOW, the low-side driver is disabled. This pin has a 10µA internal pull-up current source. Do not add a noise filter capacitor.
2	VCIN	IC bias supply. A 1µF (minimum) ceramic capacitor is recommended from this pin to CGND.
3	VDRV	Power for gate driver. A 1µF (minimum) X5R/X7R ceramic capacitor from this pin to CGND is recommended. Place it as close as possible to this pin.
4	BOOT	Bootstrap supply input. Provides voltage supply to the high-side MOSFET driver. Connect a bootstrap capacitor from this pin to PHASE.
5, 37, 41	CGND	IC ground. Ground return for driver IC.
6	GH	Gate high. For manufacturing test only. This pin must float: it must not be connected.
7	PHASE	Switch node pin for bootstrap capacitor routing; electrically shorted to VSWH pin.
8	NC	No connection. The pin is not electrically connected internally but can be connected to VIN for convenience.
9 - 14, 42	VIN	Input power voltage (output stage supply voltage).
15, 29 - 35, 43	VSWH	Switch node. Provides return for high-side bootstrapped driver and acts as a sense point for the adaptive shoot-through protection.
16 – 28	PGND	Power ground (output stage ground). Source pin of the low-side MOSFET.
36	GL	Gate low. For manufacturing test only. This pin must float. It must not be connected.
38	THWN#	Thermal warning flag, open collector output. When temperature exceeds the trip limit, the output is pulled LOW. THWN# does not disable the module.
39	DISB#	Output disable. When LOW, this pin disables the power MOSFET switching (GH and GL are held LOW). This pin has a 10µA internal pull-down current source. Do not add a noise filter capacitor.
40	PWM	PWM signal input. This pin accepts a tri-state 3.3V PWM signal from the controller.

4.3. Package Dimensions

Figure 4.2 Clip-Bond PQFN40 Physical Dimensions and Recommended Footprint



5 Circuit Board Layout Considerations

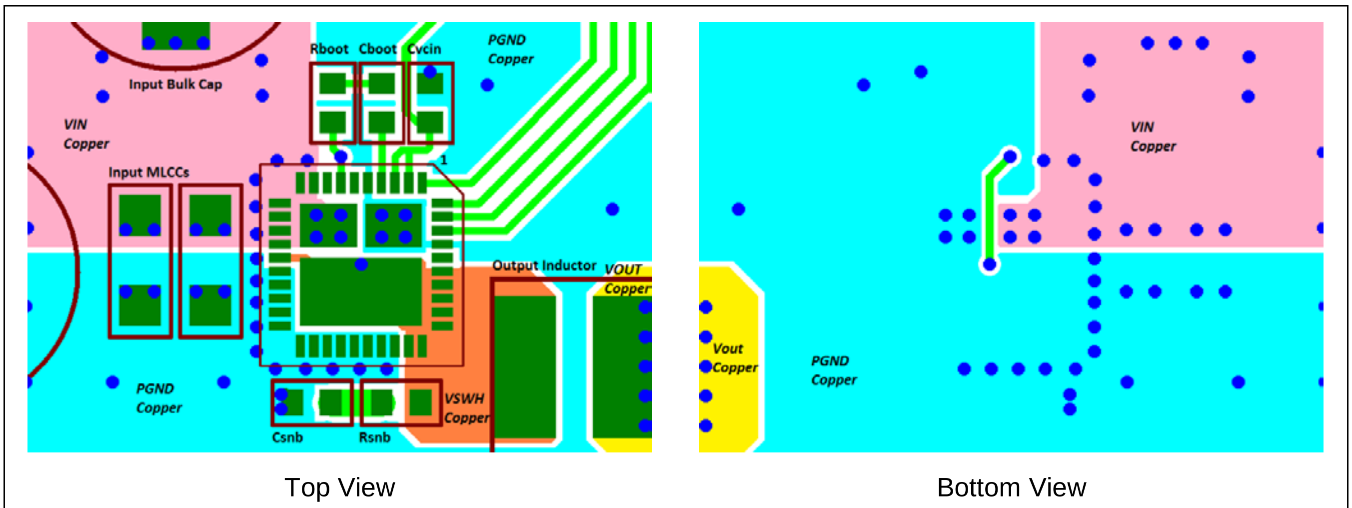
Figure 5.1 provides an example of a proper layout for the ZSPM9060 and critical components. All of the high-current paths, such as the V_{IN}, V_{SWH}, V_{OUT}, and GND copper traces, should be short and wide for low inductance and resistance. This technique achieves a more stable and evenly distributed current flow, along with enhanced heat radiation and system performance.

The following guidelines are recommendations for the printed circuit board (PCB) designer:

1. Input ceramic bypass capacitors must be placed close to the VIN and PGND pins. This helps reduce the high-current power loop inductance and the input current ripple induced by the power MOSFET switching operation.
2. The V_{SWH} copper trace serves two purposes. In addition to being the high-frequency current path from the DrMOS package to the output inductor, it also serves as a heat sink for the low-side MOSFET in the DrMOS package. The trace should be short and wide enough to present a low-impedance path for the high-frequency, high-current flow between the DrMOS and inductor to minimize losses and DrMOS temperature rise. Note that the VSWH node is a high-voltage and high-frequency switching node with a high noise potential. Care should be taken to minimize coupling to adjacent traces. Since this copper trace also acts as a heat sink for the lower MOSFET, the designer must balance using the largest area possible to improve DrMOS cooling with maintaining acceptable noise emission.
3. Locate the output inductor close to the ZSPM9060 to minimize the power loss due to the VSWH copper trace. Care should also be taken so that the inductor dissipation does not heat the DrMOS.
4. The power MOSFETs used in the output stage are effective for minimizing ringing due to fast switching. In most cases, no VSWH snubber is required. If a snubber is used, it should be placed close to the VSWH and PGND pins. The resistor and capacitor must be the proper size for the power dissipation.
5. VCIN, VDRV, and BOOT capacitors should be placed as close as possible the VCIN-to-CGND, VDRV-to-CGND, and BOOT-to-PHASE pin pairs to ensure clean and stable power. Routing width and length should be considered as well.
6. Include a trace from PHASE to VSWH to improve the noise margin. Keep the trace as short as possible.
7. The layout should include a placeholder to insert a small-value series boot resistor (R_{BOOT}) between the boot capacitor (C_{BOOT}) and the ZSPM9060 BOOT pin. The boot-loop size, including R_{BOOT} and C_{BOOT}, should be as small as possible. The boot resistor may be required when operating with V_{IN} above 15V. The boot resistor is effective for controlling the high-side MOSFET turn-on slew rate and V_{SWH} overshoot. R_{BOOT} can improve the noise operating margin in synchronous buck designs that might have noise issues due to ground bounce or high positive and negative V_{SWH} ringing. However, inserting a boot resistance lowers the DrMOS efficiency. Efficiency versus noise trade-offs must be considered. R_{BOOT} values from 0.5Ω to 3.0Ω are typically effective in reducing V_{SWH} overshoot.
8. The VIN and PGND pins handle large current transients with frequency components greater than 100MHz. If possible, these pins should be connected directly to the VIN and board GND planes. Important: the use of thermal relief traces in series with these pins is discouraged since this adds inductance to the power path. Added inductance in series with the VIN or PGND pin degrades system noise immunity by increasing positive and negative V_{SWH} ringing.

9. Connect the CGND pad and PGND pins to the GND plane copper with multiple vias for stable grounding. Poor grounding can create a noise transient offset voltage level between CGND and PGND. This could lead to faulty operation of the gate driver and MOSFETs.
10. Ringing at the BOOT pin is most effectively controlled by close placement of the boot capacitor. Do not add an additional BOOT to PGND capacitor; this could lead to excess current flow through the BOOT diode.
11. The SMOD# and DISB# pins have weak internal pull-up and pull-down current sources, respectively. Do NOT float these pins if avoidable. These pins should not have any noise filter capacitors.
12. Use multiple vias on each copper area to interconnect top, inner, and bottom layers to help distribute current flow and heat conduction. Vias should be relatively large and of reasonably low inductance. Critical high frequency components, such as R_{BOOT}, C_{BOOT}, the RC snubber, and the bypass capacitors should be located as close to the respective DrMOS module pins as possible on the top layer of the PCB. If this is not feasible, they should be connected from the backside through a network of low-inductance vias. Critical high-frequency components, such as R_{BOOT}, C_{BOOT}, RC snubber, and bypass capacitors, should be located as close to the respective ZSPM9060 module pins as possible on the top layer of the PCB. If this is not feasible, they can be connected from the backside through a network of low-inductance vias.

Figure 5.1 PCB Layout Example



6 Glossary

Term	Description
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
DISB	Driver Disable
HS	High Side
LS	Low Side
SMOD	Skip Mode Disable
THWN	Thermal Warning Flag

7 Ordering Information

Product Sales Code	Description	Package
ZSPM9060ZA1R	ZSPM9060 RoHS-Compliant Clip-Bond PQFN40 - Temperature range: -40°C to +125°C	Reel
ZSPM8060-KIT	Open-Loop Evaluation Board for ZSPM9060	Circuit Board

8 Related Documents

Document
ZSPM8060-KIT Open-Loop Evaluation Board User Guide

Visit IDT's website www.IDT.com or contact your nearest sales office for the latest version of these documents.

9 Document Revision History

Revision	Date	Description
1.00	October 24, 2012	First release
1.01	March 8, 2013	Minor edits and updates for imagery on cover and headers. Update for contact information.
	January 27, 2016	Changed to IDT branding.

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