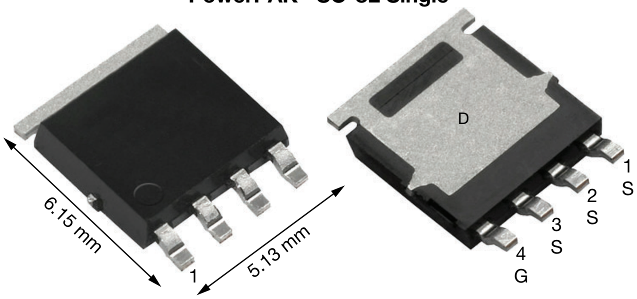
N-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω) Max.	I_D (A) [a, g]	Q_g (Typ.)
40	0.00235 at V_{GS} = 10 V	60	32 nC
	0.00320 at V_{GS} = 4.5 V	60	

PowerPAK® SO-8L Single



Top View   Bottom View

Ordering Information:
SiJA54DP-T1-GE3 (lead (Pb)-free and halogen-free)

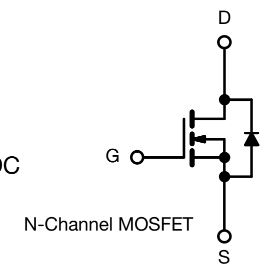
FEATURES

- TrenchFET® Gen IV power MOSFET
- Tuned for the lowest R_{DS}-Q_{oss} FOM
- 100 % R_g and UIS tested
- Q_{gd} / Q_{gs} ratio < 1 optimizes switching characteristics
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Synchronous rectification
- ORing
- High power density DC/DC
- VRMs and embedded DC/DC
- DC/AC inverters
- Load switch



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	+20, -16	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	60 [g]	A
	T_C = 70 °C		60 [g]	
	T_A = 25 °C		32.2 [b, c]	
	T_A = 70 °C		25.7 [b, c]	
Pulsed Drain Current (t = 100 μs)		I_{DM}	150	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	33.3	
	T_A = 25 °C		4 [b, c]	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	30	
Single Pulse Avalanche Energy		E_{AS}	45	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	36.7	W
	T_C = 70 °C		23.5	
	T_A = 25 °C		4.4 [b, c]	
	T_A = 70 °C		2.8 [b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +150	°C
Soldering Recommendations (Peak Temperature) [d, e]			260	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient [b, f]	t ≤ 10 s	R_{thJA}	24	28	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	2.5	3.4	

Notes

a. T_C = 25 °C.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under steady state conditions is 70 °C/W.
g. Package limited.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	40	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 μA	-	24	-	mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		-	-5.2	-	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 μA	1.1	-	2.4	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = +20 V, -16 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V	-	-	1	μA
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 55 °C	-	-	10	
On-State Drain Current [a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 10 V	30	-	-	A
Drain-Source On-State Resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 15 A	-	0.00195	0.00235	Ω
		V_{GS} = 4.5 V, I_D = 10 A	-	0.00265	0.00320	
Forward Transconductance [a]	g_{fs}	V_{DS} = 10 V, I_D = 15 A	-	106	-	S
Dynamic [b]						
Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	-	5300	-	pF
Output Capacitance	C_{oss}		-	707	-	
Reverse Transfer Capacitance	C_{rss}		-	105	-	
Total Gate Charge	Q_g	V_{DS} = 20 V,V_{GS} = 10 V, I_D = 10 A	-	69	104	nC
		V_{DS} = 20 V,V_{GS} = 4.5 V, I_D = 10 A	-	32	48	
Gate-Source Charge	Q_{gs}		-	13.5	-	
Gate-Drain Charge	Q_{gd}		-	6.9	-	
Output Charge	Q_{oss}	V_{DS} = 20 V, V_{GS} = 0 V	-	30.5	46	
Gate Resistance	R_g	f = 1 MHz	0.4	1.1	2.0	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 20 V, R_L = 2 Ω $I_D \cong$ 10 A, V_{GEN} = 10 V, R_g = 1 Ω	-	8	16	ns
Rise Time	t_r		-	8	16	
Turn-Off Delay Time	$t_{d(off)}$		-	28	56	
Fall Time	t_f		-	7	14	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 20 V, R_L = 2 Ω $I_D \cong$ 10 A, V_{GEN} = 4.5 V, R_g = 1 Ω	-	24	48	
Rise Time	t_r		-	69	138	
Turn-Off Delay Time	$t_{d(off)}$		-	23	46	
Fall Time	t_f		-	10	20	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C	-	-	33.3	A
Pulse Diode Forward Current (t = 100 μs)	I_{SM}		-	-	150	
Body Diode Voltage	V_{SD}	I_S = 5 A	-	0.72	1.1	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 10 A, dI/dt = 100 A/μs, T_J = 25 °C	-	44	88	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	58	116	nC
Reverse Recovery Fall Time	t_a		-	29	-	ns
Reverse Recovery Rise Time	t_b		-	15	-	

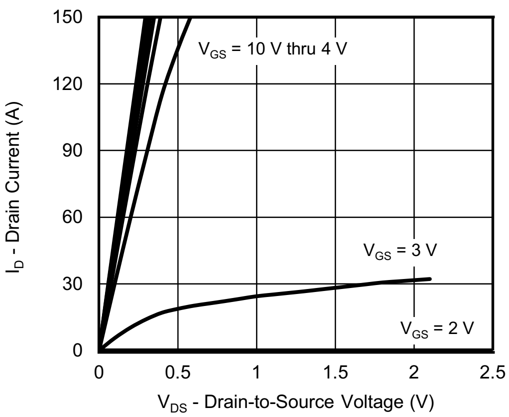
Notes

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.

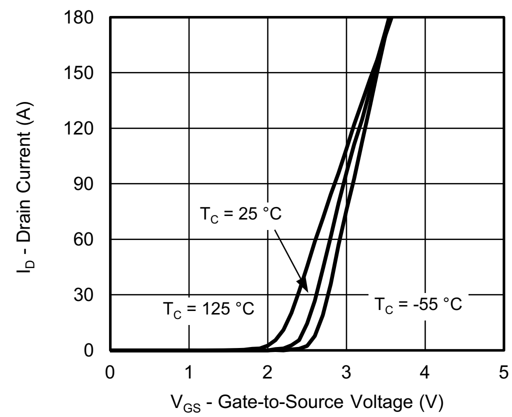
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

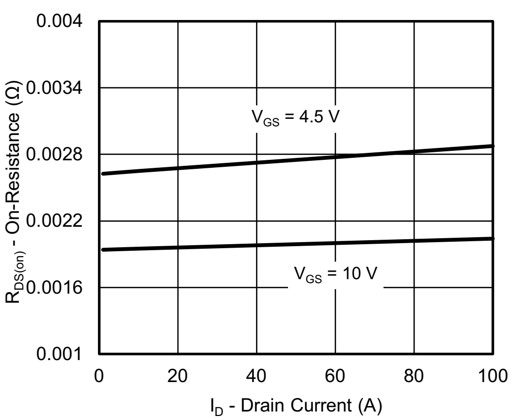
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



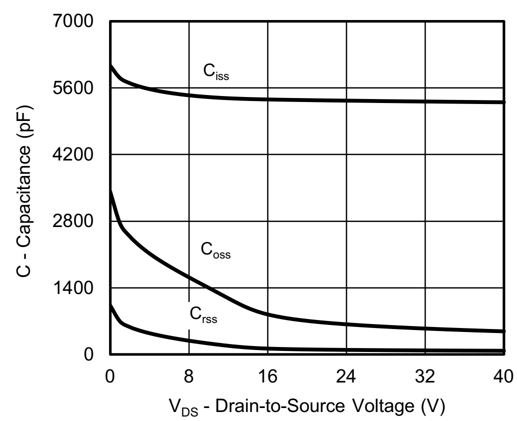
Output Characteristics



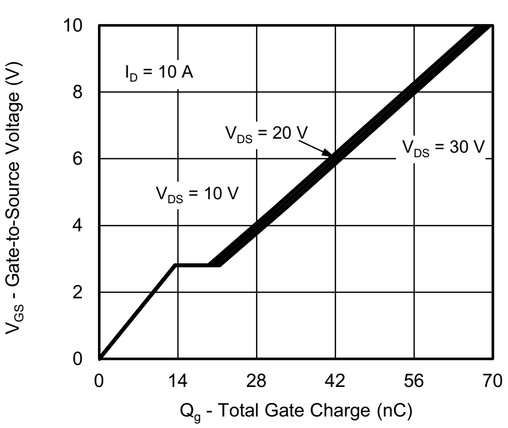
Transfer Characteristics



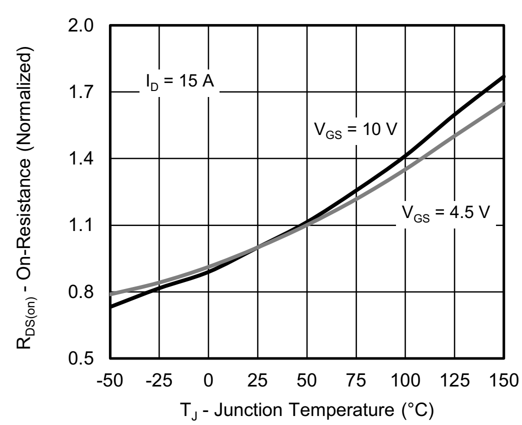
On-Resistance vs. Drain Current



Capacitance



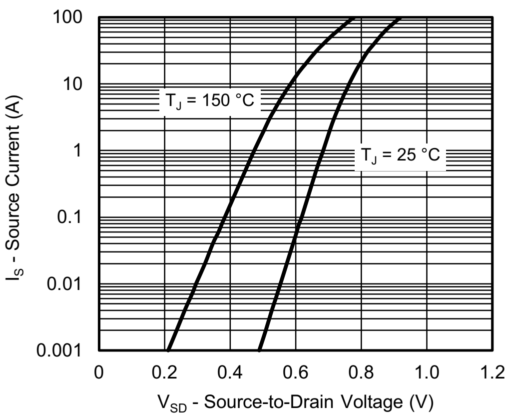
Gate Charge



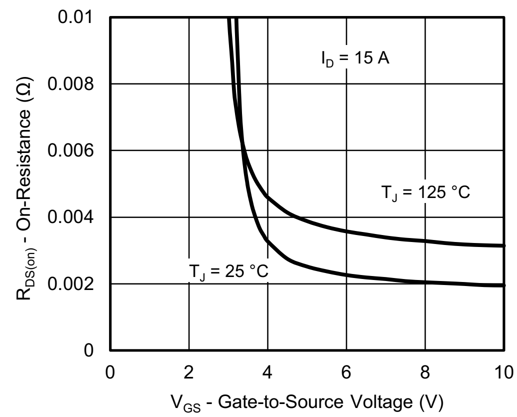
On-Resistance vs. Junction Temperature

For technical questions, contact: pmostechsupport@vishay.com

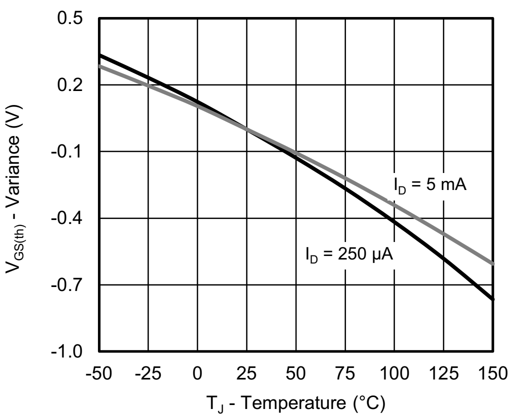
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



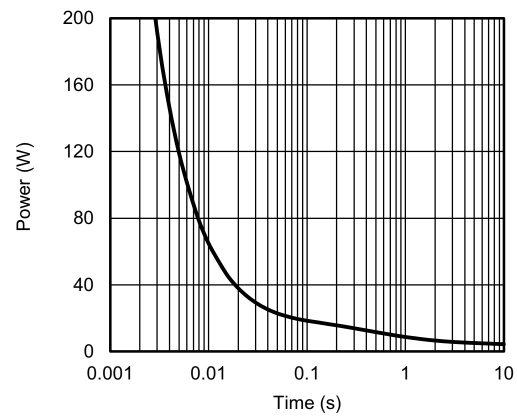
Source-Drain Diode Forward Voltage



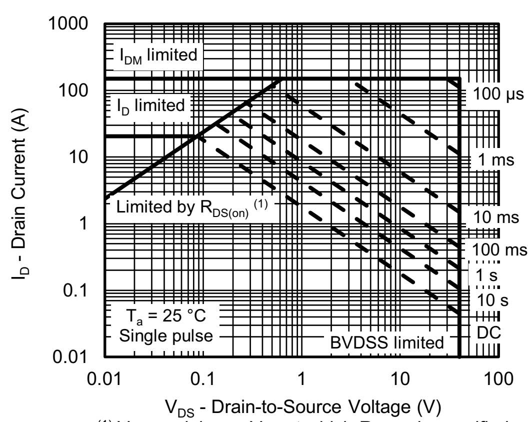
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



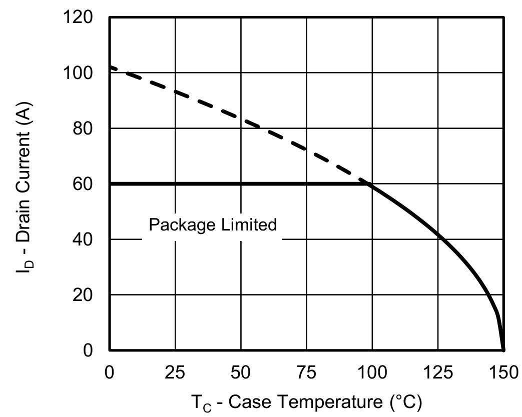
Single Pulse Power, Junction-to-Ambient



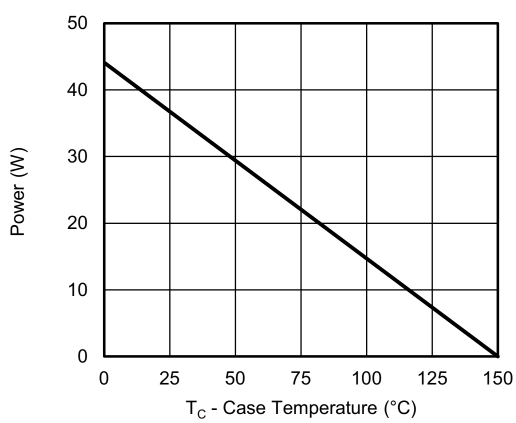
(1) V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

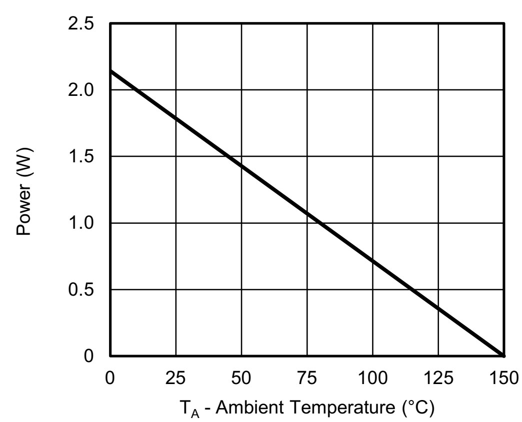
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating [a]



Power, Junction-to-Case

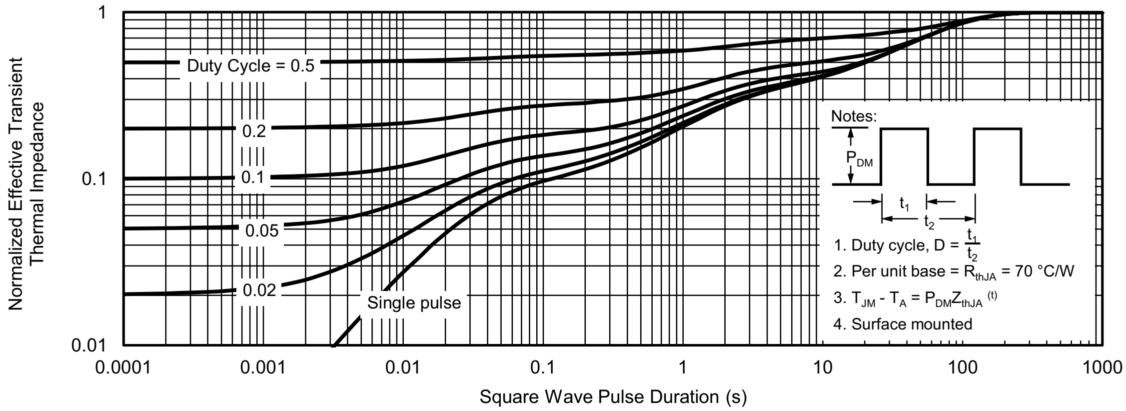


Power, Junction-to-Ambient

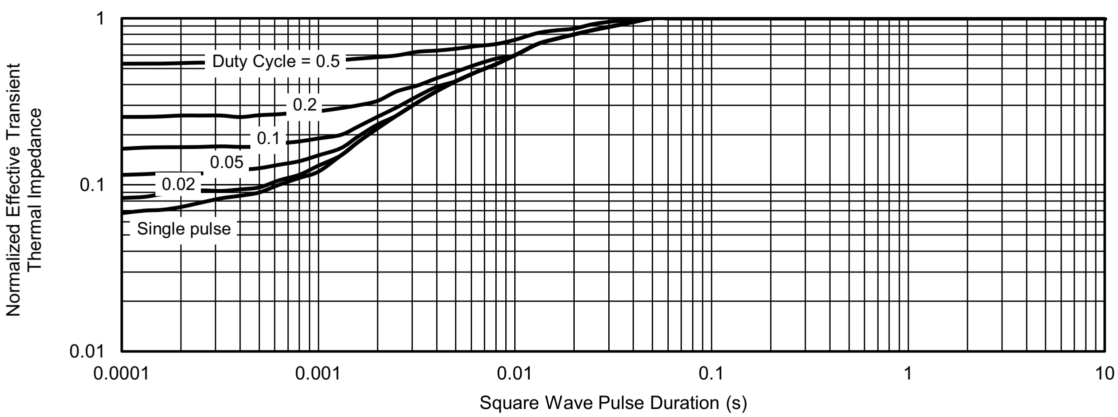
Note

a. The power dissipation P_D is based on T_J (max.) = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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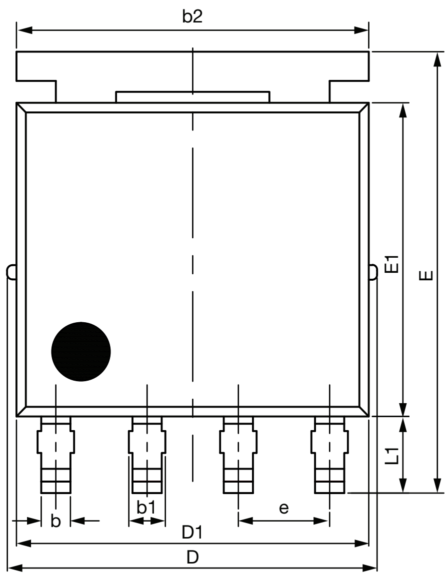
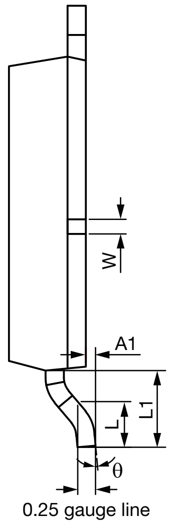
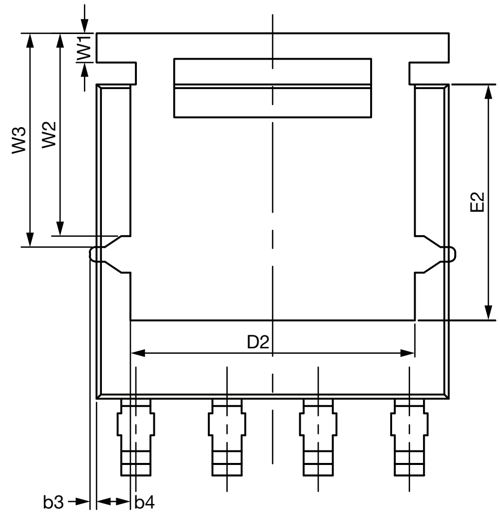
PowerPAK® SO-8L Case Outline for Non-AI Parts

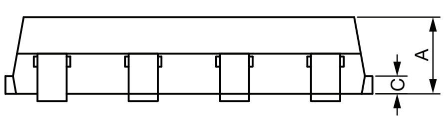


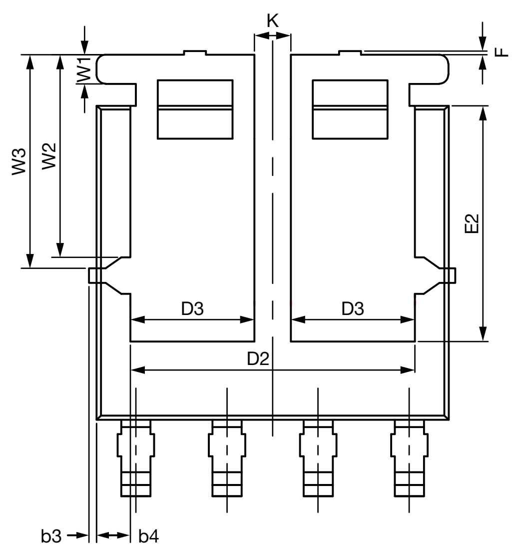


Topside view



Backside view (single)





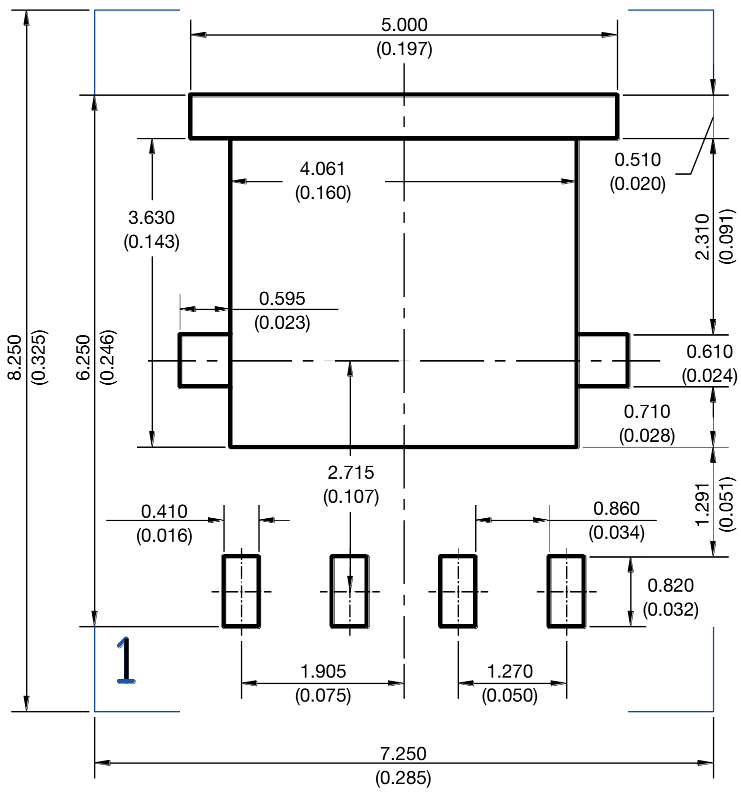
Backside view (dual)

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	-	0.127	0.00	-	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3		0.094			0.004	
b4		0.47			0.019	
c	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D3	1.63	1.73	1.83	0.064	0.068	0.072
e		1.27 BSC			0.050 BSC	
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	3.18	3.28	3.38	0.125	0.129	0.133
F	-	-	0.15	-	-	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K		0.51			0.020	
W		0.23			0.009	
W1		0.41			0.016	
W2		2.82			0.111	
W3		2.96			0.117	
θ	0°	-	10°	0°	-	10°
ECN: T16-0221-Rev. D, 16-May-16 DWG: 5976						

Note

- Millimeters will gover

RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE



Recommended Minimum Pads
Dimensions in mm (inches)

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