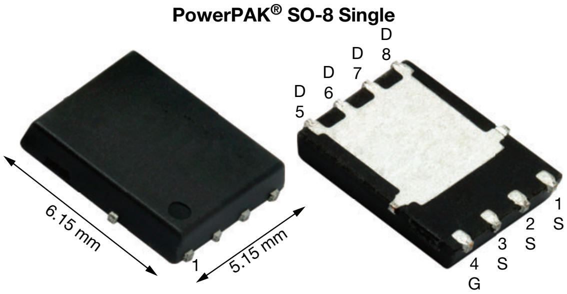
N-Channel 30 V (D-S) MOSFET



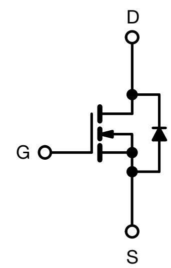
FEATURES

- TrenchFET® Gen IV power MOSFET
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- High power density DC/DC
- Synchronous rectification
- Power conversion
- Load switch



N-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	30
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.00683
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.01050
Q_g typ. (nC)	6.2
I_D (A) [a]	40
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK SO-8
Lead (Pb)-free and halogen-free	SiRA88BDP-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	30	V
Gate-source voltage		V_{GS}	+20, -16	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	40	A
	T_C = 70 °C		32	
	T_A = 25 °C		19 [b, c]	
	T_A = 70 °C		15 [b, c]	
Pulsed drain current (t = 100 μs)		I_{DM}	90	
Continuous source-drain diode current	T_C = 25 °C	I_S	16	
	T_A = 25 °C		3.4 [b, c]	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	10	
Single pulse avalanche energy		E_{AS}	5	mJ
Maximum power dissipation	T_C = 25 °C	P_D	17	W
	T_C = 70 °C		11	
	T_A = 25 °C		3.8 [b, c]	
	T_A = 70 °C		2.4 [b, c]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [d, e]			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SMYBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient [b, f]	t ≤ 10 s	R_{thJA}	25	33	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	5.5	7.2	

Notes

a. Based on T_C = 25 °C
b. Surface mounted on 1" x 1" FR4 board
c. t = 10 s
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
f. Maximum under steady state conditions is 70 °C/W

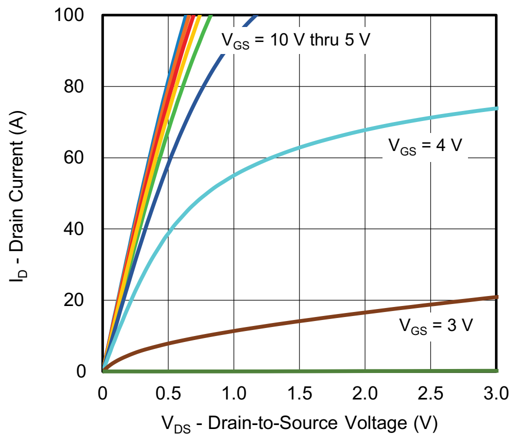
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	30	-	-	V
Drain-source breakdown voltage [c] (transient)	V_{DSt}	V_{GS} = 0 V, $I_{D(aval)}$ = 20 A, $t_{transcient}$ ≤ 50 ns	36	-	-	
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	I_D = 250 μA	-	17	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	-4.4	-	
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1.2	-	2.4	V
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = +20, -16 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	-	-	1	μA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55 °C	-	-	10	
On-state drain current [a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	30	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 10 A	-	0.00550	0.00683	Ω
		V_{GS} = 4.5 V, I_D = 8 A	-	0.00830	0.01050	
Forward transconductance [a]	g_{fs}	V_{DS} = 10 V, I_D = 20 A	-	42	-	S
Dynamic [b]						
Input capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	-	680	-	pF
Output capacitance	C_{oss}		-	266	-	
Reverse transfer capacitance	C_{rss}		-	54	-	
C_{rss}/C_{iss} ratio			-	0.08	0.16	
Total gate charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 10 A	-	12.2	19	nC
		V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 10 A	-	6.2	9.5	
Gate-source charge	Q_{gs}		-	2.3	-	
Gate-drain charge	Q_{gd}		-	2.3	-	
Output charge	Q_{oss}	V_{DS} = 15 V, V_{GS} = 0 V	-	7	-	
Gate resistance	R_g	f = 1 MHz	0.3	1.5	3	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 1.5 Ω, I_D ≅ 10 A, V_{GEN} = 10 V, R_g = 1 Ω	-	8	15	ns
Rise time	t_r		-	5	10	
Turn-off delay time	$t_{d(off)}$		-	15	30	
Fall time	t_f		-	5	10	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 1.5 Ω, I_D ≅ 10 A, V_{GEN} = 4.5 V, R_g = 1 Ω	-	12	25	
Rise time	t_r		-	55	110	
Turn-off delay time	$t_{d(off)}$		-	15	30	
Fall time	t_f		-	12	25	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	T_C = 25 °C	-	-	16	A
Pulse diode forward current [a]	I_{SM}		-	-	90	
Body diode voltage	V_{SD}	I_S = 5 A	-	0.8	1.1	V
Body diode reverse recovery time	t_{rr}	I_F = 5 A, di/dt = 100 A/μs, T_J = 25 °C	-	15	30	ns
Body diode reverse recovery charge	Q_{rr}		-	5	10	nC
Reverse recovery fall time	t_a		-	7	-	ns
Reverse recovery rise time	t_b		-	8	-	

Notes

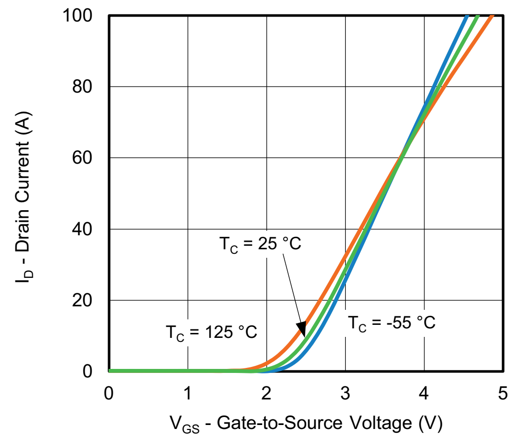
a. Pulse test: pulse width ≤ 300 μs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing
c. Based on characterization, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

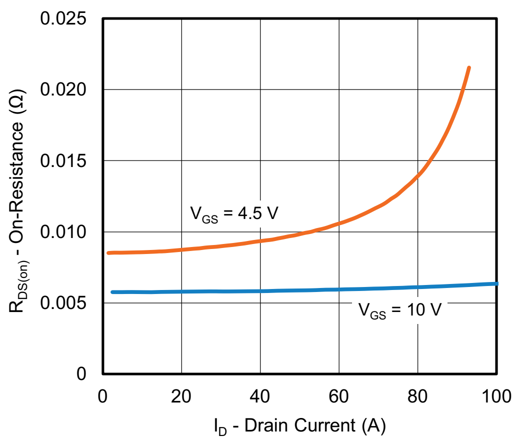
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



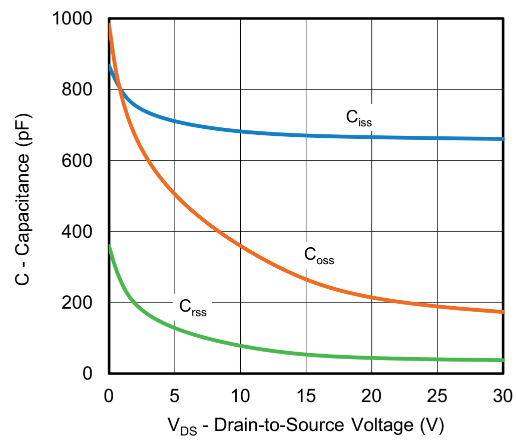
Output Characteristics



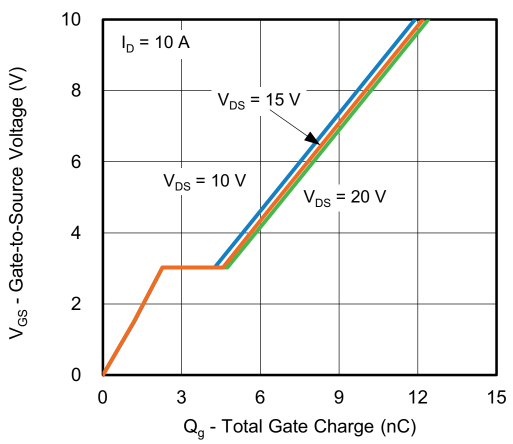
Transfer Characteristics



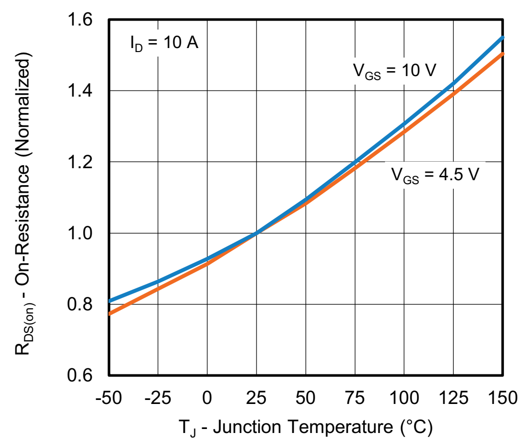
On-Resistance vs. Drain Current



Capacitance

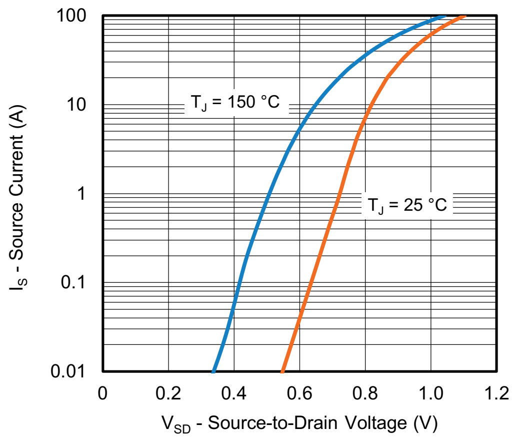


Gate Charge

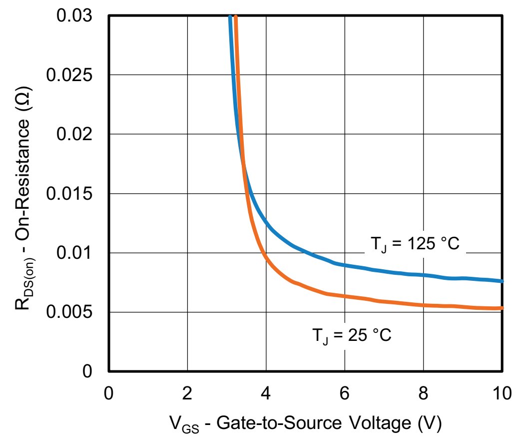


On-Resistance vs. Junction Temperature

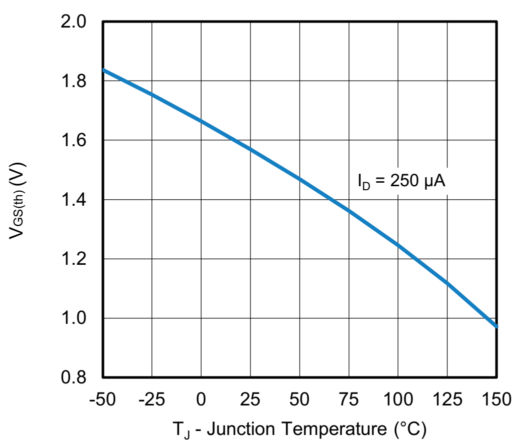
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



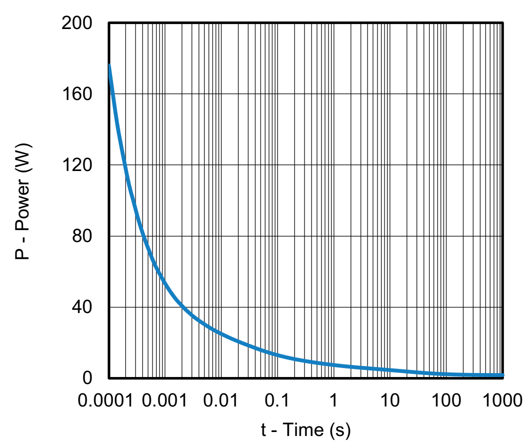
Source-Drain Diode Forward Voltage



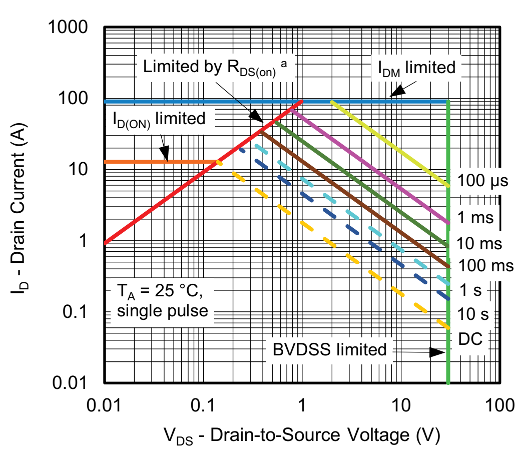
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

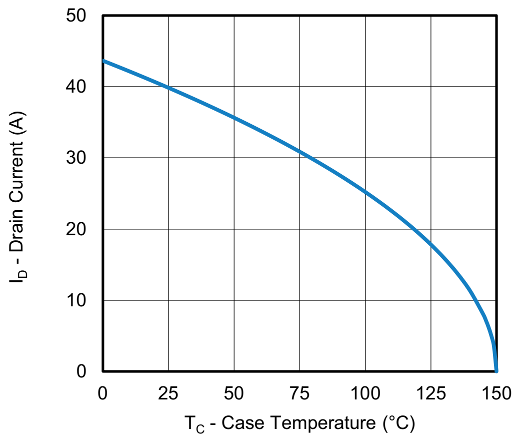


Safe Operating Area

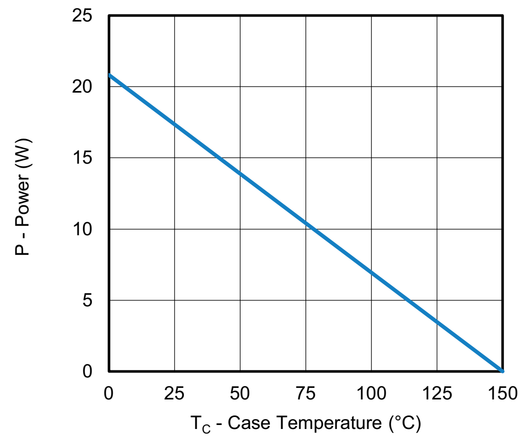
Note

a. V_{GS} > minimum VGS at which $R_{DS(on)}$ is specified

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating [a]

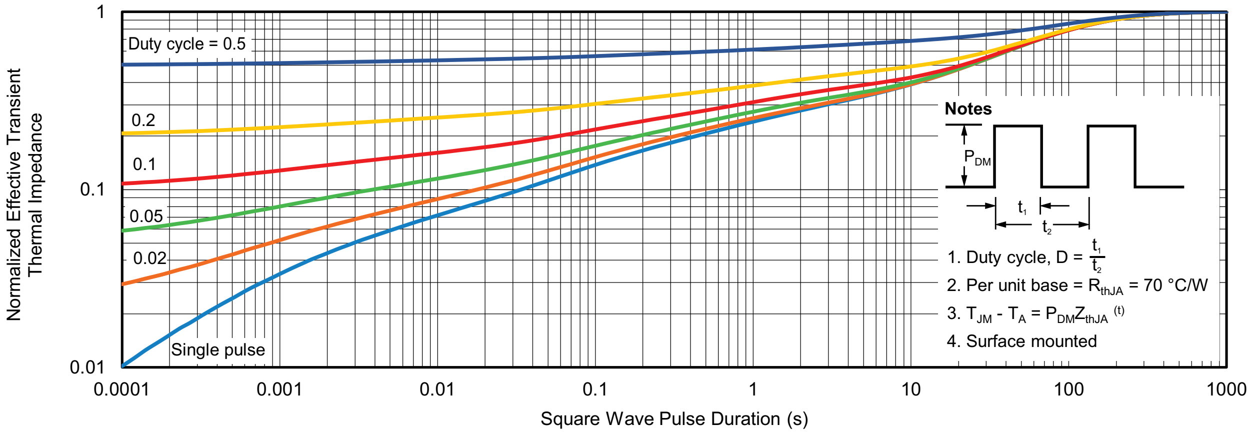


Power, Junction-to-Case

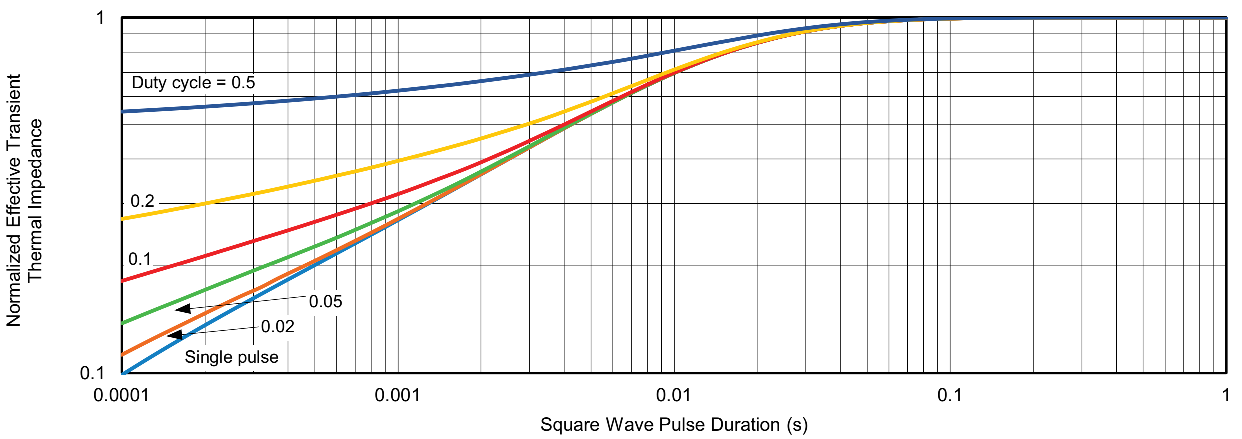
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



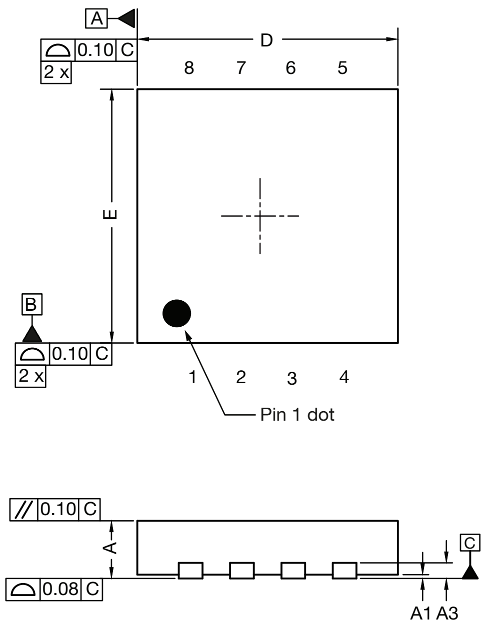
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

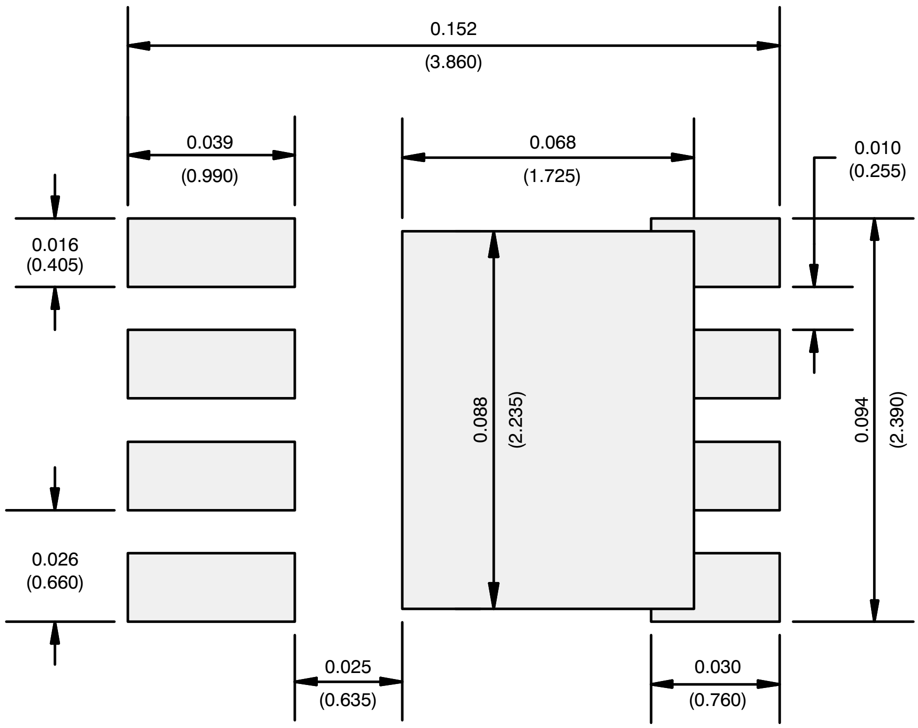
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?77158.

Case Outline for PowerPAK® 1212-SWLH



DIM.	MILLIMETERS			INCHES		
	MIN.	**NOM.**	**MAX.**	**MIN.**	**NOM.**	**MAX.**
A	0.82	0.90	0.98	0.032	0.035	0.038
A1	0.00	-	0.05	0.000	-	0.002
A3	0.20 ref.			0.008 ref.		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.15	2.25	2.35	0.085	0.089	0.093
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	1.60	1.70	1.80	0.063	0.067	0.071
e	0.65 bsc.			0.026 bsc.		
K	0.76 ref.			0.030 ref.		
K1	0.41 ref.			0.016 ref.		
L	0.33	0.43	0.53	0.013	0.017	0.021
Z	0.525 ref.			0.021 ref.		
ECN: C20-0863-Rev. B, 20-Jul-2020 DWG: 6062						

RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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