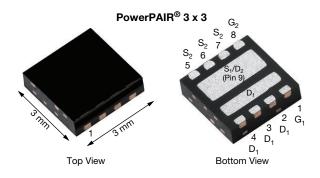


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Dual N-Channel 30 V (D-S) MOSFET

PRODUC	CT SUN	MARY		
	V _{DS} (V)	R _{DS(on)} (Ω) MAX.	I _D (A)	Q _g (Typ.)
Channel-1	30	0.0095 at V _{GS} = 10 V	30 ^a	5.6 nC
Chame-1	30	0.0137 at V _{GS} = 4.5 V	22	3.0110
Channel-2	30	0.0051 at V _{GS} = 10 V	40 a	10.1 nC
Grianner-2	30	0.0070 at V _{GS} = 4.5 V	40 a	10.1110



FEATURES

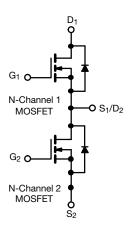
 PowerPAIR® Optimizes high-side and low-side MOSFETs for synchronous buck converters



- TrenchFET® power Mosfets
- 100 % R_g and UIS tested
- Material categorization: For definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- Synchronous buck
 - Battery charging
 - Computer system power
 - Graphic cards
- POL



Ordering Information:

SiZ340DT-T1-GE3 (lead (Pb)-free and halogen-free)

Parameter	Symbol	Channel-1	Channel-2	Unit	
Drain-Source Voltage		V_{DS}	30		
Gate-Source Voltage		V _{GS}	+20, -16		V
	T _C = 25 °C		30 ^a	40 a	
Continuous Drain Current /T 150 °C)	T _C = 70 °C	,	26.5	40 ^a	
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	I _D	15.6 b,c	22.6 b,c	
	T _A = 70 °C		12.4 b,c	18.1 ^{b,c}	
Pulsed Drain Current (t = 100 μs)		I _{DM}	100	150	Α
Continuous Courses Drain Diade Current	T _C = 25 °C	,	13.9	26	
Continuous Source Drain Diode Current	T _A = 25 °C	I _S	3.1 b,c	3.5 b,c	
Avalanche Current		I _{AS}	10	15	
Single Pulse Avalanche Energy	L = 0.1 mH	E _{AS}	5	11	mJ
	T _C = 25 °C		16.7	31	w
Mariana Paran Dissipation	T _C = 70 °C	Б	10.7	20	
Maximum Power Dissipation	T _A = 25 °C	P_D	3.7 b,c	4.2 b,c	
	T _A = 70 °C		2.4 b,c	2.7 b,c	
Operating Junction and Storage Temperature R	T _J , T _{stg}	-55 to 150		1 00	
Soldering Recommendations (Peak Temperature		260		°C	

Notes

- a. Package limited.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 10 s
- d. See solder profile (www.vishay.com/doc?73257). The PowerPAIR 3 x 3 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: Manual soldering with a soldering iron is not recommended for leadless components.

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THERMAL RESISTANCE RATINGS								
Parameter		Symbol	Chan	nel-1	Chan	nel-2	Unit	
Farameter		Symbol	Тур.	Max.	Тур.	Max.	Onit	
Maximum Junction-to-Ambient a,b	t ≤ 10 s	R_{thJA}	27	34	24	30	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	6	7.5	3.2	4	G/ V V	

Notes

- a. Surface mounted on 1" x 1" FR4 board.
- b. Maximum under steady state conditions is 69 °C/W for channel-1 and 64 °C/W for channel-2.

SPECIFICATIONS (T _J = 25 °C,						l		
Parameter	Symbol	TEST CONDITIONS		Min.	Тур.	Max.	Unit	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	Ch-1	30	-	-	V	
	- 53		Ch-2	30	-	-	_	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	$I_{D} = 250 \mu A$	Ch-1	-	18.4	-		
B6 - [F	DO 0	D r	Ch-2	-	30	-	mV/°(
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA	Ch-1	-	-4.3	-		
		·	Ch-2	-	-5	- 0.4		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu A$	Ch-1	1	-	2.4	V	
	, ,		Ch-2 Ch-1	1 -	-	± 100		
Gate Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = +20 \text{ V}, -16 \text{ V}$	Ch-2	_	-	± 100	nA	
			Ch-1	_		1		
		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$	Ch-2	_		1		
Zero Gate Voltage Drain Current	I _{DSS}		Ch-1	_	_	5	μA	
		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$	Ch-2	-	_	5		
			Ch-1	10	-	-		
On-State Drain Current ^b	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	Ch-2	10	-	-	Α	
		V _{GS} = 10 V, I _D = 15.6 A		-	0.0079	0.0095	V mV/° 4 V 000 nA 000 nA 005 137 070 S pF 84 50 95 150 nC	
Dunin Course On Chata Basistanas h		V _{GS} = 10 V, I _D = 20 A	Ch-2	-	0.0042	0.0051		
Drain-Source On-State Resistance b	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 13 A	Ch-1	-	0.0110	0.0137	Ω	
		$V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$	Ch-2	-	0.0058	0.0070		
Forward Transconductance b	q.	$V_{DS} = 15 \text{ V}, I_D = 15.6 \text{ A}$	Ch-1	-	37	-	V mV/°(1 V 100 nA 100 nA 100 nA 100 pF 100 s 100 pF 100 nC	
	9 _{fs}	V _{DS} = 15 V, I _D = 20 A CI		-	60	-	ა 	
Dynamic ^a								
Input Capacitance	C _{iss}	<u> </u>	Ch-1	-	760	-		
mpar dapastands	OISS	Channel-1 $V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	Ch-2	-	1552	-		
Output Capacitance	C _{oss}	VDS = 10 V, VGS = 0 V, 1 = 1 1VII 12	Ch-1		250	-	рF	
	- 033	Channel-2	Ch-2		450	-	'	
Reverse Transfer Capacitance	C _{rss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	Ch-1	-	32	-		
·			Ch-2	-	40	-		
C _{rss} / C _{iss} Ratio			Ch-1	0.042	-	0.084	-	
		V 15VV 10VI 15CA	Ch-2	0.025	- 10.0	0.050		
		$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 15.6 \text{ A}$ $V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	Ch-1 Ch-2	-	12.3	19 35		
Total Gate Charge	Qg	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 20 A	Ch-1	-	22.6 5.6	9		
			Ch-2	-	10.1	16		
		Channel-1	Ch-1	_	2.3	-		
Gate-Source Charge	Q_{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 15.6 \text{ A}$	Ch-2	_	4.2	_	nC	
	Q _{gd}	Observat 2	Ch-1	_	1	_	1	
Gate-Drain Charge	√gd	Channel-2 $V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 20 \text{ A}$	Ch-2	_	1.8	_		
	+	ν _{DS} = 10 ν,ν _{GS} = 4.0 ν, η = 20 Α	Ch-1	_	6.6	_		
Output Charge	Q _{oss}		Ch-2	_	12.4	-		
0.5.			Ch-1	0.3	1.7	3.4		
Gate Resistance	R_g	f = 1 MHz	Ch-2	0.3	1.3	2.6	Ω	



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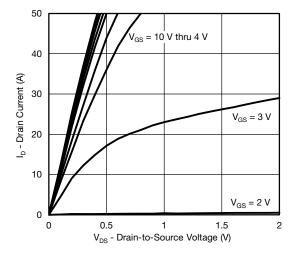
Parameter	Symbol	TEST CONDITIONS		Min.	Тур.	Max.	Unit
Dynamic ^a							
Turn-On Delay Time	t _{d(on)}		Ch-1	-	13	20	
Tulli Oli Belay Tillie	^L a(on)	Channel-1 $V_{DD} = 15 \text{ V, } R_L = 1.5 \Omega$	Ch-2	-	22	33	
Rise Time	t _r	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_a = 1 \Omega$	Ch-1	-	55	85	
Tilise Tillio	न		Ch-2	-	82	123	
Turn-Off Delay Time	t _{d(off)}	Chan nel-2	Ch-1	-	16	25	
	-4(011)	$V_{DD} = 15 \text{ V}, R_L = 1.5 \Omega$	Ch-2	-	20	30	
Fall Time	t _f	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	Ch-1	-	7	14	
			Ch-2	-	7	14	ns
Turn-On Delay Time	t _{d(on)}	Observat 4	Ch-1	-	8	16	
	u(on)	Channel-1 $V_{DD} = 15 \text{ V, R}_{L} = 1.5 \Omega$	Ch-2	-	10	20	
Rise Time	t _r	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	Ch-1	-	11	20	
	'	_	Ch-2	-	12	20	
Turn-Off Delay Time	t _{d(off)}	Channel-2	Ch-1	-	12	20	
		$V_{DD} = 15 \text{ V}, R_L = 1.5 \Omega$	Ch-2	-	16	30	
Fall Time		$I_D\cong 10~A,~V_{GEN}=10~V,~R_g=1~\Omega$	Ch-1	-	7	15	
			Ch-2	-	7	12	
Drain-Source Body Diode Characteristic	es			T	T		
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	Ch-1	-	-	13.9	
		0 1	Ch-2	-	-	25.8	Α
Pulse Diode Forward Current (t = 100 µs)	I _{SM}		Ch-1	-	-	100	
, ,			Ch-2	-	-	150	
Body Diode Voltage	V _{SD}	$I_S = 10 \text{ A}, V_{GS} = 0 \text{ V}$	Ch-1	-	0.8	1.2	V
			Ch-2	-	0.82	1.2	<u> </u>
Body Diode Reverse Recovery Time	t _{rr}		Ch-1	-	20	35	ns
			Ch-2	-	26	40	<u> </u>
Body Diode Reverse Recovery Charge	Q_{rr}	Channel-1 $I_F = 10 \text{ A}$, $dI/dt = 100 \text{ A/}\mu\text{s}$, $T_J = 25 ^{\circ}\text{C}$	Ch-1	-	9	20	nC
		- 107, απαι - 100 7, μο, 1] - 20 0	Ch-2	-	20	30	
Reverse Recovery Fall Time	ta	Channel-2	Ch-1	-	11.5	-	
-		$I_F = 10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$	Ch-2	-	18.1	-	ns
Reverse Recovery Rise Time	t _b		Ch-1	-	8.5	-	
neverse necovery hise time	ι _b		Ch-2	-	7.9	-	

Notes

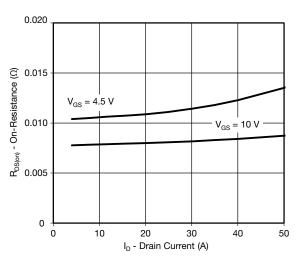
- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

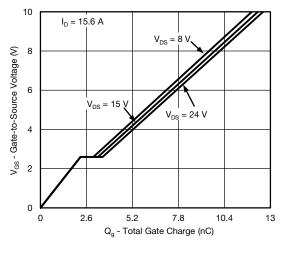




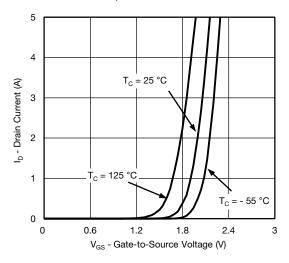
Output Characteristics



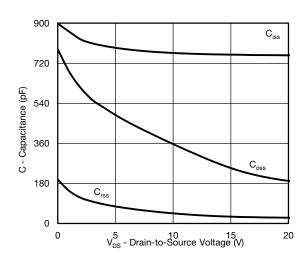
On-Resistance vs. Drain Current



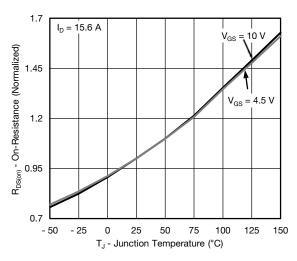
Gate Charge



Transfer Characteristics



Capacitance



On-Resistance vs. Junction Temperature

I_D = 15.6 A

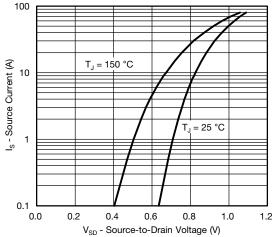
= 125 °C

T₁ = 25 °C

10



CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



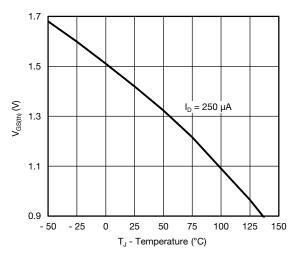


0.02

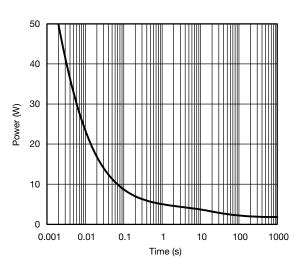
A_{DS(on)} - On-Resistance (()) 0.001 0.005

O

2



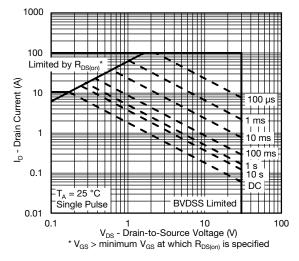
Threshold Voltage



6

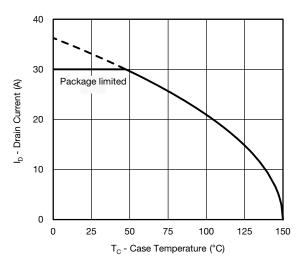
 $V_{\rm GS}$ - Gate-to-Source Voltage (V)

Single Pulse Power

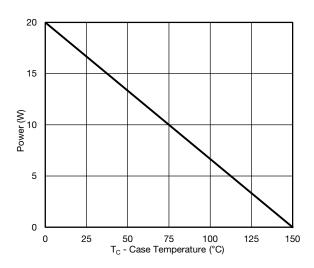


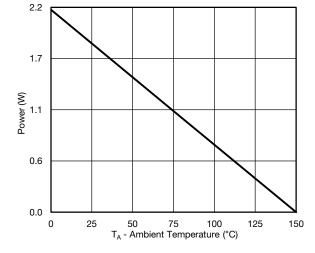
Safe Operating Area, Junction-to-Ambient





Current Derating*



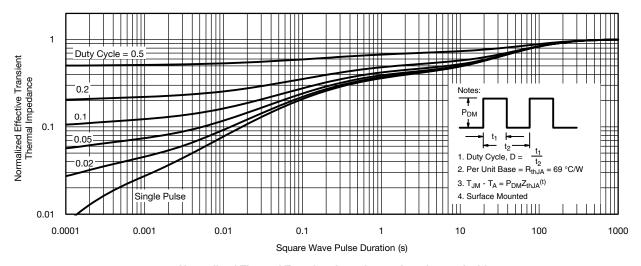


Power, Junction-to-Case

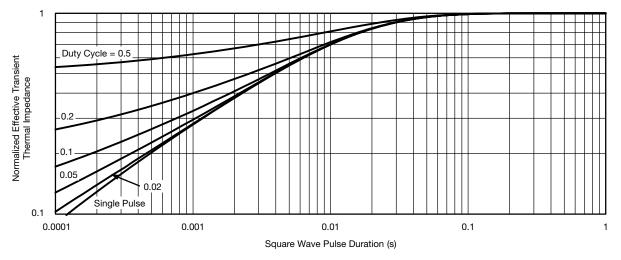
Power, Junction-to-Ambient

^{*} The power dissipation P_D is based on $T_{J \text{ (max.)}} = 150 \,^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



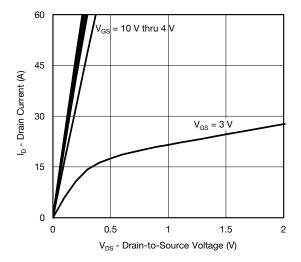


Normalized Thermal Transient Impedance, Junction-to-Ambient

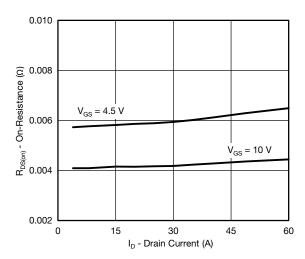


Normalized Thermal Transient Impedance, Junction-to-Case

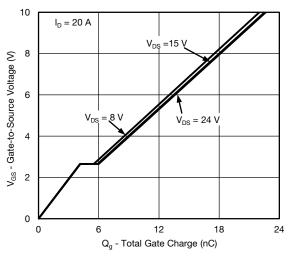




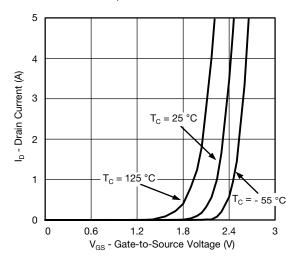
Output Characteristics



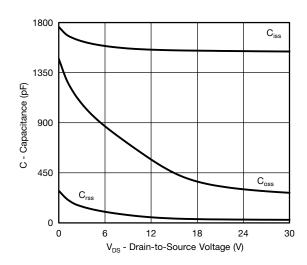
On-Resistance vs. Drain Current



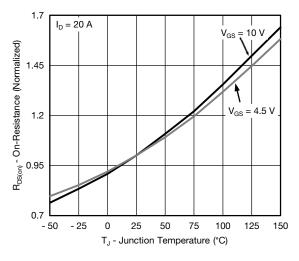
Gate Charge



Transfer Characteristics

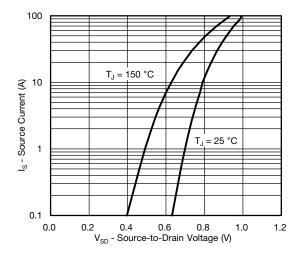


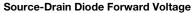
Capacitance

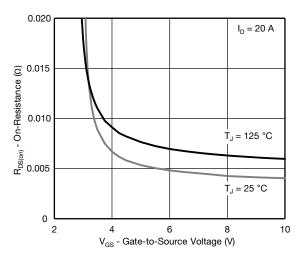


On-Resistance vs. Junction Temperature

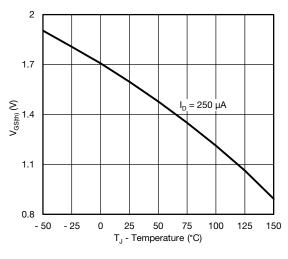




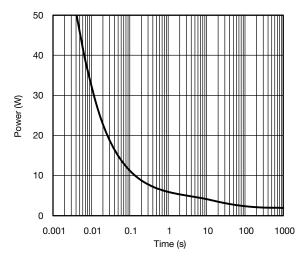




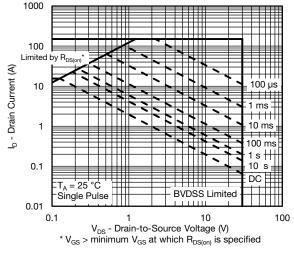
On-Resistance vs. Gate-to-Source Voltage



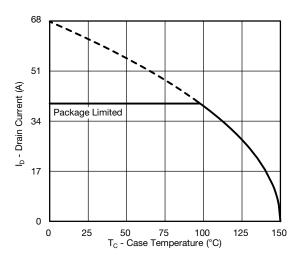
Threshold Voltage



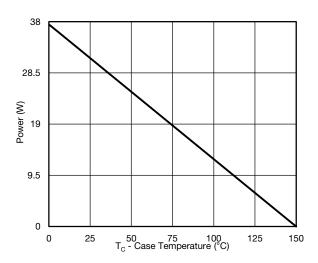
Single Pulse Power



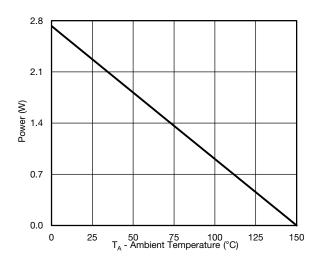




Current Derating*





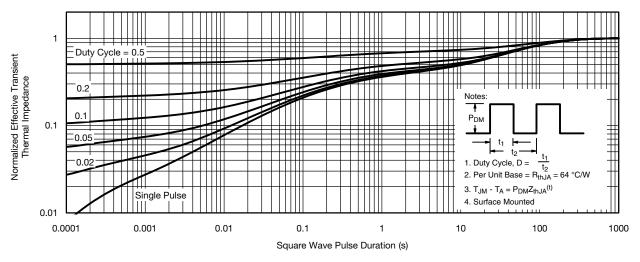


Power, Junction-to-Ambient

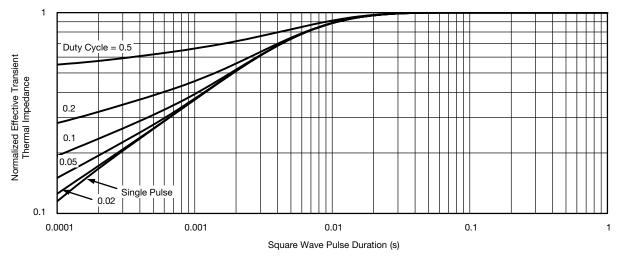
ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

^{*} The power dissipation P_D is based on $T_{J \text{ (max.)}} = 150 \,^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient



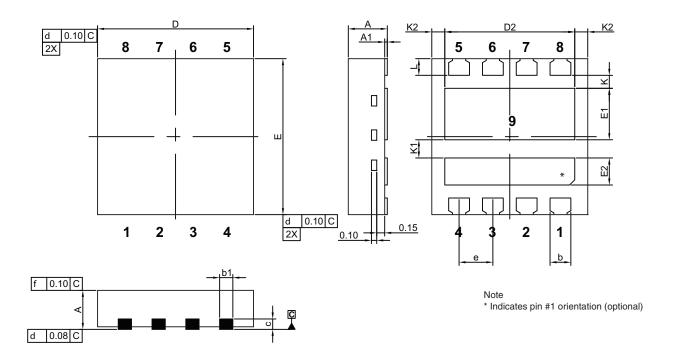
Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg262877.





PowerPAIR® 3 x 3 Case Outline



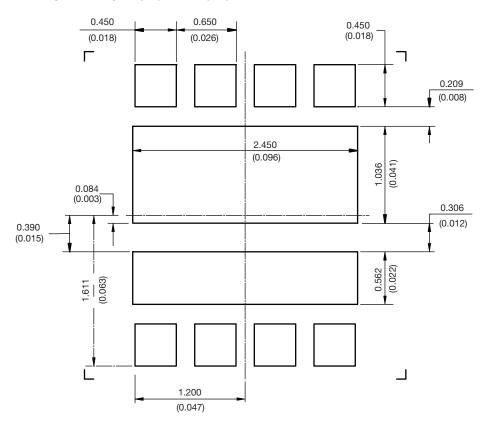
		MILLIMETERS		INCHES				
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
Α	0.70	0.75	0.80	0.028	0.030	0.031		
A1	0.00		0.05	0.000		0.002		
b	0.35	0.40	0.45	0.014	0.016	0.018		
b1	0.20	0.25	0.38	0.008	0.010	0.015		
С	0.18	0.20	0.23	0.007	0.008	0.009		
D	2.90	3.00	3.10	0.114	0.118	0.122		
D2	2.35	2.40	2.45	0.093	0.094	0.096		
E	2.90	3.00	3.10	0.114	0.118	0.122		
E1	0.94	0.99	1.04	0.037	0.039	0.041		
E2	0.47	0.52	0.57	0.019	0.020	0.022		
е		0.65 BSC			0.026 BSC			
K		0.25 typ.			0.010 typ.			
K1		0.35 typ.			0.014 typ.			
K2	0.30 typ.				0.012 typ.			
L	0.27	0.32	0.37	0.011	0.013	0.015		

DWG: 5998



Vishay Siliconix

RECOMMENDED MINIMUM PAD FOR PowerPAIR® 3 x 3



Recommended PAD for PowerPAIR 3 x 3

Dimensions in millimeters (inches)

Keep-Out 3.5 mm x 3.5 mm for non terminating traces



Legal Disclaimer Notice

Vishay

Disclaimer

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