





THERMAL RESISTANCE RATINGS							
Parameter	Symbol	Channel-1		Channel-2		Unit	
		Typ.	Max.	Typ.	Max.		
Maximum Junction-to-Ambient <sup>a,b</sup>	$t \leq 10$ s	$R_{thJA}$	27	34	24	30	°C/W
Maximum Junction-to-Case (Drain)	Steady State	$R_{thJC}$	6	7.5	3.2	4	

**Notes**

- a. Surface mounted on 1" x 1" FR4 board.
- b. Maximum under steady state conditions is 69 °C/W for channel-1 and 64 °C/W for channel-2.

SPECIFICATIONS ( $T_J = 25$ °C, unless otherwise noted)								
Parameter	Symbol	TEST CONDITIONS	Min.	Typ.	Max.	Unit		
<b>Static</b>								
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0$ V, $I_D = 250$ $\mu$ A	Ch-1	30	-	-	V	
			Ch-2	30	-	-		
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250$ $\mu$ A	Ch-1	-	18.4	-	mV/°C	
			Ch-2	-	30	-		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250$ $\mu$ A	Ch-1	-	-4.3	-	mV/°C	
			Ch-2	-	-5	-		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250$ $\mu$ A	Ch-1	1	-	2.4	V	
			Ch-2	1	-	2.4		
Gate Source Leakage	$I_{GSS}$	$V_{DS} = 0$ V, $V_{GS} = +20$ V, -16 V	Ch-1	-	-	$\pm 100$	nA	
			Ch-2	-	-	$\pm 100$		
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30$ V, $V_{GS} = 0$ V	Ch-1	-	-	1	$\mu$ A	
			Ch-2	-	-	1		
		$V_{DS} = 30$ V, $V_{GS} = 0$ V, $T_J = 55$ °C	Ch-1	-	-	5		
			Ch-2	-	-	5		
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 10$ V	Ch-1	10	-	-	A	
			Ch-2	10	-	-		
Drain-Source On-State Resistance <sup>b</sup>	$R_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 15.6$ A	Ch-1	-	0.0079	0.0095	$\Omega$	
			Ch-2	-	0.0042	0.0051		
			$V_{GS} = 4.5$ V, $I_D = 13$ A	Ch-1	-	0.0110		0.0137
				Ch-2	-	0.0058		0.0070
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15$ V, $I_D = 15.6$ A	Ch-1	-	37	-	S	
			Ch-2	-	60	-		
<b>Dynamic<sup>a</sup></b>								
Input Capacitance	$C_{iss}$	Channel-1 $V_{DS} = 15$ V, $V_{GS} = 0$ V, $f = 1$ MHz	Ch-1	-	760	-	pF	
			Ch-2	-	1552	-		
Output Capacitance	$C_{oss}$	Channel-2 $V_{DS} = 15$ V, $V_{GS} = 0$ V, $f = 1$ MHz	Ch-1	-	250	-	pF	
			Ch-2	-	450	-		
Reverse Transfer Capacitance	$C_{rss}$	Channel-2 $V_{DS} = 15$ V, $V_{GS} = 0$ V, $f = 1$ MHz	Ch-1	-	32	-	pF	
			Ch-2	-	40	-		
$C_{rss} / C_{iss}$ Ratio			Ch-1	0.042	-	0.084	-	
			Ch-2	0.025	-	0.050		
Total Gate Charge	$Q_g$	$V_{DS} = 15$ V, $V_{GS} = 10$ V, $I_D = 15.6$ A	Ch-1	-	12.3	19	nC	
			Ch-2	-	22.6	35		
		$V_{DS} = 15$ V, $V_{GS} = 10$ V, $I_D = 20$ A	Ch-1	-	5.6	9		
			Ch-2	-	10.1	16		
Gate-Source Charge	$Q_{gs}$	Channel-1 $V_{DS} = 15$ V, $V_{GS} = 4.5$ V, $I_D = 15.6$ A	Ch-1	-	2.3	-	nC	
			Ch-2	-	4.2	-		
Gate-Drain Charge	$Q_{gd}$	Channel-2 $V_{DS} = 15$ V, $V_{GS} = 4.5$ V, $I_D = 20$ A	Ch-1	-	1	-	nC	
			Ch-2	-	1.8	-		
Output Charge	$Q_{oss}$		Ch-1	-	6.6	-	nC	
			Ch-2	-	12.4	-		
Gate Resistance	$R_g$	$f = 1$ MHz	Ch-1	0.3	1.7	3.4	$\Omega$	
			Ch-2	0.3	1.3	2.6		



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
Parameter	Symbol	TEST CONDITIONS	Min.	Typ.	Max.	Unit	
<b>Dynamic <sup>a</sup></b>							
Turn-On Delay Time	t <sub>d(on)</sub>	Channel-1 V <sub>DD</sub> = 15 V, R <sub>L</sub> = 1.5 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω	Ch-1	-	13	20	ns
Rise Time	t <sub>r</sub>		Ch-2	-	22	33	
Turn-Off Delay Time	t <sub>d(off)</sub>	Chan nel-2 V <sub>DD</sub> = 15 V, R <sub>L</sub> = 1.5 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω	Ch-1	-	55	85	
			Ch-2	-	82	123	
Fall Time	t <sub>f</sub>		Ch-1	-	16	25	
			Ch-2	-	20	30	
Turn-On Delay Time	t <sub>d(on)</sub>	Channel-1 V <sub>DD</sub> = 15 V, R <sub>L</sub> = 1.5 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	Ch-1	-	7	14	
			Ch-2	-	7	14	
Rise Time	t <sub>r</sub>		Ch-1	-	8	16	
			Ch-2	-	10	20	
Turn-Off Delay Time	t <sub>d(off)</sub>	Channel-2 V <sub>DD</sub> = 15 V, R <sub>L</sub> = 1.5 Ω I <sub>D</sub> ≅ 10 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	Ch-1	-	11	20	
			Ch-2	-	12	20	
Fall Time	t <sub>f</sub>		Ch-1	-	12	20	
			Ch-2	-	16	30	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	Ch-1	-	-	13.9	A
			Ch-2	-	-	25.8	
Pulse Diode Forward Current (t = 100 μs)	I <sub>SM</sub>		Ch-1	-	-	100	
			Ch-2	-	-	150	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 10 A, V <sub>GS</sub> = 0 V	Ch-1	-	0.8	1.2	V
			Ch-2	-	0.82	1.2	
Body Diode Reverse Recovery Time	t <sub>rr</sub>		Ch-1	-	20	35	ns
			Ch-2	-	26	40	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	Channel-1 I <sub>F</sub> = 10 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C	Ch-1	-	9	20	nC
			Ch-2	-	20	30	
Reverse Recovery Fall Time	t <sub>a</sub>	Channel-2 I <sub>F</sub> = 10 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C	Ch-1	-	11.5	-	ns
			Ch-2	-	18.1	-	
Reverse Recovery Rise Time	t <sub>b</sub>		Ch-1	-	8.5	-	
			Ch-2	-	7.9	-	

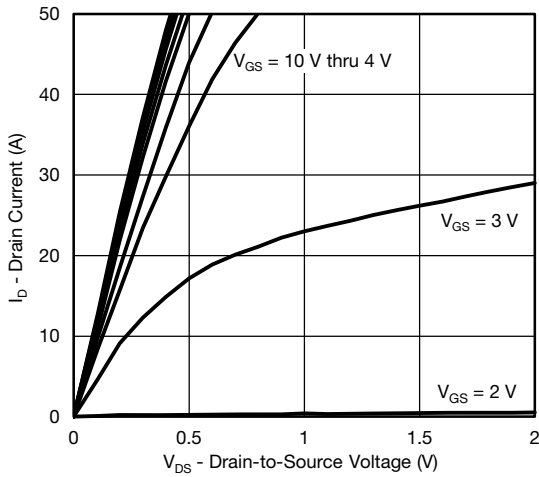
**Notes**

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.

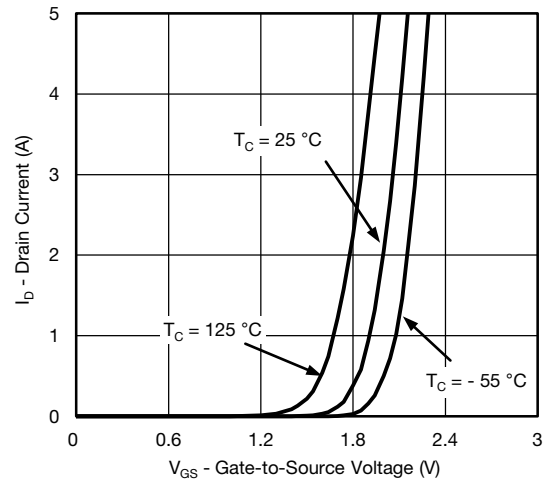
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



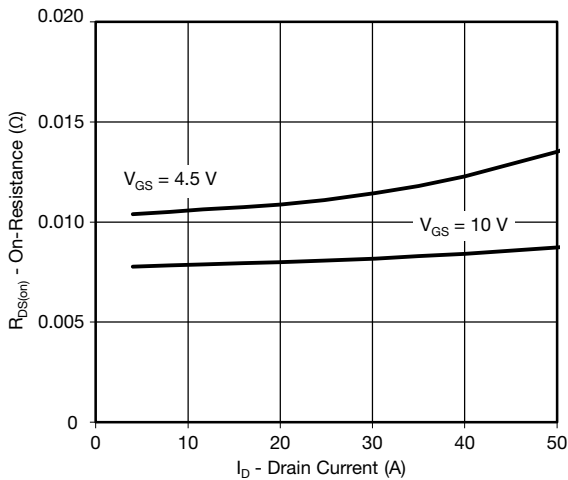
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



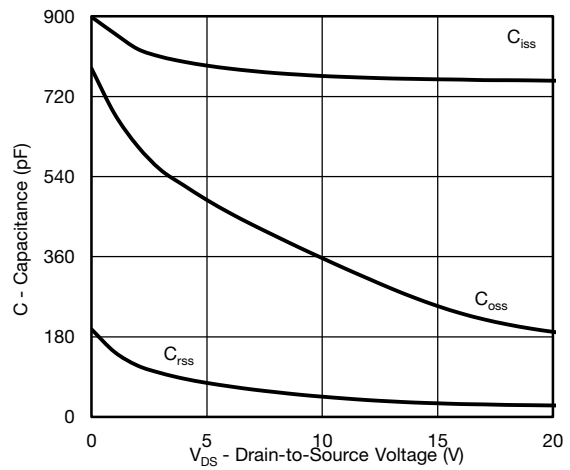
Output Characteristics



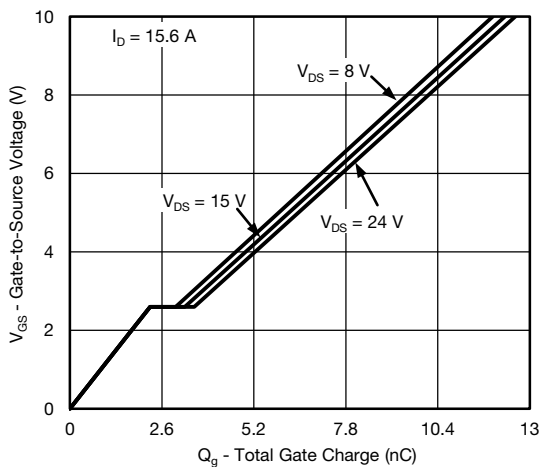
Transfer Characteristics



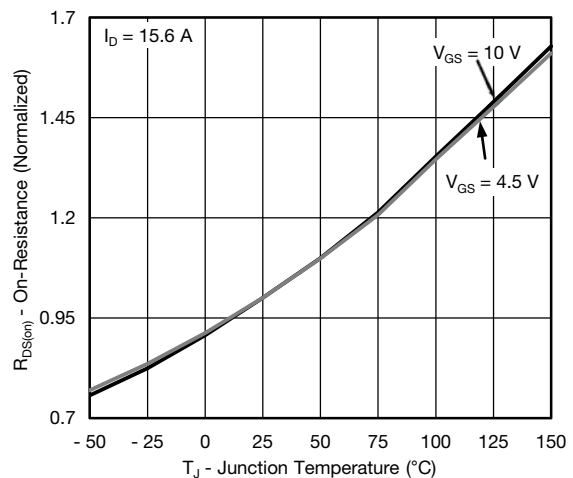
On-Resistance vs. Drain Current



Capacitance



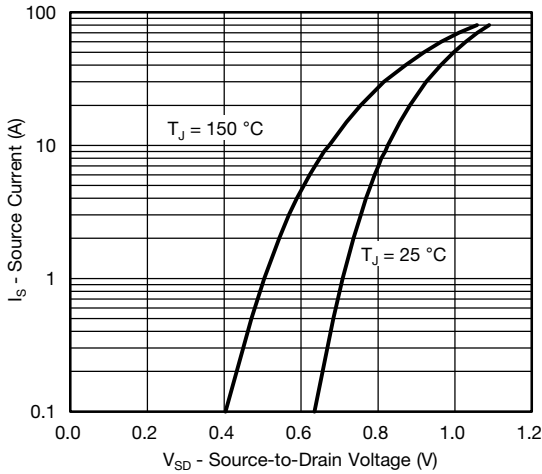
Gate Charge



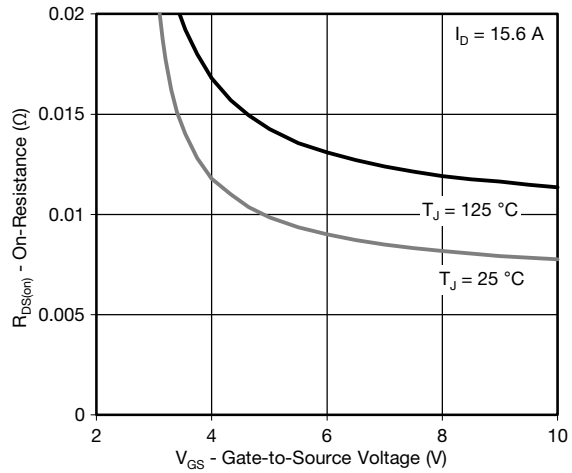
On-Resistance vs. Junction Temperature



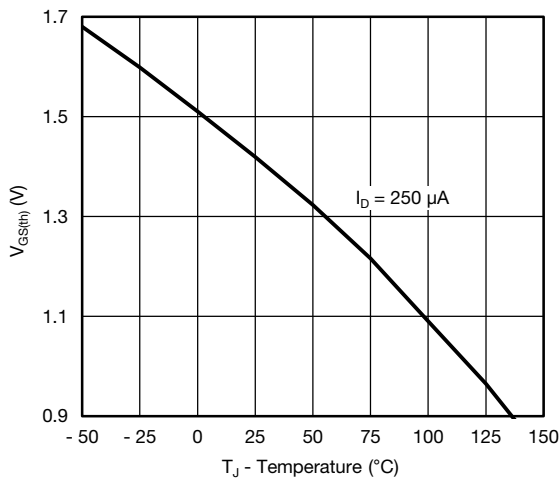
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



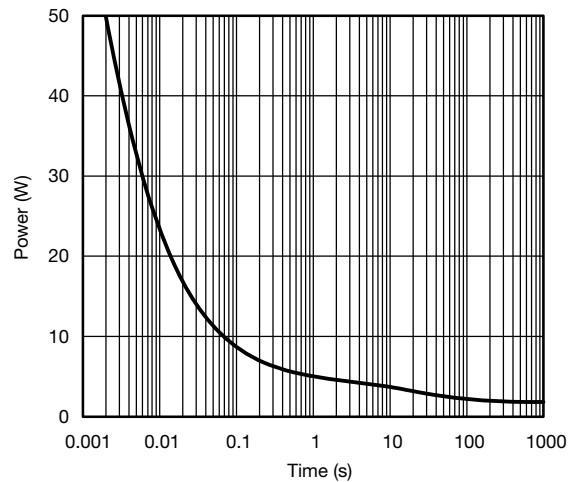
Source-Drain Diode Forward Voltage



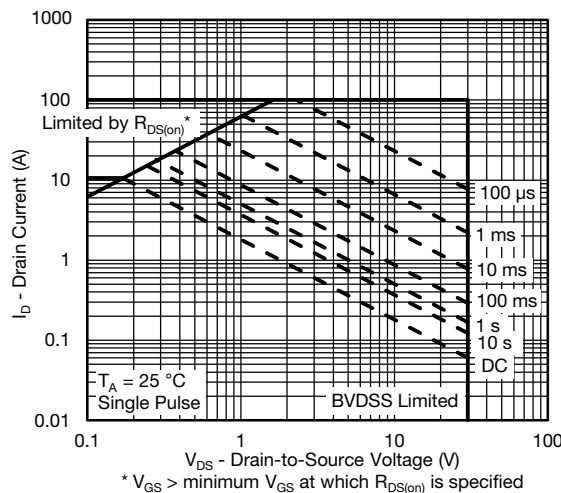
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

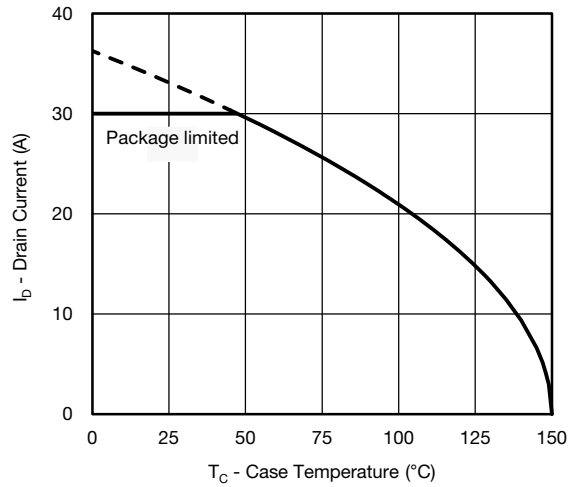


Single Pulse Power

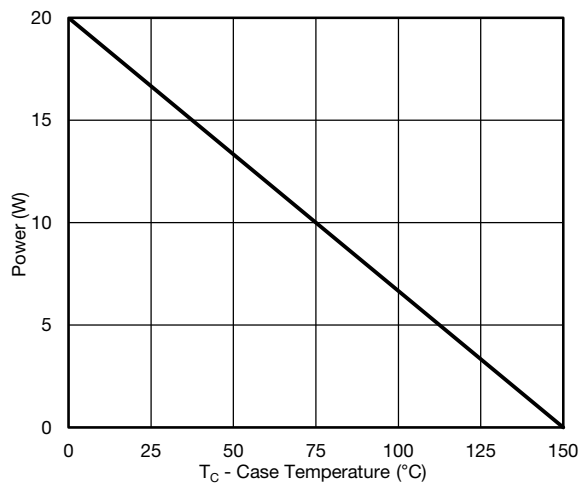


Safe Operating Area, Junction-to-Ambient

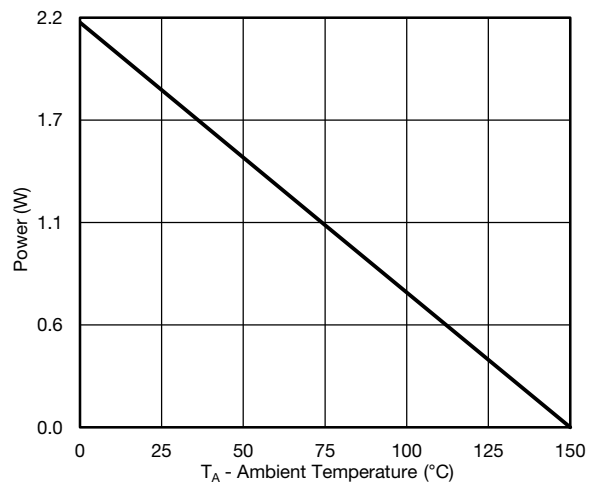
## CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



**Current Derating\***



**Power, Junction-to-Case**

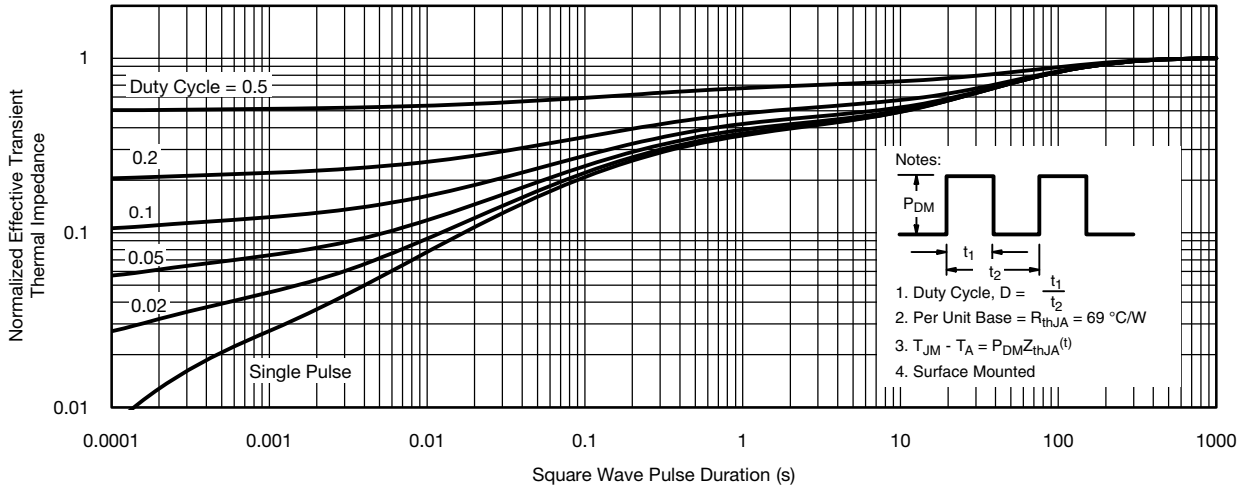


**Power, Junction-to-Ambient**

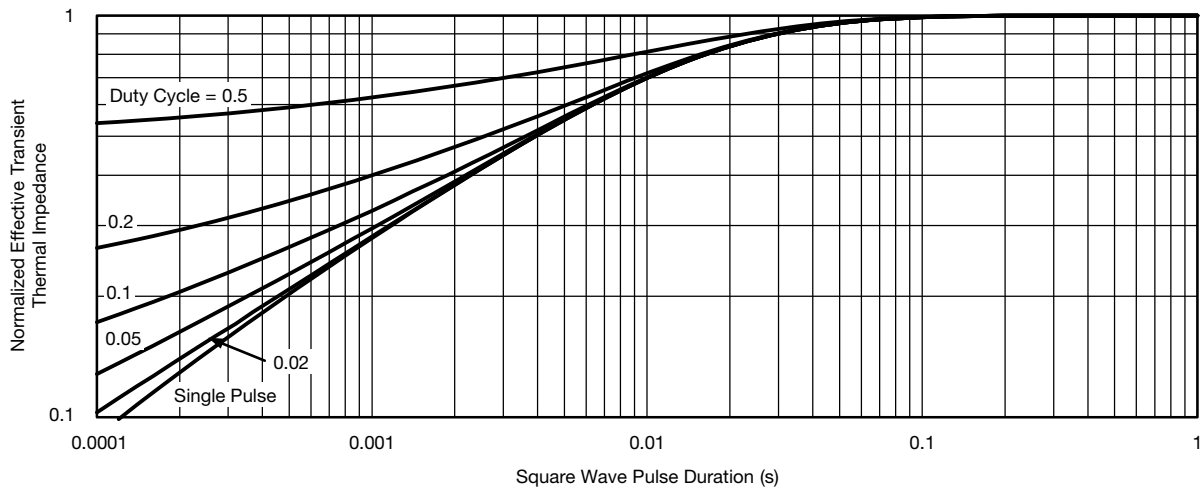
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150\text{ °C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



**CHANNEL-1 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

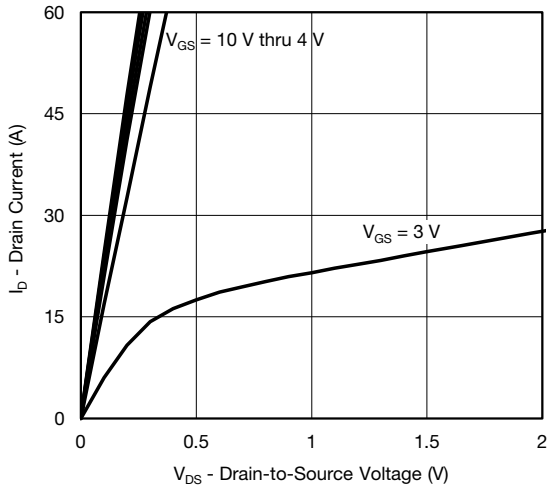


**Normalized Thermal Transient Impedance, Junction-to-Ambient**

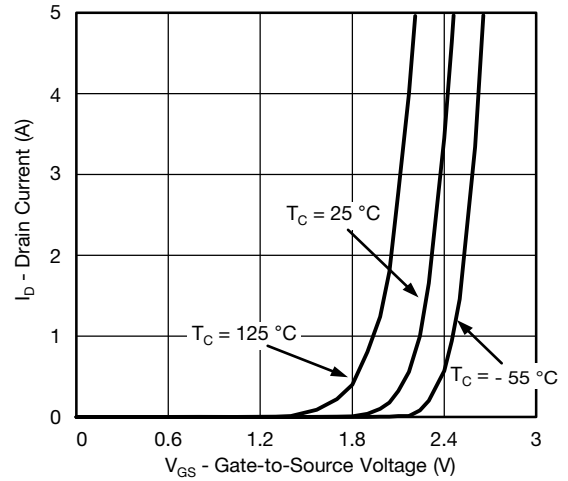


**Normalized Thermal Transient Impedance, Junction-to-Case**

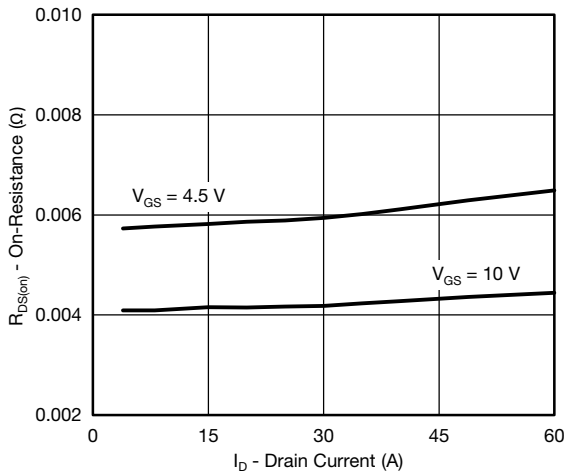
**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



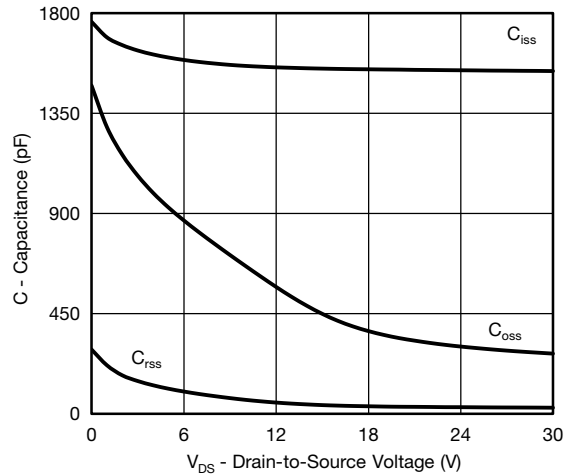
**Output Characteristics**



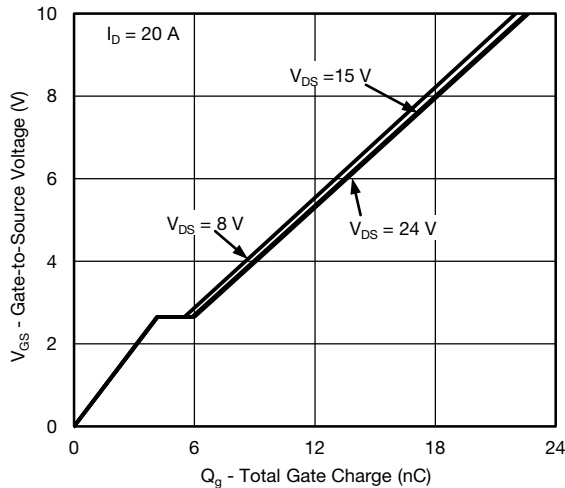
**Transfer Characteristics**



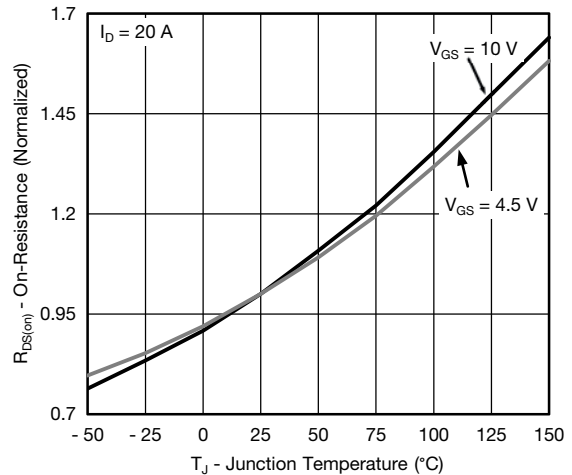
**On-Resistance vs. Drain Current**



**Capacitance**



**Gate Charge**

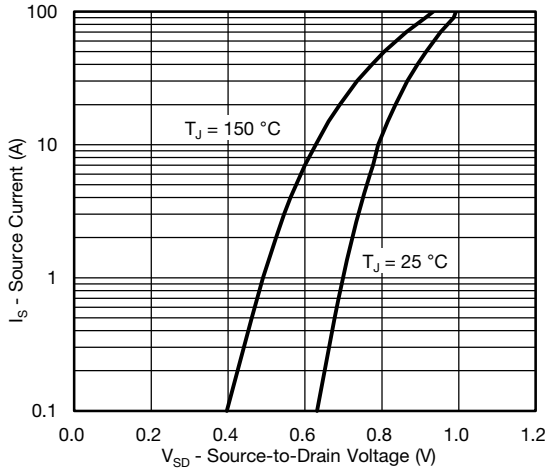


**On-Resistance vs. Junction Temperature**

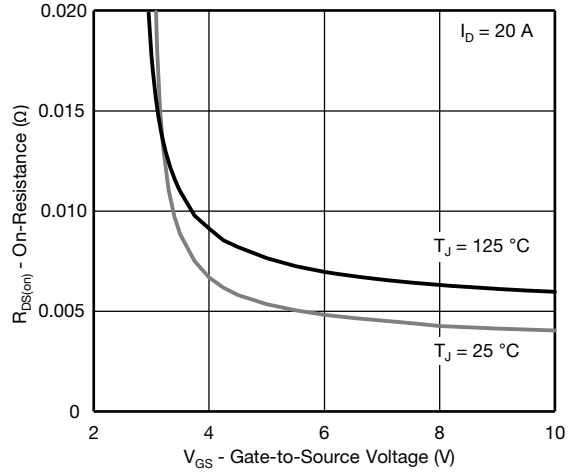




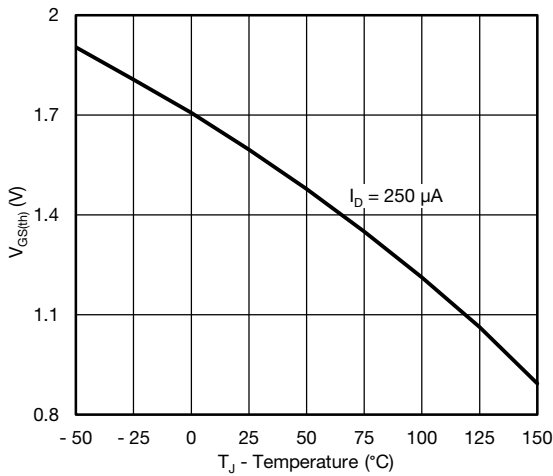
**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



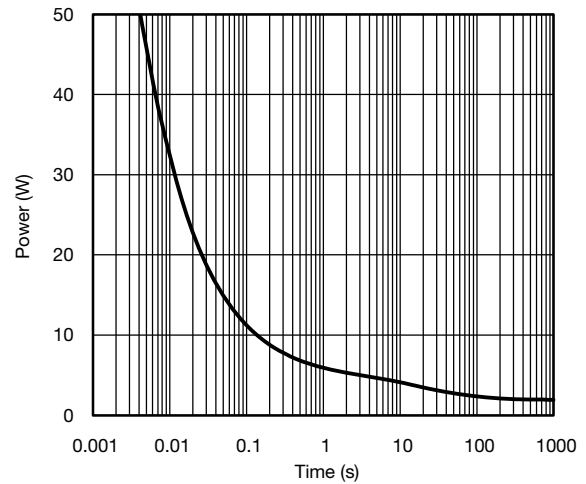
**Source-Drain Diode Forward Voltage**



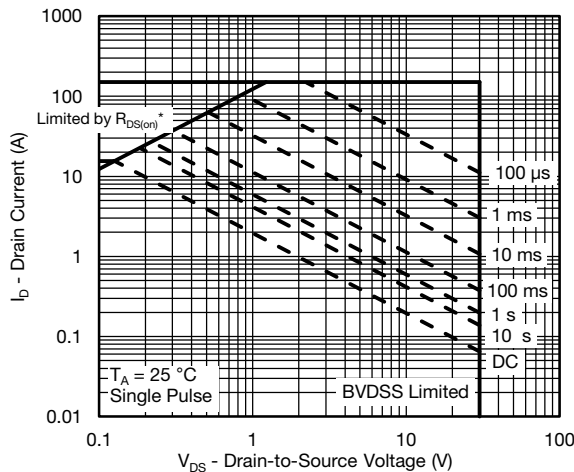
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



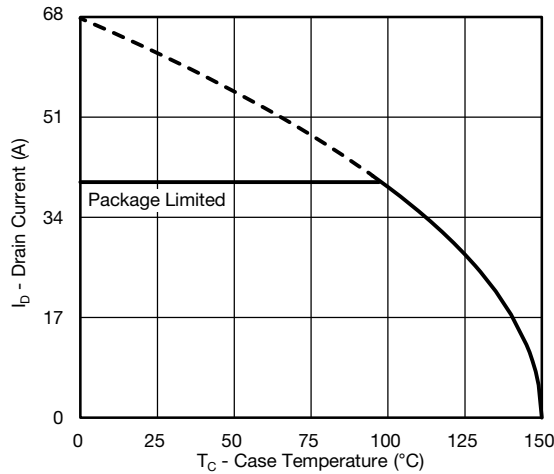
**Single Pulse Power**



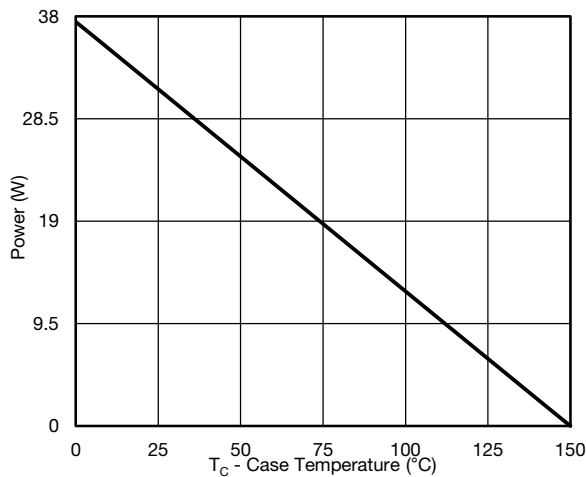
**Safe Operating Area, Junction-to-Ambient**



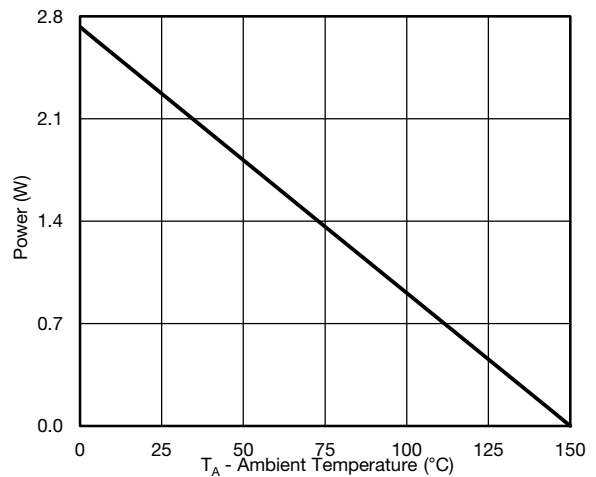
**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating\***

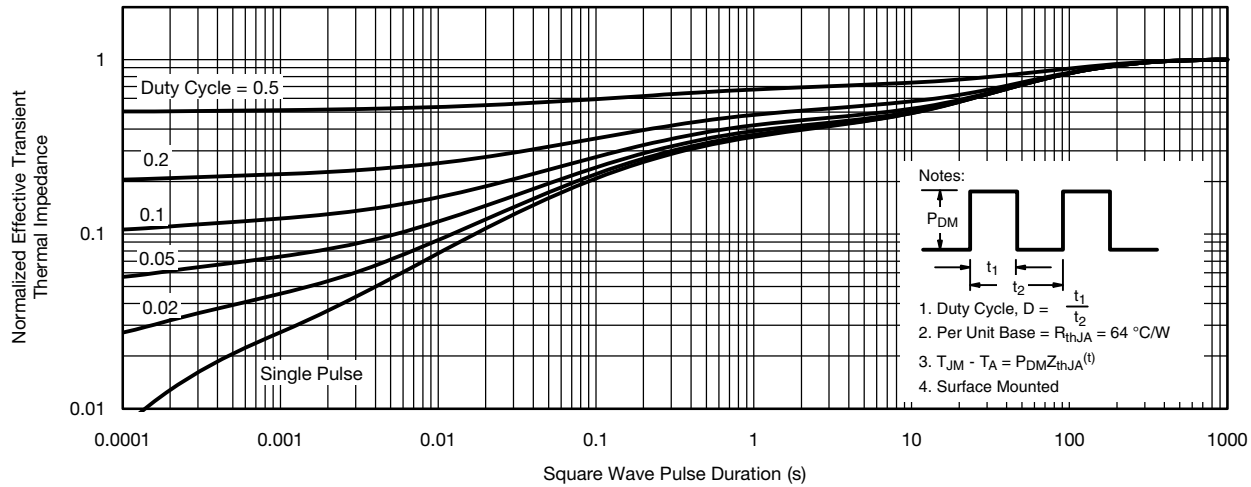
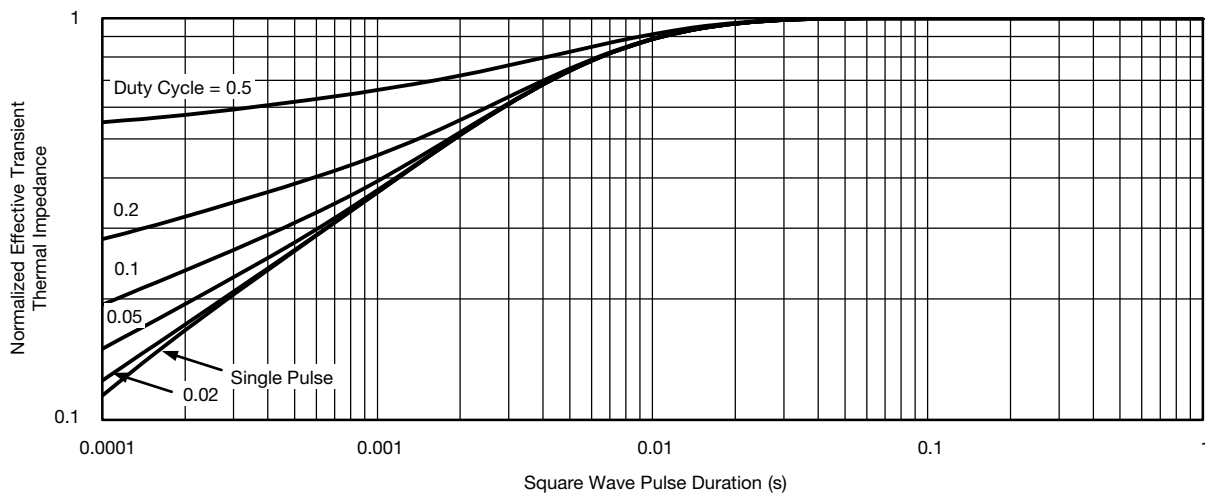


**Power, Junction-to-Case**



**Power, Junction-to-Ambient**

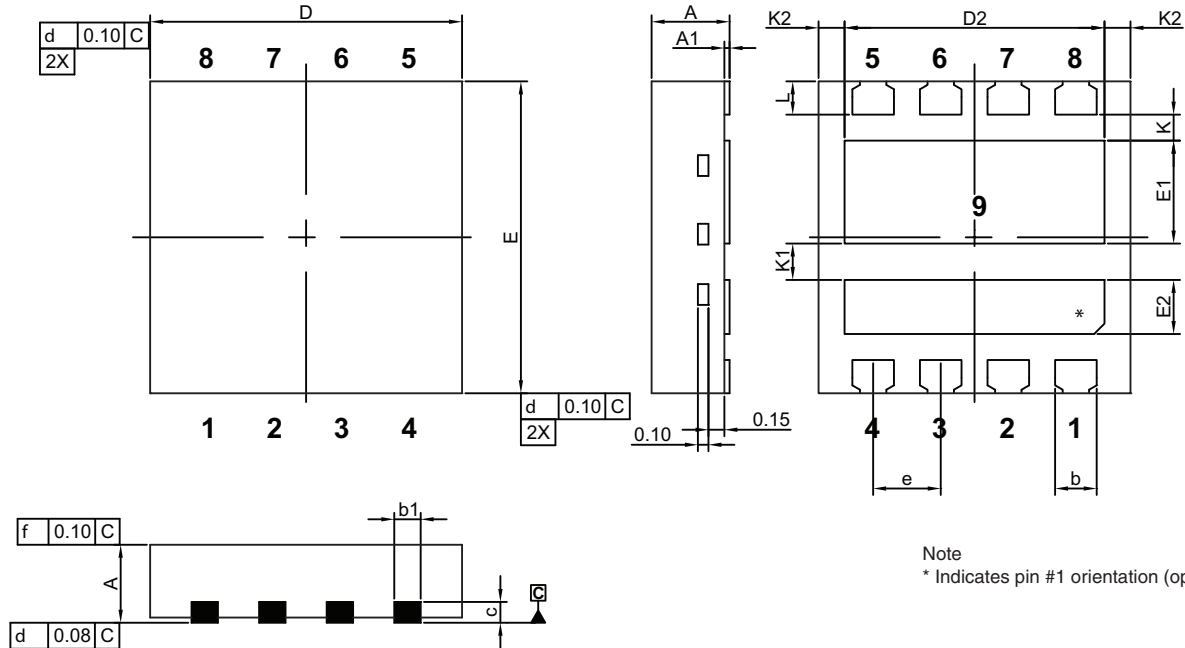
\* The power dissipation  $P_D$  is based on  $T_{J(max.)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Normalized Thermal Transient Impedance, Junction-to-Ambient**

**Normalized Thermal Transient Impedance, Junction-to-Case**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?62877](http://www.vishay.com/ppg?62877).



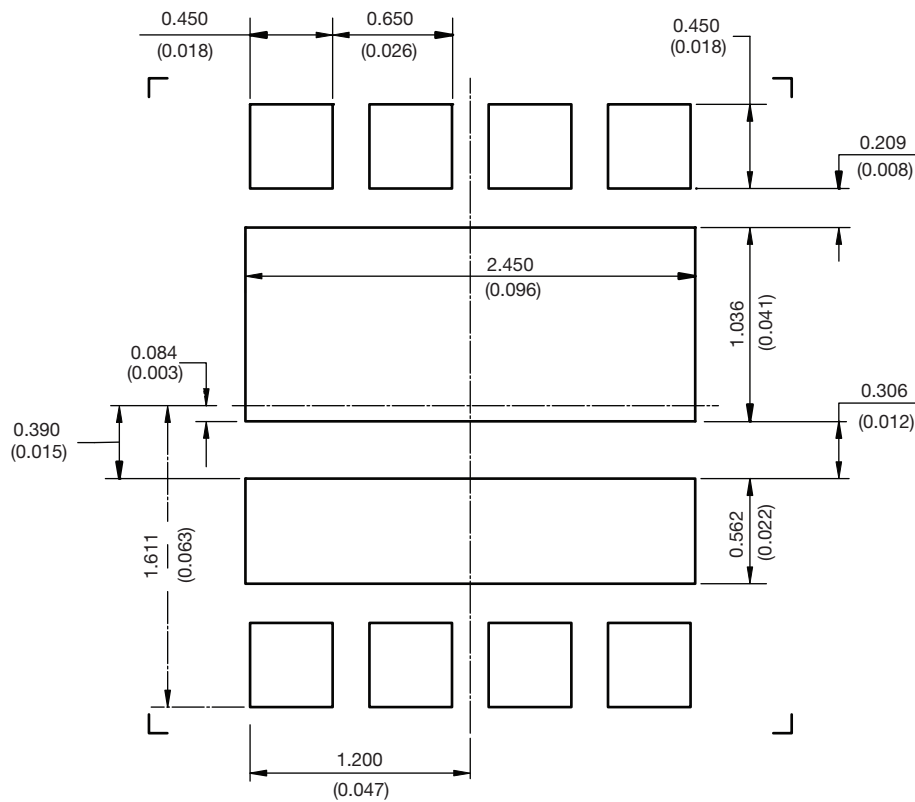
### PowerPAIR® 3 x 3 Case Outline



Note  
\* Indicates pin #1 orientation (optional)

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00		0.05	0.000		0.002
b	0.35	0.40	0.45	0.014	0.016	0.018
b1	0.20	0.25	0.38	0.008	0.010	0.015
C	0.18	0.20	0.23	0.007	0.008	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	2.35	2.40	2.45	0.093	0.094	0.096
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	0.94	0.99	1.04	0.037	0.039	0.041
E2	0.47	0.52	0.57	0.019	0.020	0.022
e	0.65 BSC			0.026 BSC		
K	0.25 typ.			0.010 typ.		
K1	0.35 typ.			0.014 typ.		
K2	0.30 typ.			0.012 typ.		
L	0.27	0.32	0.37	0.011	0.013	0.015
ECN: T12-0347-Rev. C, 18-Jun-12						
DWG: 5998						

## RECOMMENDED MINIMUM PAD FOR PowerPAIR® 3 x 3



Recommended PAD for PowerPAIR 3 x 3

Dimensions in millimeters (inches)

Keep-Out 3.5 mm x 3.5 mm for non terminating traces



## Disclaimer

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# Mouser Electronics

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