

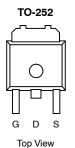
### SUD50N024-06P **Vishay Siliconix**

Pb-free

Available

## N-Channel 22-V (D-S) 175°C MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	V <sub>DS</sub> (V) r <sub>DS(on)</sub> (Ω)			
24 <sup>C</sup>	0.006 @ V <sub>GS</sub> = 10 V	80		
	0.0095 @ V <sub>GS</sub> = 4.5 V	64		



Drain Connected to Tab

Ordering Information:

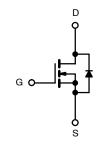
SUD50N024-06P SUD50N024-06P—E3 (Lead (Pb)-Free)

#### **FEATURES**

- TrenchFET<sup>®</sup> Power MOSFET •
- 175°C Junction Temperature
- PWM Optimized for High Efficiency •
- 100% R<sub>g</sub> Tested
  Lead (Pb)-Free Version is RoHS Compliant

#### **APPLICATIONS**

- Synchronous Buck DC/DC Conversion
  - Desktop - Server



N-Channel MOSFET

Parameter		Symbol	Limit	Uni	
Drain-Source Pulse Voltage	V <sub>DS(pulse)</sub>	24 <sup>C</sup>			
Drain-Source Voltage		V <sub>DS</sub>	22	V	
Gate-Source Voltage		V <sub>GS</sub>	±20		
	$T_{C} = 25^{\circ}C$		80 <sup>d</sup>		
Continuous Drain Current <sup>a</sup>	T <sub>C</sub> = 100°C	ID ID	56 <sup>d</sup>		
Pulsed Drain Current		I <sub>DM</sub>	100	А	
Continuous Source Current (Diode Conduction) <sup>a</sup>		IS	26		
Avalanche Current, Single Pulse	L = 0.1 mH	I <sub>AS</sub> 45			
Avalanche Energy, Single Pulse		E <sub>AS</sub>	101	mJ	
Maximum Davies Dissis attac	$T_A = 25^{\circ}C$		6.8 <sup>a</sup>	w	
Maximum Power Dissipation	$T_{C} = 25^{\circ}C$	P <sub>D</sub>	65		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to 175	°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
	$t \le 10 \text{ sec}$	R <sub>thJA</sub>	18	22	°C/W	
Maximum Junction-to-Ambient <sup>a</sup>	Steady State		40	50		
Maximum Junction-to-Case		R <sub>thJC</sub>	1.9	2.3		

Notes

Surface Mounted on FR4 Board, t  $\leq$  10 sec. a.

b. Limited by package

Calculation based on maximum allowable Junction Temperature. Package limitation current is 50 A. c. d.

### **Vishay Siliconix**



#### SPECIFICATIONS (T<sub>.1</sub> = $25^{\circ}$ C UNLESS OTHERWISE NOTED)

Parameter Symbol Test Condit		Test Condition	Min	Typ <sup>a</sup>	Max	Unit
Static	1 1					1
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS}$ = 0 V, $I_D$ = 250 $\mu$ A	22			v
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \ \mu A$	0.8		3.0	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 20 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			1	μΑ
		$V_{DS}$ = 20 V, $V_{GS}$ = 0 V, $T_{J}$ = 125 °C			50	
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	50			A
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		0.0046	0.006	
Drain-Source On-State Resistance <sup>b</sup>	r <sub>DS(on)</sub>	$V_{GS}$ = 10 V, $I_D$ = 20 A, $T_J$ = 125°C			0.0084	Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$		0.0073	0.0095	1
Forward Transconductanceb	9 <sub>fs</sub>	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 20 \text{ A}$	15			S
Dynamic <sup>a</sup>			•		•	
Input Capacitance	C <sub>iss</sub>			2550		pF
Output Capacitance	C <sub>oss</sub>	$V_{GS}$ = 0 V, $V_{DS}$ = 10 V, f = 1 MHz		900		
Reverse Transfer Capacitance	C <sub>rss</sub>			415		
Gate Resistance	Rg		0.7	1.5	2.1	Ω
Total Gate Charge <sup>c</sup>	Qg			19	30	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{DS}$ = 10 V, $V_{GS}$ = 4.5 V, $I_{D}$ = 50 A		7.5		
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			6.0		
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			11	20	- ns
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 10 \text{ V}, \text{ R}_{1} = 0.2 \Omega$		10	15	
Turn-Off Delay Timec	t <sub>d(off)</sub>	$\begin{array}{l} V_{DD} = 10 \; V,  R_L = 0.2 \; \Omega \\ I_D \; \cong \; 50 \; A,  V_{GEN} = 10 \; V,  R_g = 2.5 \; \Omega \end{array}$		24	35	
Fall Time <sup>c</sup>	t <sub>f</sub>			9	15	
Source-Drain Diode Ratings and	Characteristi	c (T <sub>C</sub> = 25°C)		•		
Pulsed Current	I <sub>SM</sub>				100	Α
Diode Forward Voltage <sup>b</sup>	V <sub>SD</sub>	$I_{F} = 50 \text{ A}, V_{GS} = 0 \text{ V}$		1.2	1.5	V
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 50 A, di/dt = 100 A/μs	1	35	70	ns

Notes

Guaranteed by design, not subject to production testing. Pulse test; pulse width  $\leq 300 \ \mu$ s, duty cycle  $\leq 2\%$ . Independent of operating temperature. a.

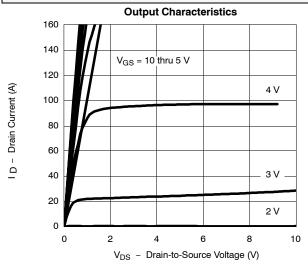
b.

c.

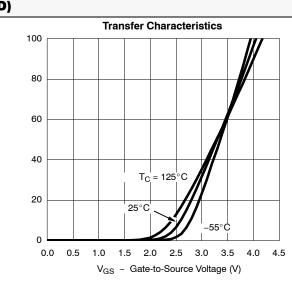
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

I D - Drain Current (A)

### TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



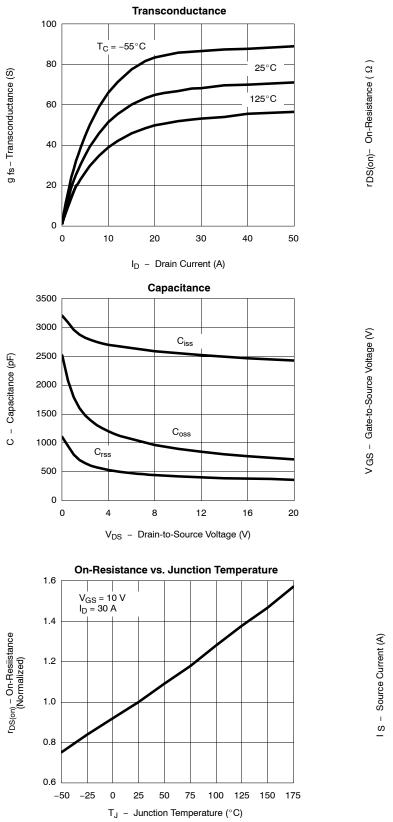


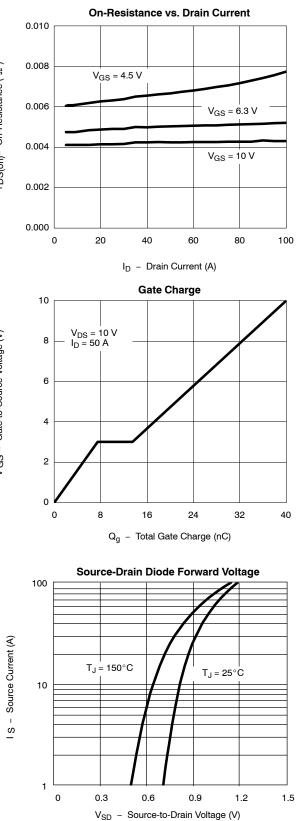




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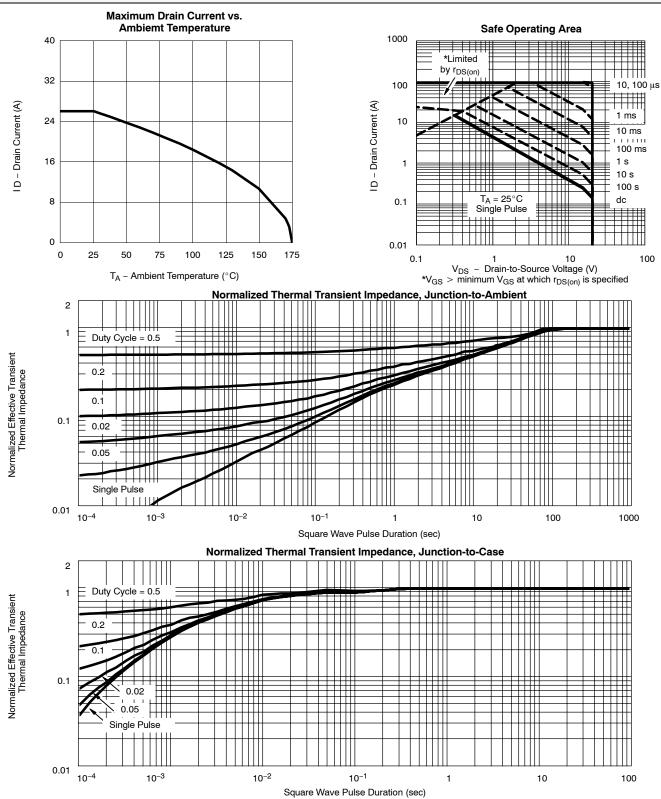
### TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





### **Vishay Siliconix**

#### THERMAL RATINGS



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?72289.



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