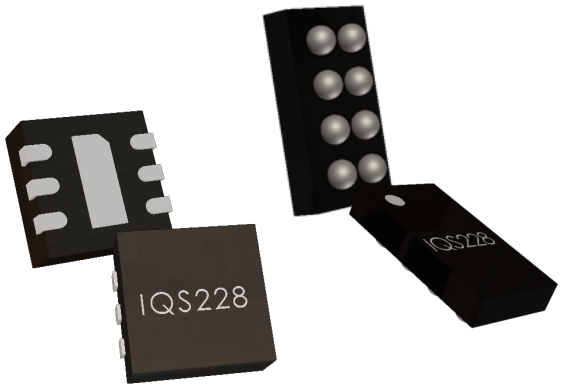
IQS228B/D DATASHEET

Single Channel Capacitive Proximity and Touch Controller

The ProxSense® **IQS228B/D** is a single channel self-capacitive sensor with Dynamic Calibration (DYCAL™) to allow for sensor drift during prolonged activation.

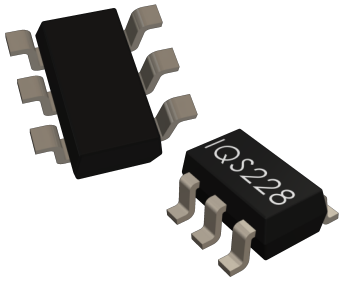
Features

- 1 Self capacitive channel
- DYCAL™: Intelligent hysteresis
- Proximity and Touch outputs
- Automatic Tuning
- Minimum external components
- 1-Wire data streaming
- I²C Debug option
- User selectable options (OTP)
- I/O Sink or Source selection
- Time-out for stuck key
- Proximity and Touch sensitivity selections



Applications

- Proximity sensors
- On-ear detection for mobile phones
- Personal Media Players
- Human Interface Devices
- SAR detection for Tablets
- 3D glasses
- White goods and appliances
- Proximity activated backlighting



RoHS2
Compliant

Packages
Representation only, not actual markings

Available Options

T_A	DFN-6	TSOT23-6	WLCSP-8
-40°C to 85°C	IQS228B IQS228D	IQS228B IQS228D	IQS228B -

Supply Voltage and Low Power Consumption

Device	Supply Voltage	Low Power Mode
IQS228B	1.8 V to 3.6 V	2.5 µA
IQS228D	2.4 V to 5.5 V	3.2 µA

Contents

List of Abbreviations

ATI	Automatic Tuning Implementation
BP	Boost Power Mode
CS	Counts (Number of Charge Transfers)
C_S	Internal Reference Capacitor
DYCAL™	Dynamic Calibration
EMI	Electromagnetic Interference
ESD	Electro-Static Discharge
FTB/EFT	(Electrical) Fast Transient Bursts
GND	Ground
HC	Halt Charge
LP	Low Power Mode
LTA	Long Term Average
THR	Threshold
TM	Touch Mode

1 Overview

1.1 Device

The IQS228B/D is a single channel capacitive proximity and touch device which employs an internal voltage regulator and reference capacitor (C_S).

The IQS228B/D device has a dedicated pin for the connection of a sense electrode (Cx) and output pin for proximity and touch events on **TOUT**. The polarity of the output pins can be configured. A 1-wire open drain data streaming protocol or I^2C interface is implemented for debugging purposes.

Special device configuration can be done by setting one time programmable (OTP) options.

The device automatically tracks slow varying environmental changes via various signal processing algorithms and has an Automatic Tuning Implementation (ATI) algorithm to calibrate the device to the sense electrode.

DYCAL™ (Dynamic Calibration) is a special form of hysteresis that can track slow varying environmental change even while the sensor is in a touch state. This is ideal for portable applications.

The *charge transfer* method of capacitive sensing is employed on the IQS228B/D. (The Charge Transfer principle is thoroughly described in the application note: *AZD004 - Azoteq Capacitive Sensing*)

1.2 Operation

The device has been designed to be used in applications where proximity is required, and touch conditions can prevail for an extended period of time which may result in uncompensated drift in conventional capacitive sensors.

A low threshold is used to detect the proximity of an object with a higher threshold for touch detection.

Dynamic Calibration is performed when a **TOUCH** condition is detected for longer than t_{DYCAL}. The hysteresis algorithm will now check for the release condition of the touch, while still tracking environmental changes.

1.3 Applicability

All specifications, except where specifically mentioned otherwise, provided by this datasheet are applicable to the following ranges:

- Temperature:
  - IQS228B/D: -40°C to 85°C
- Supply voltage (V_{DDHI}):
  - IQS228B: 1.8 V to 3.6 V
  - IQS228D: 2.4 V to 5.5 V

2 Packaging and Pin-Out

The IQS228B is available in a TSOT23-6, DFN-6 or WLCSP-8 package. The IQS228D is available in a DFN-6 or TSOT23-6 package.

2.1 Pin-out TSOT23-6

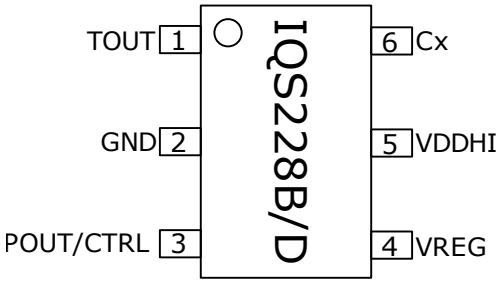


Figure 2.1: IQS228B/D TSOT23-6 Pin-out

Table 2.1: TSOT23-6 Pin-out Description

IQS228B/D TSOT23-6			
Pin	**Name**	**Type**	**Function**
1	TOUT	Digital Output	Touch output
2	GND	Ground	GND Reference
3	POUT/CTRL	Digital Input/Output	Control input or proximity output
4	VREG	Analogue Output	Internal Regulator Pin (Connect 1µF bypass capacitor)
5	VDDHI	Supply Input	Supply voltage Input
6	Cx	Analogue	Sense Electrode

2.2 Pin-out WLCSP-8

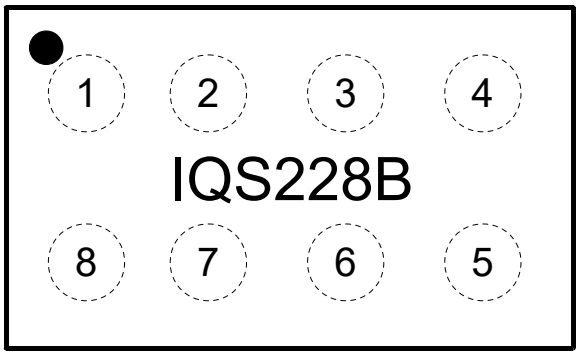


Figure 2.2: IQS228B WLCSP-8 Pin-out

Table 2.2: WLCSP-8 Pin-out Description

IQS228B WLCSP-8			
Pin	**Name**	**Type**	**Function**
1	Cx	Sense electrode	Connect to conductive area intended for sensor
2	TOUT	Digital Output	Touch output
3	VREG	Regulator output	Requires external capacitor
4	VSS	Signal GND	GND Reference
5	INPUT	Digital Input	Floating input during runtime. Recommended: Connect to POUT
6	POUT/CTRL	Digital Input/Output	Control input or proximity output
7	VDDHI	Supply Input	Supply voltage input
8	PGM	Configuration pin	Connection for OTP programming. Floating input during runtime. Recommended: Connect to TOUT pin. Programming can still be performed using this pin, provided a diode is used. (See *AZD026 - Configuration Tools Overview*)

2.3 Pin-out DFN-6

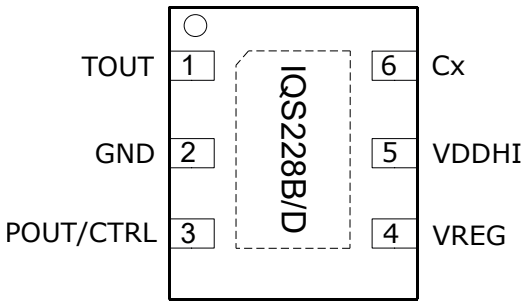


Figure 2.3: IQS228B/D DFN-6 Pin-out

Table 2.3: DFN-6 Pin-out Description

IQS228B/D DFN-6			
Pin	**Name**	**Type**	**Function**
1	TOUT	Digital Output	Touch output
2	GND	Ground	GND Reference
3	POUT/CTRL	Digital Input/Output	Control input or proximity output
4	VREG	Analogue Output	Internal Regulator Pin (Connect 1µF bypass capacitor)
5	VDDHI	Supply Input	Supply voltage Input
6	Cx	Analogue	Sense Electrode
7	PAD	VSS	Electrically connected to GND

3 Reference Schematic

3.1 TSOT23-6

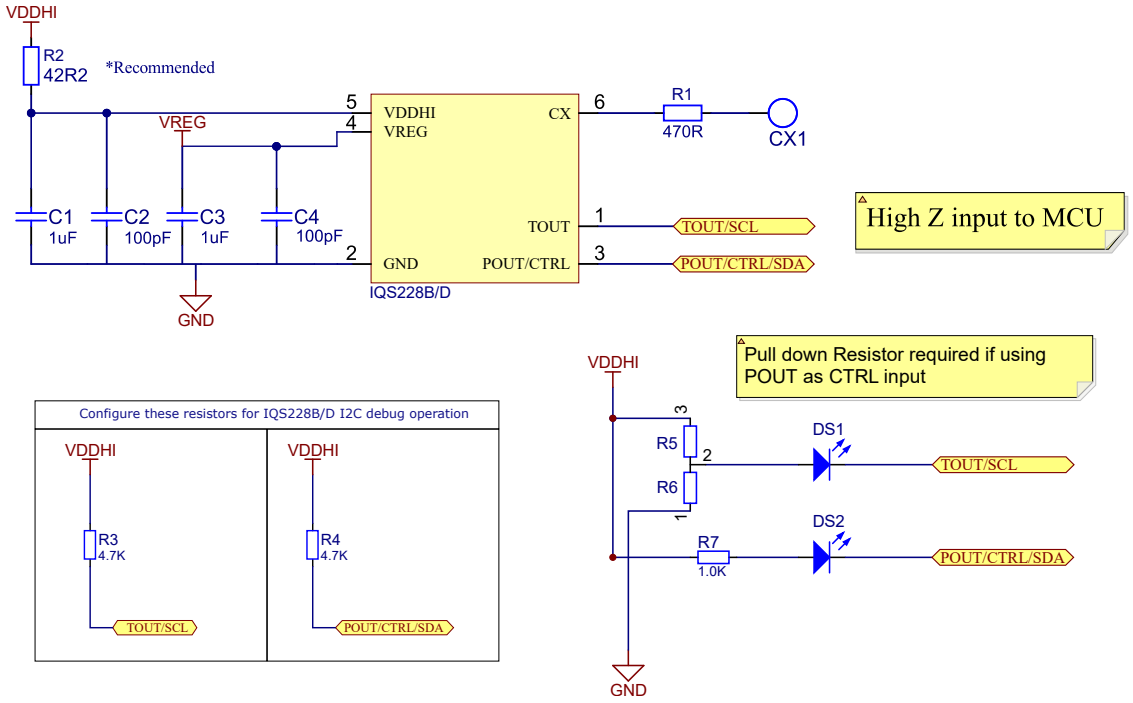


Figure 3.1: Typical application reference schematic of IQS228B/D. 100 pF capacitors are optional for added RF immunity. Place all decoupling capacitors (on VDDHI and VREG) as close to the IC as possible.

3.2 WLCSP-8

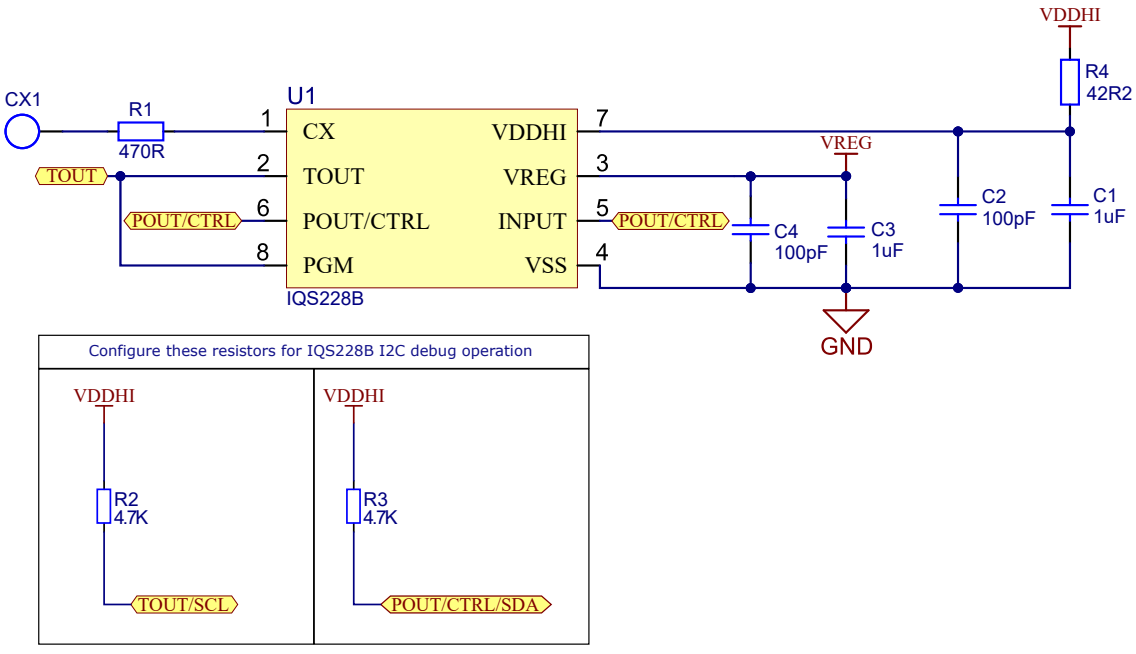


Figure 3.2: Typical application reference schematic of IQS228B WLCSP-8 Package. 100 pF capacitors are optional for added RF immunity. Place all decoupling capacitors (on VDDHI and VREG) as close to the IC as possible.

3.3 DFN-6

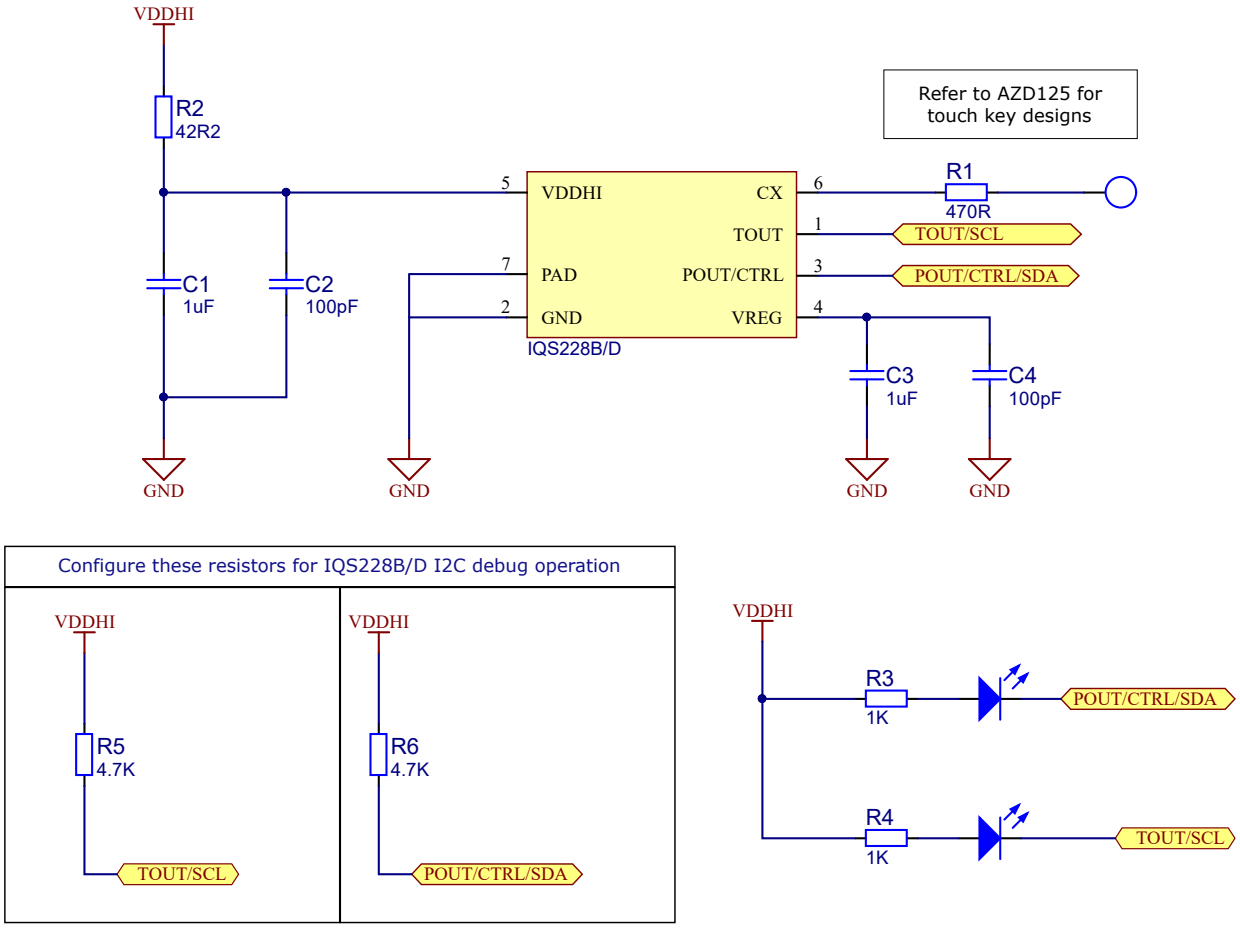


Figure 3.3: Typical application schematic of IQS228B/D. 100 pF capacitors are optional for added RF immunity. Place all decoupling capacitors (on VDDHI and VREG) as close to the IC as possible.

3.4 Additional Information and Recommendations

This section describes additional design considerations that is applicable to all reference schematics found in Section 3.1 to 3.3.

Pins TOUT and POUT/CTRL can be set as Active High or Active Low[i]. See Section 4.1 for more information.

Where a system level ESD strike is found to cause the IC to go into ESD induced latch-up, it is suggested that the supply current to the IQS228B/D IC is limited by means of a series resistor that could limit the maximum supply current to the IC to < 80 mA.

The 1 µF capacitors on VDDHI and VREG are for default power mode. See Table 3.1 to select the correct capacitors for low power modes.

The 470 Ω series resistor on the Cx pin is added for ESD protection.

[i] With the Active High setting, a pull-up resistor is not required. Adding a pull-up resistor in Active High mode negatively impacts the current usage.

3.5 Recommended Capacitor Values

The 1uF VREG capacitor(C3 in Figure 3.1, 3.2 and 3.3) value is chosen to ensure VREG does not fall the maximum remains above the maximum BOD specification stated in Table 13.2 (IQS228B) and 13.4 (IQS228D). The combination of the 1uF VREG capacitor and the 1uF VDDHI capacitor is chosen to prevent a potential ESD issue. Recommended values to prevent this is shown in Table 3.1.

Table 3.1: VDDHI and VREG capacitor size recommendation to prevent ESD issues with typical hardware combinations

Low Power Scan	8ms(default) - 32ms	64ms	128ms	160ms
Capacitor recommendation	C1 = 1 µF C3 = 1 µF	C1 = 4.7 µF C3 = 2.2 µF	C1 = 4.7 µF C3 = 2.2 µF	C1 = 4.7 µF C3 = 2.2 µF

3.6 Exception to recommended capacitor values

In applications where the VDDHI source has high internal resistance or a high resistance path, it will be required to ensure C3 > C1 to prevent a VDDHI BOD after the IC sleep cycle (see Table 13.2 and 13.4).

Table 3.2: Capacitor Values for VDDHI and VREG under certain supply voltage condition

Low Power Scan	8ms(default) - 32ms	64ms	128ms	160ms
Capacitor recommendation	C1 = 1 µF C3 = 1 µF	C1 = 2.2 µF C3 = 4.7 µF	C1 = 4.7 µF C3 = 10 µF	C1 = 4.7 µF C3 = 10 µF

4 User Configurable Options

This section lists the user configurable settings. The device is fully functional in its default state, but some applications may require alternative configuration settings. These settings are enabled by configuring One Time Programmable (OTP) user options. Popular configurations are available ex-stock - please check with the local distributor for availability. Azoteq can supply pre-configured devices for large quantities.

4.1 Configuring of Devices

Azoteq offers a Configuration Tool (CT210) and accompanying software (USBProg2.exe) that can be used to program the OTP user options for prototyping purposes.

Alternative programming solutions for the IQS228B/D also exist. For further enquiries regarding this, please contact Azoteq at *ProxSenseSupport@azoteq.com* or the local distributor.

Tables 4.1 to 4.5 all represent a hexadecimal byte in the IC configuration segment of the ordering number. As example, Table 4.1 corresponds to the last two numeric digits. These digits are shown in bold text in the caption of the table. The ordering numbers and information are explained in Section 14.1.

*Table 4.1: User Selectable Configuration Options: Bank 0 (0xC4H) – IQS228(B/D) 000000**00**DNR*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IN_EN	REL_{THR}	LOGIC	T_{THR2}	T_{THR1}	T_{THR0}	P_{THR1}	P_{THR0}

Bit 7	**IN_EN**: Input Enable 0 = Output (Proximity) 1 = Input	Section 11.2
Bit 6	**REL_{THR}**: Release threshold 0 = 75 % 1 = 85 %	Section 11.1
Bit 5	**LOGIC**: Output logic select (Only when STREAMING mode is disabled) 0 = Active Low (Open drain configuration - pull-up resistor required) 1 = Active High (Push-pull configuration - no pull-up resistor required)	Section 8.2
Bit 4-2	**T_{THR}**: Touch Threshold Selections[i] 000 = 72/256 001 = 4/256 010 = 8/256 011 = 24/256 100 = 48/256 101 = 96/256 110 = 128/256 111 = 160/256	Section 8.5
Bit 1-0	**P_{THR}**: Proximity Threshold Selections[i] 00 = 4 01 = 2 10 = 8 11 = 16	Section 8.4

[i] Refer to Section 15.1 for additional design considerations.

When Full ATI is selected in Bank 2 (Bit 2 in Table 4.3), the ATI parameters can be selected in bank 1 (Table 4.2).

*Table 4.2: User Selectable Configuration Options: Bank 1 Full ATI (0xC5H) – IQS228(B/D)0000**00**00DNR*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
t_{HALT1}	t_{HALT0}	~	~	TURBO	$BASE_2$	$BASE_1$	$BASE_0$

Bit 7-6 **t_{HALT}**: Halt times — Section 8.10
00 = 20 seconds
01 = 40 seconds
10 = Never
11 = 3 seconds

Bit 5-4 **Not used**

Bit 3 **TURBO**: DYCAL TURBO — Section 8.9
0 = Disabled
1 = Enabled

Bit 2-0 **BASE**: Base Value — Section 10.3
000 = 200
001 = 50
010 = 75
011 = 100
100 = 150
101 = 250
110 = 300
111 = 500

*Table 4.3: User Selectable Configuration Options: Bank 2 (0xC6H) - IQS228(B/D) 00**00**0000DNR*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STREAM	TRANS	COMMS	~	TARGET	ATI	LP_1	LP_0

Bit 7 **STREAM**: Streaming Method — Section 9.2
0 = 1-wire
1 = 2-wire (I^2C)

Bit 6 **TRANS**: Charge Transfer Frequency — Section 8.7
0 = 512 kHz
1 = 250 kHz

Bit 5 **COMMS**: Streaming Enable — Section 9
0 = Disabled
1 = Enabled

Bit 4 **Reserved** - Set 0

Bit 3 **TARGET**: ATI Target Counts — Section 10.2
0 = 1200
1 = 1024

Bit 2 **ATI**: ATI Selection — Section 10.1
0 = Full
1 = Partial (Not recommended - Contact Azoteq®)

Bit 1-0 **LP**: Power Mode Selection — Section 8.11
00 = BP, 9 ms (64 ms if zoom is disabled)
01 = NP, 128 ms
10 = LP1, 256 ms
11 = LP2, 512 ms (Not recommended, refer to Table 3.1 and 3.2)

*Table 4.4: User Selectable Configuration Options: Bank 3 (0xC7H) - IQS228(B/D) 0**0**000000DNR*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
~	~	~	~	ZOOM	~	~	CTRL

Bit 7-4 **Reserved**

Bit 3 **ZOOM**: Zoom Disable — Section 8.12
0 = Zoom Enabled
1 = Zoom Disabled

Bit 2-1 **Reserved**

Bit 0 **CTRL**: Control Input — Section 8.1
0 = Halt Charge
1 = Filter Halt

*Table 4.5: User Selectable Configuration Options: Bank 4 - IQS228(B/D) **0**0000000DNR*

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
~	~	~	~	ENS	~	~	~

Bit 7-4 **Reserved**

Bit 3 **ENHANCED NOISE SUPPRESSION**: Enable Enhanced Noise Suppression Section 12
0 = Enhanced Noise Suppression Disabled
1 = Enhanced Noise Suppression Enabled

Bit 2-1 **Reserved**

Bit 0 **Reserved**

5 Measuring Capacitance Using the *Charge Transfer* Method

The *charge transfer* method of capacitive sensing is employed on the IQS228B/D.

A charge cycle is used to take a measurement of the capacitance of the sense electrode (connected to Cx) relative to ground. It consists of a series of pulses charging Cx and discharging Cx to the reference capacitor, at the charge transfer frequency (f_{Cx} - refer to Section 13.2 and 13.3). The number of pulses required to reach a trip voltage on the reference capacitor is referred to as the **Count** value (CS) which is the instantaneous capacitive measurement. The Counts (CS) are used to determine if either a physical contact or proximity event occurred, based on the change in CS detected. The typical values of CS, without a touch or proximity condition range between 1344 and 1865 counts, although higher and lower counts can be used based on the application requirements. With CS larger than +/-1865 the gain of the system may become too high causing unsteady operation.

The IQS228B/D schedules a charge cycle every t_{SAMPLE} seconds to ensure regular samples for processing of results. The duration of the charge cycle is defined as t_{CHARGE} and varies according to the counts required to reach the trip voltage. Following the charge cycle other activities such as data streaming is completed (if in streaming mode), before the next charge cycle is initiated.

Please note: Attaching a probe to the Cx pin will increase the capacitance of the sense plate and therefore C_S. This may have an immediate influence on the Counts value (decrease t_{CHARGE}) and cause a proximity or touch event. After t_{HALT} seconds the system will adjust to accommodate for this charge. If the total load on Cx, with the probe attached is still lower than the maximum Cx load the system will continue to function normally after t_{HALT} seconds with the probe attached.

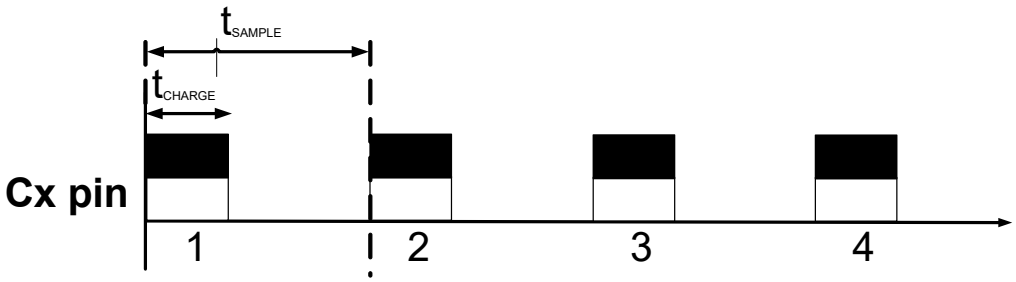


Figure 5.1: Charge cycles as can be seen on Cx.

6 DYCAL™ Operation

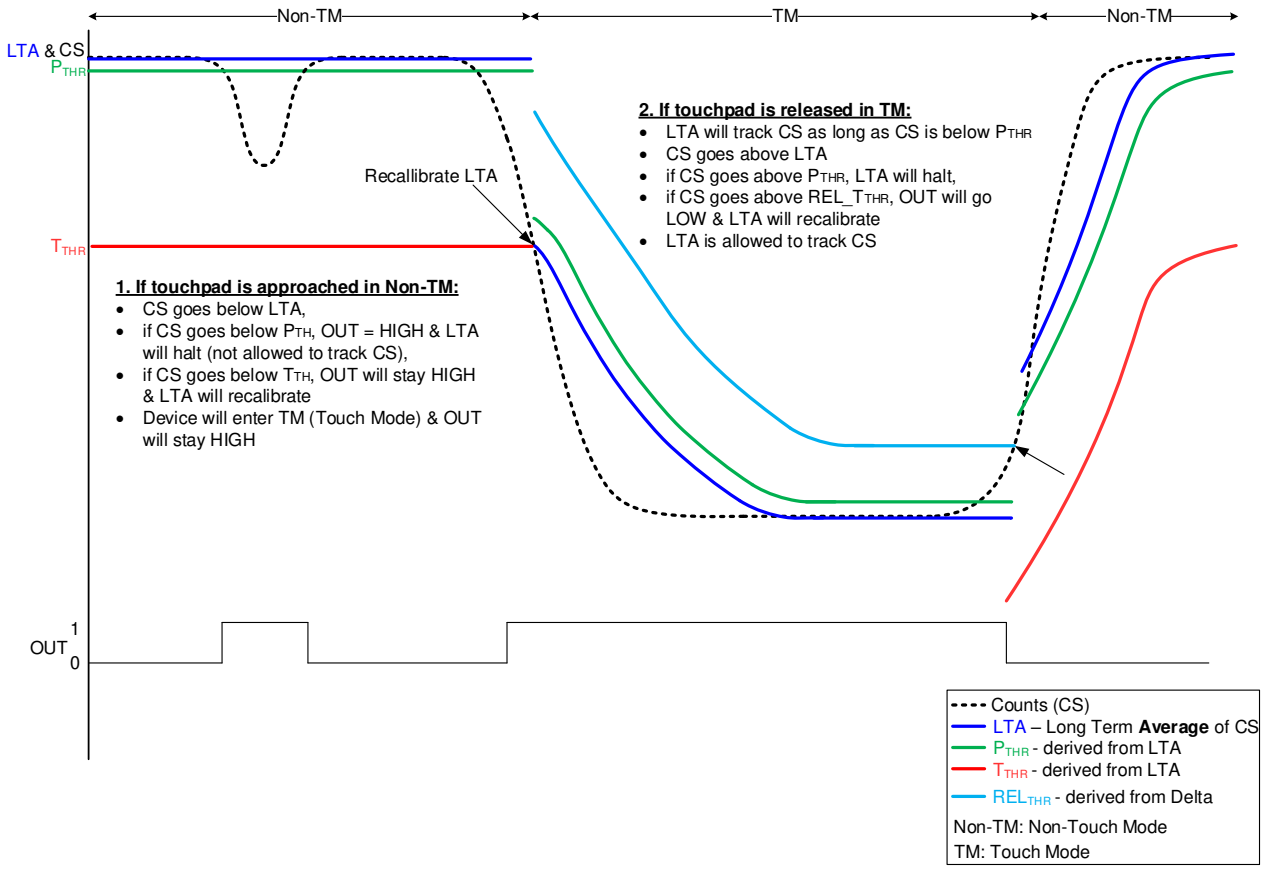


Figure 6.1: DYCAL Operation (Self Capacitive Sensing)

7 Operating Principle

Figure 6.1 is a visual representation of the DYCAL functionality. The TOUT pin is used to indicate the status of a DYCAL event (both proximity and touch event). The DYCAL functionality is summarised below.

Non-Touch Mode

The TOUT pin is activated on the successful detection of a proximity event and will remain activated for the duration of the proximity event, permitting that this event is no longer than the filter halt timings. The LTA will be halted in this time.

As soon as a touch condition is detected (Count values, or CS, fall below T_{THR}), the controller will dynamically re-calibrate its LTA to the halted LTA - T_{THR}. The IC is now Touch Mode.

Touch Mode

After re-calibration of the LTA, it will follow the Counts (CS) and be allowed to track slow varying environmental changes. If the Counts (CS) were to exceed the LTA by the release threshold (REL_T_{THR}) the touch detection will stop, and the TOUT pin will return to its original state.

8 Configurable Settings

This section describes the user configurable options of the IQS228B/D in more detail.

User programmable options are selected by configuring the OTP selections. Please refer to Section 4 for an overview of the configurable settings.

8.1 CTRL: External Control

The user has the option to control some parameters of the IQS228B/D from an external source. The IC can be used in default mode (CTRL unconnected) or the user can use the CTRL pin to select whether the master should halt the charge transfers (i.e. stop operation) or to halt LTA filter tracking on the IQS228B/D.

8.1.1 Charge Halt

If CTRL is sampled high for longer than T_{EXT_HALT}, the charge conversion cycle will be halted, once the current conversion has been completed. The device will remain in this standby mode until the CTRL line is sampled low again. An automatic reseed is performed directly after CTRL is released to compensate for any environmental changes which might have occurred during standby mode.

8.1.2 Halt LTA Filter

When configured in this mode, CTRL can be used to control the LTA halt times when sampled high. The CTRL pin has precedence over the configurations bits selected for the halt timings.

If CTRL is sampled high for longer than T_{EXT_HALT}, the filter will be halted until this pin is sampled low.

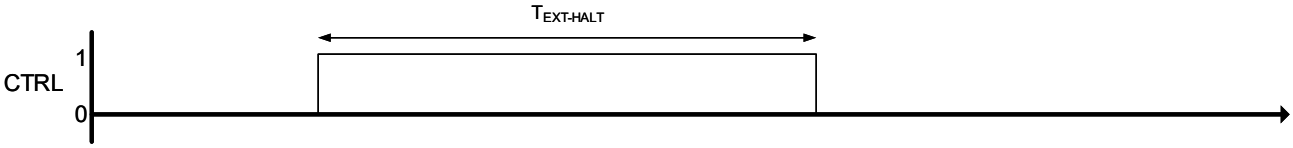


Figure 8.1: Master Output signal on CTRL pin to Halt Operation or Filter Halt

8.1.3 Pulse on CTRL:

The pulse on the POUT/CTRL pin needs to adhere to the following timing constraints:
25 ms < T_{PULSE} < 35 ms

8.1.3.1 IQS228B/D: Reseed A reseed condition can be initiated by generating a pulse on the CTRL pin. The LTA will be reset to the count, forcing the TOUT pin to its original state.

If the count value is outside its allowable limits, the device will force an ATI event to reset the system sensitivity. (Please refer to Section 10.4 for more details).

8.1.3.2 IQS228B/D: re-ATI A re-ATI condition can be initiated by generating a pulse on the CTRL pin. This function can be issued at any time.

Figure 8.2: Master Output signal on CTRL to force a Reseed Condition.

8.2 LOGIC

The logic used by the device can be selected as active HIGH or active LOW. The output pins TOUT and POUT/CTRL will function based on this selection. When configured as Active High, the outputs will remain high after POR until ATI has completed. The ATI time will vary according to the capacitive load on the sensor, but typically does not exceed 500 ms.

Configuration: *Bank 0* Bit 5

LOGIC : Logic Output Selection	
Bit	**Selection**
0	Active Low (Open drain configuration - pull-up resistor required)
1	Active High (Push-pull configuration - no pull-up resistor required)

A software open drain output is implemented for the TOUT pin when configured in active low mode. The voltage on the pull-up resistor is limited to the IQS228B/D supply voltage. A 4k7-10kΩ resistor between TOUT and VDDHI is recommended.

8.3 RF Noise on IQS228B/D

8.3.1 IQS228B/D RF Noise Immunity

Design guidelines should be followed to ensure the best noise immunity. The design of capacitive sensing applications can encompass a large range of situations but as a summary the following should

be noted to improve a design:

- A ground plane should be placed under the IC, except under the Cx line.
- All the tracks on the PCB must be kept as short as possible.
- The capacitor between VDDHI and GND as well as between VREG and GND, must be placed as close as possible to the IC.
- A 100 pF capacitor should be placed in parallel with the 1 µF capacitor between VDDHI and VSS. Another 100 pF capacitor can be placed in parallel with the 1 µF capacitor between VREG and GND.
- If the device is too sensitive for a specific order option, a parasitic capacitor (typically 20 pF) can be added between Cx line and ground.
- Proper sense electrode and button design principles must be followed. See application note *AZD125 - Capacitive Sensing Design Guide* for more information.
- Unintentional coupling of the sense electrode to ground and other circuitry must be limited by increasing the distance to these sources.

In some instances a ground plane some distance from the device and sense electrode may provide significant shielding from undesired interference.

When the capacitance between the sense electrode and ground becomes too large the sensitivity of the device may be influenced.

8.4 Proximity Threshold

The IQS228B/D has 4 proximity threshold settings indicated in counts[i]. The proximity threshold is selected by the designer to obtain the desired sensitivity and noise immunity. A proximity event is triggered if the Counts (CS) diverges more than the selected threshold from the LTA for 6 consecutive cycles.

Configuration: *Bank 0* Bit 1-0

P_{THR1}:P_{THR0} : Proximity Thresholds	
Bit	**Selection**
00	4
01	2 (Most sensitive)
10	8
11	16 (Least sensitive)

8.5 Touch Threshold

The IQS228B/D has 8 touch threshold settings indicated in counts[i]. The touch threshold is selected by the designer to obtain the desired touch sensitivity. A touch event is triggered if the Counts (CS) diverges more than the selected threshold from the LTA for 2 consecutive cycles.

In the NO-TOUCH STATE the Counts (CS) must diverge more than the touch threshold value below the LTA. Operating in the TOUCH STATE, the CS must diverge more than REL_T_{THR} of the touch threshold value above the LTA.

The following equation is used to determine if a touch or release event occurred.
NO-TOUCH STATE: LTA-CS$\leq T_{THR}$
TOUCH STATE: CS-LTA$\geq$ REL_T_{THR}

[i] Refer to Section 15.1 for additional design considerations.

Configuration: *Bank 0* Bit 4-2

T_{THR2}:T_{THR0} : Touch Thresholds		
Bit	**Selection**	
000	72/256	
001	4/256	(Most sensitive)
010	8/256	
011	24/256	
100	48/256	
101	96/256	
110	128/256	
111	160/256	(Least sensitive)

8.6 Multipliers

When using partial ATI, the base value is set up using the multipliers. Compensation will still be added automatically to reach the target.

8.7 Charge Transfer

The charge transfer frequency of the IQS228B/D is adjustable. Refer to application note *AZD102 - Series resistance limit of self capacitance charge transfers*. Two options are available:

Configuration: *Bank 2* Bit 6

TRANS : Charge Transfer Frequency	
Bit	**Selection**
0	512 kHz
1	250 kHz

8.8 Target Counts

The target of the ATI algorithm can be adjusted between 1200 (default) and 1024 counts. When less sensitivity is required, the lower counts will also increase response rate:

Configuration: *Bank 2* Bit 3

Target : ATI target counts	
Bit	**Selection**
0	1200
1	1024

8.9 DYCAL TURBO

In some applications, it may be required to improve the entry and exit speed of Touch Mode by removing the entry reseed delay, as well as turning off the AC-filters. This can be done by enabling the DYCAL TURBO mode.

Configuration: *Bank 1* Bit 3

TURBO : DYCAL TURBO	
Bit	**Selection**
0	Disabled
1	Enabled

Note that if DYCAL TURBO is enabled, the LTA will halt at the reseed point for t_{HALT} if Touch Mode is entered before a proximity event is registered.

8.10 Filter Halt

The LTA filter only executes while no proximity events are detected to ensure compensation only for environmental changes. Once touch event is detected the filter will resume operation and will no longer be halted. The halt timing configuration settings determine how long the filter is halted.

Configuration: *Bank 1* Bit 7-6

Filter Halt : Filter Halt	
Bit	**Selection**
00	20 seconds
01	40 seconds
10	Never
11	3 seconds

The presence of a proximity condition for a time exceeding the halt time will be deemed as a fault state which would trigger a reseed event where after the output state an TOUT pin will be reset to its original condition.

8.11 Low Power Modes

There are 4 low power(LP) modes. The LP modes will decrease the sampling rate which will reduce the *power consumption* of the device. However, this will also decrease the response time of the device.

Configuration: *Bank 2* Bit 1-0

LP : Power Mode Selection	
Bit	**Selection**
00	9.1 ms (BP) 64 ms if Zoom disabled
01	128 ms (Normal Power Mode)
10	256 ms (Low Power Mode 1)
11	512 ms (Low Power Mode 2) Not recommended, refer to Table 3.1 and 3.2

8.12 Zoom

The IQS228B/D has the option to disable the zoom function. This means that the sample time will stay fixed, even when proximity and touch events are made. When this is activated, boost power mode will change from a 9 ms sample time, to 64 ms.

Configuration: *Bank 3* Bit 3

ZOOM: Zoom Disable	
Bit	**Selection**
0	Enabled
1	Disabled

9 Streaming Mode

The IQS228B/D has the capability to stream data to the MCU. This provides the designer the ability to obtain the parameters and sensor data within the device in order to aid design into applications. Data streaming is performed as a 1-wire data protocol on the TOUT pin OR I^2C interface. The output function of this pin is therefore lost when the device is configured in streaming mode. Data Streaming can be enabled as indicated below:

Configuration: *Bank 2* Bit 5

COMMS : Stream Mode Enable	
0	Disabled
1	Enabled

Figure 9.1 illustrates the communication protocol for initialising and sending data with the 1-wire communication protocol.

1. Communications initiated by a START bit. Bit defined as a low condition for T_{START}.
2. Following the START bit, is a synchronisation byte (T_{INIT} = 0xAA). This byte is used by the MCU for clock synchronisation.
3. Following T_{INIT} the data bytes will be sent. 8 Bytes will be sent after each charge cycle.
4. Each byte sent will be preceded by a START bit and a STOP bit will follow every byte.
5. STOP bit indicated by taking pin 1 high. The STOP bit does not have a defined period.

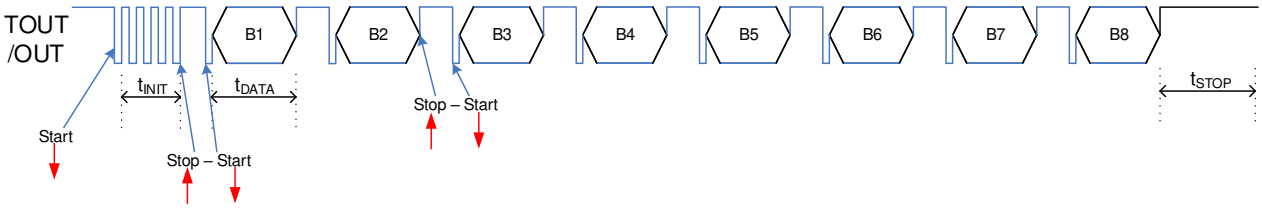


Figure 9.1: Debug: 1-wire streaming Debug Mode

The following table defines the bit definitions for the IQS228B/D devices during Streaming Mode.

Table 9.1: Byte Definitions for Streaming Mode

Byte (B)	Bit	Value
0	~	AA
1	7:0	CS High Byte
2	15:8	CS Low Byte
3	23:16	LTA High Byte
4	31:24	LTA Low Byte
5 (Sys Flags)	39 38 37 36 35 34 33 32	~ ~ Active High Filter Halt LP Active ATI Busy Noise Found In Zoom
6	47 46 45 44 43 42 41 40	Touch Proximity Multipliers Multipliers Multipliers Multipliers Multipliers Multipliers
7	55:48	Compensation
8	63:56	Counter

9.1 Event Mode

The IQS228B/D has Event Mode implemented during 1-wire communication. This allows the MCU to monitor the POUT pin for status changes (proximity or touch made or released events) instead of capturing data continuously. Upon status change, the IQS228B/D will pull the POUT pin for low to indicate to the MCU to read data. The POUT pin will stay low for 1.6 ms.

9.2 I²C

The IQS228B/D also allows for I²C streaming debugging. Data Streaming can be changed from 1-wire protocol to I²C as shown below:

Configuration: *Bank 2* Bit 7

STREAM : Streaming Mode	
0	1-Wire Protocol
1	I²C Streaming

The Memory Map for the IQS228B/D can be found in Appendix A.

The IQS228B/D can communicate on an I²C compatible bus structure. Note that 4.7 kΩ pull-up resistors should be placed on SDA and SCL.

The Control byte indicates the 7-bit device address (0x44H) and the Read/Write indicator bit.

10 Automatic Tuning Implementation (ATI)

ATI is a sophisticated technology implemented in ProxSense® devices that optimises the performance of the sensor in a wide range of applications and environmental conditions (refer to application note *AZD004 - Azoteq Capacitive Sensing*).

ATI makes adjustments through external reference capacitors unnecessary (as required by most other solutions) to obtain optimum performance.

10.1 Full ATI

The IQS228B/D implements an automatic ATI algorithm. This algorithm automatically adjusts the ATI parameters to optimise the sensing electrodes connection to the device.

The device will execute the ATI algorithm whenever the device starts-up and or when the counts are not within a predetermined range.

There are 2 important definitions to understand for ATI: ATI_{TARGET} and ATI_{BASE}. These concepts are explained next.

10.2 ATI_{Target}

ATI adjusts internal circuitry according to two parameters, the **ATI multiplier** and the **ATI compensation**.

- The **ATI multiplier** can be viewed as a course adjustment of the Counts (CS), used to achieve the ATI_{BASE} value.
- The **ATI compensation** is a fine adjustment used to reach the ATI_{TARGET} value.

With these two parameters the Counts (CS) of the IQS228B/D is tuned until as ATI_{TARGET} value of 1200 is achieved.

10.3 ATI_{BASE}: Significance of ATI Base

As mentioned above, the **ATI multiplier** is used to select a base value for the ATI. The ATI_{BASE} value is important, as this determines the sensitivity of the device. The sensitivity definition is shown in equation 1.

$$Sensitivity = \frac{ATI_{TARGET}}{ATI_{BASE}} \tag{1}$$

The ATI_{TARGET} remains fixed at 1200, and it can thus be seen from this that a large base value will result in a less sensitive device. The designer has the option to increase/reduce the sensitivity of the system through the ATI_{BASE} value. For most applications the ATI_{BASE} should be kept default.

The options for the ATI_{BASE} values are as follows:

Configuration: *Bank 1* Bit 2-0

BASE : ATI Base Selection	
Bit	**Selection**
000	200
001	50 (Not Recommended - Contact Azoteq®)
010	75
011	100
100	150
101	250
110	300
111	500

10.4 Sensitivity Due to ATI

The adjustment of the ATI parameters will result in variations in the count and sensitivity. Sensitivity can be observed as the change in count as the result of a fixed change in sensed capacitance. The ATI parameters have been chosen to provide significant overlap. It may therefore be possible to select various combinations of ATI multiplier and ATI compensation settings to obtain the same count. The sensitivity of the various options may however be different for the same count.

10.5 ATI Procedure

While the Automatic ATI algorithm is in progress, this condition will be indicated in the streaming data and proximity and touch events cannot be detected. The device will only briefly remain in this condition, and it will be entered only when relatively large shifts in the count has been detected.

The automatic ATI function aims to maintain a constant count, regardless of the capacitance of the sense electrode (within the maximum range of the device).

The effects of the auto-ATI on the application are the following:

- Automatic adjustment of the device configuration and processing parameters for a wide range of PCB and application designs to maintain an optimal configuration for proximity and touch detection.
- Automatic tuning of the sense electrode at start-up to optimise the sensitivity of the application.
- Automatic re-tuning when the device detects changes in the sensing electrodes capacitance to accommodate a large range of changes in the environment of the application that influences the sensing electrode.
- Re-tuning only occurs during device operation when a relatively large sensitivity reduction is detected. This is to ensure smooth operation of the device.
- Re-tuning may temporarily influence the normal functioning of the device, but in most instances the effect will be hardly noticeable.
- Shortly after the completion of the re-tuning process the sensitivity of a Proximity detection may be reduced slightly for a few seconds as internal filters stabilises.

Automatic ATI can be implemented so effectively due to:

- Excellent system signal-to-noise ratio (SNR)
- Effective digital signal processing to remove AC and other noise.
- The very stable core of the devices.
- The built-in capability to accommodate a large range of sensing electrode capacitances.

11 DYCAL Specific Settings

11.1 Release Threshold

The IQS228B/D has the option to increase the release threshold when in TM. This helps that small variations caused by moving a finger/hand on a touch pad will not cause the IC to exit TM, making the solution more robust. The options available are shown below:

Configuration: *Bank 0* Bit 6

REL_{THR} : Release Threshold Selection	
Bit	**Selection**
0	75 % of Entry Delta
1	87.5 % of Entry Delta

After entering TM, as soon as the LTA follows to within 16 counts, an Entry Delta value is calculated as: > Entry Delta = LTA_{entry} - $LTA_{current}$

This calculated Entry Delta a value is used for the Release Threshold as shown below.

If upon entry, the LTA value is already within 16 Counts, the Entry Delta is taken as the calculated touch threshold value.

11.2 Input Enable

The IQS228B/D can be configured to have the POUT/CTRL pin function as an output on a Proximity event.

Choosing the POUT/CTRL pin as output removes the Filter Halt and Halt Charge options of the pin as an input.

Using a touch event to activate TOUT will make the system less sensitive which is needed in some applications. The LTA will still halt with the detection of a proximity but will not have an influence on the TOUT pin. The LTA will still re-calibrate once a touch condition is detected.

Configuration: *Bank 0* Bit 7

IN_EN : Input Enable Selection	
Bit	**Selection**
0	Output
1	Input

12 Enhanced Noise Suppression

With the enhanced noise suppression active, the feature will automatically override the target value to 512 counts. This is done to complete the noise suppression algorithm as quickly as possible and ensure responsiveness.

Enhanced noise suppression will acquire 3x different samples and intelligently combine them for a more robust response when noise is present. Although the target is fixed (and less sensitive), the base value and threshold can be altered to allow for increased sensitivity.

Warning: Increased sensitivity carries a risk for false triggers when high noise levels are possible.

Configuration: *Bank 4* Bit 3

ENS : Enhanced Noise Suppression	
Bit	**Selection**
0	Enhanced Noise Suppression is Disabled
1	Enhanced Noise Suppression is Enabled

13 Electrical Specifications

13.1 Absolute Maximum Specifications

Exceeding these maximum specifications may cause damage to the device

Operating temperature		-40°C to 85°C
Supply Voltage (V_{DDHI}-V_{SS}):	IQS228B	3.6V
	IQS228D	5.5V
Maximum pin Voltage (T_{OUT}, CTRL)		V_{DDHI} + 0.3V
Minimum pin voltage (V_{DDHI}, V_{REG}, T_{OUT}, CTRL, Cx)		V_{SS} - 0.3V
Minimum power-on slope		100V/s
ESD protection (V_{DDHI}, V_{REG}, V_{SS}, T_{OUT}, CTRL, Cx)		8kV

13.2 IQS228B - General Characteristics

IQS228B devices are rated for supply voltages between 1.8V and 3.6V.

Table 13.1: IQS228B General Operating Conditions

Description	Conditions	Parameter	Min	Typ	Max	Unit
Supply voltage		V_{DDHI}	1.8	~	3.6	V
Internal regulator output	$1.8 \leq V_{DDHI} \leq 3.6$	V_{REG}	1.64	~	1.75	V
Boost operating current	$1.8 \leq V_{DDHI} \leq 3.6$	$I_{IQS228B\_BP}$	~	129	~	µA
Normal operating current	$1.8 \leq V_{DDHI} \leq 3.6$	$I_{IQS228B\_NP}$	~	6.45	~	µA
Low Power 1 operating current	$1.8 \leq V_{DDHI} \leq 3.6$	$I_{IQS228B\_LP1}$	~	3.8	~	µA
Low Power 2 operating current	$1.8 \leq V_{DDHI} \leq 3.6$	$I_{IQS228B\_LP2}$	~	<2.5	~	µA
C_x pin capacitance	$1.8 \leq V_{DDHI} \leq 3.6$	C_{X_Load}	~	~	120	pF
Charge transfer frequency range	$1.8 \leq V_{DDHI} \leq 3.6$	f_{Cx} = 512/250	-8%	f_{Cx}	+8%	kHz

Charge Transfer Timings for low power modes are found in section 8.11.

Table 13.2: IQS228B Start-up and shut-down slope Characteristics

Description	Parameter	Min	Max	Unit
Reset release voltage on V_{DDHI} rising edge	V_{DDHI} Reset Rising Edge (POR)	~	1.7	V
Reset trigger voltage on V_{DDHI} falling edge	V_{DDHI} Reset Falling Edge (BOD)	0.3	~	V
Reset release voltage on V_{REG} rising edge	V_{REG} Reset Rising Edge (POR)	~	1.58	V
Reset trigger voltage on V_{REG} falling edge	V_{REG} Reset Falling Edge (BOD)	0.3	~	V

13.3 IQS228D - General Characteristics

IQS228D devices are rated for supply voltages between 2.4V and 5.5V.

Table 13.3: IQS228D General Operating Conditions

Description	Conditions	Parameter	Min	Typ	Max	Unit
Supply voltage		V_{DDHI}	2.4	~	5.5	V
Internal regulator output	$2.4 \leq V_{DDHI} \leq 5.5$	V_{REG}	1.98	~	2.08	V
Boost operating current	$2.4 \leq V_{DDHI} \leq 5.5$	$I_{IQS228D\_BP}$	~	101	~	µA
Normal operating current	$2.4 \leq V_{DDHI} \leq 5.5$	$I_{IQS228D\_NP}$	~	6	~	µA
Low Power 1 operating current	$2.4 \leq V_{DDHI} \leq 5.5$	$I_{IQS228D\_LP1}$	~	4.5	~	µA
Low Power 2 operating current	$2.4 \leq V_{DDHI} \leq 5.5$	$I_{IQS228D\_LP2}$	~	<3.2	~	µA
C_x pin capacitance	$2.4 \leq V_{DDHI} \leq 5.5$	C_{X_Load}	~	~	120	pF
Charge transfer frequency range	$2.4 \leq V_{DDHI} \leq 5.5$	f_{Cx} = 512/250	-8%	f_{Cx}	+8%	kHz

Charge Transfer Timings for low power modes are found in section 8.11.

Table 13.4: IQS228D Start-up and shut-down slope Characteristics

Description	Parameter	Min	Max	Unit
Reset release voltage on V_{DDHI} rising edge	V_{DDHI} Reset Rising Edge (POR)	~	2.1	V
Reset trigger voltage on V_{DDHI} falling edge	V_{DDHI} Reset Falling Edge (BOD)	0.3	~	V
Reset release voltage on V_{REG} rising edge	V_{REG} Reset Rising Edge (POR)	~	1.8	V
Reset trigger voltage on V_{REG} falling edge	V_{REG} Reset Falling Edge (BOD)	0.3	~	V

13.4 IQS228B/D Input & Output Characteristics

Table 13.5: IQS228B/D Digital I/O Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{OL}	TOUT and POUT Output low voltage	I_{sink} = 10 mA	~	~	0.3	V
V_{OH}	Output high voltage	I_{source} = 5 mA	VDD – 0.3	~	~	V
V_{IL}	Input low voltage		~	~	0.3 × VDD	V
V_{IH}	Input high voltage		0.7 × VDD	~	~	V

13.5 Packaging Information

13.5.1 TSOT23-6

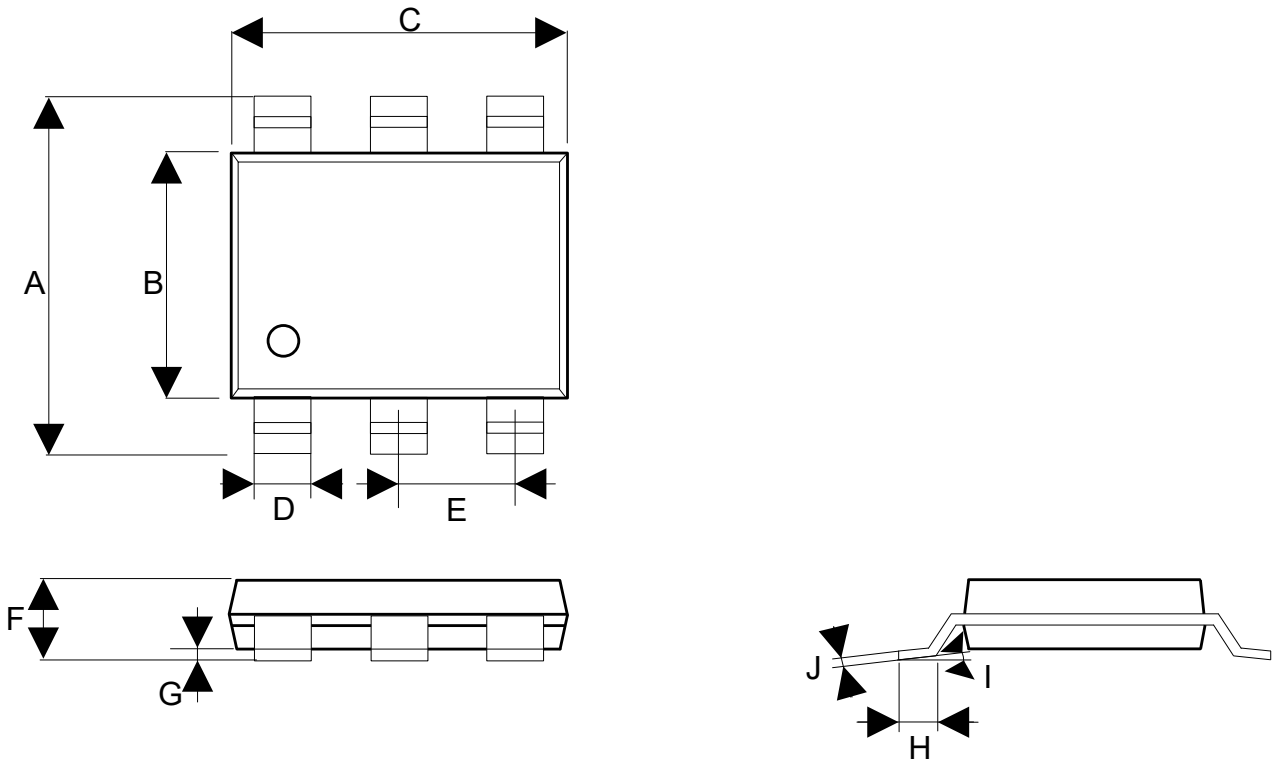


Figure 13.1: TSOT23-6 Packaging

Table 13.6: TSOT23-6 Dimensions

Dimension	Min (mm)	Max (mm)
A	2.60	3.00
B	1.50	1.70
C	2.80	3.00
D	0.30	0.50
E	0.95 Basic	
F	0.84	1.00
G	0.00	0.10
H	0.30	0.50
I	0°	8°
J	0.03	0.20

13.5.2 WLCSP-8

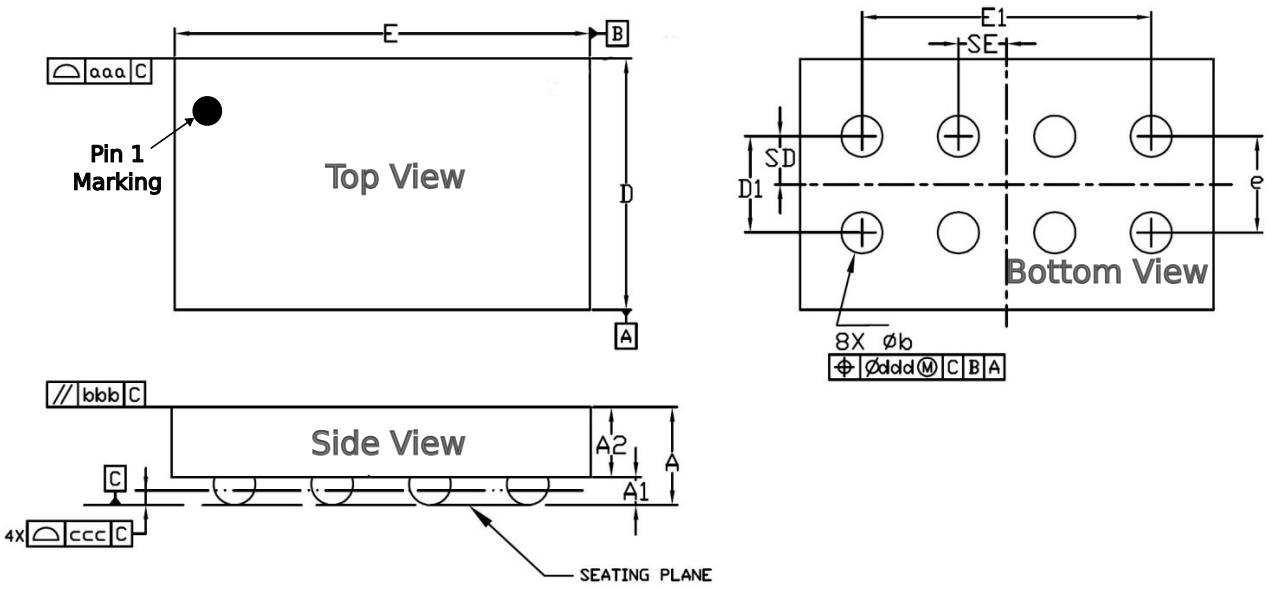


Figure 13.2: IQS228B WLCSP-8 Dimensions (in mm)

Table 13.7: WLCSP-8 Dimensions

Dimensional Ref			
REF.	**Min (mm)**	**Nom (mm)**	**Max (mm)**
A	0.310	0.350	0.390
A1	0.085	0.100	0.115
A2	0.225	0.250	0.275
D	0.865	0.880	0.895
E	1.455	1.470	1.485
D1	0.300	0.350	0.400
E1	1.000	1.050	1.100
b	0.125	0.150	0.175
e		0.350 BSC	
SD		0.175 BSC	
SE		0.175 BSC	
Tol. Form & Position			
aaa		0.10	
bbb		0.10	
ccc		0.05	
ddd		0.05	

13.5.3 DFN-6

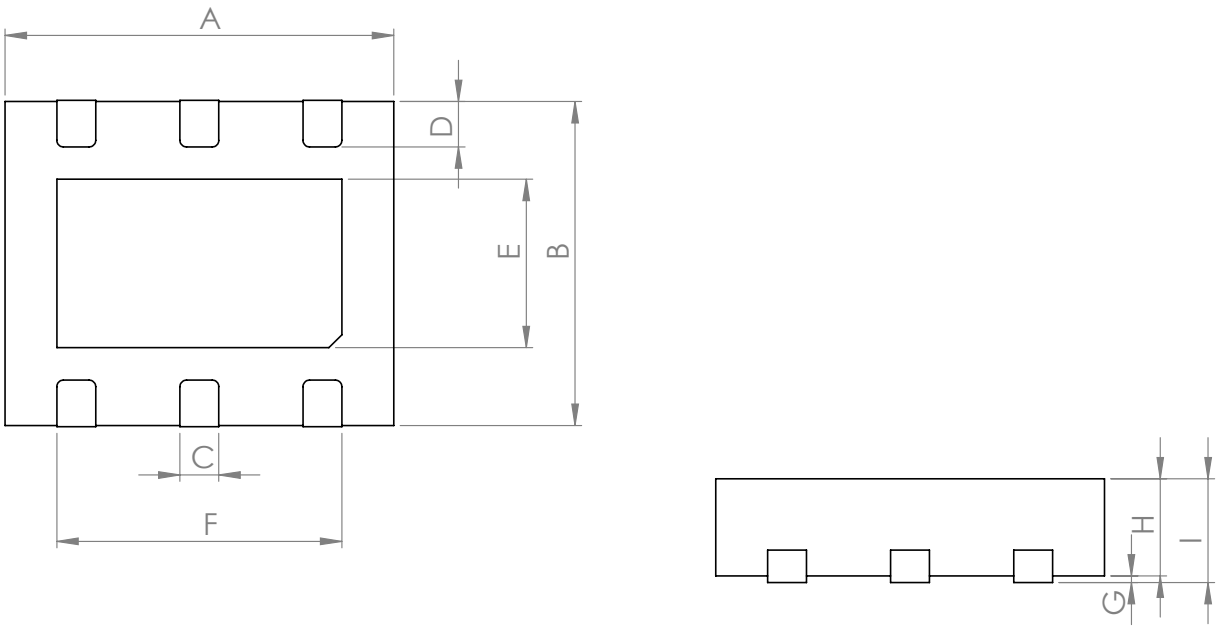


Figure 13.3: DFN-6 Packaging

Table 13.8: DFN-6 Dimensions

Dimension	Min (mm)	Max (mm)
A	3.00	3.00
B	2.50	2.50
C	0.30	0.30
D	0.35	0.35
E	1.30	1.30
F	2.20	2.20
G	0.05	0.05
H	0.75	0.75
I	0.80	0.80

13.5.4 MSL Level

Moisture Sensitivity Level (MSL) relates to the packaging and handling precautions for some semiconductors. The MSL is an electronic standard for the time period in which a moisture sensitive device can be exposed to ambient room conditions (approximately 30°C/85% RH see J-STD003C for more information) before reflow occurs.

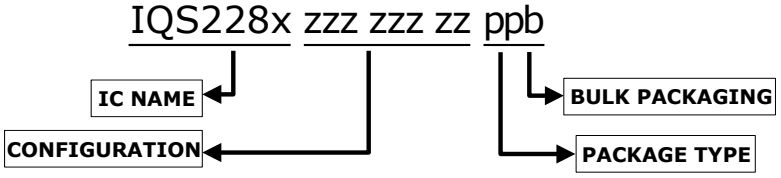
Package	Level (duration)
TSOT23-6	MSL 1 (Unlimited at $\leq$ 30°C/85% RH) Reflow profile peak temperature < 260°C for < 30 seconds
WLCSP-8	Non-encapsulated device - not moisture sensitive Reflow profile peak temperature < 260°C for < 30 seconds
DFN-6	MSL 1 (Unlimited at $\leq$ 30°C/85% RH) Reflow profile peak temperature < 260°C for < 30 seconds

14 Datasheet and Part-number Information

14.1 Ordering Information

Contact the official distributor for sample quantities. A list of the distributors can be found under the "Distributors" section of *www.azoteq.com*. Special MOQs apply for custom configurations.

The Part-number can be generated by using USBProg2.exe.



IC NAME	IQS228B	=	Self Capacitive IC with Dual Outputs (3.3V)
	IQS228D	=	Self Capacitive IC with Dual Outputs (5V)
CONFIGURATION	zzz zzz zz	=	IC Configuration (hexadecimal - See Section 4.1)
PACKAGE TYPE	TS	=	TSOT23-6 package
	CS	=	WLCSP-8 package
	DN	=	DFN-6 package
BULK Packaging	R	=	Reel
		=	TSOT23-6 (3000pcs/reel)
		=	WLCSP-8 (3000pcs/reel)
		=	DFN-6 (6000pcs/reel)
			MOQ = 1 reel. (Orders shipped as full reels)

14.2 Device Marking - Top

14.2.1 TSOT23-6 Package Markings

There are 2 marking versions in circulation for the IQS228B:

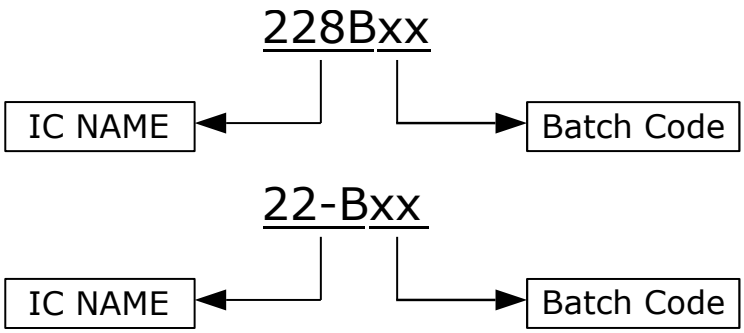


Figure 14.1: First Marking Variant of IQS228B

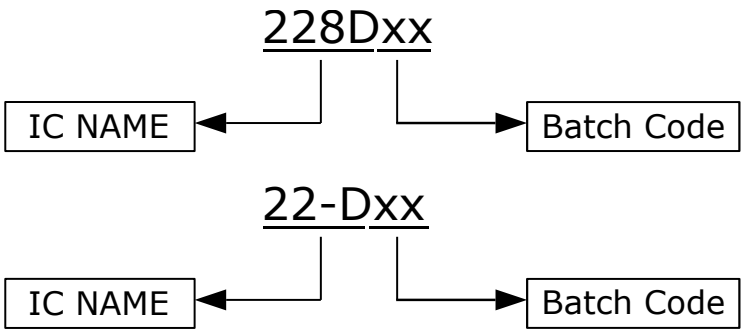


Figure 14.2: First Marking Variant of IQS228D

IC NAME	228B	=	IQS228B Self Capacitive (3.3V)
	22-B	=	IQS228B Self Capacitive (3.3V)
	228D	=	IQS228D Self Capacitive (5V)
	22-D	=	IQS228D Self Capacitive (5V)
Batch Code	xx	=	AA to ZZ

14.2.2 WLCSP-8 Package Markings

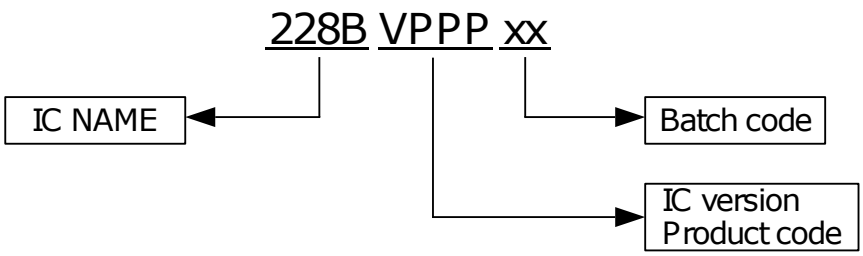


Figure 14.3: Top Marking of IQS228B WLCSP Package

IC NAME	228B	=	IQS228B Self Capacitive
Batch Code	xx	=	AA - ZZ
IC VERSION	V		
Product Code	PPP		

14.2.3 DFN-6 Package Markings

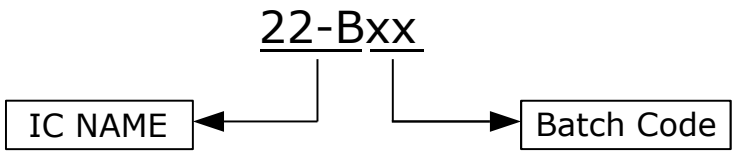


Figure 14.4: Top Marking of IQS228B

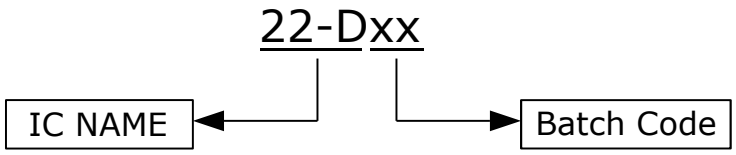
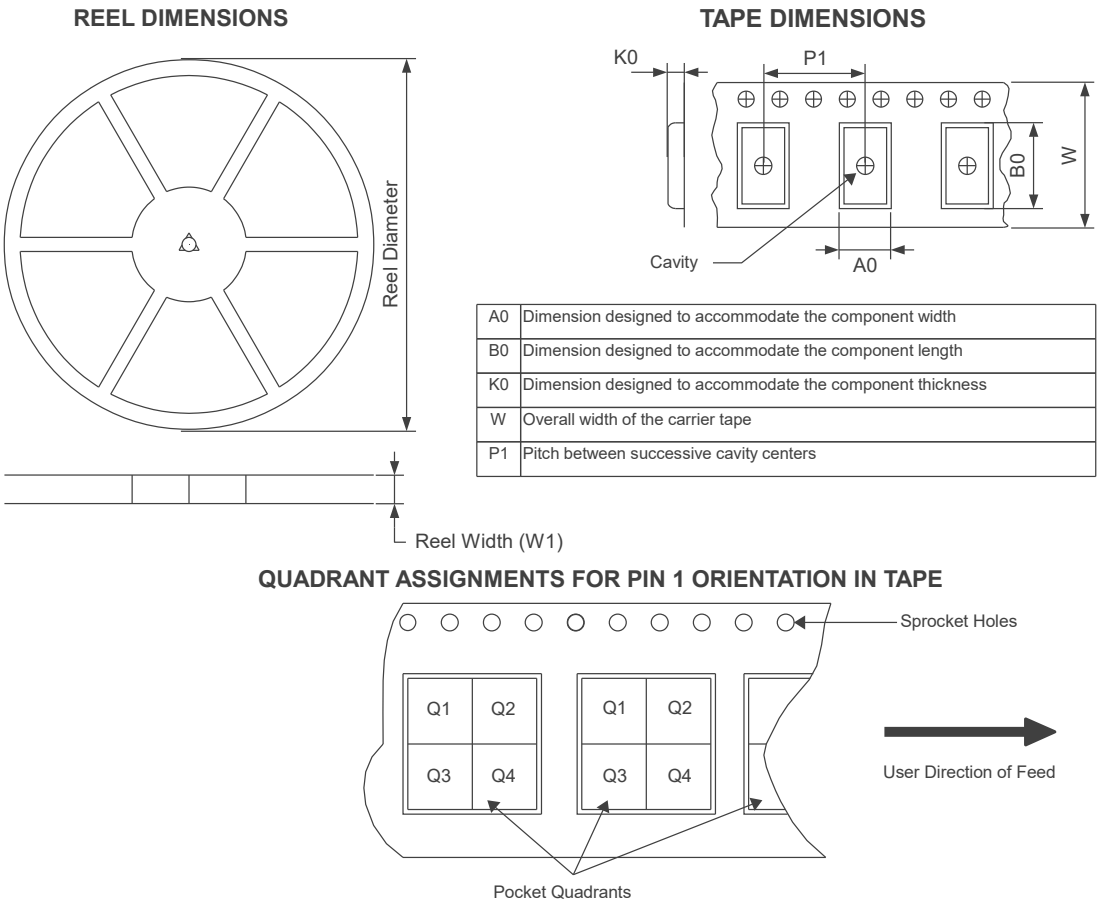


Figure 14.5: Top Marking of IQS228D

IC NAME	22-B	=	IQS228B Self Capacitive (3.3V)
	22-D	=	IQS228D Self Capacitive (5V)
Batch Code	xx	=	AA to ZZ

14.2.4 Tape and Reel Specification



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Figure 14.6: Tape and Reel Specification

Table 14.1: Tape and Reel Dimensions

Device	Package Type	Package Drawing	Pins	QTY per reel	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
IQS228B												
IQS228BzzzzzzzzTSR	TSOT23-6	TSOT23-6	6	3000	178	9.5	3.1	3.1	1.3	4	8	Q3
IQS228BzzzzzzzzCSR	WLCSP8	WLCSP-8	8	3000	179	8.4	1	1.55	0.48	4	8	Q3
IQS228BzzzzzzzzDNR	DFN6	DFN-6	6	6000	330	12	2.8	3.3	1.2	4	12	Q1
IQS228D												
IQS228DzzzzzzzzDNR	DFN6	DFN-6	6	6000	330	12	2.8	3.3	1.2	4	12	Q1
IQS228DzzzzzzzzTSR	TSOT23-6	TSOT23-6	6	3000	178	9.5	3.1	3.1	1.3	4	8	Q3

15 Known Issues

15.1 Undebounced touch without debounced proximity flag set

When a touch flag is set without the debounced proximity flag set, the LTA will reseed to the count value, quickly clearing the touch event. This effect is most pronounced with touch buttons and give missed touches with rapidly repeated touches.

Workaround:

- Ensure the proximity threshold and touch threshold are as far apart as the application and features allow it.
- The effect is less noticeable if the focus of the application is on Proximity or Touch alone instead of both.

A Memory Map

Device Information

00H		Product Number (PROD_NR)							
	Bit	7	6	5	4	3	2	1	0
Access	Value	39 (Decimal)							
R	Note								

01H		Software Number (SW_NR)							
	Bit	7	6	5	4	3	2	1	0
Access	Value	29 (Decimal)							
R	Note								

[00H] PROD_NR
The product number for the IQS228B/D is 39 (Decimal).

[01H] SW_NR
The software version number of the device ROM can be read in this byte. The latest software version is 29 (Decimal).

10H		System Flags (Sys_Flags)							
	Bit	7	6	5	4	3	2	1	0
Access	Value	~	~	Logic	Halt	LP	ATI	~	Zoom
R	Note								

[10H] SYSFLAGS0

Bit 7-6: **Reserved**

Bit 5: **Logic**: Logic Output Indication.
0 = Active Low
1 = Active High

Bit 4: **Halt**: Indicates Filter Halt Status.
0 = LTA not being Halted
1 = LTA Halted

Bit 3: **LP**: Low Power Mode.
0 = Sample time BP
1 = Sample time LP

Bit 2: **ATI**: Status of automated ATI routine.

0 = ATI is not busy

1 = ATI in progress

Bit 1: **Reserved**

Bit 0: **Zoom**: Zoom will indicate full-speed charging once an undebounced proximity is detected. In BP mode, this will not change the charging frequency.

0 = IC not zoomed in

1 = IC detected undebounced proximity and IC is charging at full speed (BP)

31H

Access
R

	Status							
Bit	7	6	5	4	3	2	1	0
Value	DYCAL	~	~	~	~	~	Touch	Prox
Note								

[31H] Status

Bit 7: **DYCAL**: DYCAL Detection.

0 = Not Active

1 = Active

Bit 6-2: **Reserved**

Bit 1: **Touch**: Touch Detection.

0 = Not Active

1 = Active

Bit 0: **Prox**: Proximity Detection.

0 = Not Active

1 = Active

42H

Access
R

	Counts_High (CS_H)							
Bit	7	6	5	4	3	2	1	0
Value	Counts High Byte							
Note								

43H

Counts_Low (CS_L)							
Bit	7	6	5	4	3	2	1	0
Value	Counts Low Byte							
Note								

Access: R

83H

LTA_High (LTA_H)							
Bit	7	6	5	4	3	2	1	0
Value	Long Term Average High Byte							
Note								

Access: R

84H

LTA_Low (LTA_L)							
Bit	7	6	5	4	3	2	1	0
Value	Long Term Average Low Byte							
Note								

Access: R

C4H

Fuse Bank 0 (FB_0)							
Bit	7	6	5	4	3	2	1	0
Value	See Table 4.1 for more details							
Note								

Access: R

C5H

Fuse Bank 1 (FB_1)							
Bit	7	6	5	4	3	2	1	0
Value	See Table 4.2 for more details							
Note								

Access: R

C6H

Fuse Bank 2 (FB_2)							
Bit	7	6	5	4	3	2	1	0
Value	See Table 4.3 for more details							
Note								

Access: R

C7H

Fuse Bank 3 (FB_3)							
Bit	7	6	5	4	3	2	1	0
Value	See Table 4.4 for more details							
Note								

Access: R

C8H		DEFAULT_COMMS_POINTER							
	Bit	7	6	5	4	3	2	1	0
Access	Value	(Beginning of Device Specific Data)							
R/W	Default	10H							

[C8H] Default Comms Pointer

The value stored in this register will be loaded into the Comms Pointer at the start of a communication window. For example, if the design only requires the Proximity Status information each cycle, then the Default Comms Pointer can be set to **ADDRESS 31H**. This would mean that at the start of each communication window, the comms pointer would already be set to the Proximity Status register, simply allowing a **READ** to retrieve the data, without the need of setting up the address.

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