IQS390 Device Datasheet

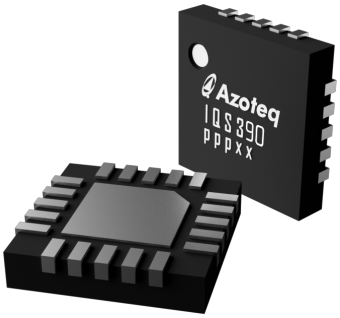
Haptics LRA driver with internal H-bridge and H-bridge protections.
I²C mode with multiple configurable waveforms and autoresonance.
PWM mode with motor direction and direct PWM input.

1 Device Overview

The IQS390 is a haptics driver capable of driving Linear Resonant Actuator (LRA) motors. The device implements an I²C mode featuring configurable composite waveforms. The I²C mode features a closed-loop autoresonance algorithm. The autoresonance algorithm matches the resonant frequency of the driven motor in real time. The PWM mode accepts an external Pulse Width Modulated (PWM) signal and a motor drive direction. Both modes implement automatic power mode management and an ultra-low power mode.

1.1 Main Features

- I²C Mode
  - I²C interface - Up to Fast Mode Plus (1 MHz)
  - Selectable I²C address
  - Highly configurable effects
  - Configure and select between multiple effects
  - Fire-and-forget interface
  - Trigger haptic pulse either through I²C or with an input pin
  - Real time closed-loop autoresonance
  - Internal or external H-bridge
  - Selectable LRA drive frequency
- PWM Mode
  - Direction and direct PWM input
- Select between modes using input pin
- Internal H-bridge protections
- Ultra-low power mode
- Automatic power mode management
- Design simplicity
  - PC software for configuration and debugging
- Supply Voltage: 1.71 V to 3.6 V
- QFN20 Package (3 × 3 × 0.55 mm) - 0.4 mm pitch



1.2 Applications

- Mouse wheel scrolling feedback
- Trackpads
- Doorbells and keypads

1.3 Block Diagram

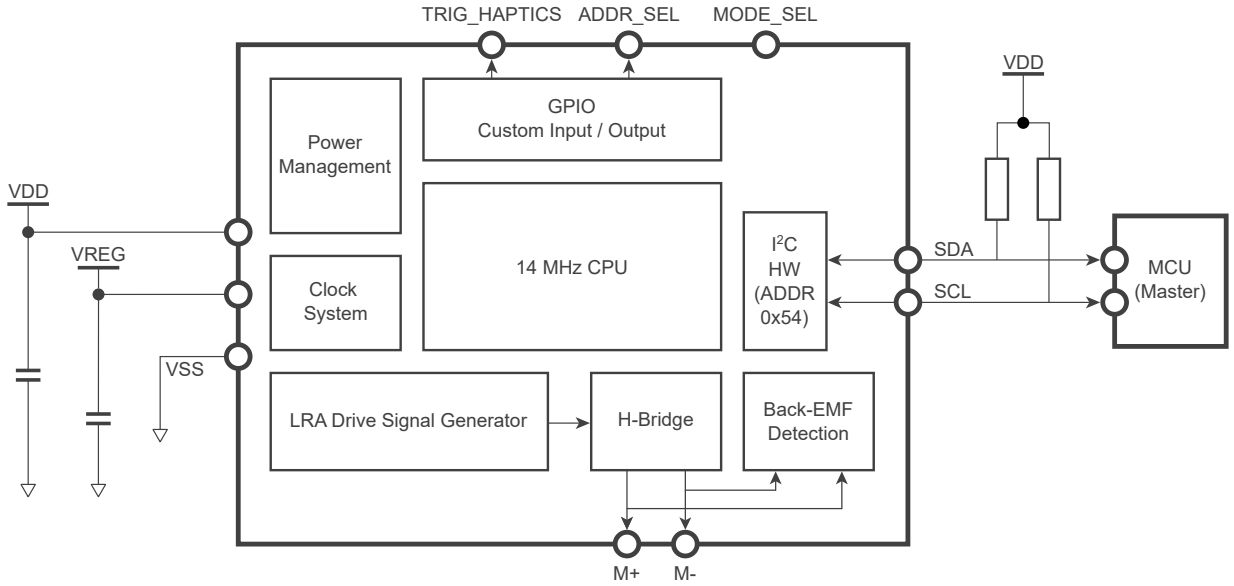


Figure 1.1: IQS390 Block Diagram

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2 Hardware Connections

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2.1.1 I²C Mode

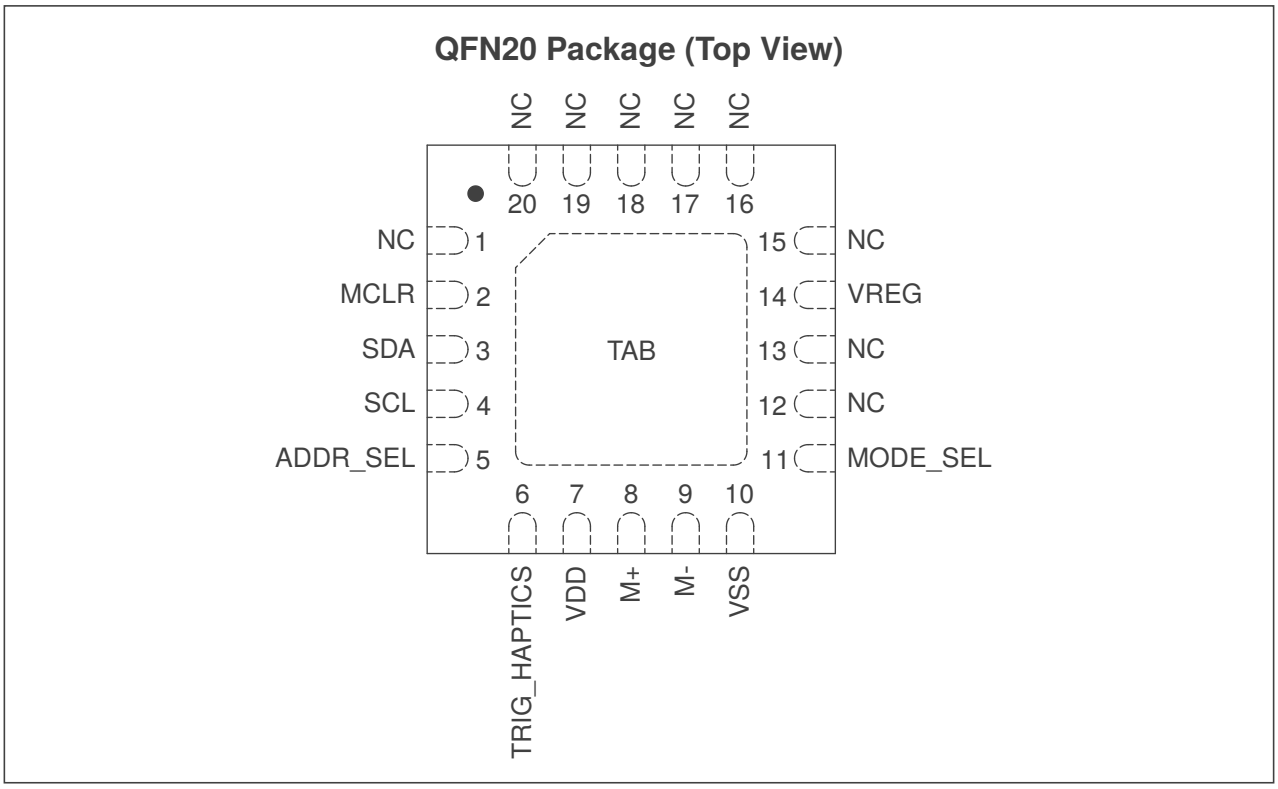


Figure 2.1: QFN20 Pinout for I²C mode

Table 2.1: QFN20 Pin Descriptions for I²C mode

Pin	Name	Type[i]	Function	Description
2	MCLR	I		Master Clear (Reset)
3	SDA	I/O	I2C	I²C data
4	SCL	I/O	I2C	I²C clock
5	ADDR_SEL	I	GPIO	I²C address selection
6	TRIG_HAPTICS	I	GPIO	Trigger haptics pin
7	VDD	P	Power	Power supply input voltage
8	M+	O	H-Bridge	
9	M-	O	H-Bridge	
10	VSS	P	Power	Analog/digital ground
11	MODE_SEL	I		Operating mode selection
*	NC	-	-	Not Connected

[i] Pin Types: I = Input, O = Output, I/O = Input or Output, P = Power

2.1.2 PWM Mode

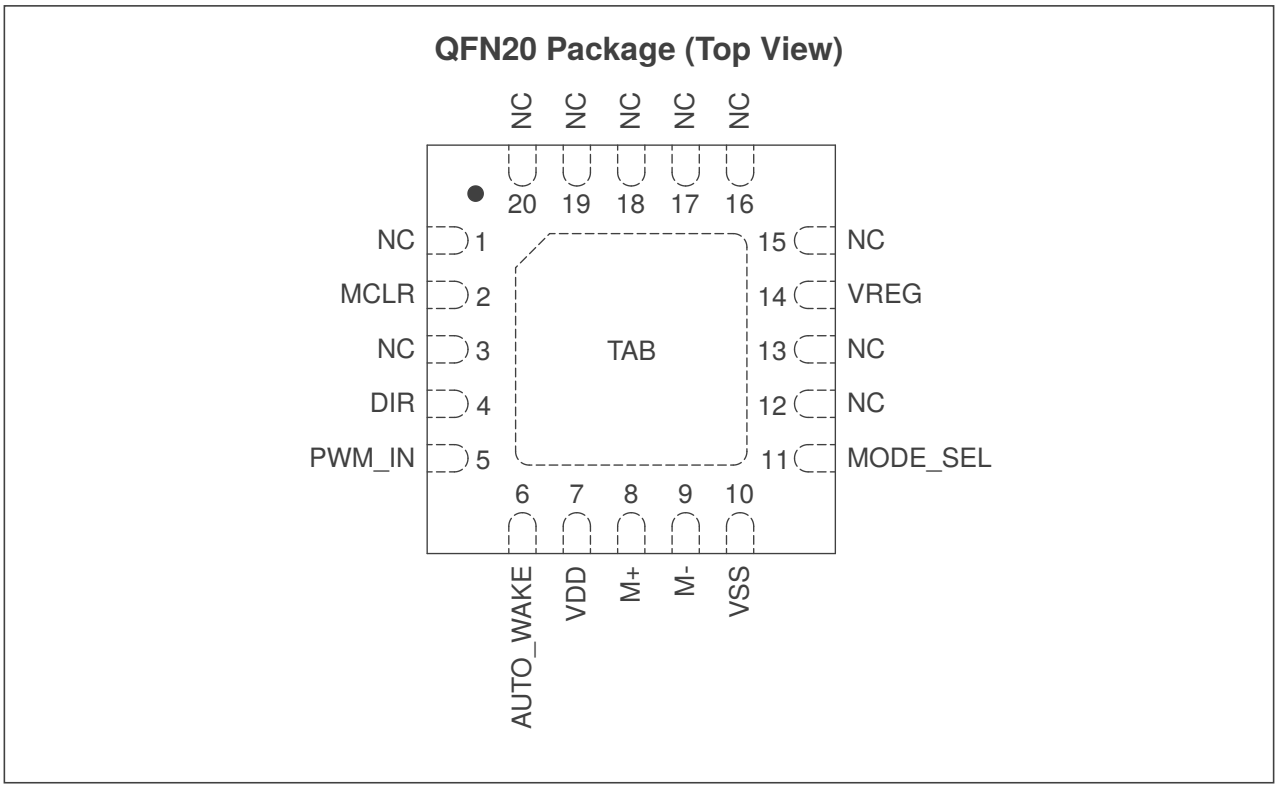


Figure 2.2: QFN20 Pinout for PWM mode

Table 2.2: QFN20 Pin Descriptions for PWM mode

Pin	Name	Type[i]	Function	Description
2	MCLR	I		Master Clear (Reset)
4	DIR	I	GPIO	Motor drive direction
5	PWM_IN	I	GPIO	PWM input
6	AUTO_WAKE	I	GPIO	Automatic wake-up from low power
7	VDD	P	Power	Power supply input voltage
8	M+	O	H-Bridge	
9	M-	O	H-Bridge	
10	VSS	P	Power	Analog/digital ground
11	MODE_SEL	I		Operating mode selection
14	VREG	P	Power	Internally-regulated supply voltage
*	NC	-	-	Not Connected

[i] Pin Types: I = Input, O = Output, I/O = Input or Output, P = Power

2.2 Reference Schematics

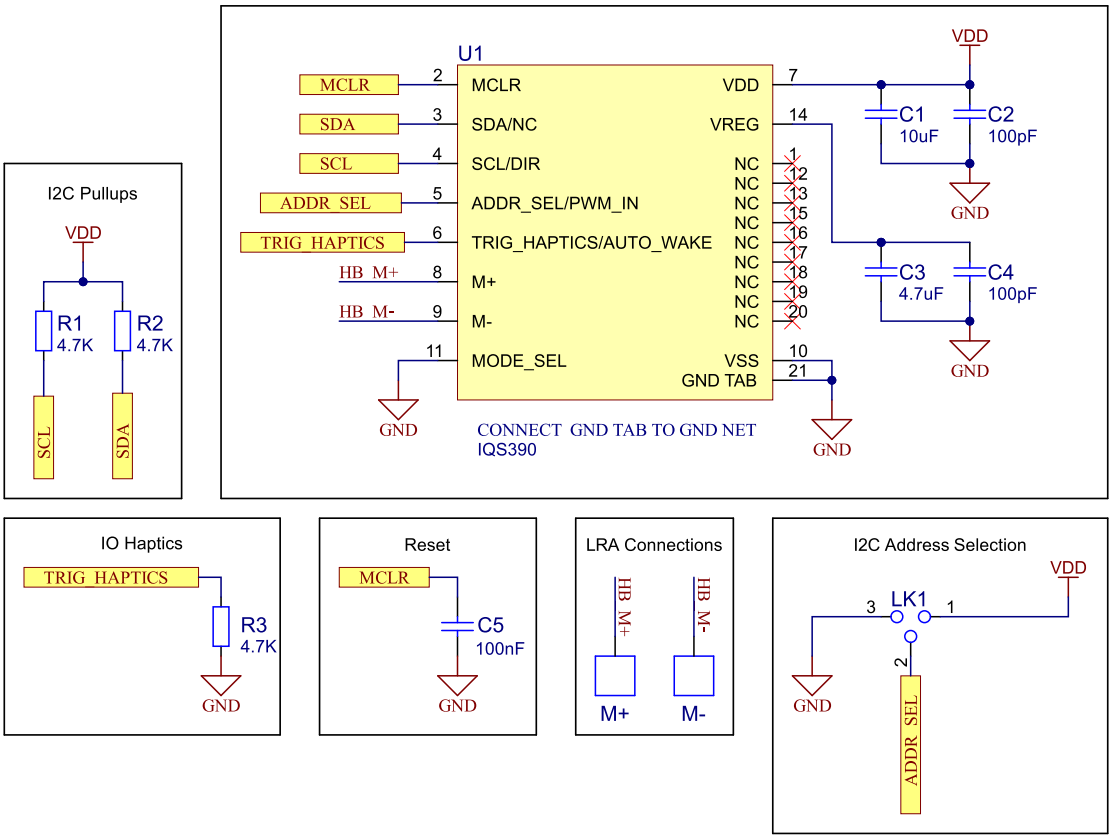


Figure 2.3: I²C Mode Reference Schematic

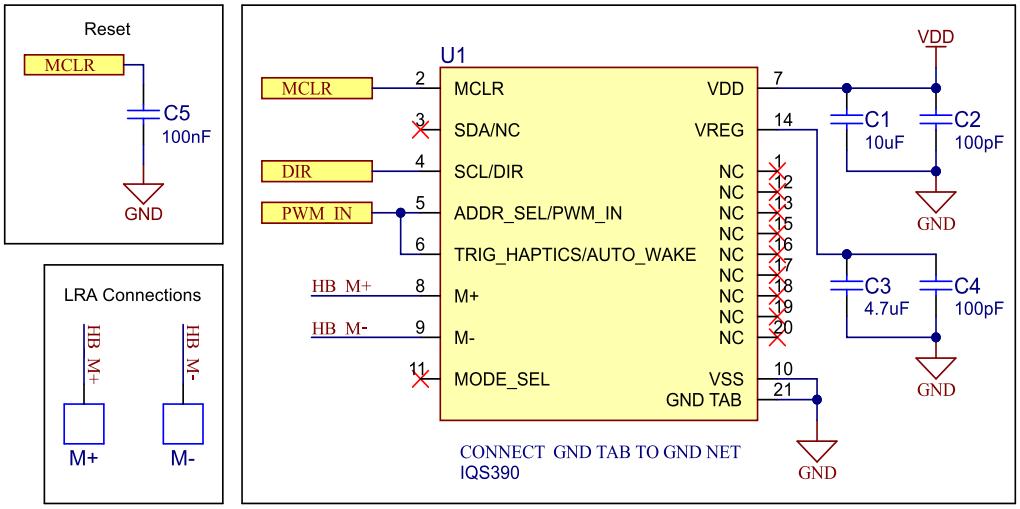


Figure 2.4: PWM Mode Reference Schematic

3 Electrical Specifications

3.1 Absolute Maximum Ratings

Table 3.1: Absolute Maximum Ratings

Symbol	Rating	Min	Max	Unit
V_{DD}	Voltage applied at VDD pin (referenced to VSS)	−0.3	3.6	V
V_{IN}	Voltage applied to any other pin (referenced to VSS)	−0.3	V_{DD} + 0.3 (3.6 V max)	V
T_{stg}	Storage temperature	−40	85	°C
T_j	Junction temperature		125	°C

3.2 General Operating Conditions

Table 3.2: General Operating Conditions

Symbol	Parameter	Typ	Unit
F_{CLK}	Master clock frequency	14	MHz
V_{REG}	Internally-regulated supply output	1.53	V

3.3 Recommended Operating Conditions

Table 3.3: Recommended Operating Conditions

Symbol	Parameter	Min	Recommended	Max	Unit
V_{DD}	Standard operating voltage, applied at VDD pin	1.71		3.6	V
T_A	Operating free-air temperature	−20		85	°C
C_{VDD}	Recommended capacitor at VDD	C_{VREG}	$2 \times C_{VREG}$		µF
C_{VREG}	Recommended external buffer capacitor at VREG (ESR $\leq$ 200 mΩ)	2.2	4.7	10	µF

3.4 H-Bridge Specifications

Table 3.4: H-Bridge Specifications

Symbol	Parameter	Min	Nominal	Max	Unit
R_L	Load resistance at V_{DD} = 3.3 V		18		Ω
I_L	Load current		150	200	mA
F_{LRA}	LRA drive frequency	100		300	Hz

3.5 ESD Rating

Table 3.5: ESD Rating

			Value	Unit
$V_{(ESD)}$	Electrostatic discharge voltage	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[i]	±2000	V

[i] JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.

3.6 Reset Levels

Table 3.6: Reset Levels

Parameter		Min	Max	Unit
V_{DD}	Power-up (Reset trigger) – slope > 100 V/s	1.65		V
	Power-down (Reset trigger) – slope < –100 V/s		0.9	

3.7 MCLR Pin Levels and Characteristics

Table 3.7: MCLR Pin Characteristics

Parameter		Min	Typ	Max	Unit
V_{IL}	MCLR input low level voltage	V_{SS} – 0.3		0.25 × V_{DD}	V
V_{IH}	MCLR input high level voltage	0.75 × V_{DD}		V_{DD} + 0.3	V
R_{PU}	MCLR pull-up equivalent resistor		210		kΩ
t_{Trig}	MCLR input pulse width – ensure trigger	250			ns

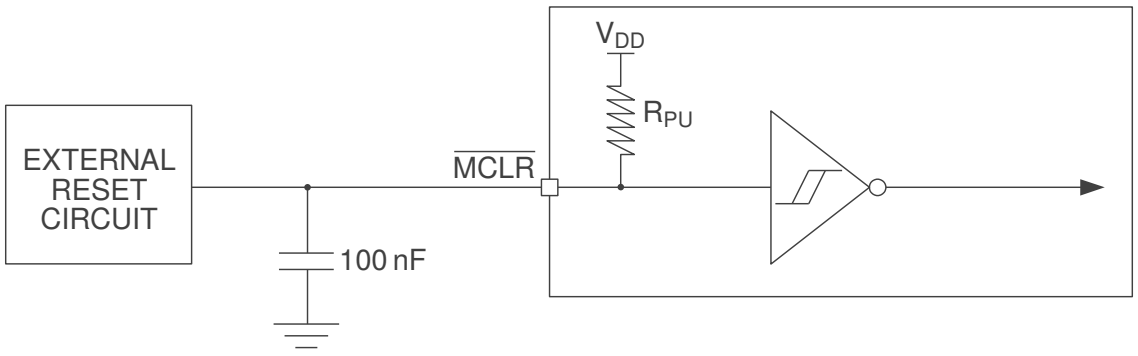


Figure 3.1: MCLR Pin Diagram

3.8 Digital I/O Characteristics

Table 3.8: Digital I/O Characteristics

Parameter		Test Conditions	Min	Max	Unit
V_{OL}	SDA & SCL output low voltage	I_{sink} = 20 mA		0.3	V
	GPIO output low voltage	I_{sink} = 10 mA		0.15	V
V_{OH}	Output high voltage	I_{source} = 20 mA	V_{DD} – 0.2		V
V_{IL}	Input low voltage		V_{SS} – 0.3	0.3 × V_{DD}	V
V_{IH}	Input high voltage		0.7 × V_{DD}	V_{DD} + 0.3	V
I_{GPIO}	Output current sunk by any GPIO pin			10	mA
	Output current sourced by any GPIO pin			20	
C_b	SDA & SCL bus capacitance			550	pF

3.9 I²C Characteristics

Table 3.9: I²C Characteristics

Parameter		Min	Max	Unit
f_{SCL}	SCL clock frequency		1000	kHz
$t_{HD,STA}$	Hold time (repeated) START condition	0.26		µs
t_{LOW}	LOW period of the SCL clock	0.5		µs
t_{HIGH}	HIGH period of the SCL clock	0.26		µs
$t_{SU,STA}$	Set-up time for a repeated START condition	0.26		µs
$t_{HD,DAT}$	Data hold time	0		ns
$t_{SU,DAT}$	Data set-up time	50		ns
$t_{SU,STO}$	Set-up time for STOP condition	0.26		µs
t_{BUF}	Bus free time between a STOP and START condition	0.5		µs
t_{SP}	Pulse duration of spikes suppressed by input filter	0	50	ns

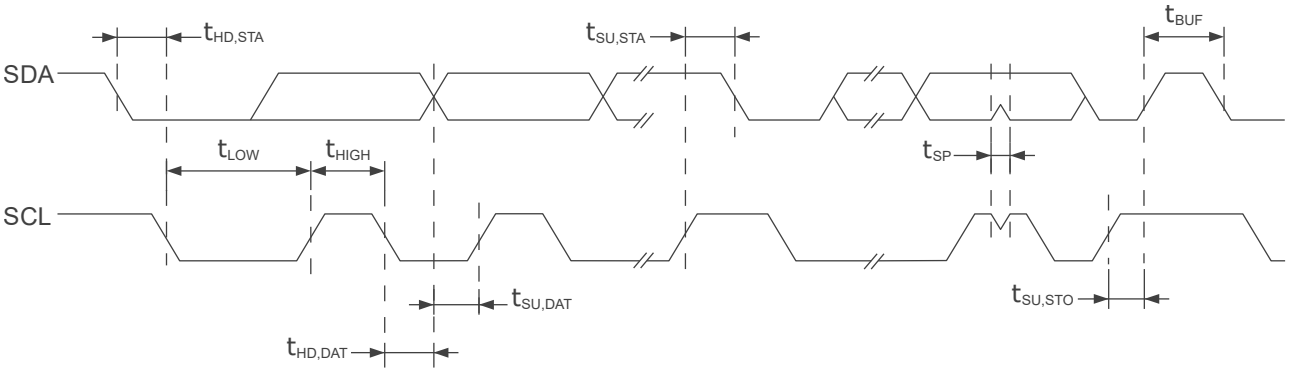


Figure 3.2: I²C Timing Diagram

3.10 Current Consumption

ULP current consumption applies to both PWM mode and I^2C mode. Fast haptics current consumption applies to only I^2C mode.

In both modes, the current consumption while haptics is active is dominated by the choice of motor.

Table 3.10: Typical Current Consumption

Power State	Current Consumption [µA]	
	Idle	Haptics Active
Fast Haptics	360	Motor Dependent
ULP	1.01	

4 LRA Drive Theory

A Linear Resonant Actuator (LRA) is a spring mass system. The mass is magnetic. A driving coil creates a magnetic field to exert force on the magnetic mass.

The coil must be driven with an Alternating Current (AC) voltage to create the magnetic field. When the frequency of this AC voltage matches the resonant frequency of the spring mass system, the maximum vibration force is exerted.

In the ideal case, the AC voltage is a pure sinusoid. The IQS390 approximates a pure sinusoid drive with a Pulse Width Modulated (PWM) drive signal. When the duty cycle of the PWM drive is varied sinusoidally, the average drive voltage follows a pure sinusoid.

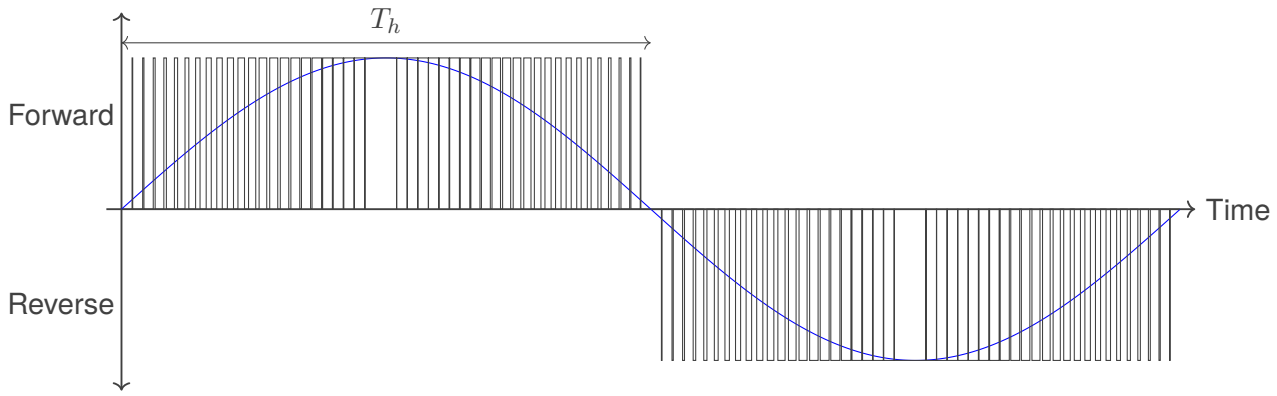


Figure 4.1: PWM Drive Approximation

Figure 4.1 shows the PWM output drive in relation to the ideal sinusoid drive. T_h is the width of a single half cycle. For a 200 Hz motor, this would be $\frac{1}{2\times200} = 2.5\,\mathrm{ms}$. The motor is driven in the forward direction for one half cycle and then in the reverse direction for one half cycle. This is repeated for the duration of the haptic pulse. The strength of vibration depends on the amplitude of the average sinusiodal drive. Since the amplitude of the average drive signal is directly related to the maximum duty cycle of the PWM drive, the vibration strength can be varied by changing the maximum duty cycle of the PWM drive signal.

It is difficult to vary the duty cycle of the PWM according to a pure sinusoid. For this reason, the IQS390 applies a further approximation to the PWM drive signal. Each half cycle of the sinusoidal modulation is approximated as three linearly interpolated segments. The first segment is linearly increasing, the second constant, and the third linearly decreasing. The IQS390 provides fine control over these segments. A detailed description of the configuration of these segments is given in Section 10.

5 Operational Modes

The IQS390 implements two distinct modes of operation. In I^2C mode, the IQS390 generates the LRA drive signal based on pre-configured settings. In PWM mode, the IQS390 accepts an external PWM signal and direction indication. These input signals are fed to the internal H-bridge, which drives the motor.

Both modes support LRA motors in the 100 – 300 Hz frequency range.

The mode is selected based on the state of the MODE_SEL pin directly after a cold boot or reset. When the MODE_SEL pin is grounded, the IQS390 will enter I^2C mode. When the MODE_SEL pin is floating, the IQS390 will enter PWM mode.

Unless explicitly otherwise stated, all remaining sections of this document describe I^2C mode only. The I^2C memory map applies to I^2C mode only. PWM mode is described in Section 13.

6 Power Management

The IQS390 distinguishes between *power mode* and *power state*. The current power state depends on the selected power mode. A trigger haptics command will wake the device from any of its sleep states. When the *Haptics Active* bit in the *System Status* register is set, the IQS390 performs no sleep function.

6.1 Power States

Two states are possible:

- Fast Haptics
- Ultra Low Power (ULP)

In the ULP state, the lowest current consumption is achieved. The digital core and non-vital peripherals are powered off. M+ and M- are tri-stated. The IQS390 takes 300 – 400 µs to wake from ULP. Thus, while in ULP, a haptic pulse will only start at least 300 – 400 µs after a trigger haptics command is given.

In the Fast Haptics state, the digital core remains powered on. After a trigger haptics command, the haptics pulse begins significantly sooner than when the IQS390 is in the ULP power state.

The current power state is indicated in the *System Status* register.

6.2 Power Mode

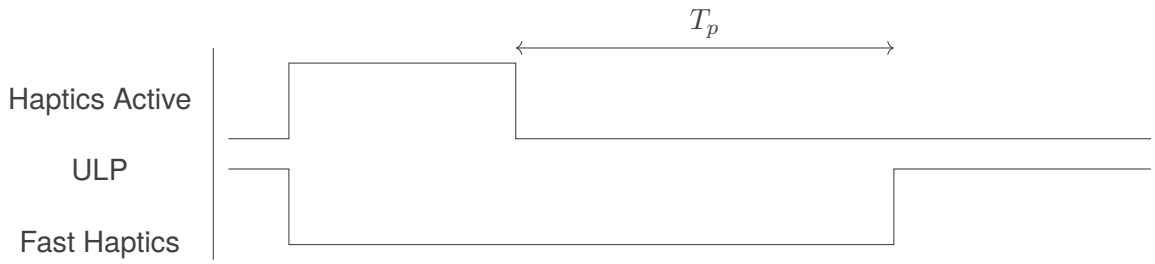
There are three possible power modes:

- Fast Haptics
- Ultra Low Power (ULP)
- Automatic

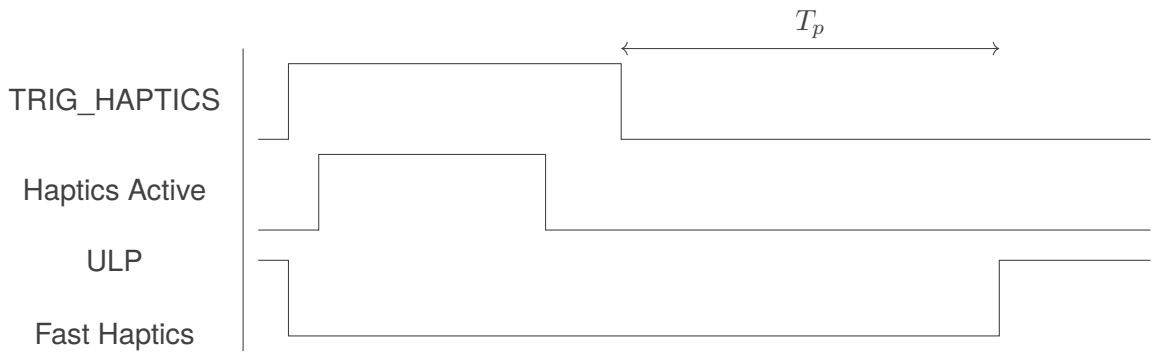
In Fast Haptics mode, the current power state is forced to ‘Fast Haptics’. In ULP mode, the current power state is forced to ‘ULP’.

In Automatic mode, the IQS390 manages the current power state automatically. If either a trigger haptics command is given or the IQS390 is addressed on the I^2C bus, the current power state will be set to ‘Fast Haptics’. The IQS390 returns the power state to ‘ULP’ when the time specified in steps of 512 ms by the *Power Mode Timeout* setting in the *System Settings* register has passed. For example, a register value of ‘2’ sets the timeout to 1024 ms. The power mode timeout is reset during haptics, when the IQS390 is addressed on the I^2C bus and when the TRIG_HAPTICS pin is high. In all power modes, the IQS390 will not enter the ULP state if the TRIG_HAPTICS pin is high. In effect, the power mode is set to ‘Fast Haptics’. These conditions are illustrated in Figure 6.1, where T_p shows the timeout.

The power mode and power mode timeout are set in the *System Settings* register.



(a) Power Mode Timeout from Haptics



(b) Power Mode Timeout from TRIG_HAPTICS Pin High

Figure 6.1: In Figure 6.1a, the haptics is active when the TRIG_HAPTICS pin is low. The timeout is effective from the end of the haptics. In Figure 6.1b, the TRIG_HAPTICS pin is high after the haptics is finished. The timeout is effective from when the TRIG_HAPTICS pin goes low.

7 System Management

System management is the process of configuring, monitoring, and controlling the device. It is advised to follow the procedures in Sections 7.4 and 7.5.

7.1 System Status

The *System Status* register shows the current state of the device. It is recommended to monitor the system status by continuously reading the *System Status* register. The *System Status* register is read only. Writing to the *System Status* register will have no effect.

7.2 Reset

The *Reset* bit in the *System Status* register will be set after a cold boot or if a device reset occurs. A device reset indicates either an error condition or that a deliberate power cycle has occurred. Under a reset condition, the master may still read and write to the device over I^2C. However, a trigger haptics command will have no effect.

If the device resets, the settings in the memory map will revert to their default values. These default values are listed in the 'Default' column of the memory map in Section 14.

Section 7.3 describes the process of acknowledging and clearing the reset condition. Section 7.4 describes the recommended procedure for configuring the device from a reset condition.

7.2.1 Hard

The IQS390 can be forced to reset at any time by pulling the MCLR pin low. Detailed specifications for this functionality are found in Section 3.7.

Please note the weak internal pullup resistor connected to the MCLR pin. There is no need for an external pullup.

7.2.2 Soft

When the *Haptics Active* bit in the *System Status* register is not set, the IQS390 can be forced to reset by asserting the *Soft Reset* bit in the *System Control* register.

7.3 ACK Reset

The *Reset* bit in the *System Status* register is cleared when the *ACK Reset* bit in the *System Control* register is set by the master. After *ACK Reset* is set, both the *ACK Reset* and *Reset* bits will be cleared by the IQS390.

If the *ACK Reset* bit is asserted when the *Reset* bit is not set, the *ACK Reset* bit will be immediately cleared and no other action will be taken.

7.4 Handling a Reset

After a reset, the master controller should first clear the *Reset* bit in the *System Status* register by following Section 7.3 and then rewrite the desired settings to the memory map over I^2C. Although it is possible to modify settings when the *Reset* bit is set, this is not a recommended order of control.

7.5 Typical Usage

Figure 7.1 shows a typical control sequence implementation. Note that the IQS390 has no events. The status of the device is obtained by polling it over I^2C.

It is not required to continuously check for a reset. It is sufficient to perform the check before sending a trigger haptics command. A reset condition is not expected to occur. Therefore, in time-sensitive applications, the check for a reset can be done less frequently.

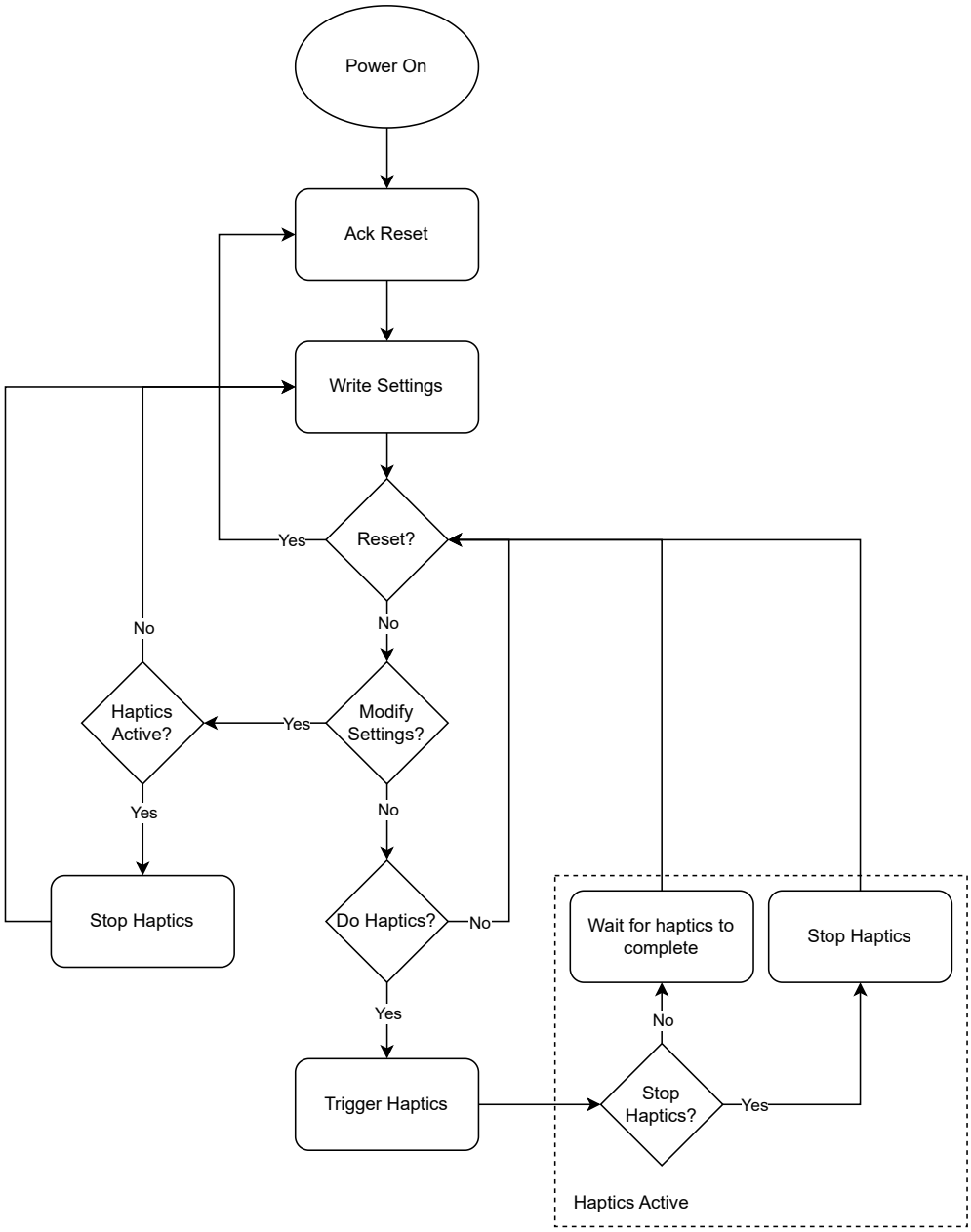


Figure 7.1: Typical Usage

8 H-Bridge

8.1 Settings

8.1.1 Slew Rate

The internal H-bridge has a slew rate-limiting function. This limits the slew rate of the PWM drive. Limiting the slew rate can help to reduce electromagnetic interference caused by the fast switching H-bridge drive signals.

The *Slew Rate Control* bit in the *H-Bridge Setup* register enables the slew rate function. When enabled, the *Slew Rate* setting selects the slew rate limit.

8.1.2 Drive Strength

The internal H-bridge is comprised of several drive stages. The *Drive Strength* setting in the *H-Bridge Setup* register controls which of these stages are active. The higher the *Drive Strength*, the more stages are active. The values in Table 3.4 are specified for a drive strength of '5'.

A drive strength of at least '1' is required for the H-bridge to function. Generally, the *Drive Strength* should be set to '5'.

Note: Overcurrent protection is disabled when the drive strength is set to '1' or '3'.

8.1.3 Ground Inactive

When the *Ground Inactive* bit in the *H-Bridge Setup* register is set, both M+ and M- will be pulled to ground when the motor is not being driven and the IQS390 is not in the ULP power state. In combination with inverted patterns, this can help to brake the motor and provide a crisper feel to the haptic pulse.

8.2 Protections

The internal H-bridge is equipped with several protection mechanisms. These are controlled by the H-bridge hardware. If enabled, they will automatically disable the H-bridge drive under the relevant error condition.

The H-bridge protections are closely related to Section 9.7.

8.2.1 Overcurrent Protection

Overcurrent protection is enabled by setting the *Overcurrent Protection* bit in the *H-Bridge Setup* register. Overcurrent protection activates when the current drawn by the load connected to M+ and M- exceeds approximately 200 mA.

Once tripped, the *Overcurrent* bit in the *System Status* register is set. The *Overcurrent* protection bit is cleared only when the *System Status* register is read over I^2C.

Note: The overcurrent protection can incorrectly trip when the pulse width of the PWM drive signal is small. This behaviour is dependent on the motor being driven. For this reason, overcurrent protection is disabled by default. The reliability of the overcurrent protection functionality should be assessed at design time.

8.2.2 Over Temperature Protection

Over temperature protection is enabled by setting the *Over Temperature Protection* bit in the *H-Bridge Setup* register. Over temperature protection activates when the temperature of the device exceeds the temperature specified by the *Over Temperature Threshold* in the *Over Temperature Settings* register.

The *Hysteresis* bit enables one-way hysteresis for over temperature detection. This ensures that the over temperature protection activates cleanly when an over temperature condition occurs. It is recommended to always have hysteresis enabled when using the over temperature protection functionality.

Once tripped, the *Over Temperature* bit in the *System Status* register is set. The *Over Temperature* protection bit is cleared only when the *System Status* register is read over I^2C.

8.2.3 Shoot-Through Protection

Shoot-through protection is enabled by setting the *Shoot-through Protection* bit in the *H-Bridge Setup* register. Shoot-through protection prevents direct shorting of VDD to GND when the H-bridge transistors are switching. It is recommended to always have shoot-through protection enabled.

8.3 External H-Bridge Support

When the *External* bit in the *H-Bridge Setup* register is set, the IQS390 will output the drive signals for one half of an external H-bridge on the M+ and M- pins. The external H-bridge circuit must invert these signals to drive the opposite side of the H-bridge.

The reference circuit for the external H-bridge is shown in Figure 8.1. M+ and M- must be connected to the PWM1 and PWM2 nets. Note that the pulldown resistors are required to prevent shorting VMOT to GND during power on and when the IQS390 is in the ULP power state.

Autoresonance cannot be used when using an external H-bridge, as there is no way to measure the back-EMF of the motor. It is the responsibility of the master to ensure autoresonance is disabled when using an external H-bridge. There are no restrictions on any other waveform configuration settings.

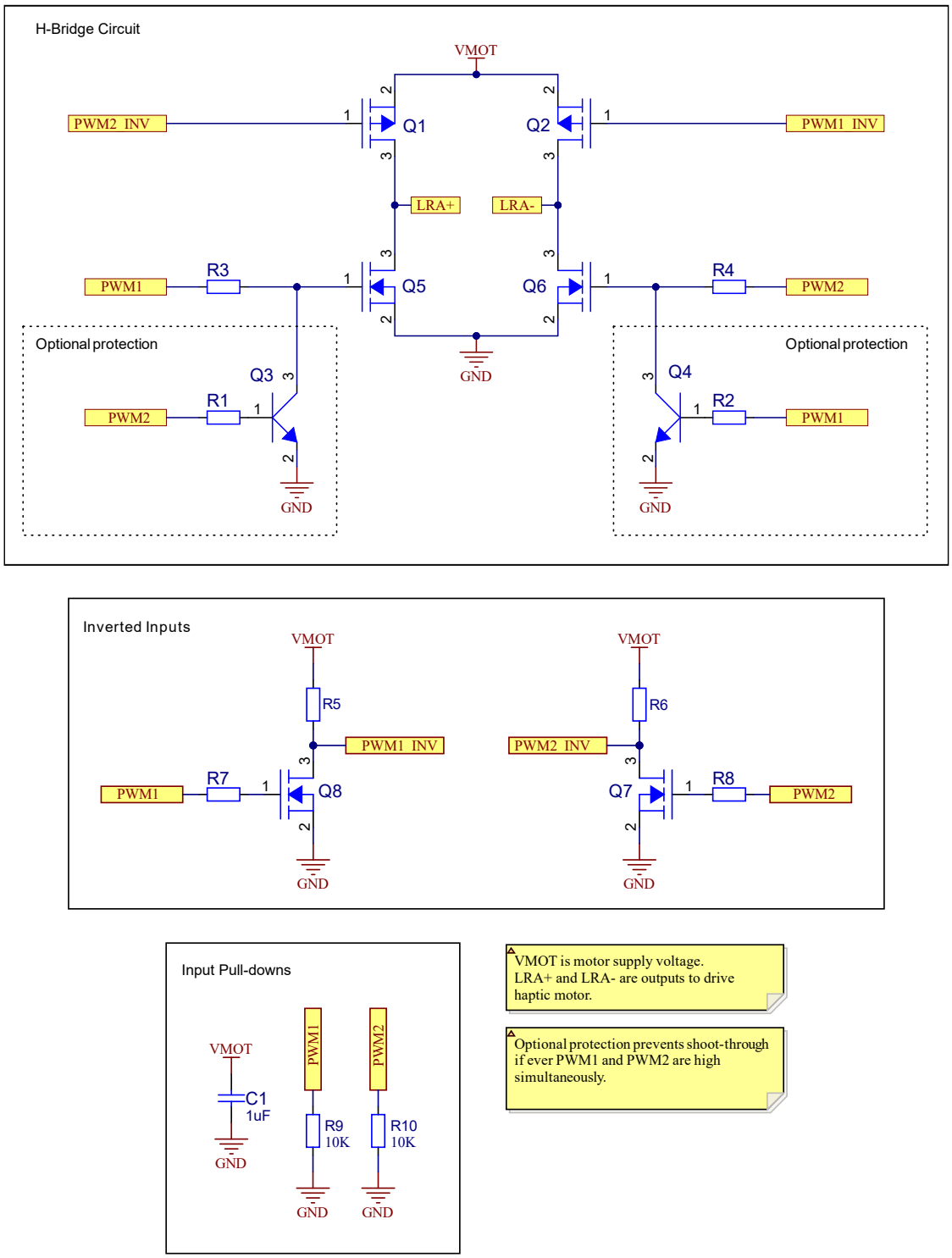


Figure 8.1: External H-Bridge Circuit

9 Haptic Control and Monitoring

The IQS390 allows up to eight unique waveforms to be stored in memory. The active waveform is chosen using the *Waveform Selection* field in the *Haptic Control* register.

While a waveform is executing, the *Haptics Active* bit in the *System Status* register will be set. Waveform settings must only be modified when the *Haptics Active* bit is clear. Modifying waveform settings while a waveform is running may result in undefined behaviour.

9.1 Trigger Haptics Command

The currently active waveform is played when a trigger haptics command is given. A trigger haptics command can be given through I^2C or by using input pin control.

A trigger haptics command issued while the *Haptics Active* bit is set will be ignored.

9.2 I^2C Control

In I^2C mode, a trigger haptics command is given by setting the *Trigger Haptics* bit in the *Haptic Control* register. The *Trigger Haptics* bit is cleared at the start of every waveform, regardless of how the waveform was triggered.

Since the *Waveform Selection* field and the *Trigger Haptics* bit are in the same register, only the address bytes plus a single data byte need to be written to both play and select a waveform.

The waveform can be stopped at any time by asserting the *Stop Haptics* bit in the *Haptic Control* register. The waveform will be halted immediately, and the *Stop Haptics* bit will be cleared. If the *Stop Haptics* bit is set when the haptics is not running, it will have no effect and will immediately be cleared.

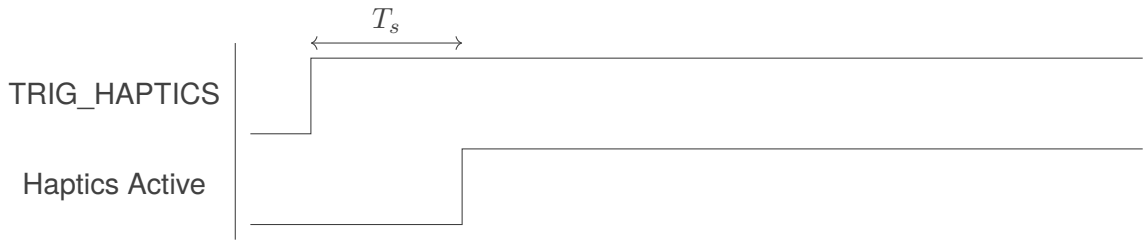
9.3 Input Pin Control

The TRIG_HAPTICS pin can be used to start and stop haptic pulses. When not controlling haptics, the pin must be pulled to ground. It is always required to hold the TRIG_HAPTICS pin high for at least 100 µs when using input pin control to start a haptic pulse.

The control type is chosen by selecting either ‘Edge Trigger’ or ‘Level Trigger’ in the *System Settings* register. In both cases, the TRIG_HAPTICS pin can be used at any time to control the haptics.

Some time is required for the IQS390 to initialise and begin a haptic pulse. This startup delay is shown in Figure 9.1. When the IQS390 is in the ULP power state, the maximum value of T_s is 400 µs. In the fast haptics power state, the maximum value of T_s is 100 µs.

(a) Start Delay in Edge Trigger Mode.



(b) Start Delay in Level Trigger Mode

Figure 9.1: Start delay for haptics when using input pin control. The maximum T_s depends on the current power state on the rising edge of the TRIG_HAPTICS signal.

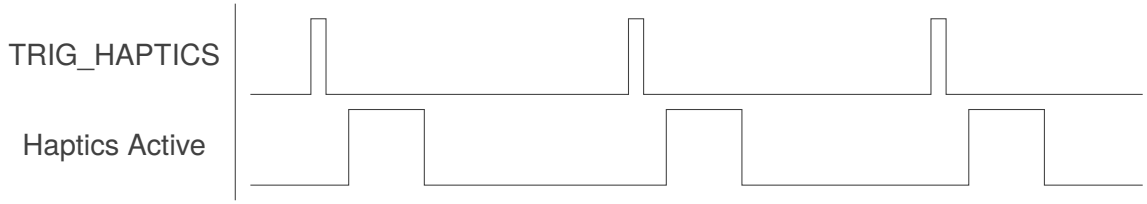
9.3.1 Edge Trigger Mode

Edge trigger mode is selected by clearing the *Trigger Mode* bit in the *System Settings* register. Edge trigger mode only affects the control of haptics with the TRIG_HAPTICS pin.

In edge trigger mode, holding the TRIG_HAPTICS pin high for 100 µs when the haptics is not running will issue a trigger haptics command. A rising edge on the TRIG_HAPTICS pin while the haptics is running will immediately stop the haptics. There are no time conditions on the stop haptics rising edge, regardless of the power mode.

Figure 9.2 demonstrates the use of the TRIG_HAPTICS pin in edge trigger mode.

(a) Starting and Stopping the Haptics



(b) Repeated Waveform

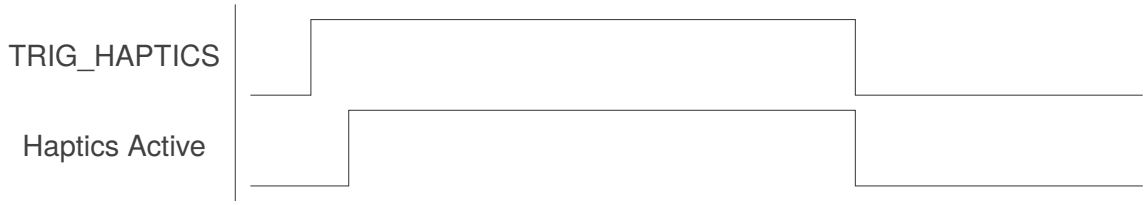
Figure 9.2: Using the TRIG_HAPTICS pin in edge trigger mode. In Figure 9.2a, the second rising edge comes when the haptics is still running. The haptics is stopped. In Figure 9.2b, the waveform finishes before each new rising edge. The rising edges trigger a new waveform.

9.3.2 Level Trigger Mode

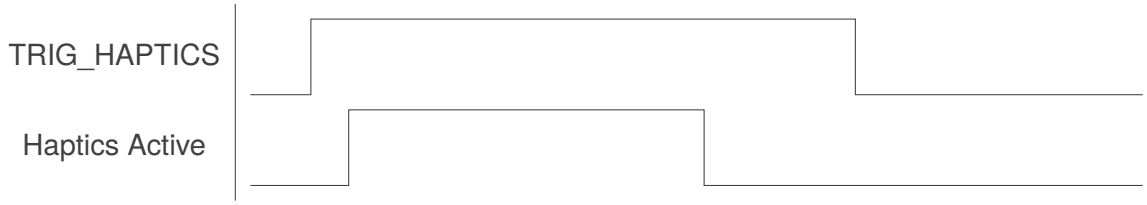
Level trigger mode is selected by setting the *Trigger Mode* bit in the *System Settings* register. Level trigger mode only affects the control of haptics with the TRIG_HAPTICS pin.

In level trigger mode, holding the TRIG_HAPTICS pin high for at least 100 µs when the haptics is not running will issue a trigger haptics command. The haptics is stopped on the next falling edge of the TRIG_HAPTICS pin. A waveform can run to completion before the falling edge. If this occurs, the falling edge will have no effect.

Figure 9.3 demonstrates the use of the TRIG_HAPTICS pin in level trigger mode.



(a) Starting and Stopping the Haptics



(b) Haptic Pulse Ends Before the Falling Edge

Figure 9.3: Using the TRIG_HAPTICS pin in level trigger mode. In Figure 9.3a, the falling edge comes when the haptics is running. The haptics is stopped. In Figure 9.3b, the waveform finishes before the falling edge. The falling edge has no effect.

9.4 Continuous Mode

If the *Continuous Mode* bit in the *System Settings* register is not set, a trigger haptics command will play the selected waveform once. When the *Continuous Mode* bit is set, a trigger haptics command will start the haptics. The active waveform will be repeated at intervals specified in milliseconds by the value in the *Continuous Mode Repeat Time* register. To run the haptics continuously with no breaks, set the *Continuous Mode Repeat Time* to '0'.

The haptics will stop when a stop haptics command is given either through I^2C or with the TRIG_HAPTICS pin. Note that a stop haptics command using the TRIG_HAPTICS pin is different for the edge and level trigger modes.

In continuous mode, the entire waveform is repeated. This includes a waveform's repeat time and repeat count.

Figure 9.4 demonstrates the use of continuous mode when using the TRIG_HAPTICS pin in edge trigger mode. T_r is the *Continuous Mode Repeat Time*. Note how the *Haptics Active* bit in the *System Status* register remains set until a stop haptics command is given. Continuous mode is also compatible with I^2C control and level trigger mode.

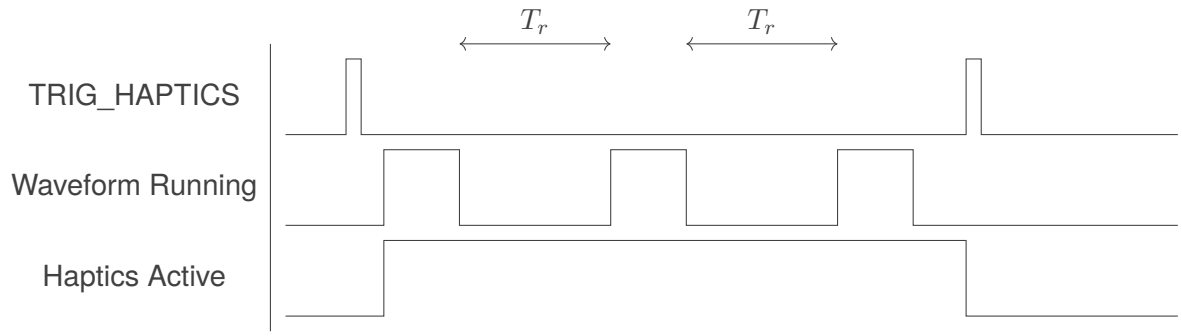


Figure 9.4: Continuous Mode Control

9.5 LRA Drive Frequency

The *LRA Frequency* register is used to set the frequency in Hertz (Hz) at which the duty cycle of the PWM output drive changes. It is also used to report the frequency measured by the autoresonance algorithm.

The *LRA Frequency* register should not be modified by the master while the *Haptics Active* bit in the *System Status* register is set. It can be read at any time.

9.6 PWM Frequency

The *PWM Frequency* register sets the frequency in Hertz (Hz) of the output PWM drive. Internally, this has an effect on the time domain resolution with which the duty cycle of the drive updates.

It is recommended to always set the *PWM Frequency* register to '20000'.

9.7 Strict Failure

In strict failure mode, the *Overcurrent* and *Over Temperature* bits in the *System Status* register must be clear for a waveform to run. More details regarding the H-bridge protections are given in Section 8.2.

If strict failure mode is disabled, the IQS390 will attempt to play a waveform regardless of the state of the *Overcurrent* and *Over Temperature* bits. If either bit is set, but the error condition is no longer present, the waveform will play as normal. If the error condition is still present, the waveform will be stopped immediately.

Strict failure mode is enabled by setting the *Strict Failure* bit in the *H-Bridge Setup* register.

10 Haptic Effect Configuration

The IQS390 defines the following concepts:

Segment	A PWM pulse with a duty cycle that is either increasing, decreasing or constant.
Pattern	A series of up to three consecutive segments.
LRA Drive Period	The time it takes for one full LRA drive cycle.
Half Cycle	A pattern lasting one half of an LRA drive period.
Stage	A pattern played for a number of half cycles, where the drive direction alternates every half cycle.
Haptic Pulse	Up to five stages, played sequentially.
Waveform	Any number of haptic pulses.
Repeat Count	The number of haptic pulses per waveform.
Repeat Time	The time between haptic pulses.

Figure 10.1 shows the basic components of a single drive cycle. The segments are denoted S_0, S_1, and S_2 and make up an approximately sinusoidal pattern. Each half cycle, denoted H_0 and H_1, consists of a single pattern. Every two-half cycles makes one LRA drive period. Every alternate half cycle is driven in the opposite direction to its predecessor.

Different haptic effects can be composed by creating combinations of these settings. For example, Figure 10.2 shows a two-stage waveform. The first stage consists of an approximately sinusoidal pattern lasting two half cycles. The second is a single half cycle driving a triangular pattern.

10.1 Pattern Definition

Each pattern can have up to three segments. A pattern is fully defined if the first N segments have valid settings when the *Segments* setting in a pattern's configuration registers is set to 'N'. Only the first N segments form part of the pattern. All other segments are ignored.

Each segment has a *Start Duty Cycle* and an *End Duty Cycle*. For every segment, the IQS390 will linearly interpolate the drive duty cycle from the *Start Duty Cycle* to the *End Duty Cycle*, and then progress to the next segment or half cycle.

The segment *Duration* parameter defines how long it will take to perform the interpolation. The *Duration* is specified as a percentage of the half cycle width, where 255 is 99%. For example, a register value of '85' will result in the segment lasting one third of every half cycle. For any given pattern, the values of all enabled segment *Duration* registers must sum to 255. For example, if two segments are used and the first segment's *Duration* register is '100', the second segment's *Duration* register must be set to '155'.

The *Invert* bit in a pattern's *Pattern Setup* register selects the drive direction for each half cycle. When the *Invert* bit is clear, even half cycles are driven in the forward direction and odd half cycles are driven in the reverse direction. Setting the *Invert* bit flips this behaviour. This allows braking patterns to be defined. The indexing begins at the start of the stages. In other words, the first half cycle of a stage is always considered even.

The *Autoresonance* bit in a pattern's *Pattern Setup* register enables autoresonance for the pattern. Any stage executing a pattern whose *Autoresonance* bit is set will perform autoresonance only for the

duration of that stage. Pattern-specific autoresonance allows for easy configuration of braking and pseudo overdrive patterns. A full description of autoresonance is in Section 11.

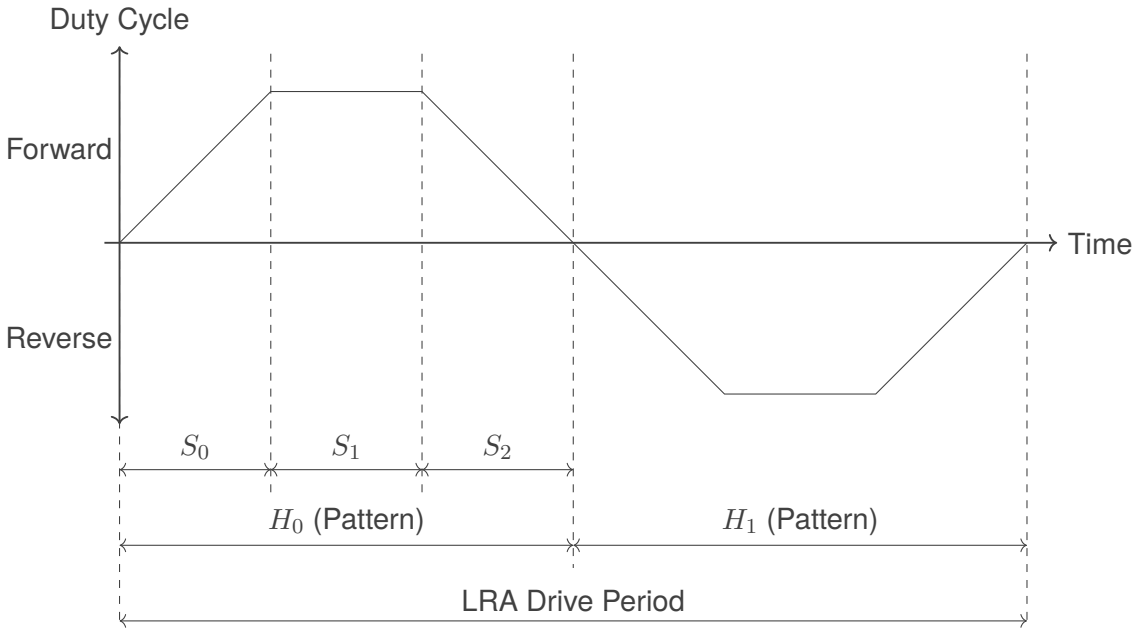


Figure 10.1: Anatomy of One Full Drive Cycle

10.2 Stages

Every waveform pulse consists of up to five stages. Patterns are packed into stages in a waveform's *Pattern Selection* register.

The 16-bit pattern select setting is laid out in groups of three-bit wide bitfields. Each bitfield corresponds to a stage. Since there are five stages, the most significant bit is ignored. If a pattern select bitfield is set to '0b000', no pattern is selected and the stage is disabled. Otherwise, it selects one of the seven definable patterns.

Every waveform has a block of five 8-bit wide half-cycle count settings. This array sets the number of half cycles to execute in each stage. Each half-cycle count corresponds to a stage. For example, the half cycle counts for waveform zero begin at memory map address 0x2052. The value loaded at address 0x2052 sets the number of half cycles for the first stage. The value loaded at address 0x2053 sets the number of half cycles for the second stage and so on.

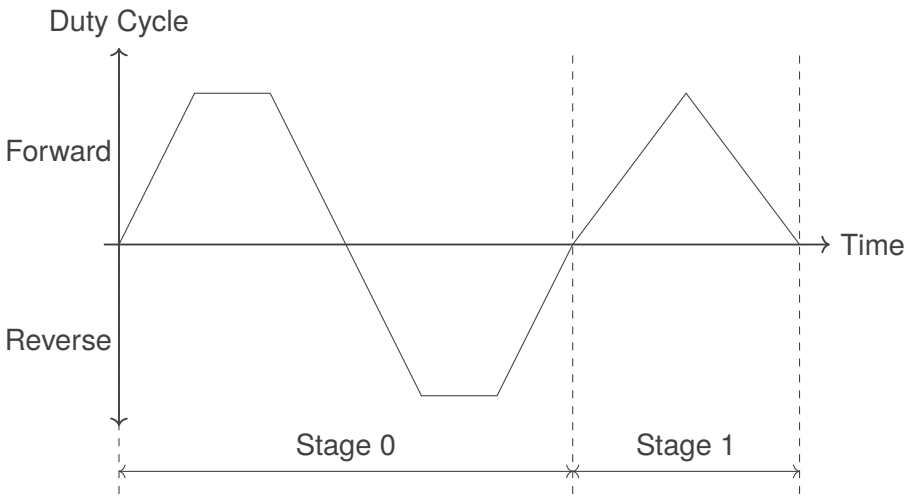


Figure 10.2: A Two Stage Waveform

10.3 Repeating Waveform Pulses

Waveform pulses are repeated as many times as specified by a waveform's *Repeat Count* register. A waveform's *Repeat Count* register must be greater than or equal to '1'. A waveform's *Repeat Time* register specifies the time in milliseconds between waveform pulses.

These settings can be used to create highly configurable effects. For example, a double click effect can be created by setting the *Repeat Count* to '2' and the *Repeat Time* to '100'.

Figure 10.3 shows a repeating haptic pulse. The *Repeat Count* is '3' and the *Repeat Time* is denoted by T_r. Note that all three of these pulses belong to the same waveform. The *Haptics Active* bit in the *r*egister will remain set during T_r.

Different register value effects can be created by combining these settings with Continuous Mode. Continuous Mode is described in Section 9.4.

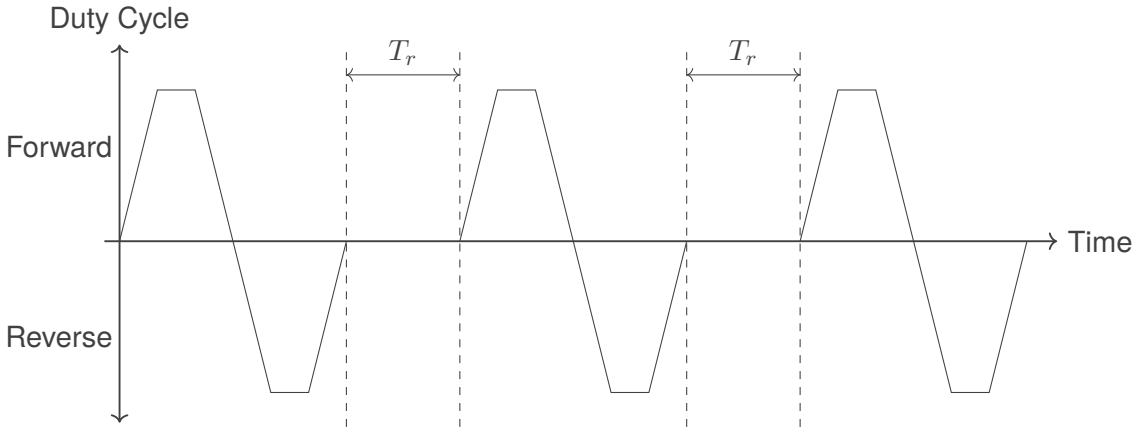


Figure 10.3: A Repeating Haptic Pulse

11 Autoresonance

11.1 Operation

The autoresonance algorithm matches the drive frequency to the resonant frequency of the driven LRA. The driver operates by monitoring the back-EMF of the motor at the end of every half cycle. By detecting the zero-cross of the back-EMF, the driver is able to track changes in the resonant frequency of the LRA. This provides consistent vibration strength in changing conditions and across production variations. It is recommended to set the initial frequency slightly higher than the expected resonant frequency.

Autoresonance is enabled per pattern. For a complete understanding of how to enable it, see Section 10.1.

11.2 Backoff

Once a frequency lock has been achieved, it is crucial that the zero-cross occurs. If the zero-cross does not occur, the driver has no information about the back-EMF and cannot make an intelligent decision about the next half cycle's drive frequency. A zero-cross may not occur when the drive frequency is far from the resonant frequency of the motor. If the drive frequency is much lower than the resonant frequency, it can take many cycles to acquire a lock. If the drive frequency is much higher than the resonant frequency, an accurate lock may never be achieved.

When a zero-cross does not occur, the driver assumes that the drive frequency is too low. The driver increases the drive frequency by a fixed percentage. This is an attempt to re-establish a frequency lock. In most cases, a zero-cross will be seen within the next few half cycles, and the frequency lock will be restored.

This effect can be mitigated by slightly increasing the drive frequency such that it is more than the exact resonant frequency as measured by the zero cross. Unless conditions change significantly, this guarantees that a zero-cross will occur on the next half cycle.

The drive frequency should be increased by as little as possible to ensure it matches the resonant frequency. The exact amount depends on the motor being driven. To this end, the *Autoresonance Backoff* setting is included in the memory map.

When a zero-cross is detected, the drive frequency will be set to the resonant frequency of the motor and then increased by a percentage equal to one hundred divided by the value in the *Autoresonance Backoff* register.

$$\text{Percentage increase} = \frac{100}{\text{Autoresonance Backoff}}$$

Setting *Autoresonance Backoff* to '0' will match the zero-cross frequency exactly.

In Figure 11.1, the current half-cycle drive is shown in red. Provided $T_{h(n)}$ is close to but less than the resonant half-cycle period, the back-EMF of the motor will lag the drive voltage. The driver detects the zero cross of the back-EMF and uses this to determine T_z. The frequency of the next half cycle is then increased from T_z in accordance with the *Autoresonance Backoff* setting to determine $T_{h(n+1)}$. This is the period of the next half cycle. Note that Figure 11.1 shows the average voltage for the driven half cycles and the instantaneous voltage for the back-EMF.

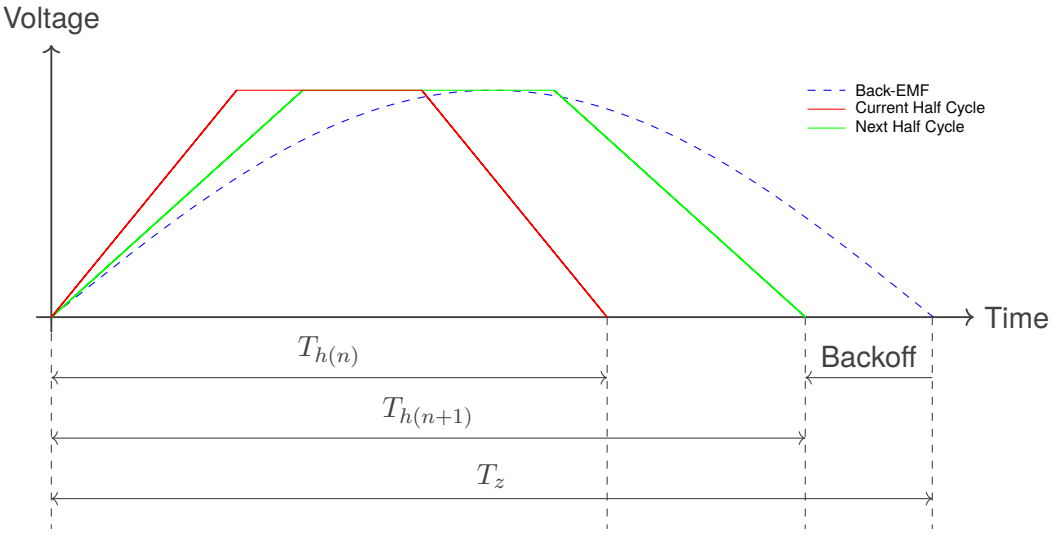


Figure 11.1: Autoresonance Backoff

11.3 Recommend Recalibrate

If the frequency at the start of a waveform differs by more than 25% from the frequency at the end of the waveform, the *Recommend Recalibrate* bit in the *System Status* register will be set. Typically, this will occur for one of three situations:

1. This is the first haptic pulse, and the starting frequency was far from the resonant frequency.
2. External conditions have changed significantly.
3. An error has occurred with the autoresonance algorithm.

The *Recommend Recalibrate* bit is cleared when the master writes to the *LRA Frequency* register over I^2C.

For item 1, the master can simply read the *LRA Frequency* register and write the same value back. This is most likely to occur during a calibration sequence, where the master initiates several autoresonance-enabled waveforms to find the motor frequency. The calibration sequence is successful when the *Recommend Recalibrate* bit is not set for several consecutive trigger haptic commands.

Items 2 and 3 are error conditions. If the *Recommend Recalibrate* bit is set outside of a calibration sequence, it indicates that either item 1 or item 2 has occurred. The calibration sequence should be done again.

12 I²C Interface

The IQS390 features a standard two-wire I²C interface supporting a maximum bit rate of 1 Mbit/s. The memory structures accessible over the I²C interface are byte-addressable with 16-bit addresses. Values wider than one byte are packed with little-endian byte order and are stored in word-aligned addresses. The IQS390 can be addressed at any time.

- Standard two-wire interface
- *Fast-Mode Plus* I²C with up to 1 Mbit/s bit rate
- Selectable 7-bit device address
- 16-bit little-endian register addressing
- One data byte stored per register address

12.1 Address Selection

Each order code allows for selection between two different I²C addresses. The available addresses are listed in Section 15.1.

The ADDR_SEL pin is used to select the address. Address 1 is selected when ADDR_SEL is pulled to ground. Address 2 is selected when ADDR_SEL is pulled to VDD.

An external pullup or pulldown resistor is not required on the ADDR_SEL pin.

12.2 Reserved Address

The IQS390 will acknowledge an additional address derived from its selected slave address. This derived address is obtained by flipping the least significant bit of the slave address.

For every order code, the IQS390 will also acknowledge an additional debug I²C address. The debug address is for debugging purposes only and should not be used during normal operation. The debug address is the primary address with the least significant bit inverted. For example, the primary address for IQS390-001 is 0x54 and its debug address is 0x55.

12.3 Read

A typical read operation is shown in Figure 12.1.

The master initiates communication by sending a start condition followed by the device address with the read-not-write bit low. The IQS390 responds with an acknowledgement, after which the master must transmit two bytes defining the starting register address to read from.

The master then sends a repeated start condition, followed by the device address with the read-not-write bit high. The IQS390 transmits data from the requested address as long as the master continues to acknowledge each byte.

The read operation is ended when the master does not acknowledge a transmitted byte. The transaction is complete when the master produces a stop condition.

If the master attempts to read from an address that is outside of the IQS390's memory map, the IQS390 will return 0xEE.

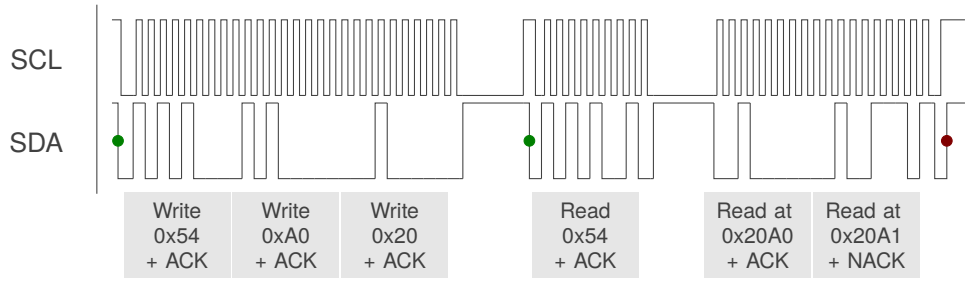


Figure 12.1: I²C Read Example

12.4 Write

A typical write operation is shown in Figure 12.2.

The master initiates communication by sending a start condition followed by the device address with the read-not-write bit low. The IQS390 responds with an acknowledgement, after which the master must transmit two bytes defining the starting register address to write to.

The master then transmits a series of bytes that are written to the IQS390. The IQS390 will acknowledge each byte. The write operation is ended when the master produces a stop condition.

Any data written to an address that is not in the IQS390's memory map will be discarded.

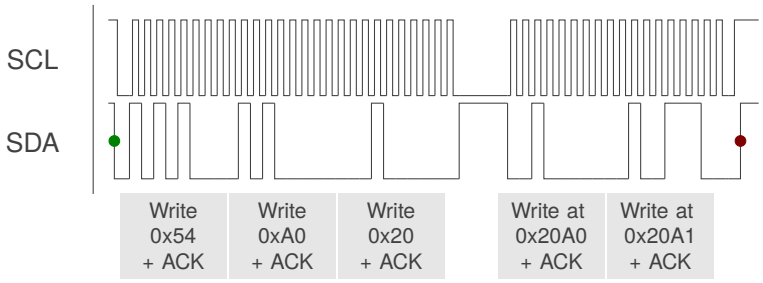


Figure 12.2: I²C Write Example

12.5 Clock Stretching

The IQS390 is not compatible with an I³C bus due to clock stretching. As per the *Fast Mode Plus* I²C specification, the IQS390 implements byte-level clock stretching on the I²C bus.

The maximum clock stretching will occur when addressing the IQS390 while it is in the ULP power state. The IQS390 will clock stretch for up to 450 µs when the master outputs the slave address on the bus.

When the device is not in the ULP power state, clock stretching is expected to last for 20 – 80 µs. Clock stretching can occur on any byte.

13 PWM Mode

The information in this section applies to PWM mode only.

In PWM mode, an external source must provide the LRA drive signals to the IQS390. The external source is responsible for modulating the duty cycle of the drive signal to match the resonant frequency of the driven motor. Autoresonance is not supported in PWM mode.

See Section 5 for information on how to select PWM mode.

13.1 Input Signals

The signal applied to the PWM_IN pin is passed directly to the internal PWM drive engine. The H-bridge is driven by the outputs of the PWM drive engine. The duty cycle mapping is one-to-one. For example, a 100% duty cycle on the input side will result in a 100% duty cycle on the motor drive pins.

The motor drive direction is chosen by pulling the DIR pin high or low. A low signal drives the motor in the forward direction, and a high signal drives the motor in the reverse direction.

Figure 13.1 illustrates a typical set of drive signals. T_h shows the width of a single half cycle. For a 200 Hz motor, $T_h = \frac{1}{2\times200} = 2.5\,\text{ms}$. Various effects can be created by modulating the duty cycle of the PWM input signal in different ways. The strength of vibration depends on the maximum duty cycle of the PWM input.

The IQS390 expects the frequency of the input PWM signal to be 20 kHz.

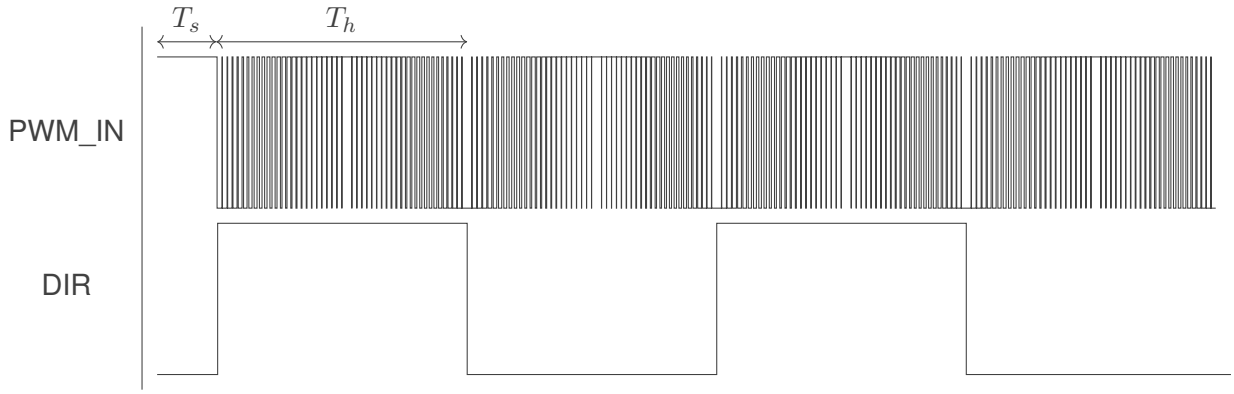


Figure 13.1: Input Signals for PWM Mode

13.2 Ultra Low Power

The IQS390 enters an ultra-low power sleep state when it detects that the signal applied to the PWM_IN pin has been low for longer than one 20 kHz PWM period.

The AUTO_WAKE pin implements automatic wake-up from the ultra-low power state. It must be directly connected to the PWM_IN pin with an external connection.

The automatic wake-up requires that the AUTO_WAKE pin is held high for at least 100 µs. Therefore, the external PWM input signal must begin by holding the AUTO_WAKE pin high before modulating the duty cycle. This is marked on Figure 13.1 by T_s.

13.3 Over Temperature Protection

PWM mode features always-on over temperature protection. If the temperature of the device exceeds 81 °C, the internal H-bridge will be automatically disabled. Once the temperature is below 81 °C, the H-bridge will be automatically enabled again.

Over temperature protection ensures the IQS390 will not be permanently damaged under short-circuit conditions.

14 I²C Memory Map

Address	Length	Description	Default	Notes
Read Only		**Version Information**		
0x0000	2	Product Number	2489	
0x0001				
0x0002	2	Major Version	1	
0x0003				
0x0004	2	Minor Version	0	
0x0005				
Read Write		**Status and Control**		
0x1000	1	System Status		Read Only Appendix A.1
0x1001	1	Do Not Care		
0x1002	1	System Settings	0x22	Appendix A.2
0x1003	1	Over Temperature Settings	0x1A	Appendix A.3
0x1004	2	Continuous Mode Repeat Time	0x0000	
0x1005				
0x1006	1	System Control		Appendix A.4
0x1007	1	Haptic Control		Appendix A.5
Read Write		**Haptic Configuration**		
0x2000	2	H-Bridge Setup	0x353E	Appendix A.6
0x2001				
0x2002	1	Pattern 1 Segments	3	Range 0-3
0x2003	1	Pattern 1 Segment 0 Start Duty Cycle	0	Range 0-99
0x2004	1	Pattern 1 Segment 0 End Duty Cycle	99	Range 0-99
0x2005	1	Pattern 1 Segment 0 Duration	85	
0x2006	1	Pattern 1 Segment 1 Start Duty Cycle	99	Range 0-99
0x2007	1	Pattern 1 Segment 1 End Duty Cycle	99	Range 0-99
0x2008	1	Pattern 1 Segment 1 Duration	85	
0x2009	1	Pattern 1 Segment 2 Start Duty Cycle	99	Range 0-99
0x200A	1	Pattern 1 Segment 2 End Duty Cycle	0	Range 0-99
0x200B	1	Pattern 1 Segment 2 Duration	85	
0x200C	1	Pattern 1 Setup	0x00	Appendix A.7
0x200D	1	Pattern 2 Segments	0x00	Range 0-3
0x200E	1	Pattern 2 Segment 0 Start Duty Cycle	0x00	Range 0-99
0x200F	1	Pattern 2 Segment 0 End Duty Cycle	0x00	Range 0-99
0x2010	1	Pattern 2 Segment 0 Duration	0x00	
0x2011	1	Pattern 2 Segment 1 Start Duty Cycle	0x00	Range 0-99
0x2012	1	Pattern 2 Segment 1 End Duty Cycle	0x00	Range 0-99
0x2013	1	Pattern 2 Segment 1 Duration	0x00	
0x2014	1	Pattern 2 Segment 2 Start Duty Cycle	0x00	Range 0-99
0x2015	1	Pattern 2 Segment 2 End Duty Cycle	0x00	Range 0-99
0x2016	1	Pattern 2 Segment 2 Duration	0x00	
0x2017	1	Pattern 2 Setup	0x00	Appendix A.7
0x2018	1	Pattern 3 Segments	0x00	Range 0-3

Continued on next page

0x2019	1	Pattern 3 Segment 0 Start Duty Cycle	0x00	Range 0-99
0x201A	1	Pattern 3 Segment 0 End Duty Cycle	0x00	Range 0-99
0x201B	1	Pattern 3 Segment 0 Duration	0x00	
0x201C	1	Pattern 3 Segment 1 Start Duty Cycle	0x00	Range 0-99
0x201D	1	Pattern 3 Segment 1 End Duty Cycle	0x00	Range 0-99
0x201E	1	Pattern 3 Segment 1 Duration	0x00	
0x201F	1	Pattern 3 Segment 2 Start Duty Cycle	0x00	Range 0-99
0x2020	1	Pattern 3 Segment 2 End Duty Cycle	0x00	Range 0-99
0x2021	1	Pattern 3 Segment 2 Duration	0x00	
0x2022	1	Pattern 3 Setup	0x00	Appendix A.7
0x2023	1	Pattern 4 Segments	0x00	Range 0-3
0x2024	1	Pattern 4 Segment 0 Start Duty Cycle	0x00	Range 0-99
0x2025	1	Pattern 4 Segment 0 End Duty Cycle	0x00	Range 0-99
0x2026	1	Pattern 4 Segment 0 Duration	0x00	
0x2027	1	Pattern 4 Segment 1 Start Duty Cycle	0x00	Range 0-99
0x2028	1	Pattern 4 Segment 1 End Duty Cycle	0x00	Range 0-99
0x2029	1	Pattern 4 Segment 1 Duration	0x00	
0x202A	1	Pattern 4 Segment 2 Start Duty Cycle	0x00	Range 0-99
0x202B	1	Pattern 4 Segment 2 End Duty Cycle	0x00	Range 0-99
0x202C	1	Pattern 4 Segment 2 Duration	0x00	
0x202D	1	Pattern 4 Setup	0x00	Appendix A.7
0x202E	1	Pattern 5 Segments	0x00	Range 0-3
0x202F	1	Pattern 5 Segment 0 Start Duty Cycle	0x00	Range 0-99
0x2030	1	Pattern 5 Segment 0 End Duty Cycle	0x00	Range 0-99
0x2031	1	Pattern 5 Segment 0 Duration	0x00	
0x2032	1	Pattern 5 Segment 1 Start Duty Cycle	0x00	Range 0-99
0x2033	1	Pattern 5 Segment 1 End Duty Cycle	0x00	Range 0-99
0x2034	1	Pattern 5 Segment 1 Duration	0x00	
0x2035	1	Pattern 5 Segment 2 Start Duty Cycle	0x00	Range 0-99
0x2036	1	Pattern 5 Segment 2 End Duty Cycle	0x00	Range 0-99
0x2037	1	Pattern 5 Segment 2 Duration	0x00	
0x2038	1	Pattern 5 Setup	0x00	Appendix A.7
0x2039	1	Pattern 6 Segments	0x00	Range 0-3
0x203A	1	Pattern 6 Segment 0 Start Duty Cycle	0x00	Range 0-99
0x203B	1	Pattern 6 Segment 0 End Duty Cycle	0x00	Range 0-99
0x203C	1	Pattern 6 Segment 0 Duration	0x00	
0x203D	1	Pattern 6 Segment 1 Start Duty Cycle	0x00	Range 0-99
0x203E	1	Pattern 6 Segment 1 End Duty Cycle	0x00	Range 0-99
0x203F	1	Pattern 6 Segment 1 Duration	0x00	
0x2040	1	Pattern 6 Segment 2 Start Duty Cycle	0x00	Range 0-99
0x2041	1	Pattern 6 Segment 2 End Duty Cycle	0x00	Range 0-99
0x2042	1	Pattern 6 Segment 2 Duration	0x00	
0x2043	1	Pattern 6 Setup	0x00	Appendix A.7
0x2044	1	Pattern 7 Segments	0x00	Range 0-3
0x2045	1	Pattern 7 Segment 0 Start Duty Cycle	0x00	Range 0-99
0x2046	1	Pattern 7 Segment 0 End Duty Cycle	0x00	Range 0-99

Continued on next page

0x2047	1	Pattern 7 Segment 0 Duration	0x00	
0x2048	1	Pattern 7 Segment 1 Start Duty Cycle	0x00	Range 0-99
0x2049	1	Pattern 7 Segment 1 End Duty Cycle	0x00	Range 0-99
0x204A	1	Pattern 7 Segment 1 Duration	0x00	
0x204B	1	Pattern 7 Segment 2 Start Duty Cycle	0x00	Range 0-99
0x204C	1	Pattern 7 Segment 2 End Duty Cycle	0x00	Range 0-99
0x204D	1	Pattern 7 Segment 2 Duration	0x00	
0x204E	1	Pattern 7 Setup	0x00	Appendix A.7
0x204F	1	Do Not Care		
0x2050	2	Waveform 0 Pattern Selection	0x0001	Appendix A.8
0x2051				
0x2052	1	Waveform 0 Stage 0 Half Cycles	0x04	
0x2053	1	Waveform 0 Stage 1 Half Cycles	0x00	
0x2054	1	Waveform 0 Stage 2 Half Cycles	0x00	
0x2055	1	Waveform 0 Stage 3 Half Cycles	0x00	
0x2056	1	Waveform 0 Stage 4 Half Cycles	0x00	
0x2057	1	Waveform 0 Repeat Count	0x01	
0x2058	1	Waveform 0 Repeat Time	0x00	
0x2059	1	Do Not Care		
0x205A	2	Waveform 1 Pattern Selection	0x0000	Appendix A.8
0x205B				
0x205C	1	Waveform 1 Stage 0 Half Cycles	0x00	
0x205D	1	Waveform 1 Stage 1 Half Cycles	0x00	
0x205E	1	Waveform 1 Stage 2 Half Cycles	0x00	
0x205F	1	Waveform 1 Stage 3 Half Cycles	0x00	
0x2060	1	Waveform 1 Stage 4 Half Cycles	0x00	
0x2061	1	Waveform 1 Repeat Count	0x00	
0x2062	1	Waveform 1 Repeat Time	0x00	
0x2063	1	Do Not Care		
0x2064	2	Waveform 2 Pattern Selection	0x0000	Appendix A.8
0x2065				
0x2066	1	Waveform 2 Stage 0 Half Cycles	0x00	
0x2067	1	Waveform 2 Stage 1 Half Cycles	0x00	
0x2068	1	Waveform 2 Stage 2 Half Cycles	0x00	
0x2069	1	Waveform 2 Stage 3 Half Cycles	0x00	
0x206A	1	Waveform 2 Stage 4 Half Cycles	0x00	
0x206B	1	Waveform 2 Repeat Count	0x00	
0x206C	1	Waveform 2 Repeat Time	0x00	
0x206D	1	Do Not Care		
0x206E	2	Waveform 3 Pattern Selection	0x0000	Appendix A.8
0x206F				
0x2070	1	Waveform 3 Stage 0 Half Cycles	0x00	
0x2071	1	Waveform 3 Stage 1 Half Cycles	0x00	
0x2072	1	Waveform 3 Stage 2 Half Cycles	0x00	
0x2073	1	Waveform 3 Stage 3 Half Cycles	0x00	
0x2074	1	Waveform 3 Stage 4 Half Cycles	0x00	

Continued on next page

0x2075	1	Waveform 3 Repeat Count	0x00	
0x2076	1	Waveform 3 Repeat Time	0x00	
0x2077	1	Do Not Care		
0x2078	2	Waveform 4 Pattern Selection	0x0000	Appendix A.8
0x2079				
0x207A	1	Waveform 4 Stage 0 Half Cycles	0x00	
0x207B	1	Waveform 4 Stage 1 Half Cycles	0x00	
0x207C	1	Waveform 4 Stage 2 Half Cycles	0x00	
0x207D	1	Waveform 4 Stage 3 Half Cycles	0x00	
0x207E	1	Waveform 4 Stage 4 Half Cycles	0x00	
0x207F	1	Waveform 4 Repeat Count	0x00	
0x2080	1	Waveform 4 Repeat Time	0x00	
0x2081	1	Do Not Care		
0x2082	2	Waveform 5 Pattern Selection	0x0000	Appendix A.8
0x2083				
0x2084	1	Waveform 5 Stage 0 Half Cycles	0x00	
0x2085	1	Waveform 5 Stage 1 Half Cycles	0x00	
0x2086	1	Waveform 5 Stage 2 Half Cycles	0x00	
0x2087	1	Waveform 5 Stage 3 Half Cycles	0x00	
0x2088	1	Waveform 5 Stage 4 Half Cycles	0x00	
0x2089	1	Waveform 5 Repeat Count	0x00	
0x208A	1	Waveform 5 Repeat Time	0x00	
0x208B	1	Do Not Care		
0x208C	2	Waveform 6 Pattern Selection	0x0000	Appendix A.8
0x208D				
0x208E	1	Waveform 6 Stage 0 Half Cycles	0x00	
0x208F	1	Waveform 6 Stage 1 Half Cycles	0x00	
0x2090	1	Waveform 6 Stage 2 Half Cycles	0x00	
0x2091	1	Waveform 6 Stage 3 Half Cycles	0x00	
0x2092	1	Waveform 6 Stage 4 Half Cycles	0x00	
0x2093	1	Waveform 6 Repeat Count	0x00	
0x2094	1	Waveform 6 Repeat Time	0x00	
0x2095	1	Do Not Care		
0x2096	2	Waveform 7 Pattern Selection	0x0000	Appendix A.8
0x2097				
0x2098	1	Waveform 7 Stage 0 Half Cycles	0x00	
0x2099	1	Waveform 7 Stage 1 Half Cycles	0x00	
0x209A	1	Waveform 7 Stage 2 Half Cycles	0x00	
0x209B	1	Waveform 7 Stage 3 Half Cycles	0x00	
0x209C	1	Waveform 7 Stage 4 Half Cycles	0x00	
0x209D	1	Waveform 7 Repeat Count	0x00	
0x209E	1	Waveform 7 Repeat Time	0x00	
0x209F	1	Do Not Care		
0x20A0	2	PWM Frequency	20000	Range 15000-20000
0x20A1				

Continued on next page

0x20A2 0x20A3	2	LRA Frequency	170	Range 100-300
0x20A4	1	Autoresonance Backoff	40	Range 0-100
0x20A5	1	Reserved	0x00	Set to ’0x00’

15 Ordering Information

15.1 Ordering Code

IQS390 zzz ppb

Table 15.1: Order Code Description

IC NAME				IQS390
CONFIGURATION	zzz	=	001	I^2C Address 1 = 0x54 I^2C Address 2 = 0x40
PACKAGE TYPE	pp	=	QF	QFN-20 Package
BULK PACKAGING	b	=	R	QFN-20 Reel (2000 pcs/reel)

Example : IQS390-001QFR

15.2 Top Marking

Figure 15.1: IQS390-QFN20 Package Top Marking

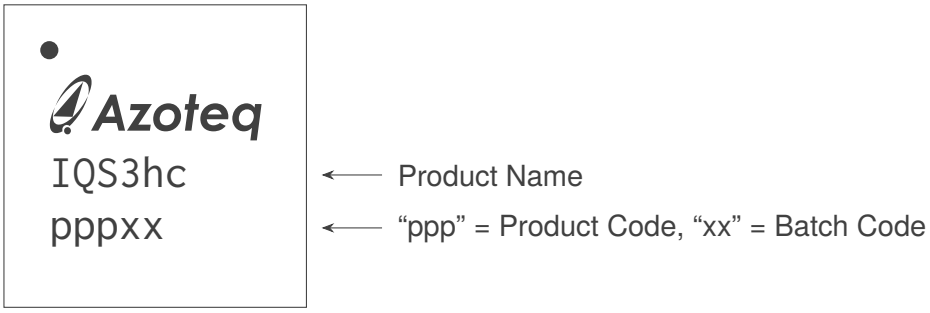
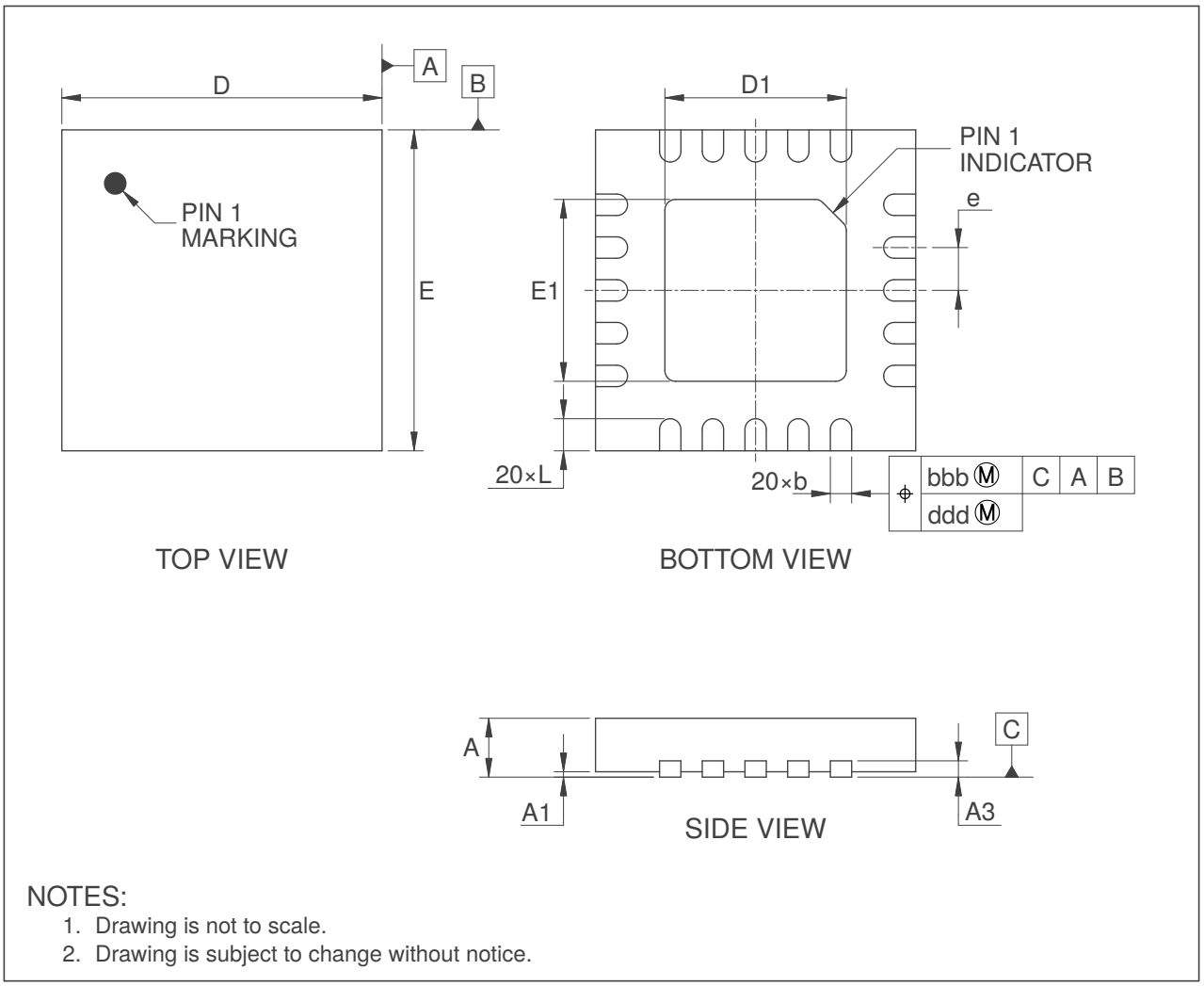


Figure 15.2: QFN20 Generic Package Top Marking

16 Package Information

16.1 QFN20 Package Outline



NOTES:
1. Drawing is not to scale.
2. Drawing is subject to change without notice.

Figure 16.1: QFN20 Package Outline

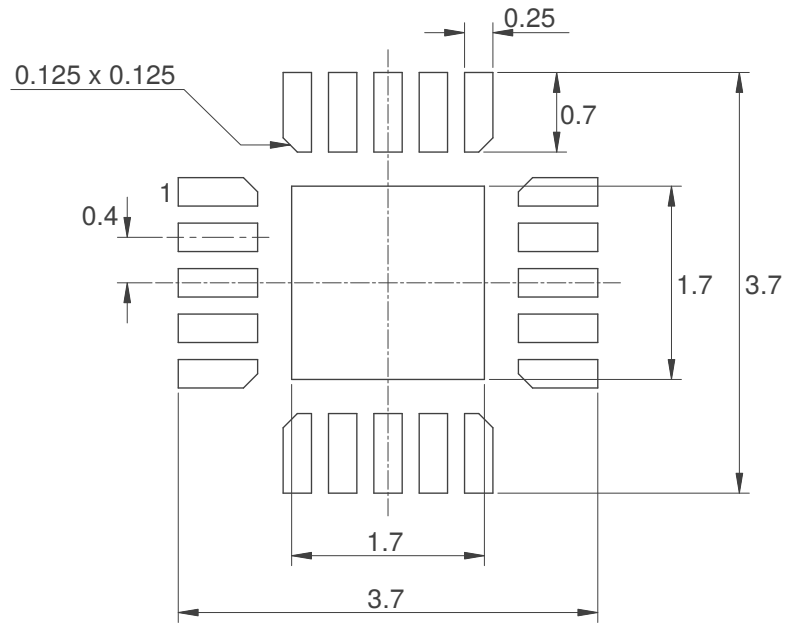
Table 16.1: QFN20 Package Dimensions [mm]

Dimension	Millimeters		
	Min	Typ	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D		3.00 BSC	
E		3.00 BSC	
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e		0.40 BSC	
L	0.25	0.30	0.35

Table 16.2: QFN20 Package Tolerances [mm]

Tolerance	Millimeters
bbb	0.07
ddd	0.05

16.2 QFN20 Recommended Footprint

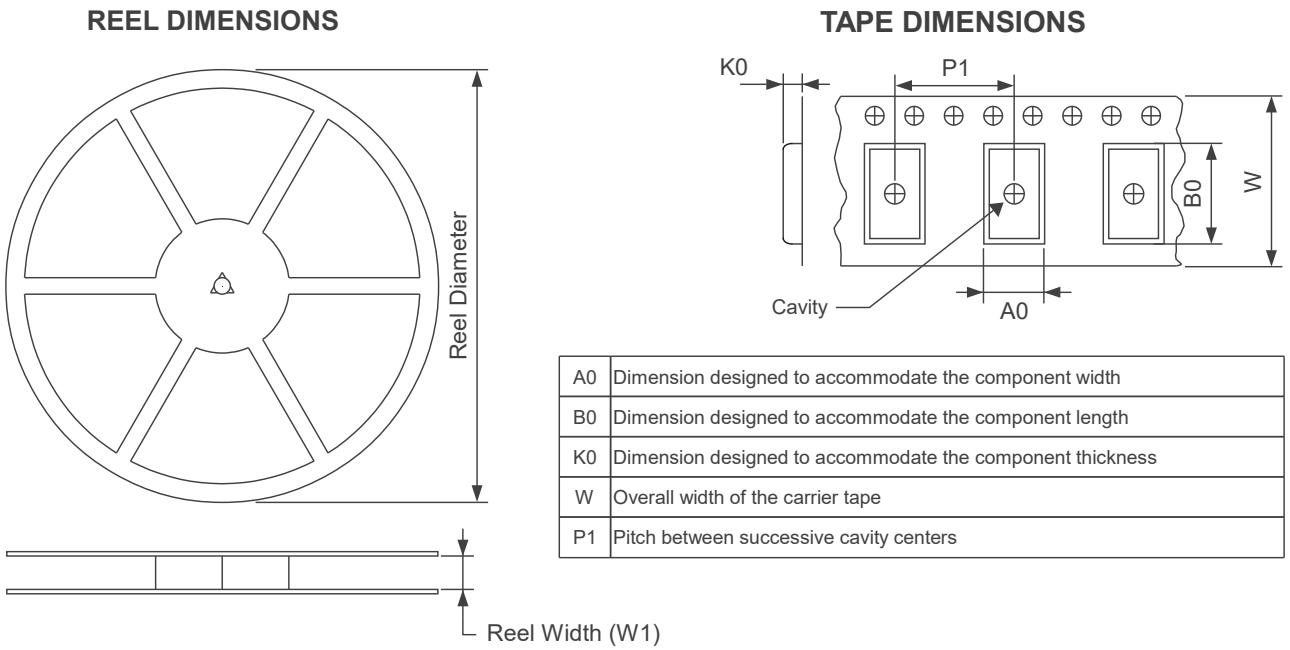


NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.

Figure 16.2: QFN20 Recommended Footprint

16.3 Tape and Reel Specifications



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Figure 16.3: Tape and Reel Specification

Table 16.3: Tape and Reel Specifications

Package Type	Pins	Dimension [Millimeters]							Pin 1 Quadrant
		Reel Diameter	Reel Width	A0	B0	K0	P1	W	
QFN20	20	180	12.4	3.3	3.3	0.8	8	12	Q2

A Memory Map Descriptions

A.1 System Status (0x1000)

Bit	7	6	5	4	3	2	1	0
Description	Reserved		Over Temperature	Overcurrent	Current Power State	Recommend Recalibrate	Haptics Active	Reset

- Bit 5: **Over Temperature**
  - 0: No fault condition
  - 1: An over temperature condition has been detected
  - Bit cleared on read
- Bit 4: **Overcurrent**
  - 0: No fault condition
  - 1: An overcurrent condition has been detected
  - Bit cleared on read
- Bit 3: **Current Power State**
  - 0: The device is in the 'Fast Haptics' state
  - 1: The device is in the 'ULP' state
- Bit 2: **Recommend Recalibrate**
  - See Section 11.3
- Bit 1: **Haptics Active**
  - 0: The internal haptic engine is inactive
  - 1: The internal haptic engine is running
- Bit 0: **Reset**
  - 0: Device is not in a reset condition
  - 1: Device is in a reset condition

A.2 System Settings (0x1002)

Bit	7	6	5	4	3	2	1	0
Description	Continuous Mode	Trigger Mode	Power Mode Timeout				Power Mode	

- Bit 7: **Continuous Mode**
  - 0: Use normal mode control
  - 1: Use continuous mode control
- Bit 6: **Trigger Mode**
  - 0: Select 'Edge Trigger' mode
  - 1: Select 'Level Trigger' mode
- Bit 2-5: **Power Mode Timeout**
  - Actual timeout in milliseconds = (512 × bitfield value)
- Bit 0-1: **Power Mode**
  - 0: Select 'Fast Haptics'
  - 1: Select 'ULP'
  - 2: Select 'Automatic'

A.3 Over Temperature Settings (0x1003)

Bit	7	6	5	4	3	2	1	0
Description	Reserved			Hysteresis	Over Temperature Threshold			

- Bit 4: **Hysteresis**
  - 0: Disabled
  - 1: Enabled

- Bit 0-3: **Over Temperature Threshold**
  - 0: 29 °C
  - 1: 36 °C
  - 2: 44 °C
  - 3: 49 °C
  - 4: 56 °C
  - 5: 64 °C
  - 6: 71 °C
  - 7: 81 °C
  - 8: 89 °C
  - 9: 99 °C
  - 10: 106 °C
  - 11: 116 °C
  - 12: 126 °C
  - 13: 136 °C
  - 14: 146 °C
  - 15: 159 °C

A.4 System Control (0x1006)

Bit	7	6	5	4	3	2	1	0
Description	Reserved						Soft Reset	ACK Reset

- Bit 1: **Soft Reset**
  - 0: No action
  - 1: Soft reset the device
- Bit 0: **ACK Reset**
  - 0: No action
  - 1: Acknowledge a device reset
  - Bit automatically cleared

A.5 Haptic Control (0x1007)

Bit	7	6	5	4	3	2	1	0
Description	Reserved			Stop Haptics	Waveform Selection			Trigger Haptics

- Bit 4: **Stop Haptics**
  - 0: No action
  - 1: Immediately stop the haptics if it is active
  - Bit automatically cleared
- Bit 1-3: **Waveform Selection**
  - Waveform to run. Range 0-7.
    Corresponds to memory map settings from address 0x2050 to 0x209E.
- Bit 0: **Trigger Haptics**
  - 0: No action
  - 1: Play the waveform selected by *Waveform Selection*
  - Bit automatically cleared

A.6 H-Bridge Setup (0x2000)

Bit	15	14	13	12	11	10	9	8
Description	Reserved		Ground Inactive	Strict Failure	External	Drive Strength		

Bit	7	6	5	4	3	2	1	0
Description	Reserved		Slew Rate		Slew Rate Control	Shoot-through Protection	Over Temperature Protection	Overcurrent Protection

- Bit 13: **Ground Inactive**
  - 0: Float M+ and M- when motor is not being driven
  - 1: Pull M+ and M- to ground when motor is not being driven
- Bit 12: **Strict Failure**
  - 0: Allow haptics at any time
  - 1: Use Strict Failure mode
- Bit 11: **External**
  - 0: Use internal H-bridge
  - 1: Output drive signals for an external H-bridge on M+ and M-
- Bit 8-10: **Drive Strength**
  - Range 0-5.
    Typical: 5
- Bit 4-5: **Slew Rate**
  - 0: 20 V/µs
  - 1: 40 V/µs
  - 2: 80 V/µs
  - 3: 160 V/µs
- Bit 3: **Slew Rate Control**
  - 0: Disabled
  - 1: Enabled
- Bit 2: **Shoot-through Protection**
  - 0: Disabled
  - 1: Enabled
- Bit 1: **Over Temperature Protection**
  - 0: Disabled
  - 1: Enabled
- Bit 0: **Overcurrent Protection**
  - 0: Disabled
  - 1: Enabled

A.7 Pattern Setup (0x200C, 0x2017, 0x2022, 0x202D, 0x2038, 0x2043, 0x204E)

Bit	7	6	5	4	3	2	1	0
Description	Reserved						Auto-resonance	Invert

- Bit 1: **Autoresonance**
  - 0: Disabled for this pattern
  - 1: Enabled for this pattern
- Bit 0: **Invert**
  - See Section 10.1

A.8 Waveform Pattern Selection (0x2050, 0x205A, 0x2064, 0x206E, 0x2078, 0x2082, 0x208C, 0x2096)

Bit	15	14	13	12	11	10	9	8
Description	Reserved	Stage 4			Stage 3			Stage 2

Bit	7	6	5	4	3	2	1	0
Description	Stage 2		Stage 1			Stage 0		

- Bit 12-14: **Stage 4**
  - Pattern to run in this stage
  - 0: None
  - 1-7: Pattern corresponding to memory map settings from address 0x2002 to 0x204D
- Bit 9-11: **Stage 3**
  - Pattern to run in this stage
  - 0: None
  - 1-7: Pattern corresponding to memory map settings from address 0x2002 to 0x204D
- Bit 6-8: **Stage 2**
  - Pattern to run in this stage
  - 0: None
  - 1-7: Pattern corresponding to memory map settings from addresses 0x2002 to 0x204D
- Bit 3-5: **Stage 1**
  - Pattern to run in this stage
  - 0: None
  - 1-7: Pattern corresponding to memory map settings from addresses 0x2002 to 0x204D
- Bit 0-2: **Stage 0**
  - Pattern to run in this stage
  - 0: None
  - 1-7: Pattern corresponding to memory map settings from addresses 0x2002 to 0x204D

B Revision History

Release	Date	Comments
v1.0	2024/10/18	Initial document released

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